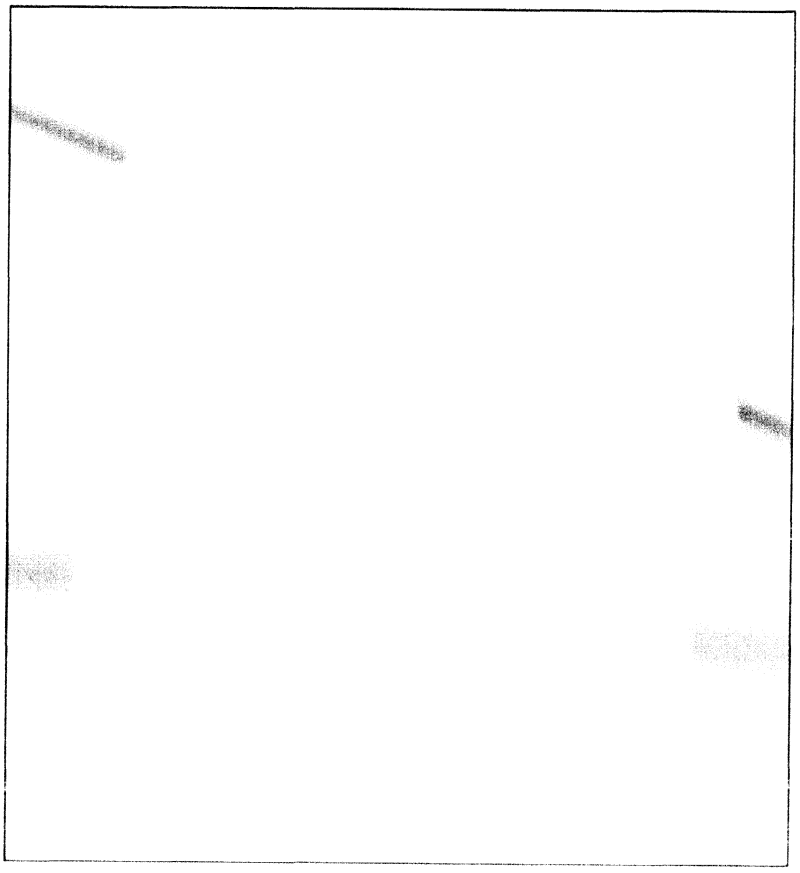

Linear & Telecom ICs

FOR ANALOG SIGNAL PROCESSING APPLICATIONS

1993-94

HARRIS SEMICONDUCTOR

New High Speed Linear Products —

VIDEO OP AMPS AND BUFFERS

HFA1105
LOW POWER VIDEO OP AMP

AnswerFAX DOCUMENT # 3395

- -3dB Bandwidth (A_V = +2) 350MHz
- High Slew Rate 1000V/µs
- Gain Flatness to 50MHz..... ±0.04dB
- Fast Settling Time (0.1%)..... 15ns
- Differential Gain/Phase .....0.02%/0.02 Degrees
- Low Supply Current 6mA
- 8 Lead PDIP and SOIC

HFA1115
LOW POWER PROGRAMMABLE GAIN VIDEO BUFFER

AnswerFAX DOCUMENT # 3606

- Wide -3dB Bandwidth 225MHz
- High Slew Rate 1100V/µs
- Differential Gain/Phase ..... 0.02%/0.03 Degrees
- User Programmable Gain (+2, ±1)
- User Programmable Output Limiting
- Low Supply Current.....7mA
- 8 Lead PDIP and SOIC

HFA1106
VIDEO OP AMP WITH COMPENSATION

AnswerFAX DOCUMENT # 3922

- Wide -3dB Bandwidth 315MHz
- High Slew Rate 700V/µs
- Differential Gain/Phase.....0.02%/0.05 Degrees
- Low Supply Current 6mA
- Compensation Pin for Bandwidth Limiting
- 8 Lead PDIP and SOIC

HFA1135
VIDEO OP AMP WITH OUTPUT LIMITING

AnswerFAX DOCUMENT # 3653

- Wide -3dB Bandwidth 360MHz
- High Slew Rate 1200V/µs
- Fast Settling Time (0.1%) 15ns
- Differential Gain/Phase ..... 0.02%/0.04 Degrees
- Low Supply Current.....7mA
- User Programmable Output Limiting
- Fast Overdrive Recovery.....<1ns
- 8 Lead PDIP and SOIC

HFA1113
PROG. GAIN VIDEO BUFFER WITH OUTPUT LIMITING

AnswerFAX DOCUMENT # 1342

- Wide -3dB Bandwidth 850MHz
- High Slew Rate 2400V/µs
- Differential Gain/Phase.....0.02%/0.04 Degrees
- User Programmable Gain of +2, ±1
- User Programmable Output Limiting
- 8 Lead PDIP and SOIC

HFA1145
LOW POWER VIDEO OP AMP WITH DISABLE

AnswerFAX DOCUMENT # 3395

- -3dB Bandwidth (A_V = +2).....350MHz
- High Slew Rate 1000V/µs
- Differential Gain/Phase ..... 0.02%/0.02 Degrees
- Gain Flatness to 50MHz..... ±0.04dB
- Low Supply Current.....6mA
- Output Enable/Disable (T_{ON}/T_{OFF} = 180ns/35ns)
- 8 Lead PDIP and SOIC

HFA1114
CABLE DRIVING BUFFER WITH SUMMING NODE

AnswerFAX DOCUMENT # 3151

- Wide -3dB Bandwidth 850MHz
- High Slew Rate 2400V/µs
- Differential Gain/Phase.....0.02%/0.04 Degrees
- User Programmable Gain (+2, ±1)
- Summing Node Pinout Enables Tailoring of System Response For Cable Length
- 8 Lead PDIP and SOIC

HFA1205
DUAL LOW POWER VIDEO OP AMP

AnswerFAX DOCUMENT # 3605

- -3dB Bandwidth (A_V = +2).....400MHz
- High Slew Rate 1275V/µs
- Differential Gain/Phase ..... 0.03%/0.03 Degrees
- Low Supply Current..... 6mA/Op Amp
- Gain Flatness to 50MHz..... ±0.03dB
- 8 Lead PDIP and SOIC

New High Speed Linear Products (Continued)

VIDEO OP AMPS AND BUFFERS (Continued)

HFA1212
DUAL PROGRAMMABLE GAIN VIDEO BUFFER

AnswerFAX DOCUMENT # 3607

- -3dB Bandwidth (A_V = +2) 340MHz
- High Slew Rate 1100V/µs
- Differential Gain/Phase.....0.02%/0.03 Degrees
- User Programmable Gain (+2, ±1)
- Low Supply Current.....6mA/Op Amp
- 8 Lead PDIP and SOIC

HFA1245
DUAL LOW POWER VIDEO AMP WITH DISABLE

AnswerFAX DOCUMENT # 3682

- -3dB Bandwidth (A_V = +2) 530MHz
- High Slew Rate 1050V/µs
- Differential Gain/Phase.....0.02%/0.03 Degrees
- Gain Flatness to 50MHz.....±0.11dB
- Low Supply Current.....6mA/Op Amp
- Output Enable/Disable (T_{ON}/T_{OFF} = 160ns/20ns)
- 14 Lead PDIP and SOIC

HFA1405
QUAD LOW POWER VIDEO OP AMP

AnswerFAX DOCUMENT # 3604

- -3dB Bandwidth (A_V = +2) 550MHz
- High Slew Rate 1100V/µs
- Differential Gain/Phase.....0.02%/0.03 Degrees
- Gain Flatness to 50MHz.....±0.03dB
- Low Supply Current.....6mA/Op Amp
- 14 Lead SOIC

HFA1412
QUAD PROGRAMMABLE GAIN VIDEO BUFFER

AnswerFAX DOCUMENT # 3607

- -3dB Bandwidth (A_V = +2) 340MHz
- High Slew Rate 1100V/µs
- Differential Gain/Phase.....0.02%/0.03 Degrees
- User Programmable Gain (+2, ±1)
- Low Supply Current.....6mA/Op Amp
- 14 Lead PDIP and SOIC

HA5013
TRIPLE 125MHz VIDEO OP AMP

AnswerFAX DOCUMENT # 3654

- Wide -3dB Bandwidth 125MHz
- High Slew Rate 475V/µs
- Differential Gain/Phase ..... 0.03%/0.03 Degrees
- High ESD Protection 4000V
- Low Supply Current.....7.5mA/Op Amp
- 14 Lead PDIP and SOIC

HA5022
DUAL 125MHz VIDEO AMP WITH DISABLE

AnswerFAX DOCUMENT # 3392

- Wide -3dB Bandwidth 125MHz
- High Slew Rate 475µV/µs
- Differential Gain/Phase ..... 0.03%/0.03 Degrees
- High ESD Protection 4000V
- Low Supply Current.....7.5mA/Op Amp
- Individual Output Disable/Enable
- 16 Lead PDIP and SOIC

HA5023
DUAL 125MHz VIDEO OP AMP

AnswerFAX DOCUMENT # 3393

- Wide -3dB Bandwidth 125MHz
- High Slew Rate 475V/µs
- Differential Gain/Phase ..... 0.03%/0.03 Degrees
- High ESD Protection 4000V
- Low Supply Current.....7.5mA/Op Amp
- 8 Lead PDIP and SOIC

HA5024
QUAD 125MHz VIDEO OP AMP WITH DISABLE

AnswerFAX DOCUMENT # 3550

- Wide -3dB Bandwidth 125MHz
- High Slew Rate 475V/µs
- Differential Gain/Phase ..... 0.03%/0.03 Degrees
- High ESD Protection 4000V
- Low Supply Current.....7.5mA/Op Amp
- Individual Output Disable/Enable
- 20 Lead PDIP and SOIC

New High Speed Linear Products (Continued)

VIDEO OP AMPS AND BUFFERS (Continued)

HA5025
QUAD 125MHz VIDEO OP AMP

AnswerFAX DOCUMENT # 3591

- Wide -3dB Bandwidth 125MHz
- High Slew Rate 475V/µs
- Differential Gain/Phase.....0.03%/0.03 Degrees
- High ESD Protection 4000V
- Low Supply Current.....7.5mA/Op Amp
- 14 Lead PDIP and SOIC

WIRELESS COMMUNICATIONS

HFA3101
GILBERT CELL TRANSISTOR ARRAY

AnswerFAX DOCUMENT # 3663

- NPN Transistor Array Configured as a Gilbert Cell
- High Gain Bandwidth Product 10GHz
- High Power Gain BW Product 5GHz
- Current Gain (h_{FE}).....70
- Low Collector Leakage Current ..... <0.01nA
- Pin Compatible to UPA101
- 8 Lead SOIC

HFA3102
DUAL DIFFERENTIAL AMPLIFIER

AnswerFAX DOCUMENT # 3635

- High Gain Bandwidth Product 10GHz
- High Power Gain BW Product 5GHz
- High Current Gain (h_{FE}).....70
- Pin Compatible to UPA102G
- 14 Lead SOIC

HFA3600
LOW NOISE AMPLIFIER/MIXER

AnswerFAX DOCUMENT # 3655

- Low Noise Figure
  - LNA ..... 2.3dB at 900MHz
  - Mixer ..... 12.1dB at 900MHz
  - LNA + Mixer..... 3.97dB at 900MHz
- High Power Gain
  - LNA ..... 12.8dB at 900MHz
  - Mixer ..... 7.0dB at 900MHz
  - LNA + Mixer..... 19.8dB at 900MHz
- High Intercept
  - LNA ..... +12.8dBm at Output
  - Mixer ..... +3.2dBm at Output
  - LNA + Mixer..... -16.7dBm at Input
- 14 Lead SOIC

$5.00

HARRIS SEMICONDUCTOR

HARRIS SEMICONDUCTOR

This Linear and Telecom Databook represents the full line of Harris Semiconductor Linear and Telecom products for Commercial and Industrial applications and supersedes all previously published Harris Linear and Telecom databooks. Military (MIL-STD-883, DESC SMD, and JAN) Products are listed in the Harris Analog Military Products Databook. For a complete listing of all Harris Semiconductor products, please refer to the Product Selection Guide (PSG-201R; ordering information below).

For complete, current and detailed technical specifications on any Harris devices please contact the nearest Harris sales, representative or distributor office. Literature requests may also be directed to:

Harris Semiconductor Literature Department
P.O. Box 883, MS 53-204
Melbourne, FL 32902
Phone: 1-800-442-7747
Fax: 407-724-7240

See Section 12 for Data Sheets Available on AnswerFAX

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Shinjuku-ku, Tokyo 163 Japan
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LINEAR AND TELECOM PRODUCTS

Harris Semiconductor is a pioneer in developing and producing advanced Linear and Telecom products for the most demanding Commercial, Industrial and Automotive applications in this world -- and beyond.

This databook fully describes Harris Semiconductor's line of Linear and Telecom IC's. It includes a complete set of datasheets for product specifications, application notes with design details for specific applications of Harris products, and a description of the Harris Quality and Reliability program. A New AnswerFAX section has been added to allow Users to request the latest datasheets and have them delivered immediately to your FAX machine. A detailed listing of SPICE Models and product Packaging provides a wide variety of information at your fingertips.

Harris offers an extensive line of Linear components including; High Speed and General Purpose Op Amps, Comparators, Sample and Hold Amplifiers, Transistor Arrays and Special Analog Circuits found in Sections 2 through 7.

Harris Telecommunications components include SLIC - Subscriber Line Interface Circuits, Crosspoint Switches, CVSD's, DTMF Receivers and Tone Generators, PCM CODEC's and Transcoders and is found in Section 8.

It is our intention to provide you with the most up-to-date information on Linear and Telecom Products. For complete, current and detailed technical specifications on any Harris devices please contact the nearest Harris sales, representative or distributor office, listed at the end of the databook; or direct literature requests to:

Harris Semiconductor Literature Department
P.O. Box 883, MS 53-204
Melbourne, FL 32902
Phone: 1-800-442-7747
Fax: 407-724-7240

See Section 12 for Data Sheets Available on AnswerFAX

Harris Semiconductor products are sold by description only. All specifications in this product guide are applicable only to packaged products; specifications for die are available upon request. Harris reserves the right to make changes in circuit design, specifications and other information at any time without prior notice. Accordingly, the reader is cautioned to verify that information in this publication is current before placing orders. Reference to products of other manufacturers are solely for convenience of comparison and do not imply total equivalency of design, performance, or otherwise.

HARRIS SEMICONDUCTOR

LINEAR INTEGRATED CIRCUITS

FOR COMMERCIAL AND INDUSTRIAL APPLICATIONS

* Product Selection Guide located at the beginning of section.

TECHNICAL ASSISTANCE

For technical assistance on the Harris products listed in this databook, please contact the Field Applications Engineering staff available at one of the following Harris Sales Offices:

UNITED STATES		
CALIFORNIA	Calabasas	818-878-7950
	Costa Mesa	714-433-0600
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GEORGIA	Duluth	404-476-2035
ILLINOIS	Schaumburg	708-240-3480
INDIANA	Carmel	317-843-5180
MASSACHUSETTS	Burlington	617-221-1850
NEW JERSEY	Voorhees	609-751-3425
NEW YORK	Hauppauge	516-342-0291
	Wappingers Falls	914-298-1920
TEXAS	Dallas	214-733-0800
INTERNATIONAL		
FRANCE	Paris	33-1-346-54046
GERMANY	Munich	49-89-63813-0
HONG KONG	Kowloon	852-723-6339
ITALY	Milano	39-2-262-0761
JAPAN	Tokyo	81-3-3265-7571
KOREA	Seoul	82-2-551-0931
SINGAPORE	Singapore	65-291-0203
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LINEAR 1

GENERAL INFORMATION

ALPHA NUMERIC PRODUCT INDEX

NOTE: Bold Type Designates a New Product from Harris.

ALPHA NUMERIC PRODUCT INDEX (Continued)

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PRODUCT INDEX BY FAMILY

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HARRIS SEMICONDUCTOR

Commercial Linear Product Cross Reference

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
3507J	HA2-2525-5	Yes	
3508J	HA2-2625-5	Yes	
3551J	HA2-5162-5	*	Reduced Ibias/Greater Bandwidth
3551S	HA2-5160-2	*	Reduced Ibias/Greater Bandwidth
3554AM	HFA1-0001-9	No	Greater Bandwidth/Faster Ts/Lower price
3554BM	HFA1-0001-9	No	Greater Bandwidth/Faster Ts/Lower price
3554SM	HFA1-0001-9	No	Greater Bandwidth/Faster Ts/Lower price
AD3554AM	HFA1-0001-9	No	Greater Bandwidth/Faster Ts/Lower price
AD3554BM	HFA1-0001-9	No	Greater Bandwidth/Faster Ts/Lower price
AD3554SM	HFA1-0001-9	No	Greater Bandwidth/Faster Ts/Lower price
AD389BD	HA1-5320-2	No	Faster Acquisition/Reduced Droop
AD389KD	HA1-5320-5	No	Faster Acquisition/Reduced Droop
AD507JH	HA2-2625-5	Yes	
AD507KH	HA2-2625-5	Yes	
AD507SH	HA2-2620-2	Yes	
AD509JH	HA2-2525-5	Yes	Substitute HA2-2529-5
AD509KH	HA2-2525-5	Yes	Substitute HA2-2529-5
AD509SH	HA2-2520-2	Yes	Substitute HA2-2529-2
AD518JH	HA2-2515-5	Yes	
AD518JN	HA3-2515-5	Yes	
AD518KH	HA2-2515-5	Yes	
AD518SH	HA2-2510-2	Yes	
AD539JD	HA1-2547-5	No	Enhanced Bandwidth
AD539KD	HA1-2547-5	No	Enhanced Bandwidth
AD539SD	HA1-2547-9	No	Enhanced Bandwidth
AD542JH	HA1-5170-5	*	Enhanced ACs
AD5539JN	HA3-2839-5	*	
AD5539JQ	HA1-2839-5	*	
AD5539SQ	HA1-2539-2	*	
AD582KD	HA1-2425-5	No	Faster Acquisition/Enhanced ACs
AD582SD	HA1-2420-2	No	Faster Acquisition/Enhanced ACs
AD583KD	HA1-2425-5	Yes	Faster Acquisition/Greater Iout
AD585AQ	HA1-5320-5	No	Faster Acquisition/Reduced Droop
AD585SQ	HA1-5320-2	No	Faster Acquisition/Reduced Droop
AD811AN	HA3-5020-9	Yes	Lower Power, Price
AD811SQ/883	HA7-5020/883	Yes	Lower Power, Price
AD821AQ	CA5160AE (PDIP)	*	Reduced Ibias/Enhanced ACs
AD821AS	CA5160AE (PDIP)	*	Reduced Ibias/Enhanced ACs
AD821JN	CA5160AE	*	Reduced Ibias/Enhanced ACs
AD840JN	HA3B2840-5	Yes	Lower Cost
AD840JQ	HA1-2840-5	Yes	Lower Cost
AD840KN	HA3B2840-5	Yes	Lower Cost
AD840KQ	HA1-2840-5	Yes	Lower Cost
AD840SQ	HA1-2840/883	Yes	Lower Cost
AD840SQ/883	HA1-2840/883	Yes	Lower Cost
AD841JH	HA2-2541-5	Yes	
AD841JN	HA3-2841-5	Yes	Lower Cost

* Primary pins are pin-to-pin; Secondary/optional pins are not

Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
AD841JQ	HA1-2541-5	Yes	
AD841KH	HA2-2541-5	Yes	
AD841KN	HA3-2841-5	Yes	Lower Cost
AD841KQ	HA7-2841-5	Yes	Enhanced ACs/Lower Power
AD841SH	HA2-2541/883	Yes	Enhanced ACs/Lower Power
AD841SQ	HA1-2841/883	Yes	Lower Cost
AD841SQ/883	HA1-2841/883	Yes	Lower Cost
AD842JH	HA2-2542-5	Yes	
AD842JN	HA3B2842-5	Yes	Lower Cost
AD842JQ	HA1-2542-5	Yes	
AD842KH	HA2-2542-5	Yes	
AD842KN	HA3B2842-5	Yes	Lower Cost
AD842KQ	HA1-2542-5	Yes	
AD842SH	HA2-2542/883	Yes	Enhanced ACs/Lower Cost
AD842SQ	HA1-2842/883	Yes	Lower Cost
AD842SQ/883	HA1-2842/883	Yes	Lower Cost
AD844AN	HA3-5020-9	Yes	Enhanced ACs and Video Performance
AD844AQ	HA7-5020-9	Yes	Enhanced ACs and Video Performance
AD844BQ	HA7-5020-9	Yes	Enhanced ACs and Video Performance
AD844SQ/883B	HA7-5020/883	Yes	Enhanced ACs and Video Performance
AD846AN	HA3-5020-9	Yes	Enhanced ACs/Lower Cost
AD846AQ	HA7-5020-9	Yes	Enhanced ACs/Lower Cost
AD846BQ	HA7-5020-9	Yes	Enhanced ACs/Lower Cost
AD846SQ	HA7-5020/883	Yes	Enhanced ACs/Lower Cost
AD847JN	HA3-2544C-5	Yes	
AD847SQ	HA7-2544-2	Yes	
AD9610BH	HA1-5004-9	No	Greater Bandwidth/Lower Cost Monolithic
AD9617JN	HFA3-0001-5	Yes	Greater Bandwidth/Lower Cost
AD9620AD	HFA1110IJ	Yes	Performance, Price
AD9620SD	HFA1110MJ/883	Yes	Performance, Price
AD9630AN	HFA1110IP	Yes	Performance, Price
AD9630AQ	HFA1110IJ	Yes	Performance, Price
AD9630AR	HFA1110IB	Yes	Performance, Price
AD9630SQ	HFA1110MJ/883	Yes	Performance, Price
AD96685BH	HFA2-0003L-9	Yes	Better Performance
AD96685BQ	HFA1-0003L-9	Yes	Better Performance
AD96685BR	HFA9P0003L-5	Yes	Faster Propagation Delay/Lower Cost
ADLH0032CG	HA2-2542-5	*	Monolithic/Lower Cost
ADLH0032G	HA2-2542-2	*	Monolithic/Lower Cost
ADLH0033CG	HA2-5033-5	*	Enhanced ACs/Monolithic/Lower Cost
ADLH0033G	HA2-5033-2	*	Enhanced ACs/Monolithic/Lower Cost
ADOP27AH	HA2-5127A-2	Yes	Enhanced ACs/Reduced Icc
ADOP27AQ	HA7-5127A-2	Yes	Enhanced ACs/Reduced Icc
ADOP27EH	HA2-5127A-5	Yes	Enhanced ACs/Reduced Icc
ADOP27EQ	HA7-5127A-5	Yes	Enhanced ACs/Reduced Icc
ADOP27GH	HA2-5127-5	Yes	Enhanced ACs/Reduced Icc
ADOP27GQ	HA7-5127-5	Yes	Enhanced ACs/Reduced Icc

* Primary pins are pin-to-pin; Secondary/optional pins are not

Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
ADOP37AH	HA2-5137A-2	Yes	Enhanced ACs/Reduced Icc
ADOP37AQ	HA7-5137A-2	Yes	Enhanced ACs/Reduced Icc
ADOP37EH	HA2-5137A-5	Yes	Enhanced ACs/Reduced Icc
ADOP37EQ	HA7-5137A-5	Yes	Enhanced ACs/Reduced Icc
ADOP37GH	HA2-5137-5	Yes	Enhanced ACs/Reduced Icc
ADOP37GQ	HA7-5137-5	Yes	Enhanced ACs/Reduced Icc
AM-450-2	HA2-2505-5	Yes	Guaranteed DCs/ACs
AM-450-2M	HA2-2502-2	Yes	Guaranteed DCs/ACs
AM-452-2	HA2-2525-5	Yes	Guaranteed DCs/ACs
AM-452-2M	HA2-2522-2	Yes	Guaranteed DCs/ACs
AM-460-2	HA2-2605-5	Yes	Guaranteed DCs/ACs
AM-460-2M	HA2-2602-2	Yes	Guaranteed DCs/ACs
AM-462-2	HA2-2625-5	Yes	Guaranteed DCs/ACs
AM-462-2M	HA2-2620-2	Yes	Guaranteed DCs/ACs
AM-7650-1	ICL7650SCPD	Yes	Almost Identical
AM-7650-2	ICL7650SCTV-1	Yes	Almost Identical
BB3554AM	HFA1-0001-9	No	Greater Bandwidth/Faster Ts/Lower Cost
BB3554BM	HFA1-0001-9	No	Greater Bandwidth/Faster Ts/Lower Cost
BB3554SM	HFA1-0001-9	No	Greater Bandwidth/Faster Ts/Lower Cost
CA3054	CA3054	Yes	SOIC Version Available
CA3146P	CA3146E	Yes	
CLC110A8D	HFA1110MJ/883	Yes	Better Performance
CLC110AID	HFA1110IJ	Yes	Better Performance
CLC110AJP	HFA1110IP	Yes	Better Performance
CLC110ALC	HFA1110Y	N/A	Die
CLC400A8D	HFA1120MJ/883	*	Better Performance
CLC400AID	HFA1120IJ	*	Better Performance
CLC400AID	HFA1-0001-9	*	Faster Transient Response
CLC400AJE	HFA1120IB	*	Better Performance
CLC400AJP	HFA1120IP	*	Better Performance
CLC400AJP	HFA3-0001-9	*	Faster Transient Response
CLC400ALC	HFA1120Y	N/A	Die
CLC401A8D	HFA1100MJ/883	Yes	Better Performance
CLC401AID	HFA1100IJ	Yes	Better Performance
CLC401AID	HFA1-0005-9	*	Faster Transient Response
CLC401AJP	HFA1100IP	Yes	Better Performance
CLC401AJP	HFA3-0005-9	*	Faster Transient Response
CLC401ALC	HFA1100Y	N/A	Die
CLC402A8D	HFA1100MJ/883	Yes	Better Performance
CLC402AID	HFA1100IJ	Yes	Better Performance
CLC402AJE	HFA1100IB	Yes	Better Performance
CLC402AJP	HFA1100IP	Yes	Better Performance
CLC402ALC	HFA1100Y	N/A	Die
CLC402BJP	HFA3-0005-5	Yes	
CLC404A8D	HFA1100MJ/883	Yes	Better Performance
CLC404AID	HFA1100IJ	Yes	Better Performance
CLC404AJE	HFA1100IB	Yes	Better Performance

* Primary pins are pin-to-pin; Secondary/optional pins are not

Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
CLC404AJP	HFA1100IP	Yes	Better Performance
CLC404ALC	HFA1100Y	N/A	Die
CLC406A8D	HFA1100MJ/883	Yes	Better Performance
CLC406AID	HFA1100IJ	Yes	Better Performance
CLC406AJE	HFA1100IB	Yes	Better Performance
CLC406AJP	HFA1100IP	Yes	Better Performance
CLC406ALC	HFA1100Y	N/A	Die
CLC409A8D	HFA1100MJ/883	Yes	Better Performance
CLC409AID	HFA1100IJ	Yes	Better Performance
CLC409AJE	HFA1100IB	Yes	Better Performance
CLC409AJP	HFA1100IP	Yes	Better Performance
CLC409ALC	HFA1100Y	N/A	Better Performance
CLC410A8D	HFA1120MJ/883	*	CLC Has Enable
CLC410AID	HFA1120IJ	*	CLC Has Enable
CLC410AJE	HFA1120IB	*	CLC Has Enable
CLC410AJP	HFA1120IP	*	CLC Has Enable
CLC410ALC	HFA1120Y	N/A	CLC Has Enable
CLC420A8D	HFA7-0002/883	Yes	Use HFA For Gains >10
CLC420AID	HFA7-0002-9	Yes	Use HFA For Gains >10
CLC420AJE	HFA9P0002-9	Yes	Use HFA For Gains >10
CLC420AJP	HFA3-0001-5	Yes	
CLC420AJP	HFA3-0002-9	Yes	Use HFA For Gains >10
CLC420AJP	HFA3-0005-5	Yes	
CLC420B8D	HFA7-0002/883	Yes	Use HFA For Gains >10
CLC420BID	HFA7-0002-9	Yes	Use HFA For Gains >10
CLC420BJE	HFA9P0002-9	Yes	Use HFA For Gains >10
CLC420BJP	HFA3-0001-5	Yes	
CLC420BJP	HFA3-0002-9	Yes	Use HFA For Gains >10
CLC424A8D	HFA7-0002/883	Yes	Use HFA For Gains >10
CLC424AID	HFA7-0002-9	Yes	Use HFA For Gains >10
CLC424AJE	HFA9P0002-9	Yes	Use HFA For Gains >10
CLC424AJP	HFA3-0001-5	Yes	
CLC424AJP	HFA3-0002-9	Yes	Use HFA For Gains >10
CLC424AJP	HFA3-0005-5	Yes	
CLC430	HA-5020	Yes	Enhanced AC and Video Performance
CLC430AID	HA7-5020-9	Yes	Better AC Performance
CLC430AJE	HA9P5020-9	Yes	Better AC Performance
CLC430AJP	HA3-5020-9	Yes	Better AC Performance
CLC501A8D	HFA1130MJ/883	Yes	Better Performance
CLC501AID	HFA1130IJ	Yes	Better Performance
CLC501AJE	HFA1130IB	Yes	Better Performance
CLC501AJP	HFA1130IP	Yes	Better Performance
CLC502A8D	HFA1130MJ/883	Yes	Better Performance
CLC502AID	HFA1130IJ	Yes	Better Performance
CLC502AJE	HFA1130IB	Yes	Better Performance
CLC502AJP	HFA1130IP	Yes	Better Performance
EHA1-2539-2	HA1-2539-2	Yes	

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Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
EHA1-2539-5	HA1-2539-5	Yes	
EHA1-2539-5	HA1-2839-5	Yes	Lower Cost
EHA1-2539/883B	HA1-2839/883	Yes	Lower Cost
EHA1-2540-2	HA1-2540-2	Yes	
EHA1-2540-5	HA1-2540-5	Yes	
EHA1-2540-5	HA1-2840-5	Yes	Lower Cost
EHA1-2540/883	HA1-2840/883	Yes	Lower Cost
EHA1-5190-2	HA1-5190-2	Yes	
EHA1-5195-5	HA1-5195-5	Yes	
EHA2-2500-2	HA2-2500-2	Yes	
EHA2-2502-2	HA2-2502-2	Yes	
EHA2-2505-5	HA2-2505-5	Yes	
EHA2-2510-2	HA2-2510-2	Yes	
EHA2-2512-2	HA2-2512-2	Yes	
EHA2-2515-5	HA2-2515-5	Yes	
EHA2-2520-2	HA2-2520-2	Yes	Substitute HA2-2529-2
EHA2-2522-2	HA2-2522-2	Yes	Substitute HA2-2529-2
EHA2-2525-5	HA2-2525-5	Yes	Substitute HA2-2529-5
EHA2-2600-2	HA2-2600-2	Yes	
EHA2-2602-2	HA2-2602-2	Yes	
EHA2-2605-5	HA2-2605-5	Yes	
EHA2-2620-2	HA2-2620-2	Yes	
EHA2-2622-2	HA2-2622-2	Yes	
EHA2-2625-5	HA2-2625-5	Yes	
EHA2-5190-2	HA2-5190-2	Yes	
EHA2-5195-5	HA2-5195-5	Yes	
EHA3-2539-5	HA3-2539-5	Yes	
EHA3-2539-5	HA3-2839-5	Yes	Lower Cost
EHA3-2540-5	HA3B2840-5	Yes	Lower Cost
EHA3-2540-5	HA3-2540-5	Yes	
EHA7-2500-2	HA7-2500-2	Yes	
EHA7-2502-2	HA7-2502-2	Yes	
EHA7-2505-5	HA7-2505-5	Yes	
EHA7-2510-2	HA7-2510-2	Yes	
EHA7-2512-2	HA7-2512-2	Yes	
EHA7-2515-5	HA7-2515-5	Yes	
EHA7-2520-2	HA7-2520-2	Yes	
EHA7-2522-2	HA7-2522-2	Yes	
EHA7-2525-5	HA7-2525-5	Yes	
EHA7-2600-2	HA7-2600-2	Yes	
EHA7-2602-2	HA7-2602-2	Yes	
EHA7-2605-5	HA7-2605-5	Yes	
EHA7-2620-2	HA7-2620-2	Yes	
EHA7-2622-2	HA7-2622-2	Yes	
EHA7-2625-5	HA7-2625-5	Yes	
EL2003CH	HA2-5002-5	Yes	Greater Slew Rate/Reduced Icc
EL2003CJ	HA7-5002-5	No	Greater Slew Rate/Reduced Icc

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Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
EL2003CN	HA3-5002-5	No	Greater Slew Rate/Reduced Icc
EL2003CPL	HA9P5002-9	No	Greater Slew Rate/Reduced Icc
EL2003H	HA2-5002-2	Yes	Greater Slew Rate/Reduced Icc
EL2003J	HA7-5002-2	No	Greater Slew Rate/Reduced Icc
EL2005CG	HA2-5033-5	*	Greater Bandwidth
EL2005G	HA2-5033-2	*	Greater Bandwidth
EL2020CJ	HA7-5020-5	Yes	Better Performance
EL2020CM	HA9P5020-5	*	Enhanced ACs and DCs/Lower Cost
EL2020CN	HA3-5020-5	Yes	Better Performance
EL2020J	HA7-5020/883	Yes	Enhanced ACs and DCs/Lower Cost
EL2020J/883B	HA7-5020/883	Yes	Better Performance
EL2030CJ	HA7-5020-5	*	Enhanced DCs/Lower Cost
EL2030CN	HA3-5020-5	Yes	Disable Feature
EL2030J/883B	HA7-5020/883	*	Enhanced DCs/Lower Cost
EL2033CJ	HA7-5002-5	*	Greater Slew Rate/Reduced Icc
EL2033CN	HA3-5002-5	*	Greater Slew Rate/Reduced Icc
EL2033J	HA7-5002-2	*	Greater Slew Rate/Reduced Icc
EL2039CJ	HA1-2839-5	Yes	Lower Cost
EL2039CN	HA3-2839-5	Yes	Lower Cost
EL2039J	HA1-2839/883	Yes	Enhanced ACs/Lower Power/Lower Cost
EL2039J/883	HA1-2839/883	Yes	Lower Cost
EL2040CJ	HA1-2840-5	Yes	Lower Cost
EL2040CN	HA3B2840-5	Yes	Lower Cost
EL2040J	HA1-2840/883	Yes	Enhanced ACs/Lower Power/Lower Cost
EL2040J/883	HA1-2840/883	Yes	Lower Cost
EL2041CG	HA2-2541-5	Yes	Enhanced ACs/Lower Power/Lower Cost
EL2041CJ	HA1-2841-5	Yes	Enhanced ACs/Lower Power/Lower Cost
EL2041G	HA2-2841/883	Yes	Enhanced ACs/Lower Power/Lower Cost
EL2041J	HA1-2841/883	Yes	Enhanced ACs/Lower Power/Lower Cost
EL2044CN	HA3-2841-5	Yes	Low Power
EL2044CN	HA3-2841-5	*	
EL2044CS	HA9P2841-5	*	
EL2070CN	HFA1120IP	*	Better Performance
EL2070CS	HFA1120IB	*	Better Performance
EL2070J/883B	HFA1120MJ/883	*	Better Performance
EL2071CN	HFA1100IP	*	Better Performance
EL2071CS	HFA1120IB	*	Better Performance
EL2071J/883B	HFA1120MJ/883	*	Better Performance
EL2072CN	HFA1110IP	Yes	Better Performance
EL2072CS	HFA1110IB	Yes	Better Performance
EL2072J/883B	HFA1110MJ/883	Yes	Better Performance
EL2073CN	HFA3-0005-5	*	
EL2073CS	HFA9P0005-5	*	
EL2073J/883B	HFA7-0005/883	*	
EL2074CN	HFA3-0005-5	*	
EL2074CS	HFA9P0005-5	*	
EL2074J/883B	HFA7-0005/883	*	

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Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
EL2075CN	HFA3-0002-5	*	
EL2075CS	HFA9P0002-5	*	
EL2075J/883B	HFA7-0002/883	*	
EL2120CN	HA3-5020-5	Yes	Lower Power
EL2120CS	HA9P5020-5	Yes	Lower Power
EL2130CN	HFA1100IP	Yes	Better Performance
EL2130CS	HFA1100IB	Yes	Better Performance
EL2171CN	HFA1100IP	Yes	Better Performance
EL2171CS	HFA1100IB	Yes	Better Performance
EL2171J/883B	HFA1100IJ/883	Yes	Better Performance
EL2190G	HA2-5190-2	Yes	
EL2190J	HA1-5190-2	Yes	
EL2195CG	HA2-5195-5	Yes	
EL2195CJ	HA1-5195-5	Yes	
EL400CN	HFA1120IP	*	Better Performance
EL400CS	HFA1120IB	*	Better Performance
EL400J/883B	HFA1120MJ/883	*	Better Performance
ELH0032CG	HA2-2542-5	*	
ELH0032G	HA2-2542-2	*	
ELH0033CG	HA2-5033-5	*	Greater Bandwidth
ELH0033G	HA2-5033-2	*	Greater Bandwidth
HOS050	HA2-2542-2	*	Lower Cost
HOS050A	HA2-2542-2	*	Lower Cost
HOS050C	HA2-2542-2	*	Lower Cost
HOS-100AH	HA2-5033-2	*	Greater Bandwidth/Lower Cost
HOS-100SH	HA2-5033-2	*	Greater Bandwidth/Lower Cost
ICL7611ACPA	ICL7611ACPA	Yes	
ICL7611ACTV	ICL7611ACTV	Yes	
ICL7611AMTV	ICL7611AMTV	Yes	
ICL7611BCPA	ICL7611BCPA	Yes	
ICL7611BCTV	ICL7611BCTV	Yes	
ICL7611BMTV	ICL7611BMTV	Yes	
ICL7611DCPA	ICL7611DCPA	Yes	
ICL7611DCSA	ICL7611DCBA	Yes	
ICL7611DCTV	ICL7611DCTV	Yes	
ICL7611DMTV	ICL7611DMTV	Yes	
ICL7612ACPA	ICL7612ACPA	Yes	
ICL7612ACTV	ICL7612ACTV	Yes	
ICL7612AMTV	ICL7612AMTV	Yes	
ICL7612BCPA	ICL7612BCPA	Yes	
ICL7612BCTV	ICL7612BCTV	Yes	
ICL7612BMTV	ICL7612BMTV	Yes	
ICL7612DCPA	ICL7612DCPA	Yes	
ICL7612DCSA	ICL7612DCBA	Yes	
ICL7612DCTV	ICL7612DCTV	Yes	
ICL7612DMTV	ICL7612DMTV	Yes	
ICL7621ACPA	ICL7621ACPA	Yes	

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Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
ICL7621ACTV	ICL7621ACTV	Yes	
ICL7621AMTV	ICL7621AMTV	Yes	
ICL7621BCPA	ICL7621BCPA	Yes	
ICL7621BCTV	ICL7621BCTV	Yes	
ICL7621BMTV	ICL7621BMTV	Yes	
ICL7621DCPA	ICL7621DCPA	Yes	
ICL7621DCSA	ICL7621DCBA	Yes	
ICL7621DCTV	ICL7621DCTV	Yes	
ICL7621DMTV	ICL7621DMTV	Yes	
ICL7641CCPD	ICL7641CCPD	Yes	
ICL7641ECPD	ICL7641ECPD	Yes	
ICL7642CCJD	ICL7642CCJD	Yes	
ICL7642CCPD	ICL7642CCPD	Yes	
ICL7642CMJD	ICL7642CMJD	Yes	
ICL7642ECJD	ICL7642ECJD	Yes	
ICL7642ECPD	ICL7642ECPD	Yes	
ICL7642EMJD	ICL7642EMJD	Yes	
ICL7650BCPA-1	ICL7650SCPA-1	Yes	Reduced Vio/Ibias
ICL7650BCPD	ICL7650SCPD	Yes	Reduced Vio/Ibias
ICL7650BCTV-1	ICL7650SCTV-1	Yes	Reduced Vio/Ibias
ICM7242IPA	ICM7242IPA	Yes	
ICM7555CD	ICM7555CBA	Yes	
ICM7555CN	ICM7555IPA	Yes	Wider Operating Voltage Range
ICM7555IN	ICM7555IPA	Yes	Wider Operating Voltage Range
ICM7555IPA	ICM7555IPA	Yes	Wider Operating Voltage Range
ICM7555ITV	ICM7555ITV	Yes	
ICM7555MTV	ICM7555MTV	Yes	
ICM7556IPD	ICM7556IPD	Yes	Wider Operating Supply Range
ICM7556MJD	ICM7556MJD	Yes	Wider Operating Supply Range
KF351N	CA3140E	Yes	Reduced Ibias/Iio
KS272ACN	CA5260AE	Yes	Specified @ +5V Supply
KS272AIN	CA5260AE	Yes	Specified @ +5V Supply
KS272CN	CA5260E	Yes	Specified @ +5V Supply
KS272IN	CA5260E	Yes	Specified @ +5V Supply
KS274CN	CA5470E	Yes	Greater Bandwidth/Spec. @ +5V Supply
KS274IN	CA5470E	Yes	Greater Bandwidth/Spec. @ +5V Supply
LF157H	CA3130AT	Yes	Reduced Ibias
LF198AH	HA1-2420-2 (CDIP)	No	Faster Acquisition
LF198H	HA1-2420-2 (CDIP)	No	Faster Acquisition
LF351D	CA3140M	Yes	Reduced Ibias/Iio
LF351H	CA3140T	Yes	Reduced Ibias/Iio
LF351M	CA3140M	Yes	Reduced Ibias/Iio
LF351N	CA3140E	Yes	Reduced Ibias/Iio
LF351P	CA3140E	Yes	Reduced Ibias/Iio
LF353N	CA3240E	Yes	Reduced Ibias/Iio
LF353P	CA3240E	Yes	Reduced Ibias/Iio
LF357AH	CA3130AT	Yes	Reduced Ibias

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Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
LF357H	CA3130T	Yes	Reduced Ibias/Iio
LF357M	CA3130M	Yes	Reduced Ibias/Iio
LF357N	CA3130E	Yes	Reduced Ibias/Iio
LF398AH	HA1-2425-5 (CDIP)	No	Faster Acquisition
LF398AN	HA3-2425-5	No	Faster Acquisition
LF398H (CAN)	HA1-2425-5 (CDIP)	No	Faster Acquisition
LF398N	HA3-2425-5	No	Faster Acquisition
LF400CH	CA3100T	*	Similar ACs
LF411CD	CA3140AM	Yes	Reduced Ibias/Iio
LF411CH	CA3140AT	Yes	Reduced Ibias/Iio
LF411CN	CA3140AE	Yes	Reduced Ibias/Iio
LF411CP	CA3140AE	Yes	Reduced Ibias/Iio
LF411MH	CA3140AT	Yes	Reduced Ibias/Iio
LF412CD	CA3240AE	Yes	Reduced Ibias/Iio
LF412CN	CA3140AE	Yes	Reduced Ibias/Iio
LF412CP	CA3240AE	Yes	Reduced Ibias/Iio
LH0002CH	HA2-5002-5	*	Enhanced ACs/DCs/Monolithic
LH0002CN	HA3-5002-5	No	Enhanced ACs/DCs/Monolithic
LH0002H	HA2-5002-2	*	Enhanced ACs/DCs/Monolithic
LH0022CD	CA3140AE (PDIP)	No	Greater Bandwidth/Slew Rate
LH0022CH	CA3140AT	Yes	Greater Bandwidth/Slew Rate
LH0032ACG	HA2-2542-S	Yes	Monolithic/Lower Cost
LH0032AG	HA2-2542-2	Yes	Monolithic/Lower Cost
LH0032CG	HA2-2542-5	Yes	Monolithic/Lower Cost
LH0032G	HA2-2542-2	Yes	Monolithic/Lower Cost
LH0033ACG	HA2-5033-5	*	Greater Bandwidth/Monolithic/Lower Cost
LH0033AG	HA2-5033-2	*	Monolithic/Lower Cost
LH0033CG	HA2-5033-5	*	Greater Bandwidth/Monolithic/Lower Cost
LH0033CJ	HA3-5033-5	*	Monolithic/Lower Cost
LH0033G	HA2-5033-2	*	Monolithic/Lower Cost
LH0042CD	CA3140E (PDIP)	No	Greater Bandwidth/Slew Rate
LH0042CH	CA3140T	Yes	Greater Bandwidth/Slew Rate
LH4004CD	HA1-5004-5	No	Monolithic/Lower Cost
LH4004D	HA1-5004-9	No	Monolithic/Lower Cost
LH4161CH	HA2-2544-5	No	PDIP Substitute is HA3-2544C-5
LH4161CJ	HA7-2544-5	No	
LH4161H	HA2-2544-2	No	
LH4161J	HA7-2544-2	No	
LM143H	HA2-2640-2	*	Enhanced ACs
LM193H	CA3290AT	Yes	MOSFET Input
LM2901N	CA3290AE	Yes	MOSFET Input
LM2903N	CA3290AE	Yes	MOSFET Input
LM293H	CA3290AT	Yes	MOSFET Input
LM3045J	CA3045F	Yes	
LM3046D	CA3046M	Yes	
LM3046N	CA3046E	Yes	
LM3080AN	CA3080AE	Yes	

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Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
LM3080N	CA3080E	Yes	
LM3086J	CA3086F	Yes	
LM3086M	CA3086M	Yes	
LM3086N	CA3086	Yes	
LM3146M	CA3146M	Yes	Enhanced "A" Version Offered
LM3146N	CA3146E	Yes	Enhanced "A" Version Offered
LM3302N	CA3290E/LM3302N	Yes	
LM343H	HA2-2645-5	*	Enhanced ACs
LM393H	CA3290AT	Yes	MOSFET Input
LM393N	CA3290AE	Yes	MOSFET Input
LM556CN	ICM7556IPD	Yes	CMOS/Reduced Icc
LM604ACM	HA9P2406-5	No	Enhanced ACs
LM604ACN	HA3-2406-5	No	Enhanced ACs
LM604AMJ	HA1-2400-2	No	Enhanced ACs
LM604CM	HA9P2406-5	No	Enhanced ACs
LM604CN	HA3-2406-5	No	Enhanced ACs
LM6118J	HA7-5222-9	Yes	Lower Vio
LM6161J	HA7-2544-2	*	Guaranteed Differential Phase/Gain
LM6164J	HA1-5190-2	No	Reduced Voltage Noise
LM6165J	HA1-2540-2	No	Enhanced Slew Rate/Avol
LM6218AH	HA2-5222-9	No	Lower Vio
LM6218AJ	HA7-5222-9	Yes	Lower Vio
LM6361N	HA3-2544C-5	*	Guaranteed Differential Phase/Gain
LM6364N	HA1-5195-5	No	Reduced Voltage Noise
LM6365N	HA3-2540C-5	No	Enhanced Slew Rate/Avol
LMC555CH	ICM7555ITV	Yes	Reduced Icc/Wider Supply Range
LMC555CM	ICM7555CBA	Yes	Reduced Icc/Wider Supply 7yRange
LMC555CN	ICM7555IPA	Yes	Reduced Icc/Wider Supply Range
LMC668ACJ	ICL7650SIJD	Yes	Enhanced DCs
LMC668ACJ-8	ICL7650SIJA-1	Yes	Enhanced DCs
LMC668ACN	ICL7650SIPD	Yes	Enhanced DCs
LS204AT	HA2-5102-2	Yes	Reduced Noise Voltage
LS204CB	HA3-5102-5	Yes	Reduced Noise Voltage
LS204CM	HA9P-5102-5	Yes	Reduced Noise Voltage
LS204CT	HA2-5102-5	Yes	Reduced Noise Voltage
LS204T	HA2-5102-2	Yes	Reduced Noise Voltage
LS404CB	HA3-5104-5	Yes	Reduced Noise Voltage
LS404CM	HA9P-5104-5		Reduced Noise Voltage
LS404M	HA9P-5104-9		Reduced Noise Voltage
LS776CB	CA3440AE	Yes	MOS Input
LS776T	CA3440AT	Yes	MOS Input
LT1001CH	HA2-5177-5	Yes	Enhanced ACs/Reduced Icc
LT1001CJ8	HA7-5177-5	Yes	Enhanced ACs/Reduced Icc
LT1001MH	HA2-5177-2	Yes	Enhanced ACs/Reduced Icc
LT1001MJ8	HA7-5177-2	Yes	Enhanced ACs/Reduced Icc
LT1014ACJ	HA1-5134A-5	Yes	Reduced Vio/Enhanced ACs
LT1014ACJ	HA5234IJ	Yes	Lower Cost, Better ACs

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Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
LT1014AMJ	HA1-5134A-2	Yes	Reduced Vio/Enhanced ACs
LT1014CJ	HA1-5134-5	Yes	Reduced Vio/Enhanced ACs
LT1014CN	HA5234IP	Yes	Lower Cost, Better ACs
LT1014DN	HA5234IP	Yes	Lower Cost, Better ACs
LT1014MJ	HA1-5134-2	Yes	Reduced Vio/Enhanced ACs
LT1022CH	HA2-5160-5	*	Greater Bandwidth/Slew Rate
LT1022MH	HA2-5160-2	*	Greater Bandwidth/Slew Rate
LT1037ACH	HA2-5137A-5	Yes	Enhanced ACs/Reduced Icc
LT1037ACJ8	HA7-5137A-5	Yes	Enhanced ACs/Reduced Icc
LT1037AMH	HA2-5137A-2	Yes	Enhanced ACs/Reduced Icc
LT1037AMJ8	HA7-5137A-2	Yes	Enhanced ACs/Reduced Icc
LT1037CH	HA2-5137-5	Yes	Enhanced ACs/Reduced Icc
LT1037CJ8	HA7-5137-5	Yes	Enhanced ACs/Reduced Icc
LT1037MH	HA2-5137-2	Yes	Enhanced ACs/Reduced Icc
LT1037MJ8	HA7-5137-2	Yes	Enhanced ACs/Reduced Icc
LT1126ACN8	HA3-5222-5	Yes	
LT1126AMJ8	HA7-5222/883	Yes	
LT1126CJ8	HA7-5222-5	Yes	
LT1126CN8	HA3-5222-5	Yes	
LT1126MJ8	HA7-5222/883	Yes	
LT1190CJ8	HFA7-0005-5	*	Much Wider Bandwidth
LT1190CN8	HFA3-0005-5	*	Much Wider Bandwidth
LT1190CS8	HFA9P0005-5	*	Much Wider Bandwidth
LT1190MJ8	HFA7-0005/883	*	Much Wider Bandwidth
LT1191CJ8	HFA7-0005-5	*	Much Wider Bandwidth
LT1191CN8	HFA3-0005-5	*	Much Wider Bandwidth
LT1191CS8	HFA9P0005-5	*	Much Wider Bandwidth
LT1191MJ8	HFA7-0005/883	*	Much Wider Bandwidth
LT1192CJ8	HFA7-0002-5	*	For Gains >10
LT1192CN8	HFA3-0002-5	*	For Gains >10
LT1192CS8	HFA9P0002-5	*	For Gains >10
LT1192MJ8	HFA7-0002/883	*	For Gains >10
LT1220CN8	HA3-2841-5	Yes	
LT1221CN8	HA3-2841-5	Yes	
LT1221MJ8	HA7-2841/883	Yes	
LT1222CJ8	HA7-2840-5	*	
LT1222CN8	HA3-2840-5	*	
LT1222MJ8	HA7-2840/883	*	
LT1223CJ8	HA7-5020-5	Yes	Better Video Specifications
LT1223CJ8	HA7-5020-5	Yes	Enhanced ACs and Video Performance
LT1223CN8	HA3-5020-5	Yes	Better Video Specifications
LT1223CN8	HA3-5020-5	Yes	Enhanced ACs and Video Performance
LT1223CS8	HA9P5020-5	Yes	Enhanced ACs and Video Performance
LT1223CS8	HA9P5020-5	Yes	Better Video Specifications
LT1223MJ8	HA7-5020/883	Yes	Better Video Specifications
LT1223MJ8	HA7-5020/883	Yes	Enhanced ACs and Video Performance
LT1224CN8	HA3-2841-5	Yes	Better Video Specifications

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Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
LT1224CS8	HA9P2841-5	Yes	Better Video Specifications
LT1224MJ8	HA7-2841/883	Yes	Better Video Specifications
LT1225CN8	HA3-2841-5	Yes	For Gains > 5
LT1225CS8	HA9P2841-5	Yes	For Gains > 5
LT1225MJ8	HA7-2841/883	Yes	For Gains > 5
LT1226CJ8	HA7-2840-5	*	For Gains > 25
LT1226CN8	HA3-2840-5	*	For Gains > 25
LT1226CS8	HA9P2840-5	*	For Gains > 25
LT1226MJ8	HA7-2840/883	*	For Gains > 25
LT1227CN8	HA3-5020-5	Yes	Lower Cost
LT1227CS8	HA9P5020-5	Yes	Lower Cost
LT1227MJ8	HA7-5020/883	Yes	Lower Cost
LTC1050ACH	ICL7650SITV-1	*	Reduced Ibias/Iio
LTC1050ACN8	ICL7650SIPA-1	*	Reduced Ibias/Iio
LTC1050AMH	ICL7650SMTV-1	*	Reduced Ibias/Iio
LTC1050CH	ICL7650SITV-1	*	Reduced Ibias/Iio/Greater Avol
LTC1050CN8	ICL7650SIPA-1	*	Reduced Ibias/Iio/Greater Avol
LTC1050CP	ICL7650SIPA-1	*	Reduced Ibias/Iio
LTC1050MH	ICL7650SMTV-1	*	Reduced Ibias/Iio/Greater Avol
MAX460IGC	HA2-5033-5	*	Greater Bandwidth
MAX460MGC	HA2-5033-2	*	Greater Bandwidth
MAX9685CJE	HFA1-0003L-5	Yes	Better Performance
MAX9685CPE	HFA3-0003L-5	Yes	Better Performance
MAX9685CSE	HFA9P0003L-5	Yes	
MAX9685CTW	HFA2-0003L-5	Yes	Better Performance
MAX9690CJA	HFA1-0003L-5	Yes	Better Performance
MAX9690CPA	HFA3-0003-5	Yes	Better Performance
MAX9690CSA	HFA9P0003-5	Yes	
MC1776CD	ICL7611DCBA	Yes	Lower Power Drain
MC1776CG	ICL7611BCTV	Yes	Lower Power Drain
MC1776CP1	ICL7611BCPA	Yes	Lower Power Drain
MC1776G	ICL7611BMTV	Yes	Lower Power Drain
MC3302N	CA3290E	Yes	MOSFET Input
MC3303D	CA5470M	Yes	MOS Input/Enhanced ACs
MC3303N	CA5470E	Yes	FEMOS Input/Enhanced ACs
MC33071P	CA3140AE	Yes	Reduced Ibias/Iio
MC33072P	CA3240AE	Yes	Reduced Ibias/Iio
MC3346D	CA3046M	Yes	Full - 55 to 125 Degrees C Operation
MC3346P	CA3046E	Yes	Full -55 to 125 Degrees C Operation
MC34001BG	CA3140AT	Yes	Reduced Ibias/Iio
MC34001BP	CA3140AE	Yes	Reduced Ibias/Iio
MC34001G	CA3140T	Yes	Reduced Ibias/Iio
MC34001P	CA3140E	Yes	Reduced Ibias/Iio
MC34002BG	CA3240AT	Yes	Reduced Ibias/Iio
MC34002BP	CA3240AE	Yes	Reduced Ibias/Iio
MC34002G	CA3240T	Yes	Reduced Ibias/Iio
MC34002P	CA3240E	Yes	Reduced Ibias/Iio

* Primary pins are pin-to-pin; Secondary/optional pins are not

Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
MC3403D	CA5470M	Yes	MOS Input/Enhanced ACs
MC3403N	CA5470E	Yes	MOS Input/Enhanced ACs
MC34071P	CA3140AE	Yes	Reduced Ibias/Iio
MC34072P	CA3240AE	Yes	Reduced Ibias/Iio
MC3456L	ICM7556MJD	Yes	CMOS/Reduced Icc
MC3456P	ICM7556IPD	Yes	CMOS/Reduced Icc
MC3556L	ICM7556MJD	Yes	CMOS/Reduced Icc
MC668ACN-8	ICL7650SCPA-1	Yes	Enhanced DCs
NE5230N	CA5160AE	No	MOS Input
NE5517AN	CA3280AE	No	Reduced Vio
NE5517D	CA3280M	No	Reduced Vio
NE5517N	CA3280E	No	Reduced Vio
NE5532AFE	HA7-5102-5	Yes	Enhanced DCs/Reduced Icc
NE5532AN	HA3-5102-5	Yes	Enhanced DCs/Reduced Icc
NE5532FE	HA7-5102-5	Yes	Enhanced DCs/Reduced Icc
NE5532N	HA3-5102-5	Yes	Enhanced DCs/Reduced Icc
NE5534AFE	HA7-5101-5	*	Enhanced DCs
NE5534AN	HA3-5101-5	*	Enhanced DCs
NE5534FE	HA7-5101-5	*	Enhanced DCs
NE5534N	HA3-5101-5	*	Enhanced DCs
NE5539D	HA9P-2539-5	*	Specified @ +/- 15V Supplies
NE5539F	HA1-2839-5	*	Specified @ +/- 15V Supplies
NE5539N	HA3-2839-5	*	Specified @ +/- 15V Supplies
NE556N	ICM7556IPD	Yes	CMOS/Reduced Icc
NE556-1N	ICM7556IPD	Yes	CMOS/Reduced Icc
OP11AY	HA1-5134-2	Yes	Enhanced ACs
OP11EY	HA1-5134-5		Enhanced ACs
OP11FY	HA1-5104-5	Yes	Enhanced ACs
OP160GP	HA3-5020-9	Yes	
OP160GS	HA9P5020-5	Yes	
OP215GZ	CA3240AE (PDIP)	Yes	
OP220CJ	HA2-5142-2	Yes	Enhanced ACs
OP220CZ	HA7-5142-2	Yes	Enhanced ACs
OP220GJ	HA2-5142-5	Yes	Enhanced ACs
OP220GZ	HA7-5142-5	Yes	Enhanced ACs
OP271AZ	HA7-5102-2	Yes	Lower Voltage Noise/Greater Bandwidth
OP271EZ	HA7-5102-5	Yes	Lower Voltage Noise/Greater Bandwidth
OP271FZ	HA7-5102-5	Yes	Lower Voltage Noise/Greater Bandwidth
OP271GP	HA3-5102-5	Yes	Lower Voltage Noise/Greater Bandwidth
OP271GS	HA9P-5102-9	Yes	Lower Voltage Noise/Greater Bandwidth
OP27AH	HA2-5127A-2	Yes	Enhanced ACs/Reduced Icc
OP27AJ	HA2-5127A-2	Yes	Enhanced ACs/Reduced Icc
OP27AJ8	HA7-5127A-2	Yes	Enhanced ACs/Reduced Icc
OP27AZ	HA7-5127A-2	Yes	Enhanced ACs/Reduced Icc
OP27CH	HA2-5127-2	Yes	Enhanced ACs/Reduced Icc
OP27CJ	HA2-5127-2	Yes	Enhanced ACs/Reduced Icc
OP27CJ8	HA7-5127-2	Yes	Enhanced ACs/Reduced Icc

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Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
OP27CZ	HA7-5127-2	Yes	Enhanced ACs/Reduced Icc
OP27EH	HA2-5127A-5	Yes	Enhanced ACs/Reduced Icc
OP27EJ	HA2-5127A-5	Yes	Enhanced ACs/Reduced Icc
OP27EJ8	HA7-5127A-5	Yes	Enhanced ACs/Reduced Icc
OP27EZ	HA7-5127A-5	Yes	Enhanced ACs/Reduced Icc
OP27GH	HA2-5127-5	Yes	Enhanced ACs/Reduced Icc
OP27GJ	HA2-5127-5	Yes	Enhanced ACs/Reduced Icc
OP27GJ8	HA7-5127-5	Yes	Enhanced ACs/Reduced Icc
OP27GZ	HA7-5127-5	Yes	Enhanced ACs/Reduced Icc
OP37AH	HA2-5137A-2	Yes	Enhanced ACs/Reduced Icc
OP37AJ	HA2-5137A-2	Yes	Enhanced ACs/Reduced Icc
OP37AJ8	HA7-5137A-2	Yes	Enhanced ACs/Reduced Icc
OP37AZ	HA7-5137A-2	Yes	Enhanced ACs/Reduced Icc
OP37CH	HA2-5137-2	Yes	Enhanced ACs/Reduced Icc
OP37CJ	HA2-5137-2	Yes	Enhanced ACs/Reduced Icc
OP37CJ8	HA7-5137-2	Yes	Enhanced ACs/Reduced Icc
OP37CZ	HA7-5137-2	Yes	Enhanced ACs/Reduced Icc
OP37EH	HA2-5137A-5	Yes	Enhanced ACs/Reduced Icc
OP37EJ	HA2-5137A-5	Yes	Enhanced ACs/Reduced Icc
OP37EJ8	HA7-5137A-5	Yes	Enhanced ACs/Reduced Icc
OP37EZ	HA7-5137A-5	Yes	Enhanced ACs/Reduced Icc
OP37GH	HA2-5137-5	Yes	Enhanced ACs/Reduced Icc
OP37GJ	HA2-5137-5	Yes	Enhanced ACs/Reduced Icc
OP37GJ8	HA7-5137-5	Yes	Enhanced ACs/Reduced Icc
OP37GZ	HA7-5137-5	Yes	Enhanced ACs/Reduced Icc
OP400AY	HA1-5134A-2	Yes	
OP400EY	HA1-5134A-5	Yes	
OP400EY	HA5234IJ	Yes	Lower Cost, Better ACs
OP400FY	HA1-5134-5	Yes	
OP400FY	HA5234IJ	Yes	Lower Cost, Better ACs
OP400GP	HA5234IP	Yes	Lower Cost, Better ACs
OP400GS	HA5234IB	Yes	Lower Cost, Better ACs
OP400HP	HA5234IP	Yes	Lower Cost, Better ACs
OP400HS	HA5234IB	Yes	Lower Cost, Better ACs
OP41EJ	CA3193AT	Yes	Reduced Vio/Noise Voltage
OP41FJ	CA3193T	Yes	Reduced Vio/Noise Voltage
OP41GP	CA3193E	Yes	Reduced Vio/Noise Voltage
OP420BY	HA1-5144-2	Yes	Enhanced ACs
OP420CY	HA1-5144-2	Yes	Enhanced ACs
OP420HY	HA1-5144-5	Yes	Enhanced ACs
OP470AY	HA1-5104-2	Yes	
OP470EY	HA1-5104-5	Yes	
OP470FY	HA1-5104-5	Yes	
OP470GP	HA3-5104-5	Yes	
OP470GS	HA9P5104-5	Yes	
OP47AD	HA7-5147A-2	Yes	Greater Bandwidth/Min Acl=10
OP47AT	HA2-5147A-2	Yes	Greater Bandwidth/Min Acl=10

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Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
OP47CD	HA7-5147-2	Yes	Greater Bandwidth/Min Acl=10
OP47CT	HA2-5147-2	Yes	Greater Bandwidth/Min Acl=10
OP47EN	HA7-5147A-5 (CDIP)	Yes	Greater Bandwidth/Min Acl=10
OP47GN	HA7-5147-5 (CDIP)	Yes	Greater Bandwidth/Min Acl=10
OP62AJ	HA2-5221-9	*	Greater Slew Rate
OP62AZ	HA7-5221-9	*	Greater Slew Rate
OP62EJ	HA2-5221-9	*	Greater Slew Rate
OP62EZ	HA7-5221-9	*	Greater Slew Rate
OP62FJ	HA2-5221-9	*	Greater Slew Rate
OP62FZ	HA7-5221-9	*	Greater Slew Rate
OP63AJ	HA2-5221-9	*	Reduced Vio
OP63AZ	HA7-5221-9	*	Reduced Vio
OP63EJ	HA2-5221-9	*	Reduced Vio
OP63EZ	HA7-5221-9	*	Reduced Vio
OP63FJ	HA2-5221-9	*	Reduced Vio
OP63FZ	HA7-5221-9	*	Reduced Vio
OP64AJ	HA2-5221-9	*	Reduced Vio
OP64AZ	HA7-5221-9	*	Reduced Vio
OP64EJ	HA2-5221-9	*	Reduced Vio
OP64EZ	HA7-5221-9	*	Reduced Vio
OP64FJ	HA2-5221-9	*	Reduced Vio
OP64FZ	HA7-5221-9	*	Reduced Vio
OP65AJ	HA2-2548-9	*	Lower Vio/Guaranteed Ts
OP65AZ	HA7-2548-9	*	Lower Vio/Guaranteed Ts
OP65EJ	HA2-2548-9	*	Lower Vio/Guaranteed Ts
OP65EZ	HA7-2548-9	*	Lower Vio/Guaranteed Ts
OP65FJ	HA2-2548-9	*	Lower Vio/Guaranteed Ts
OP65FZ	HA7-2548-9	*	Lower Vio/Guaranteed Ts
OP65GP	CA3450E	No	Greater Bandwidth /Slew Rate
OP77BJ	HA2-5177-2	Yes	Greater Bandwidth/Reduced Icc
OP77BZ	HA7-5177-2	Yes	Greater Bandwidth/Reduced Icc
OP77FJ	HA2-5177-5	Yes	Greater Bandwidth/Reduced Icc
OP77FZ	HA7-5177-5	Yes	Greater Bandwidth/Reduced Icc
OP80FJ	CA5420AT	*	Single Supply Operation
OP80GJ	CA5420T	*	Single Supply Operation
OP80GP	CA5420E	*	Single Supply Operation
OPA121KP	CA3140AE	*	MOS Input/Enhanced ACs
OPA2111KM	HA2-5102-5	Yes	Greater Bandwidth
OPA2111KP	HA3-5102-5	Yes	Greater Bandwidth
OPA27AJ	HA2-5127A-2	Yes	Enhanced ACs/Reduced Icc
OPA27AZ	HA7-5127A-2	Yes	Enhanced ACs/Reduced Icc
OPA27CJ	HA2-5127-2	Yes	Enhanced ACs/Reduced Icc
OPA27CZ	HA7-5127-2	Yes	Enhanced ACs/Reduced Icc
OPA27EJ	HA2-5127A-5	Yes	Enhanced ACs/Reduced Icc
OPA27EZ	HA7-5127A-5	Yes	Enhanced ACs/Reduced Icc
OPA27GJ	HA2-5127-5	Yes	Enhanced ACs/Reduced Icc
OPA27GZ	HA7-5127-5	Yes	Enhanced ACs/Reduced Icc

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Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
OPA37AJ	HA2-5137A-2	Yes	Enhanced ACs/Reduced Icc
OPA37AZ	HA7-5137A-2	Yes	Enhanced ACs/Reduced Icc
OPA37CJ	HA2-5137-2	Yes	Enhanced ACs/Reduced Icc
OPA37CZ	HA7-5137-2	Yes	Enhanced ACs/Reduced Icc
OPA37EJ	HA2-5137A-5	Yes	Enhanced ACs/Reduced Icc
OPA37EZ	HA7-5137A-5	Yes	Enhanced ACs/Reduced Icc
OPA37GJ	HA2-5137-5	Yes	Enhanced ACs/Reduced Icc
OPA37GZ	HA7-5137-5	Yes	Enhanced ACs/Reduced Icc
OPA404AG	HA1-5114-5	Yes	Lower Voltage Noise/Enhanced ACs
OPA404BG	HA1-5114-5	Yes	Lower Voltage Noise/Enhanced ACs
OPA404KP	HA3-5114-5	Yes	Lower Voltage Noise/Enhanced ACs
OPA404KU	HA9P-5114-5	Yes	Lower Voltage Noise/Enhanced ACs
OPA404SG	HA1-5114-2	Yes	Lower Voltage Noise/Enhanced ACs
OPA445AP	HA7-2645-5	Yes	
OPA445BM	HA2-2640-2	Yes	
OPA445SM	HA2-2640-2	Yes	
OPA620KG	HFA7-0005-5	*	Enhanced ACs
OPA620KP	HFA3-0005-5	*	Enhanced ACs
OPA620LG	HFA7-0005-5	*	Enhanced ACs
OPA620SG	HFA7-0005-9	*	Enhanced ACs
OPA621KG	HFA7-0002-5	*	Lower Voltage Noise/Temco
OPA621KP	HFA3-0002-5	*	Lower Voltage Noise/Temco
OPA621LG	HFA7-0002-5	*	Lower Voltage Noise/Temco
OPA621SG	HFA7-0002-9	*	Lower Voltage Noise/Temco
OPA633AH	HA2-5033-2	Yes	
OPA633KP	HA3-5033-5	Yes	
OPA633SH	HA2-5033-5	Yes	
OP-15CH	CA3140AT	Yes	Reduced Ibias/Iio
OP-15GN8	CA3140AE	Yes	Reduced Ibias/Iio
RC3403AN	CA5470E	Yes	MOS Input/Enhanced ACs
RC4741D	HA1-4741-2	Yes	Guaranteed ACs
RC4741M	HA9P-4741-5	Yes	Guaranteed ACs
RC5532AN	HA3-5102-5	Yes	Enhanced DCs/Reduced Icc
RC5532N	HA3-5102-5	Yes	Enhanced DCs/Reduced Icc
RC5534AN	HA3-5101-5	*	Enhanced DCs/Reduced Icc
RC5534N	HA3-5101-5	*	Enhanced DCs/Reduced Icc
RM5334T	HA2-5101-2	*	Reduced Icc
RM5532AD	HA7-5102-2	Yes	Reduced Icc
RM5532AT	HA2-5102-2	Yes	Reduced Icc
RM5532D	HA7-5102-2	Yes	Reduced Icc
RM5532T	HA2-5102-2	Yes	Reduced Icc
RM5534AD	HA7-5101-2	*	Reduced Icc
RM5534AT	HA2-5101-2	*	Reduced Icc
RM5534D	HA7-5101-2	*	Reduced Icc
SA5230N	CA5160AE	No	MOS Input
SA556N	ICM7556IPD	Yes	CMOS/Reduced Icc
SA556-1N	ICM7556IPD	Yes	CMOS/Reduced Icc

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Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
SE5532AFE	HA7-5102-2	Yes	Reduced Icc
SE5532FE	HA7-5102-2	Yes	Reduced Icc
SE5534AFE	HA7-5101-2	*	Reduced Ibias/Iio
SE5534FE	HA7-5101-2	*	Reduced Ibias/Iio
SE5539F	HA1-2539-2	*	Specified @ +/- 15V Supplies
SE556F	ICM7556MJD	Yes	CMOS/Reduced Icc
SE556-1CN	ICM7556MJD	Yes	CMOS/Reduced Icc
SE556-1F	ICM7556MJD	Yes	CMOS/Reduced Icc
SG1536T	HA2-2640-2	*	Reduced Vio/Enhanced ACs
SG1536Y	HA7-2640-2	*	Reduced Vio/Enhanced ACs
SG3045J	CA3045F	Yes	
SG3049T	CA3049T	Yes	Greater Bandwidth/Reduced Noise
SG3083	CA3083	Yes	
SG3183D	CA3183M	Yes	Identical Specs @ 25 degrees C
SG3183N	CA3183E	Yes	Identical Specs @ 25 degrees C
SHC5320KH	HA1-5320-5	Yes	
SHC5320SH	HA1-5320-2	Yes	
SHC85	HA1-2425-5	No	Enhanced ACs
SHC85ET	HA1-2420-2	No	Enhanced ACs
SHM-20C	HA1-5320-5	Yes	Guaranteed Acquisition Time
SHM-20M	HA1-5320-2	Yes	Guaranteed Acquisition Time
SHM-IC-1	HA1-2425-5	Yes	Almost Identical
SHM-IC-1M	HA1-2420-2	Yes	Almost Identical
SL3045C-DG	CA3045F	Yes	
SL3046C-DP	CA3046E	Yes	
SL3127C-DC	CA3127F	Yes	SOIC Version Available
SL3127C-DP	CA3127E	Yes	
SL3145C-DC	CA3045F	Yes	Greater Breakdown Voltages
SL3145C-DP	CA3046E	Yes	Greater Breakdown Voltages
SL3227-DP	CA3227E	Yes	Greater Breakdown Voltages
SL3227-MP	CA3227M	Yes	Greater Breakdown Voltages
SL3245-DP	CA3246E	Yes	Programmable Biasing Current
SL3245-MP	CA3246M	Yes	Faster Acquisition/Lower Droop
SL6310C-DP	CA3094E	No	Faster Acquisition/Lower Droop
SMP10AY	HA1-2420-2	*	Faster Acquisition/Lower Droop
SMP10BY	HA1-2420-2	*	Faster Acquisition/Lower Droop
SMP10EY	HA1-2425-5	*	Faster Acquisition/Lower Droop
SMP10FY	HA1-2425-5	*	Faster Acquisition/Lower Droop
SMP11AY	HA1-2420-2	*	Faster Acquisition/Lower Droop
SMP11BY	HA1-2420-2	*	Faster Acquisition/Lower Droop
SMP11EY	HA1-2425-5	*	*
SMP11FY	HA1-2425-5	*	*
SP1-2541-2	HA1-2541-2	Yes	
SP1-2541-5	HA1-2541-5	Yes	
SP1-2542-2	HA1-2542-2	Yes	
SP1-2542-5	HA1-2542-5	Yes	
SP1-5330-2	HA1-5330-2	Yes	

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Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
SP1-5330-5	HA1-5330-5	Yes	
SP2-2500-2	HA2-2500-2	Yes	
SP2-2502-2	HA2-2502-2	Yes	
SP2-2505-5	HA2-2505-5	Yes	
SP2-2510-2	HA2-2510-2	Yes	
SP2-2512-2	HA2-2512-2	Yes	
SP2-2515-5	HA2-2515-5	Yes	
SP2-2520-2	HA2-2520-2	Yes	Substitute HA2-2529-2
SP2-2522-2	HA2-2522-2	Yes	Substitute HA2-2529-2
SP2-2525-5	HA2-2525-5	Yes	Substitute HA2-2529-5
SP2-2541-2	HA2-2541-2	Yes	
SP2-2541-5	HA2-2541-5	Yes	
SP2-2542-2	HA2-2542-2	Yes	
SP2-2542-5	HA2-2542-5	Yes	
SP2-2600-2	HA2-2600-2	Yes	
SP2-2602-2	HA2-2602-2	Yes	
SP2-2605-5	HA2-2605-5	Yes	
SP2-2620-2	HA2-2620-2	Yes	
SP2-2622-2	HA2-2622-2	Yes	
SP2-2625-5	HA2-2625-5	Yes	
SP3-2505-5	HA3-2505-5	Yes	
SP3-2515-5	HA3-2515-5	Yes	
SP3-2525-5	HA3-2525-5	Yes	Substitute HA3-2529-5
SP3-2542-5	HA3B2842-5	Yes	
SP3-2605-5	HA3-2605-5	Yes	
SP3-2625-5	HA3-2625-5	Yes	
SP7-2500-2	HA7-2500-2	Yes	
SP7-2502-2	HA7-2502-2	Yes	
SP7-2505-5	HA7-2505-5	Yes	
SP7-2510-2	HA7-2510-2	Yes	
SP7-2512-2	HA7-2512-2	Yes	
SP7-2515-5	HA7-2515-5	Yes	
SP7-2520-2	HA7-2520-2	Yes	Substitute HA7-2529-2
SP7-2522-2	HA7-2522-2	Yes	Substitute HA7-2529-2
SP7-2525-5	HA7-2525-5	Yes	Substitute HA7-2529-5
SP7-2600-2	HA7-2600-2	Yes	
SP7-2602-2	HA7-2602-2	Yes	
SP7-2605-5	HA7-2605-5	Yes	
SP7-2620-2	HA7-2620-2	Yes	
SP7-2622-2	HA7-2622-2	Yes	
SP7-2625-5	HA7-2625-5	Yes	
TA75393P	CA3290AE/CA3290E	Yes	Reduced Ibias/Iio/Icc
TA75557F	HA9P5102-9	No	Greater Bandwidth/Reduced Vnoise
TA75557P	HA3-5102-5	Yes	Greater Bandwidth/Reduced Vnoise
TA75559F	HA9P5112-9	No	Greater Bandwidth/Reduced Vnoise
TA75559P	HA3-5112-5	Yes	Greater Bandwidth/Reduced Vnoise
TCA520BN	CA5130AE	*	MOS Input/Enhanced ACs

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Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
TCA520TD	CA5130M	*	MOS Input/Enhanced ACs
TCA971	CA3146AE/CA3046E	Yes	Greater Vcbo With CA3146
TCA971G	CA3146AM/CA3046M	Yes	Greater Vcbo With CA3146
TCA991	CA3146E/CA3046E	Yes	Greater Vcbo With CA3146
TCA991G	CA3146M/CA3046M	Yes	Greater Vcbo With CA3146
TD62507F	CA3183AM	No	Alt. Product Is CA3083
TD62507P	CA3183AE	No	Alt. Product Is CA3083
TDB2046DP	CA3046E	Yes	Full -55 to 125 Degrees C Operation
TDB2046FP	CA3046M	Yes	Full -55 to 125 Degrees C Operation
TLC251ACP	CA3440AE	*	
TLC251CP	CA3440E	*	
TLC252ACD	CA5260AM	Yes	Specified @ +5V Supply
TLC252ACP	CA5260AE	Yes	Specified @ +5V Supply
TLC252CD	CA5260M	Yes	Specified @ +5V Supply
TLC252CP	CA5260E	Yes	Specified @ +5V Supply
TLC254CD	CA5470M	Yes	Specified @ +5V Supply
TLC254CN	CA5470E	Yes	Specified @ +5V Supply
TLC272ACD	CA5260AM	Yes	Greater Vout Range/Reduced Icc
TLC272ACP	CA5260AE	Yes	Greater Vout Range/Reduced Icc
TLC272AID	CA5260AM	Yes	Greater Vout Range/Reduced Icc
TLC272AIP	CA5260AE	Yes	Greater Vout Range/Reduced Icc
TLC272CD	CA5260M	Yes	Greater Vout Range/Reduced Icc
TLC272CP	CA5260E	Yes	Greater Vout Range/Reduced Icc
TLC272ID	CA5260M	Yes	Greater Vout Range/Reduced Icc
TLC272IP	CA5260E	Yes	Greater Vout Range/Reduced Icc
TLC272MJG	CA5260E (PDIP)	Yes	Greater Vout Range/Reduced Icc
TLC274CD	CA5470M	Yes	Greater Vout/Bandwidth/Slew Rate
TLC274CN	CA5470E	Yes	Greater Vout/Bandwidth/Slew Rate
TLC274ID	CA5470M	Yes	Greater Vout/Bandwidth/Slew Rate
TLC274IN	CA5470E	Yes	Greater Vout/Bandwidth/Slew Rate
TLC274MJ	CA5470E (PDIP)	Yes	Greater Vout/Bandwidth/Slew Rate
TLC27M2ACD	CA5260AM	Yes	Greater Vout/Bandwidth/Slew Rate
TLC27M2ACP	CA5260AE	Yes	Greater Vout/Bandwidth/Slew Rate
TLC27M2AID	CA5260AM	Yes	Greater Vout/Bandwidth/Slew Rate
TLC27M2AIP	CA5260AE	Yes	Greater Vout/Bandwidth/Slew Rate
TLC27M2CD	CA5260M	Yes	Greater Vout/Bandwidth/Slew Rate
TLC27M2CP	CA5260E	Yes	Greater Vout/Bandwidth/Slew Rate
TLC27M2ID	CA5260M	Yes	Greater Vout/Bandwidth/Slew Rate
TLC27M2IP	CA5260E	Yes	Greater Vout/Bandwidth/Slew Rate
TLC27M2MJG	CA5260E (PDIP)	Yes	Greater Vout/Bandwidth/Slew Rate
TLC555CD	ICM7555CBA	Yes	Reduced Icc
TLC555IP	ICM7555IPA	Yes	Reduced Icc
TLC556CN	ICM7556IPD	Yes	Reduced Icc
TLC556IN	ICM7556IPD	Yes	Reduced Icc
TLC556MJ	ICM7556MJD	Yes	Reduced Icc
TP1321	HA-5195	Yes	
TP1322	HA-2520	Yes	

* Primary pins are pin-to-pin; Secondary/optional pins are not

Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
TP1326	HA-2600	Yes	
TP1332	HA-2645	Yes	
TP1339	HA-2620	No	
TP1341	HA-2840	Yes	
TP1342	HA-2839	Yes	
TP1344	HA-5160	Yes	
TP1345	HA-5162	Yes	
TP4856	HA1-2420/25	Yes	Guaranteed Acquisition Time
TP4866	HA1-5320	Yes	Guaranteed Acquisition Time
TSC7650ACPA	ICL7650SCPA-1	Yes	Reduced Tempco/Voltage Noise
TSC7650ACPD	ICL7650SCPD	Yes	Reduced Tempco/Voltage Noise
TSC7650AIJA	ICL7650SIJA-1	Yes	Reduced Tempco/Voltage Noise
TSC7650AIJD	ICL7650SIJD	Yes	Reduced Tempco/Voltage Noise
UC0P01CN	CA3140AE	Yes	MOSFET Input
UC0P01GJ	CA3140AE (PDIP)	Yes	MOSFET Input
ULN2046A-1	CA3146E	Yes	Full -40 to 85 Degree C Operation
ULN2046L-1	CA3146M	Yes	
ULN2083A	CA3083	Yes	Full -55 to 125 Degree C Operation
ULN2083A-1	CA3183E	Yes	Full -40 to 85 Degree C Operation
ULN2083L	CA3083M	Yes	Full -55 to 125 Degree C Operation
ULN2086A	CA3086	Yes	Full -55 to 125 Degree C Operation
uPA103G	HFA3046B	Yes	Lower Cost
uPC357C	CA3130E	Yes	Reduced Ibias
uPC4741C	HA3-4741-5	Yes	Guaranteed Specs Over Temp
uPC4741G2	HA9P4741-5	*	Guaranteed Specs Over Temp
uPD5555C	ICM7555CPA	Yes	Reduced Icc
uPD5556C	ICM7556CPD	Yes	Reduced Icc
XR-13600AP	CA3280AE	No	Reduced Vio/Enhanced ACs
XR-13600CP	CA3280E	No	Reduced Vio/Enhanced ACs
XR-2242CP	ICM7242IPA	Yes	Greatly Reduced Icc
XR-3403CP	CA5470E	Yes	MOS Input/Enhanced ACs
XR-4739CN	HA7-5102-5	No	Enhanced ACs/DCs
XR-4739CP	HA3-5102-5	No	Enhanced ACs/DCs
XR-4741CN	HA1-4741-5	Yes	Guaranteed Channel Separation
XR-4741CP	HA3-4741-5	Yes	Guaranteed Channel Separation
XR-4741M	HA1-4741-2	Yes	Guaranteed Channel Separation
XR-5532AN	HA7-5102-5	Yes	Reduced Vio/Ibias
XR-5532AP	HA3-5102-5	Yes	Reduced Vio/Ibias
XR-5532N	HA7-5102-5	Yes	Reduced Vio/Ibias
XR-5532P	HA3-5102-5	Yes	Reduced Vio/Ibias
XR-5534ACN	HA7-5101-5	*	Greater Avol/Reduced Vio
XR-5534ACP	HA3-5101-5	*	Greater Avol/Reduced Vio
XR-5534AM	HA7-5101-2	*	Greater Avol
XR-5534CN	HA7-5101-5	*	Greater Avol/Reduced Vio
XR-5534CP	HA3-5101-5	*	Greater Avol/Reduced Vio
XR-5534M	HA7-5101-2	*	Greater Avol
XR-8038CN	ICL8038CCJD	Yes	

* Primary pins are pin-to-pin; Secondary/optional pins are not

Commercial Linear Product Cross Reference (Continued)

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
XR-8038CP	ICL8038CCPD	Yes	
XR-8038M	ICL8038AMJD	Yes	
XR-8038N	ICL8038BCJD	Yes	
APPLICATION-SPECIFIC PRODUCTS FOR TELECOMMUNICATION APPLICATIONS			
M3493	CD22M3493	Yes	
M093	CD22M3493	Yes	
MT8812	CD22M3493	Yes	
78A093A	CD22M3493	Yes	
M3494	CD22M3494	Yes	
MT8816	CD22M3494	Yes	
TP5089	CD22859	No	
MJ1440	HC5560	No	
MJ1471	HC5560	No	
TCM2201	HC5560	No	
MC145439	HC5560	Yes	
MC142100	CD22100	Yes	
MC142101	CD22101	Yes	
MC142103	CD33103	Yes	
MJ1471	CD22103	Yes	
75T202	CD22202	Yes	
75T203	CD22203	Yes	
75T204	CD22204	Yes	
MC145436	CD22204	Yes	
TP3054	CD22354A	Yes	
TP3054B	CD22354A	Yes	
ETC5054	CD22354A	Yes	
TP3057	CD22357A	Yes	
TP3057B	CD22357A	Yes	
ETC3057	CD22357A	Yes	

HARRIS SEMICONDUCTOR

* Primary pins are pin-to-pin; Secondary/optional pins are not

Data Acquisition Products

A/D CONVERTERS DISPLAY

CA3162/CA3162A	A/D Converter for $3^1/_2$-Digit Display
ICL71C03/ICL8052	Precision $4^1/_2$-Digit A/D Converter
ICL71C03/ICL8068	Precision $4^1/_2$-Digit A/D Converter
ICL7106	$3^1/_2$-Digit LCD Single-Chip A/D Converter
ICL7107	$3^1/_2$-Digit LED Single-Chip A/D Converter
ICL7116/7117	$3^1/_2$-Digit with Display Hold Single-Chip A/D Converter
ICL7126	$3^1/_2$-Digit Low Power Single-Chip A/D Converter
ICL7129	$4^1/_2$-Digit LCD Single-Chip A/D Converter
ICL7136	$3^1/_2$-Digit LCD Low Power A/D Converter
ICL7137	$3^1/_2$-Digit LED Low Power Single-Chip A/D Converter
ICL7139	$3^3/_4$-Digit Autoranging Multimeter
ICL7149	Low Cost $3^3/_4$-Digit Autoranging Multimeter
HI-7166/7167	Improved $3^1/_2$ Digit LCD/LED Single Chip A/D Converters

A/D CONVERTERS INTEGRATING

HI-7159	Microprocessor-Compatible $5^1/_2$-Digit A/D Converter
ICL7104/ICL8052	14/16-Bit µP-Compatible 2-Chip A/D Converter
ICL7104/ICL8068	14/16-Bit µP-Compatible 2-Chip A/D Converter
ICL7109	12-Bit µP-Compatible A/D Converter
ICL7135	$4^1/_2$-Digit BCD Output A/D Converter

A/D SUCCESSIVE APPROXIMATION

ADC0802/3/4	8-Bit µP-Compatible A/D Converter
CA3310/CA3310A	CMOS 10-Bit A/D Converter with Internal Track and Hold
HI-574A	Fast, Complete 12-Bit A/D Converter with Microprocessor Interface
HI5812	Low Power, Sampling 12-Bit A/D Converter
HI-674A	I2µs, Complete 12-Bit A/D Converter with Microprocessor Interface
HI-774	8µs Complete 12-Bit A/D Converter with Microprocessor Interface
HI-7153	8-Channel 10-Bit High-Speed A/D Converter with Track and Hold

A/D CONVERTERS FLASH

CA3304	CMOS Video-Speed 4-Bit Flash A/D Converter
CA3306	CMOS Video-Speed 6-Bit Flash A/D Converter
CA3318	CMOS Video-Speed 8-Bit Flash A/D Converter
HI-5700	8-Bit, 20MSPS Flash A/D Converter
HI-5701	6-Bit, 30MSPS Flash A/D Converter
HI-5800	12-Bit, 3MSPS Sampling A/D Converter

FOR MORE INFORMATION CONTACT YOUR LOCAL SALES OFFICE OR DISTRIBUTOR

D/A CONVERTERS

AD7520	10/12-Bit Multiplying DIA Converter
AD7521	10/12-Bit Multiplying DIA Converter
AD7530	10/12-Bit Multiplying DIA Converter
AD7531	10/12-Bit Multiplying D1A Converter
AD7523	8-Bit Multiplying D/A Converter
AD7533	10-Bit Multiplying D/A Converter
AD7541	12-Bit Multiplying D/A Converter
AD7545	12-Bit Buffered Multiplying CMOS DAC
CA3338	CMOS Video-Speed 8-Bit R-2R D/A Converter
HI-565A	High-Speed Monolithic D/A Converter with Reference
HI-DAC80V	12-Bit, Low Cost, Monolithic D/A Converter
HI-DAC85V	12-Bit, Low Cost, Monolithic D/A Converter

ANALOG SWITCHES

DG200	Dual SPST CMOS Analog Switch
DG201	Quad SPST CMOS Analog Switch
DG201A	Quad Monolithic SPST CMOS Analog Switch
DG202	Quad Monolithic SPST CMOS Analog Switch
DG211	Quad Monolithic SPST CMOS Analog Switch
DG212	Quad Monolithic SPST CMOS Analog Switch
DG300A	Dual SPST TTL Compatible CMOS Analog Switch
DG301A	SPDT TTL Compatible CMOS Analog Switch
DG302A	Dual DPST TTL Compatible CMOS Analog Switch
DG303A	Dual SPDT TTL Compatible CMOS Analog Switch
DG308A	Quad Monolithic SPST CMOS Analog Switch
DG309	Quad Monolithic SPST CMOS Analog Switch
DG401/403/405	Dual CMOS Analog Switches
DG411/412/413	Quad SPST CMOS Analog Switches
DG441/442	Quad SPST CMOS Analog Switches
HI-200	Dual SPST CMOS Analog Switch
HI-201	Quad SPST CMOS Analog Switch
HI-201HS	High-Speed Quad SPST CMOS Analog Switch
HI-222	High Frequency Video Switch
HI-300	Dual SPST CMOS Analog Switch
HI-301	SPDT CMOS Analog Switch
HI-302	Dual DPST CMOS Analog Switch
HI-303	Dual SPDT CMOS Analog Switch
HI-304	Dual SPST CMOS Analog Switch
HI-305	SPDT CMOS Analog Switch

FOR MORE INFORMATION CONTACT YOUR LOCAL SALES OFFICE OR DISTRIBUTOR

ANALOG SWITCHES (Continued)

HI-306	Dual DPST CMOS Analog Switch
HI-307	Dual SPDT CMOS Analog Switch
HI-381	Dual SPST CMOS Analog Switch
HI-384	Dual DPST CMOS Analog Switch
HI-387	SPDT CMOS Analog Switch
HI-390	Dual SPDT CMOS Analog Switch
HI-5040	SPST CMOS Analog Switch
HI-5041	Dual SPST CMOS Analog Switch
HI-5042	SPDT CMOS Analog Switch
HI-5043	Dual SPDT CMOS Analog Switch
HI-5044	DPST CMOS Analog Switch
HI-5045	Dual DPST CMOS Analog Switch
HI-5046	DPDT CMOS Analog Switch
HI-5046A	DPDT CMOS Analog Switch
HI-5047	4PST CMOS Analog Switch
HI-5047A	4PST CMOS Analog Switch
HI-5048	Dual SPST CMOS Analog Switch
HI-5049	Dual DPST CMOS Analog Switch
HI-5050	SPDT CMOS Analog Switch
HI-5051	Dual SPDT CMOS Analog Switch
IH401A	Quad Varafet Analog Switch
IH5040	SPST 75 Ohm High-Level CMOS Analog Switch
IH5041	Dual SPST 75 Ohm High-Level CMOS Analog Switch
IH5042	SPDT 75 Ohm High-Level CMOS Analog Switch
IH5043	Dual SPDT 75 Ohm High-Level CMOS Analog Switch
IH5044	DPST 75 Ohm High-Level CMOS Analog Switch
IH5045	Dual DPST 75 Ohm High-Level CMOS Analog Switch
IH5046	DPDT 75 Ohm High-Level CMOS Analog Switch
IH5047	4PST 75 Ohm High-Level CMOS Analog Switch
IH5052	Quad SPST CMOS Analog Switch
IH5053	Quad SPST CMOS Analog Switch
IH5140	SPST High-Level CMOS Analog Switch
IH5141	Dual SPST High-Level CMOS Analog Switch
IH5142	SPDT High-Level CMOS Analog Switch
IH5143	Dual SPDT High-Level CMOS Analog Switch
IH5144	DPST High-Level CMOS Analog Switch
IH5145	Dual DPST High-Level CMOS Analog Switch
IH5148	Dual SPST High-Level CMOS Analog Switch
IH5149	Dual DPST High-Level CMOS Analog Switch

FOR MORE INFORMATION CONTACT YOUR LOCAL SALES OFFICE OR DISTRIBUTOR

ANALOG SWITCHES (Continued)

IH5150	SPDT High-Level CMOS Analog Switch
IH5151	Dual SPDT High-Level CMOS Analog Switch
IH5341	Dual SPST CMOS RF/Video Switch
IH5352	Quad SPST CMOS RF/Video Switch

MULTIPLEXERS

DG408/409	Single 8-Channel/Differential 4-Channel CMOS Analog Multiplexers
DG458/459	Single 8-Channel/Differential 4-Channel Fault Protected Multiplexers
DG506A	16-Channel/Dual 8-Channel CMOS Analog Multiplexer
DG507A	16-Channel/Dual 8-Channel CMOS Analog Multiplexer
DG508A	8-Channel/Dual 4-Channel CMOS Analog Multiplexer
DG509A	8-Channel/Dual 4-Channel CMOS Analog Multiplexer
DG526	16-Channel/Dual 8-Channel CMOS Latchable Multiplexer
DG527	16-Channel/Dual 8-Channel CMOS Latchable Multiplexer
DG528	8-Channel/Dual 4-Channel Latchable Multiplexer
DG529	8-Channel/Dual 4-Channel Latchable Multiplexer
HI-1818A/1828A	Low Resistance Single 8/Differential 4-Channel CMOS Analog Multiplexers
HI-506	Single 16/Differential 8-Channel CMOS Analog Multiplexer
HI-507	Single 16/Differential 8-Channel CMOS Analog Multiplexer
HI-506A	Single 16/Differential 8-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-507A	Single 16/Differential 8-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-508	Single 8/Differential 4-Channel CMOS Analog Multiplexer
HI-509	Single 8/Differential 4-Channel CMOS Analog Multiplexer
HI-508A	Single 8/Differential 4-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-509A	Single 8/Differential 4-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-516	16-Channel/Differential 8-Channel CMOS High-Speed Analog Multiplexer
HI-518	8-Channel/Differential 4-Channel CMOS High-Speed Analog Mulitplexer
HI-524	4-Channel Wideband and Video Multiplexer
HI-539	Monolithic, 4-Channel, Low Level, Differential Multiplexer
HI-546	Single 16/Differential 8-Channel CMOS Analog Mulitplexer with Active Overvoltage Protection
HI-547	Single 16/Differential 8-Channel CMOS Analog Mulitplexer with Active Overvoltage Protection
HI-548	Single 8/Differential 4-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-549	Single 8/Differential 4-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
IH6108	8-Channel CMOS Analog Multiplexer
IH6208	4-Channel Differential CMOS Analog Multiplexer

DISPLAY DRIVERS

CA3161	BCD to Seven Segment Decoder/Driver
CA3168	2-Digit BCD to Seven Segment Decoder/Driver
ICM7211	4-Digit LCD/LED Display Driver

FOR MORE INFORMATION CONTACT YOUR LOCAL SALES OFFICE OR DISTRIBUTOR

Data Acquisition Products (Continued)

DISPLAY DRIVERS (Continued)

ICM7212	4-Digit LCD/LED Display Driver
ICM7218	8-Digit LED Multiplexed Display Driver
ICM7228	8-Digit LED Multiplexed Display Driver
ICM7231	Numeric/Alphanumeric Triplexed LCD Display Driver
ICM7232	Numeric/Alphanumeric Triplexed LCD Display Driver
ICM7243	8-Character µP-Compatible LED Display Driver

REAL-TIME CLOCK

ICM7170	µP-Compatible Real-Time Clock

COUNTERS WITH DISPLAY DRIVERS/TIMEBASE GENERATORS

ICM7207/A	CMOS Timebase Generator
ICM7208	7-Digit LED Display Counter
ICM7209	Timebase Generator
ICM7213	One Second/One Minute Timebase Generator
ICM7216A/B/D	8-Digit Multi-Function Frequency Counter/Timer
ICM7217	4-Digit LED Display Programmable Up/Down Counter
ICM7224	$4^1/_2$-Digit LCD/LED Display Counter
ICM7225	$4^1/_2$-Digit LCD/LED Display Counter
ICM7226A/B	8-Digit Multi-Function Frequency Counter/Timer
ICM7249	$5^1/_2$-Digit LCD µ-Power Event/Hour Meter

SPECIAL PURPOSE

AD590	2-Wire Current Output Temperature Transducer
ICL8069	Low Voltage Reference

DATA COMMUNICATIONS

ICL232	+5 Volt Powered Dual RS-232 Transmitter/Receiver

FOR MORE INFORMATION CONTACT YOUR LOCAL SALES OFFICE OR DISTRIBUTOR

HARRIS SEMICONDUCTOR

Digital Signal Processing Products

MULTIPLIERS

HMA510	16 x 16-Bit CMOS Parallel Multiplier Accumulator
HMU1 6/HMU17	16 x 16-Bit CMOS Parallel Multipliers

ONE DIMENSIONAL FILTERS

DECI • MATE	Harris HSP43220 Decimating Digital Filter Development Software
HSP43168	Dual FIR Filter
HSP43216	Half Band Filter
HSP43220	Decimating Digital Filter
HSP43481	Digital Filter
H5P43881	Digital Filter
HSP43891	Digital Filter

TWO DIMENSIONAL FILTERS

HSP48901	3 x 3 Image Filter
HSP48908	Two Dimensional Convolver

SIGNAL SYNTHESIZERS

HSP45102	12-Bit Numerically Controlled Oscillator
HSP45106	16-Bit Numerically Controlled Oscillator
HSP45116	Numerically Controlled Oscillator/Modulator
HSP45116-DB	HSP45116 Evaluation Daughter Board

SPECIAL FUNCTION

HSP45240	Address Sequencer
HSP45256	Binary Correlator
HSP48410	Histogrammer/Accumulating Buffer
HSP50016	Digital Down Converter
HSP9501	Programmable Data Buffer
HSP9520/9521	Binary Correlator
HSP-EVAL	DSP Evaluation Platform

FOR MORE INFORMATION CONTACT YOUR LOCAL SALES OFFICE OR DISTRIBUTOR

HARRIS SEMICONDUCTOR

LINEAR 2

OPERATIONAL AMPLIFIERS

Operational Amplifiers (Continued)

Operational Amplifiers (Continued)

Selection Guide

WIDEBAND: Min/Max Limits at +25°C, Unless Otherwise Specified

DEVICE	GBWP (typ) (MHz)	FPBW (typ) (MHz)	SLEW RATE (typ) (V/μs)	A_{VOL} (dB)/ A_{ZOL} (V/mA)*	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA/Op Amp)
BUFFERS										
HFA1112	**850**	**260**	**2400**	**-**	**+1, -1, +2**	**25**	**35000**	**-**	**39**	**26**
HFA1113	**850**	**260**	**2400**	**-**	**+1, -1, +2**	**25**	**35000**	**-**	**39**	**26**
HFA1110	**750**	**290**	**1300**	**-**	**+1**	**25**	**40000**	**-**	**39**	**26**
HA-5033	250	41	1300	-	+1	15	35000	-	54	25
HA-5002	110	41	1300	-	+1	20	7000	-	54	10
SINGLE										
HFA-0002	1000	13.3	250	98	10	0.7	700	105	90	15.0
HFA1100	**850**	**350**	**2300**	**500**	**1**	**6**	**40000**	**40**	**45**	**26**
HFA1120	**850**	**350**	**2300**	**500**	**1**	**6**	**40000**	**40**	**45**	**26**
HFA1130	**850**	**350**	**2300**	**500**	**1**	**6**	**40000**	**40**	**45**	**26**
HA-2539	600	9.5	600	80	10	10.0	20000	60	60	25.0
HA-2839	**500**	**10.0**	**625**	**86**	**10**	**2.0**	**14500**	**75**	**75**	**15**
HA-2840	**500**	**10.0**	**625**	**86**	**10**	**2.0**	**14500**	**75**	**75**	**15**
HA-2850	**400**	**5.4**	**340**	**86**	**10**	**2.0**	**14500**	**75**	**75**	**7.5**
HA-2540	400	6.0	400	80	10	10.0	20000	60	60	25.0
HFA-0001	350	53.00	1000	43	1	15.0	50000	45	35	75.0
HFA-0005	300	22.00	420	43	1	15.0	50000	45	40	40.0
CA3450	170	6.56	330	60	1	15.0	350	50	60	35.0
HA-2548	150	1.91	120	114	5	0.9	50	80	86	18.0
HA-5190	150	6.5	200	83	5	5.0	15000	74	70	28.0
HA-5195	150	6.5	200	83	5	5.0	15000	74	70	28.0
HA-5147	140	0.5	35	117	10	0.1	80	100	96	3.5
HA-5147A	120	0.5	35	120	10	0.03	40	114	100	3.5
HA-5004	100	100	1200	100	1	5.0	5000	58	50	16
HA-5020	**100**	**9.6**	**600**	**3500**	**1**	**8.0**	**8000**	**60**	**65**	**10**
HA-2620	100	0.6	35	100	5	4.0	15	80	80	3.7
HA-2622	100	0.6	35	98	5	5.0	25	74	74	4.0
HA-2625	100	0.6	35	98	5	5.0	25	74	74	4.0
HA-5111	100	0.8	50	120	10	3.0	200	80	80	6.0
HA-5160	100	1.9	120	97	10	3.0	0.05	74	74	8.0
NA-5162	100	1.10	70	90	10	15.0	0.065	70	70	8.0
HA-5221	100	0.4	25	106	1	0.75	80	86	86	8.0
HA-2842	**80**	**6.0**	**400**	**94**	**2**	**3.0**	**10000**	**85**	**70**	**14**
HA-2841	**50**	**3.8**	**240**	**90**	**1**	**3.0**	**10000**	**80**	**70**	**11**

NOTE: Bold type designates a new product from Harris.

Selection Guide

WIDEBAND: Min/Max Limits at +25°C, Unless Otherwise Specified **(Continued)**

DEVICE	GBWP (typ) (MHz)	FPBW (typ) (MHz)	SLEW RATE (typ) (V/µs)	A_{VOL} (dB)/ A_{ZOL} (V/mA)*	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA/Op Amp)
DUAL										
HA-5222	100.0	0.40	25	106	1	0.8	80.0	86	86	11.0
HA-5112	60.0	0.32	20	100	10	2.0	200.0	86	86	2.5
CA3280	9.0	1.99	125	94	1	3.0	5000.0	80	86	2.4
CA3280A	9.0	1.99	125	94	1	0.5	5000.0	94	94	2.4
HA-5102	8.0	0.05	3	100	1	2.0	200.0	86	86	2.5
CA3240	4.5	0.14	9	86	1	15.0	0.05	70	76	6.0
CA3240A	4.5	0.14	9	86	1	5.0	0.04	70	76	6.0
CA3260	4.0	0.16	10	94	1	15.0	0.05	70	70	1.5
CA3260A	4.0	0.16	10	94	1	5.0	0.03	80	76	1.5
CA5260	3.0	0.10	5	80	1	15.0	0.02	70	70	2.0
CA5260A	3.0	0.10	5	83	1	4.0	0.02	80	75	2.0
QUAD										
HA-5114	60.0	0.32	20.0	100	10	2.5	200.0	86	86	1.63
HA-2444	**45.0**	**5.1**	**160**	**71**	**1**	**7.0**	**15000**	**70**	**65**	**6.25**
HA-2400	40.0	0.25	30.0	94	1	9.0	200.0	80	74	1.50
HA-2404	40.0	0.25	30.0	94	1	9.0	200.0	80	74	1.50
HA-2405	40.0	0.25	30.0	94	1	9.0	250.0	74	74	1.50
HA-2406	30.0	0.24	20.0	92	1	10.0	250.0	74	74	1.75
CA5470	16.0	0.22	7.0	80	1	22.0	0.05	55	60	3.00
HA-5104	8.0	0.05	3.0	100	1	2.5	200.0	86	86	1.63
HA-5134A	4.0	0.02	0.8	123	1	0.1	25.0	115	110	2.00

* A_{ZOL} applies to current feedback amplifiers only (HA-5004, HA-5020, HFA1100, HFA1120, HFA1130)

NOTE: Bold type designates a new product from Harris.

Selection Guide

HIGH SLEW RATE: Min/Max Limits at +25°C, Unless Otherwise Specified

DEVICE	SLEW RATE (typ) (V/µs)	GBWP (typ) (MHz)	FPBW (typ) (MHz)	A_{VOL} (dB)/ A_{ZOL} (V/mA)*	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA/Op Amp)
BUFFERS										
HFA1112	**2400**	**850**	**260**	-	**+1, -1, +2**	**25**	**35000**	-	**39**	**26**
HFA1113	**2400**	**850**	**260**	-	**+1, -1, +2**	**25**	**35000**	-	**39**	**26**
HFA1110	**1300**	**750**	**290**	-	**+1**	**25**	**40000**	-	**39**	**26**
HA-5002	1300	110	41	-	+1	20	7000	-	54	10
HA-5033	1300	250	41	-	+1	15	35000	-	54	25
SINGLE										
HFA1100	**2300**	**850**	**350**	**500**	**1**	**6**	**40000**	**40**	**45**	**26**
HFA1120	**2300**	**850**	**350**	**500**	**1**	**6**	**40000**	**40**	**45**	**26**
HFA1130	**2300**	**850**	**350**	**500**	**1**	**6**	**40000**	**40**	**45**	**26**
HA-5004	1200	100	100	100	1	5.0	5000	58	50	16
HFA-0001	1000	350	53	43	1	15.0	50000	45	35	75.0
HA-5020	**800**	**100**	**12.7**	**3500**	**1**	**8.0**	**8000**	**60**	**64**	**10**
HA-2839	**625**	**500**	**10.0**	**86**	**10**	**2.0**	**14500**	**75**	**75**	**15**
HA-2840	**625**	**500**	**10.0**	**86**	**10**	**2.0**	**14500**	**75**	**75**	**15**
HA-2539	600	600	9.5	80	10	10.0	20000	60	60	25.0
HFA-0005	420	300	22.0	43	1	15.0	50000	45	40	40.0
HA-2540	400	400	6.0	80	10	10.0	20000	60	60	25.0
HA-2842	**400**	**80**	**6.0**	**94**	**2**	**3.0**	**10000**	**85**	**70**	**14**
HA-2542	350	70	5.5	80	2	10.0	35000	70	70	35.0
HA-2850	**340**	**400**	**5.4**	**86**	**10**	**2.0**	**14500**	**75**	**75**	**7.5**
CA3450	330	170	6.6	60	1	15.0	350	50	60	35.0
HA-2841	**240**	**50**	**3.8**	**90**	**1**	**3.0**	**10000**	**80**	**70**	**11**
HA-2541	250	40	4.0	80	1	2.0	25000	70	70	40.0
HFA-0002	250	1000	13.3	98	10	0.7	700	105	90	15.0
HA-5190	200	150	6.5	83	5	5.0	15000	74	70	28.0
HA-5195	200	150	6.5	83	5	5.0	15000	74	70	28.0
HA-2529	150	20	2.1	80	3	5.0	200	80	80	6.0
HA-2544	150	50	3.2	71	1	15.0	15000	75	70	12.0
HA-2520	120	20	1.5	80	3	8.0	200	80	80	6.0
HA-2522	120	20	1.2	78	3	10.0	250	74	74	6.0
HA-2525	120	20	1.2	78	3	10.0	250	74	74	6.0
HA-2548	120	150	1.91	114	5	0.9	50	80	86	18.0
HA-5160	120	100	1.9	97	10	3	0.05	74	74	8

NOTE: Bold type designates a new product from Harris.

Selection Guide

HIGH SLEW RATE: Min/Max Limits at +25°C, Unless Otherwise Specified **(Continued)**

DEVICE	SLEW RATE (typ) (V/µs)	GBWP (typ) (MHz)	FPBW (typ) (MHz)	A_{VOL} (dB)/ A_{ZOL} (V/mA)*	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA/Op Amp)
DUAL										
CA3280	125	9.0	1.99	94	1	3.0	5000	80	86	2.4
CA3280A	125	9.0	1.99	94	1	0.5	5000	94	94	2.4
HA-5222	25	100	0.40	106	1	0.75	80	86	86	11.0
HA-5112	20	60	0.32	100	10	2.0	200	86	86	2.5
CA3260	10	4.0	0.16	94	1	15.0	0.05	70	70	1.5
CA3260A	10	4.0	0.16	94	1	5.0	0.03	80	76	1.5
CA3240	9.0	4.5	0.14	86	1	15.0	0.05	70	76	6.0
CA3240A	9.0	4.5	0.14	86	1	5.0	0.04	70	76	6.0
CA5260A	5.0	3.0	0.10	83	1	4.0	0.015	80	75	2.0
QUAD										
HA-2444	**160**	**45**	**5.1**	**71**	**1**	**7.0**	**15000**	**70**	**65**	**6.25**
HA-2400	30	40	0.25	94	1	9.0	200	80	74	1.50
HA-2404	30	40	0.25	94	1	9.0	200	80	74	1.50
HA-2405	30	40	0.25	94	1	9.0	250	74	74	1.50
HA-2406	20	30	0.24	92	1	10.0	250	74	74	1.75
HA-5114	20	60	0.32	100	10	2.5	200	86	86	1.63
CA5470	7.0	16	0.22	80	1	22.0	0.05	55	60	3.0

* A_{ZOL} applies to current feedback amplifiers only (HA-5004, HA-5020, HFA1100, HFA1120, HFA1130)

NOTE: Bold type designates a new product from Harris.

Selection Guide

VIDEO: Typical Values at +25°C, Unless Otherwise Specified

DEVICE	FEATURES	DIFFERENTIAL GAIN (%)	DIFFERENTIAL PHASE (DEG)	0.1dB FLAT GAIN (MHz)	GBWP (MHz)	SLEW RATE (V/µs)	OUTPUT CURRENT (mA)	SUPPLY VOLTAGE RANGE (±V)	SUPPLY CURRENT (mA/Op Amp)
BUFFERS									
HFA1110	**+1, Std. Buffer Pinout**	**0.02**	**0.02**	**>100**	**750**	**1300**	**60**	**4.5 - 5.5**	**21.0**
HFA1112	**-1,+1,+2 (Selectable) Standard Op Amp Pinout**	**0.02**	**0.04**	**>100**	**850**	**2400**	**60**	**4.5 - 5.5**	**21.0**
HFA1113	**-1,+1,+2 (Selectable) Standard Op Amp Pinout, V_{OUT} Clamps**	**0.02**	**0.04**	**>100**	**850**	**2400**	**60**	**4.5 - 5.5**	**21.0**
HA-5033	+1, Std. Buffer Pinout	0.03	0.02	-	250	1300	100	5 - 16	21.0
HA-5002	+1, Std. Buffer Pinout	0.06	0.21	-	110	1300	200	5 - 20	8.3
SINGLE									
HA-2842	**$A_V \geq 2$, Cable Driver**	**0.02**	**0.03**	**>10**	**80**	**400**	**100**	**6 - 17**	**14.2**
HA-5020	**$A_V \geq 1$, Output Disable, CFB (Current Feedback)**	**0.02**	**0.03**	**5**	**100**	**1100**	**32**	**4.5 - 18**	**7.5**
HFA1100	**$A_V \geq 1$, CFB**	**0.03**	**0.05**	**75**	**850**	**2300**	**60**	**4.5 - 5.5**	**21.0**
HFA1120	**HFA1100 with Offset Adjust**	**0.03**	**0.05**	**75**	**850**	**2300**	**60**	**4.5 - 5.5**	**21.0**
HFA1130	**$A_V \geq 1$, CFB, Programmable Output Clamps**	**0.03**	**0.05**	**75**	**850**	**2300**	**60**	**4.5 - 5-5**	**21.0**
HA-2544	$A_V \geq 1$	0.03	0.03	5	50	150	35	8 - 17	10.0
HA-2841	**$A_V \geq 1$, Low I_{CC}**	**0.03**	**0.03**	**>10**	**50**	**240**	**30**	**6 - 17**	**10.0**
HFA1105	**$A_V \geq 1$, Low I_{CC}, CFB**	**0.04**	**0.04**	**>25**	**450**	**2000**	**40**	**4.5 - 5.5**	**6.0**
HFA1106	**HFA1105 with Compensation Pin**	**0.04**	**0.04**	**>25**	**450**	**2000**	**40**	**4.5 - 5.5**	**6.0**
HFA1135	**$A_V \geq 1$, Low I_{CC}, CFB, Programmable Output Clamps**	**0.04**	**0.04**	**>25**	**450**	**2000**	**40**	**4.5 - 5.5**	**6.0**
HFA1145	**$A_V \geq 1$, Low I_{CC}, CFB, Output Disable**	**0.04**	**0.04**	**>25**	**450**	**2000**	**40**	**4.5 - 5.5**	**6.0**
DUAL									
HA-5022	**$A_V \geq 1$, CFB**	**0.02**	**0.03**	**5**	**100**	**1100**	**32**	**4.5 - 18**	**7.5**
HA-5023	**$A_V \geq 1$, CFB, Output Disable**	**0.02**	**0.03**	**5**	**100**	**1100**	**32**	**4.5 - 18**	**7.5**
QUAD									
HA-5024	**$A_V \geq 1$, CFB**	**0.02**	**0.03**	**5**	**100**	**1100**	**32**	**4.5 - 18**	**7.5**
HA-5025	**$A_V \geq 1$, CFB, Output Disable**	**0.02**	**0.03**	**5**	**100**	**1100**	**32**	**4.5 - 18**	**7.5**
HA-2444	**$A_V \geq 1$, 4-Channel, Mux'd Output**	**0.03**	**0.03**	**10**	**50**	**160**	**25**	**8.5 - 17**	**20.0**
SPECIAL FUNCTION									
HA-2546*	Multiplier, 2 Quad, Voltage Output	<0.1	<0.1	5	40	300	45	7 - 17	23.0
HA-2547*	Multiplier, 2 Quad, Current Output	-	-	-	100	t_R = 5ns	2.0	7 - 17	20.0
HA-2556*	**Multiplier, 4 Quad, Voltage Output**	**<0.1**	**<0.1**	**10**	**45**	**450**	**45**	**5 - 17**	**18.0**
HA-2557*	**Multiplier, 4 Quad, Current Output**	**-**	**-**	**-**	**100**	**t_R = 5ns**	**1.6**	**5 - 17**	**13.0**
HA-2444	**$A_V \geq 1$, 4-Channel, Mux'd Output**	**0.03**	**0.03**	**10**	**50**	**160**	**25**	**8.5 - 17**	**20.0**
CA3256*	**Video Switch and Amplifier**	**1.0**	**1.0**	**-**	**25**	**200**	**16**	**4 - 18****	**20**

* See Section 7 (Special Analog Circuits) for data sheets.

** Single Supply Range.

NOTE: Bold type designates a new product from Harris.

Selection Guide

LOW NOISE: Min/Max Limits at +25°C, Unless Otherwise Specified

DEVICE	NOISE VOLTAGE 1kHz (typ) (nV/√Hz)	NOISE CURRENT 1kHz (typ) (pA/√Hz)	GBWP (typ) (MHz)	SLEW RATE (typ) (V/µs)	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	SUPPLY CURRENT (mA/Op Amp)
SINGLE								
HFA-0002	2.7	4.5	1000	250	10	1.0	1000	20.0
HA-5004	2.2	6.0*	100	1200	1	5.0	5000*	16.0
HA-5127A	3.0	0.4	8.5	10	1	0.025	40	4.0
HA-5137A	3.0	0.4	63	20	5	0.025	40	4.0
HA-5147A	3.0	0.4	120	35	10	0.025	40	4.0
HA-5101	3.3	1.1	10	10	1	3.0	200	7.0
HA-5111	3.3	1.1	100	50	10	3.0	200	7.0
HA-5221	3.4	1.0	100	25	1	0.75	100	11.0
HA-5020	**4.5**	**2.5***	**100**	**1100**	**1**	**8.0**	**8000***	**10.0**
HA-5190	6.0	5.0	150	200	5	5.0	15000	28.0
HA-2839	**6.0**	**6.0**	**600**	**625**	**10**	**2.0**	**14500**	**15.0**
HA-2840	**6.0**	**6.0**	**600**	**625**	**10**	**2.0**	**14500**	**15.0**
HA-2539	6.0	6.0	600	600	10	10.0	20000	25.0
HA-2540	6.0	6.0	400	400	10	10.0	20000	25.0
HA-2548A	8.3	0.4	150	120	5	0.3	50	18.0
HA-5177	8.8	1.2	2.0	0.8	1	0.6	6	1.7
HA-5170	10.0	0.01	8.0	8.0	1	0.3	0.1	2.5
HA-2542	10.0	3.0	70	350	2	10.0	35000	40.0
HA-2541	10.0	4.0	40	250	1	2.0	35000	40.0
DUAL								
HA-5222	3.4	1.0	100	25	1	0.75	100	11.0
HA-5102	4.3	0.6	8.0	3.0	1	2.0	200	2.5
HA-5112	4.3	0.6	60	20	10	2.0	200	2.5
QUAD								
HA-5104	4.3	0.6	8.0	3.0	1	2.5	200	1.63
HA-5114	4.3	0.6	60	20	10	2.5	200	1.63
HA-5134A	7.0	1.0	4.0	1.0	1	0.1	25	2.0

* +Input. These are current feedback amplifiers, so value for -Input will be larger.

NOTE: Bold type designates a new product from Harris.

Selection Guide

GENERAL PURPOSE: Typical Values at +25°C, Unless Otherwise Specified

DEVICE	DESCRIPTION	MINIMUM STABLE GAIN	GBWP (MHz)	SLEW RATE (V/μs)	OFFSET VOLTAGE (mV)	BIAS CURRENT (μA)	MAXIMUM SUPPLY VOLTAGE (±V)	SUPPLY CURRENT (mA/Op Amp)
SINGLE								
HA-2544	Ultra-Stable, High Performance	1	50	150	6.0	7.00	17.5	10.0
CA3100	Wideband Amplifier	1	38	70	1.0	0.7	18	8.5
CA3130A	BiMOS, CMOS Output, Output Strobe	1	15	30	2.0	5.0pA	8	2.0
CA5130A	Mil Temp Version of CA3130A	1	15	30	2.0	5.0pA	8	2.0
HA-2605	Wideband, Compensated, High Input Impedance	1	12	7	3.0	0.005	22.5	3.0
HA-5101	Low Noise, High Performance	1	10	10	0.5	0.1	20	4.0
HA-5127A	Low Noise, Precision, Compensated	1	8.5	10	0.01	0.01	22	3.5
HA-5170	JFET Input, Precision	1	8	8	0.1	20pA	22	1.9
CA3140A	BiMOS, Output Strobe Capability	1	4.5	9	2.0	10.0pA	18	4.0
HA-2645	High Voltage, Compensated	1	4	5	2.0	0.012	50	3.2
CA3160A	BiMOS, CMOS Output, Output Strobe	1	4	10	2.0	5.0pA	8	2.0
CA5160A	Mil Temp Version of CA3160A	1	4	10	2.0	5.0pA	8	2.0
CA3080	Operational Transconductance Amp.	1	2	75	0.4	2.0	18	1.0
CA3193A	BiMOS, Instrumentation Amplifier	1	1.2	0.25	0.14	0.01	18	2.3
HA-2525	Uncompensated	3	20	120	5.0	0.125	20	4.0
HA-2529	Uncompensated, High Output Current	3	20	150	2.0	0.05	20	4.5
HA-5137A	Low Noise, Precision	5	80	20	0.01	0.01	22	3.5
HA-2625	Wideband, Uncompensated, High Input Impedance	5	100	35	3.0	0.005	22.5	3.0
HA-5195	Wideband, Fast Settling	5	150	200	3.0	5.0	17.5	19.0
HA-2548A	Wideband, Precision	5	150	110	0.1	0.005	20	12.0
HA-5147A	Low Noise, Precision, Wideband	10	140	35	0.01	0.01	22	3.5
HA-5111	Low Noise, High Performance, Uncompensated	10	100	50	0.5	0.1	20	4.0

NOTE: Bold type designates a new product from Harris.

Selection Guide

GENERAL PURPOSE: Typical Values at +25°C, Unless Otherwise Specified (Continued)

DEVICE	DESCRIPTION	MINIMUM STABLE GAIN	GBWP (MHz)	SLEW RATE (V/μs)	OFFSET VOLTAGE (mV)	BIAS CURRENT (μA)	MAXIMUM SUPPLY VOLTAGE (±V)	SUPPLY CURRENT (mA/Op Amp)
DUAL								
CA3280A	Operational Transconductance Amp.	1	9	125	0.25	1.8	18	2.0
HA-5102	Low Noise, High Performance	1	8	3	0.5	0.13	20	1.5
CA3240A	BiMOS, High Input Impedance	1	4.5	9	2.0	10.0pA	18	4.0
CA3260A	BiMOS, CMOS Output, High Input Impedance	1	4	10	2.0	5.0pA	8	0.6
CA5260A	Mil Temp Version of CA3260A	1	3	5	2.0	5.0pA	8	0.6
CA158A	Wide Supply Range	1	1	0.25	1.0	0.02	16	0.75
HA-5112	Low Noise, High Performance, Uncompensated	10	60	20	0.5	0.13	20	1.5
TRIPLE								
CA3060	Operational Transconductance Amp.	1	0.11	1.0	1.0	2.5	18	0.85
QUAD								
CA5470	High Input Impedance, Wide Supply Range	1	14	5	5.0	1.0pA	8	2.5
HA-5104	Low Noise, High Performance	1	8	3	0.5	0.13	20	1.25
CA124	Wide Supply Range	1	1	0.5	2.0	0.045	16	0.2
HA-5114	Low Noise, High Performance, Uncompensated	10	60	20	0.5	0.13	20	1.25

NOTE: Bold type designates a new product from Harris.

Selection Guide

PRECISION: Min/Max Limits at +25°C, Unless Otherwise Specified

DEVICE	OFFSET VOLTAGE (mV)	V_{IO} DRIFT (typ) (µV/°C)	BIAS CURRENT (nA)	OFFSET CURRENT (nA)	CMRR (dB)	PSRR (dB)	GBWP (typ) (MHz)	SLEW RATE (typ) (V/µs)	A_{VOL} (dB)	SUPPLY CURRENT (mA/Op Amp)
SINGLE										
ICL7650S	0.005	0.02	0.01	0.005	120	120	2.0	2.5	135	3.0
HA-5127A	0.025	0.20	40.0	35.0	114	86	8.5	10.0	120	3.5
HA-5130	0.025	0.40	2.0	2.0	110	100	2.5	0.8	120	1.3
HA-5137A	0.025	0.20	40.0	35.0	114	100	63.0	20.0	120	3.5
HA-5147A	0.025	0.20	40.0	35.0	114	100	120.0	35.0	120	3.5
HA-5177	0.060	0.20	6.0	6.0	110	110	2.0	0.8	126	1.7
HA-5135	0.075	0.40	4.0	4.0	106	94	2.5	0.8	120	1.7
HA-5137	0.100	0.40	80.0	75.0	100	96	63.0	20.0	117	3.5
HA-5147	0.100	0.40	80.0	75.0	100	96	140.0	35.0	117	3.5
CA3193A	0.200	1.00	20.0	5.0	110	100	1.2	0.25	110	3.5
HA-5170	0.300	2.0	0.1	0.03	85	85	8.0	8.0	109	2.5
HA-2548A	0.300	3.0	50.0	50.0	80	86	150.0	120.0	120	18.0
HA-5221	0.750	0.5	80.0	50.0	86	86	100.0	25.0	106	11.0
DUAL										
HA-5232	**0.5**	**5.0**	**10**	**10**	**100**	**100**	**0.8**	**0.15**	**108**	**0.73**
HA-5222	0.75	0.5	80	50	86	86	100.0	25.0	106	11.0
CA158A	2.0	7.0	50	10	70	65	1.0	0.5	94	1.5
HA-5102	2.0	3.0	200	75	86	86	8.0	3.0	100	2.5
HA-5112	2.0	3.0	200	75	86	86	60.0	20.0	100	2.5
ICL7621	2.0	10.0	0.05	0.03	76	80	0.5	0.16	80	0.25
CA3280	3.0	5.0	5000	700	80	86	9.0	125.0	94	2.4
CA258A	3.0	7.0	80	15	70	65	1.0	0.5	94	1.5
CA358A	3.0	7.0	100	30	65	65	1.0	0.5	88	1.5
HA-5142	6.0	3.0	100.0	10.0	77	77	0.4	1.5	86	0.15
QUAD										
HA-5134A	0.1	0.3	25.0	25.0	115	110	4.0	0.75	123	2.0
HA-5234	**0.50**	**5.0**	**10**	**10**	**100**	**100**	**0.8**	**0.15**	**108**	**0.73**
HA-5114	2.5	3.0	200.0	75.0	86	86	60.0	20.0	100	1.63
HA-5104	2.5	3.0	200.0	75.0	86	86	8.0	3.0	100	1.63
CA124	5.0	7.0	150.0	30.0	70	65	1.0	0.5	94	0.5
HA-5144	6.0	3.0	100.0	10.0	77	77	0.4	1.5	86	0.15
CA224	7.0	7.0	250.0	50.0	65	65	1.0	0.5	88	0.5
CA324	7.0	7.0	250.0	50.0	65	65	1.0	0.5	86	0.5
CA2902	7.0	7.0	250.0	50.0	65	65	1.0	0.5	86	0.3

NOTE: Bold type designates a new product from Harris.

Selection Guide

LOW BIAS CURRENT: Min/Max Limits at +25°C, Unless Otherwise Specified

DEVICE	BIAS CURRENT (nA)	OFFSET CURRENT (nA)	OFFSET VOLTAGE (mV)	CM RANGE (±V)	A_{VOL} (dB)	GBWP (typ) (MHz)	SLEW RATE (typ) (V/μs)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA/Op Amp
SINGLE										
CA5420A	0.001	0.0005	5.0	3.7	85	0.5	0.5	75	75	0.50
CA5420	0.002	0.0010	10.0	3.7	85	0.5	0.5	70	70	0.50
CA3420	0.005	0.004	10.0	1.0	80	0.5	0.5	55	60	0.65
CA3420A	0.005	0.004	5.0	1.0	86	0.5	0.5	60	70	0.65
CA5130A	0.010	0.005	4.0	2.5	90	4.0	10.0	75	60	0.10
CA5160A	0.010	0.005	4.0	2.5	90	4.0	10.0	75	60	0.10
ICL7650S	0.010	0.005	0.005	3.5	135	2.0	2.5	120	120	3.00
CA5130	0.015	0.010	10.0	2.5	85	4.0	10.0	70	55	0.10
CA5160	0.015	0.010	10.0	2.5	85	4.0	10.0	70	55	0.10
CA3130A	0.030	0.020	5.0	10.0	94	15.0	9.0	80	80	15.00
HA-5160	0.050	0.010	3.0	10.0	98	100.0	120	74	74	10.0
HA-5170	0.100	0.060	0.3	10.0	110	8.0	8.0	90	90	2.50
DUAL										
CA5260	0.015	0.01	15.0	11.0	80	3.0	5.0	70	70	2.0
CA5260A	0.015	0.01	4.0	2.5	83	3.0	5.0	80	75	2.0
CA3260A	0.03	0.02	5.0	10.0	94	4.0	10.0	80	76	1.5
CA3240A	0.04	0.02	5.0	13.0	86	4.5	9.0	70	76	6.0
CA3240	0.05	0.03	15.0	12.0	86	4.5	9.0	70	76	6.0
CA3260	0.05	0.03	15.0	10.0	94	4.0	10.0	70	70	1.5
ICL7621	0.05	0.03	2.0	12.0	80	0.5	0.16	76	80	0.25
HA-5232	**10.0**	**10**	**0.5**	**12.0**	**108**	**0.8**	**0.15**	**100**	**100**	**0.73**
CA158A	50.0	10.0	2.0	13.0	94	1.0	0.5	70	65	1.50
QUAD										
CA5470	0.05	0.005	22.0	3.5	80	14.0	5.0	55	60	3.0
ICL7641	0.05	0.03	10.0	4.2	80	1.4	1.60	70	80	2.5
ICL7642	0.05	0.03	10.0	4.2	80	0.04	0.02	70	80	0.02
HA-5234	**10.0**	**10**	**0.5**	**12**	**108**	**0.8**	**0.15**	**100**	**100**	**0.73**
HA-5134A	25.0	25.0	0.1	10.0	123	4.0	0.75	115	110	2.0

NOTE: Bold type designates a new product from Harris.

Selection Guide

5V SINGLE-SUPPLY: Min/Max Limits at +25°C, Unless Othewise Specified

DEVICE	SUPPLY* CURRENT (typ) (mA/Op Amp)	INPUT OFFSET VOLTAGE (mV)	DOES INPUT INCLUDE GROUND	RAIL-TO-RAIL OUTPUT?	INPUT BIAS CURRENT (nA)	GAIN BANDWIDTH PRODUCT (typ) (MHz)	SLEW RATE (typ) V/μs	MINIMUM SINGLE SUPPLY VOLTAGE (V)	OUTPUT CURRENT (mA)
SINGLE									
CA3440A	0.005	5	YES	NO	0.04	0.063	0.03	5.0	15
CA3440	0.005	10	YES	NO	0.05	0.063	0.03	5.0	15
ICL7612A	0.01	2	YES	YES	0.05	0.04	0.016	2.0	0.04
ICL7611A	0.01	2	NO	YES	0.05	0.04	0.016	2.0	0.04
ICL7612D	0.01	15	YES	YES	0.05	0.04	0.016	2.0	0.04
ICL7611D	0.01	15	NO	YES	0.05	0.04	0.016	2.0	0.04
CA3078A	0.025	3.5	NO	NO	12	1.5	0.5	1.5	12
CA5160A	0.05	4	YES	YES	0.01	4	10	5.0	4
CA5130A	0.05	4	YES	YES	0.01	4	10	4.0	4
CA5160	0.05	10	YES	YES	0.015	4	10	5.0	4
CA5130	0.05	10	YES	YES	0.015	4	10	4.0	4
CA3078	0.130	4.5	NO	NO	170	8	1.5	1.5	12
CA3130A	0.30	5	YES	YES	0.03	15	10	5.0	12
CA3130	0.30	15	YES	YES	0.05	15	10	5.0	12
CA3160A	0.30	5	YES	YES	0.03	4	10	5.0	12
CA3160	0.30	15	YES	YES	0.05	4	10	5.0	12
CA5420A	0.40	5	YES	YES	0.001	0.5	0.5	2.0	1.2
CA5420	0.40	10	YES	YES	0.002	0.5	0.5	2.0	1.2
CA3420A	0.45	5	YES	YES	0.005	0.5	0.5	2.0	2.6
CA3420	0.45	10	YES	YES	0.005	0.5	0.5	2.0	2.6
CA3140A	1.60	5	YES	NO	0.04	3.7	9	4.0	12
CA3140	1.60	15	YES	NO	0.05	3.7	9	4.0	12

NOTE: Bold type designates a new product from Harris.

Selection Guide

5V SINGLE-SUPPLY: Min/Max Limits at +25°C, Unless Othewise Specified **(Continued)**

DEVICE	SUPPLY* CURRENT (typ) (mA/Op Amp)	INPUT OFFSET VOLTAGE (mV)	DOES INPUT INCLUDE GROUND	RAIL-TO-RAIL OUTPUT?	INPUT BIAS CURRENT (nA)	GAIN BANDWIDTH PRODUCT (typ) (MHz)	SLEW RATE (typ) V/µs	MINIMUM SINGLE SUPPLY VOLTAGE (V)	OUTPUT CURRENT (mA)
DUAL									
HA-5142	0.05	6	YES	NO	100	0.4	1.5	3.0	4.5
ICL7621A	0.10	2	NO	YES	0.05	0.5	0.16	2.0	0.3
ICL7621D	0.10	15	NO	YES	0.05	0.5	0.16	2.0	0.3
CA158A	0.35	3	YES	NO	100	1	0.5	3.0	20
CA358	0.35	7	YES	NO	250	1	0.5	3.0	20
CA3260A	0.60	5	YES	YES	0.03	4	10	4.0	12
CA3260	0.60	15	YES	YES	0.05	4	10	4.0	12
HA5232	0.70	0.5	NO	NO	10	0.8	0.15	5.0	6.0
CA5260A	0.80	4	YES	YES	0.015	3	5	4.5	1.75
CA5260	0.80	15	YES	YES	0.015	3	5	4.5	1.75
CA3240A	2.00	5	YES	NO	0.04	3.7	9	5.0	12
CA3240	2.00	15	YES	NO	0.05	3.7	9	5.0	12
QUAD									
ICL7642C	0.01	10	NO	YES	0.05	0.044	0.016	2.0	0.04
ICL7642E	0.01	20	NO	YES	0.05	0.044	0.016	2.0	0.04
HA-5144	0.05	6	YES	NO	100	0.4	1.5	3.0	4.5
CA324	0.20	7	YES	NO	250	1	0.5	5.0	10
CA124	0.20	5	YES	NO	150	1	0.5	5.0	10
HA5234	0.70	0.5	NO	NO	10	0.8	0.15	5.0	6.0
ICL7641C	1.00	10	NO	YES	0.05	1.4	1.6	5.0	0.7
ICL7641E	1.00	20	NO	YES	0.05	1.4	1.6	5.0	0.7
CA5470	1.50	22	YES	NO	0.05	14	5	3.0	4

* Supply Current for single 5V supply, if specified in data sheet.

NOTE: Bold type designates a new product from Harris.

Selection Guide

LOW POWER: Min/Max Limits at +25°C, Unless Otherwise Specified

DEVICE	SUPPLY CURRENT (mA/Op Amp)	MAX V+, V- (±V)	SLEW RATE (typ) (V/µs)	GBWP (typ) (MHz)	CM RANGE (±V)	OUTPUT VOLTAGE SWING (±V)	OUTPUT CURRENT (mA)	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	PSRR (dB)
SINGLE										
CA3440	0.017	12.5	0.03	0.063	3.5	3.0	15.0	10.0	0.050	70
CA3440A	0.017	12.5	0.03	0.063	3.5	3.0	15.0	5.0	0.040	70
CA3078A	0.02	18.0	0.5	1.5	5.5	5.1	12.0	3.5	12.0	70
ICL7611A	0.02	9.0	0.02	0.044	4.4	4.9	0.1	2.0	0.05	80
ICL7612A	0.02	9.0	0.02	0.044	5.3	4.9	0.1	2.0	0.05	80
CA5130	0.10	8.0	10.0	4.0	2.5	2.5	4.0	10.0	0.015	55
CA5130A	0.10	8.0	10.0	4.0	2.5	2.5	4.0	4.0	0.010	60
CA5160	0.10	8.0	10.0	4.0	2.5	2.5	4.0	10.0	0.015	55
CA5160A	0.10	8.0	10.0	4.0	2.5	2.5	4.0	4.0	0.010	60
CA3078	0.13	7.0	1.5	8.0	5.5	5.1	12.0	4.5	170.0	70
HA-2705	0.15	22	20	1.0	11.0	12	10	5.0	40	80
CA3094	0.40	12.0	50.0	30.0	12.0	14.9	100.0	5.0	5000.0	70
CA3094A	0.40	18.0	50.0	30.0	12.0	14.9	100.0	5.0	5000.0	70
CA3094B	0.40	22.0	50.0	30.0	12.0	14.9	100.0	5.0	5000.0	70
CA5420A	0.55	11	0.5	0.5	9.0	9.7	1.2	5.0	0.005	70
CA3420A	1.0	11	0.5	0.5	9.0	9.7	1.2	5.0	0.005	70
DUAL										
HA-5142	0.15	17.5	1.5	0.4	10.0	10	0.2	6.0	100	77
ICL7621A	0.25	9.0	0.16	0.5	4.2	4.9	1.0	2.0	0.05	80
HA-5232	**0.73**	**18**	**0.15**	**0.8**	**12**	**12**	**6.0**	**0.5**	**10**	**100**
CA158A	1.5	13.0	0.5	1.0	13.0	13.0	20.0	2.0	50.0	65
CA258A	1.5	6.5	0.5	1.0	13.0	13.0	20.0	3.0	80.0	65
CA2904	1.5	6.5	0.5	1.0	13.0	13.0	20.0	7.0	250.0	50
CA258	1.5	6.5	0.5	1.0	13.0	13.0	20.0	5.0	150.0	65
CA358	1.5	13.0	0.5	1.0	13.0	13.0	20.0	7.0	250.0	65
CA158	1.5	16.0	0.5	1.0	13.0	13.0	20.0	5.0	150.0	65
CA358A	1.5	13.0	0.5	1.0	13.0	13.0	20.0	3.0	100.0	65
CA3260A	1.5	8	10	4	+3/-8	+4/-8	12	5.0	0.03	77
CA5260A	2.0	8.0	5.0	3.0	2.5	4.4	12.0	5.0	0.030	76
QUAD										
ICL7642	0.02	9.0	0.02	0.04	4.2	4.5	0.1	10.0	0.05	80
HA-5144	0.15	17.5	1.5	0.4	10.0	10	0.2	6.0	100.0	77
CA124	0.5	16.0	0.5	1.0	13.0	26.0	10.0	5.0	150.0	65
CA224	0.5	16.0	0.5	1.0	13.0	13.0	10.0	7.0	250.0	65
CA324	0.5	16.0	0.5	1.0	13.0	13.0	10.0	7.0	250.0	65
HA-5234	**0.7**	**18**	**0.15**	**0.8**	**12**	**12**	**6.0**	**0.5**	**10**	**100**
ICL7641	2.50	9.0	1.6	1.4	4.2	4.5	8.0	10.0	0.05	80

NOTE: Bold type designates a new product from Harris.

CA Type Ordering Information

Linear (CA Series)

Linear ICs are available in a wide variety of package designs. These packages are identified by suffix letters indicated in the chart below. When ordering Linear devices, it is important that the appropriate suffix letter be affixed to the type number as indicated on the price schedule.

PACKAGE	CA SERIES
Dual-In-Line Ceramic Sidebraze	D
Dual-In-Line Plastic	E
Frit-Seal Dual-In-Line Ceramic	F
Quad-In-Line Plastic	Q
Plastic Lead Chip Carrier	Q
Dual-In-Line Formed Lead TO-5	S
TO-5 Style Package	T
Small Outline (SOIC) Plastic	M

Extra Value Screening

Linear product with extra value screening has an X added to the standard type number in the price list, and is also branded as such. A white dot will indicate location of Pin 1.

Example:

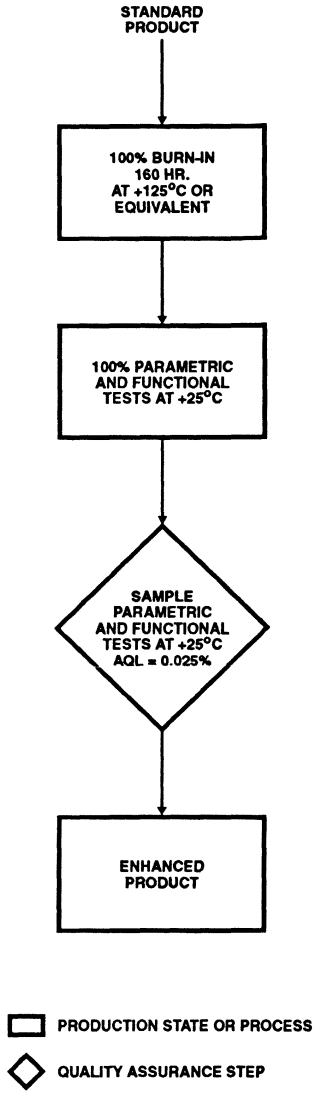
A CA3080E with Extra Value screening is designated CA3080EX in the price list. It is branded CA3080EX plus a white dot at pin number 1.

Tape and Reel for Small Outline Packages

With the introduction of small outline packages, Harris now offers its customers the convenient tape and reel style packaging. Small outline devices, which can be tape and reeled, are denoted wtih the suffix "M96" or "AM96" in the linear and high speed logic product lines. Devices must be ordered in multiples of quantities listed below. Any returns must be full and unopened reels.

LEAD COUNT	TAPE WIDTH (mm)	REEL SIZE (INCHES)	DEVICES PER REEL
8	12	13	2500
14	16	13	2500
16	16	13	2500
24	24	13	1000

PRODUCT FLOW



HARRIS SEMICONDUCTOR

CA124, CA224, CA324 LM324*, LM2902*

Quad Operational Amplifiers for Commercial, Industrial, and Military Applications

March 1993

Features

- Operation from Single or Dual Supplies
- Unity-Gain Bandwidth ..... 1MHz (Typ.)
- DC Voltage Gain ..... 100dB (Typ.)
- Input Bias Current ..... 45nA (Typ.)
- Input Offset Voltage ..... 2mV (Typ.)
- Input Offset Current
  - CA224, CA324, LM324, LM2902 ..... 5nA (Typ.)
  - CA124 ..... 3nA (Typ.)
- Replacement for Industry Types 124, 224, 324

Applications

- Summing Amplifiers
- Multivibrators
- Oscillators
- Transducer Amplifiers
- DC Gain Blocks

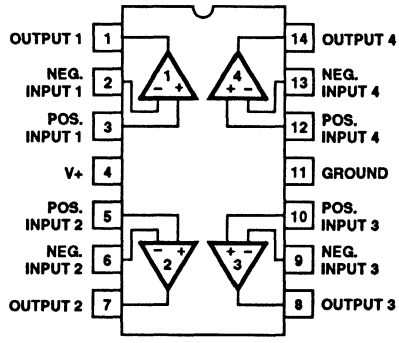
Description

The CA124, CA224, CA324, LM324, and LM2902 consist of four independent, high-gain operational amplifiers on a single monolithic substrate. An on-chip capacitor in each of the amplifiers provides frequency compensation for unity gain. These devices are designed specially to operate from either single or dual supplies, and the differential voltage range is equal to the power-supply voltage. Low power drain and an input common-mode voltage range from 0V to V+ -1.5V (single-supply operation) make these devices suitable for battery operation.

The CA124, CA224, CA324, LM324 and LM2902 are supplied in both 14-lead dual-in-line plastic (E suffix) and 14-lead (150 mil) small outline (M suffix) packages. The CA324 is available in chip form (H suffix).

Pinout

CA124, CA224, CA324, LM324, LM2902
(PDIP, SOIC)
TOP VIEW



* Technical Data on LM Branded types is identical to the corresponding CA Branded types.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

Absolute Maximum Ratings

Supply Voltage ..... 32V to ±16V
Differential Input Voltage 32V
Input Voltage ..... -0.3V to +32V
Input Current (V_I < -0.3V) (Note 1) 50mA
Output Short Circuit Duration (V+ ≤ 15V) (Note 2) ..... Continuous
Power Dissipation
  Up to T_A = +55°C 750mW
  Above T_A = +55°C ..... Derate Linearly at 6.67mW/°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

Values Apply for Each Operational Amplifier. Supply Voltage (V+) = 5V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	CA124 LIMITS			UNITS
			MIN	TYP	MAX	
T_A = +25°C						
Input Offset Voltage	V_{IO}	(Note 5)	-	2	5	mV
Output Voltage Swing	V_{OPP}	R_L = 2kΩ	0	-	V+ -1.5	V
Input Common Mode Voltage Range	V_{ICR}	(Note 4), V+ = 30V	0	-	V+ -1.5	V
Input Offset Current	I_{IO}	I_I+ - I_I-	-	3	30	nA
Input Bias Current	I_{IB}	I_I+ or I_I-, (Note 3)	-	45	150	nA
Output Current (Source)	I_O	V_I+ = +1V, V_I- = 0V, V+ = 15V	20	40	-	mA
Output Current (Sink)	I_O	V_I+ = 0V, V_I- = 1V, V+ = 15V	10	20	-	mA
		V_I+ = 0V, V_I- = 1V, V_O = 200mV	12	50	-	µA
Large Signal Voltage Gain	A_{OL}	R_L ≥ 2kΩ, V+ = 15V (For large V_O swing)	94	100	-	dB
Common Mode Rejection Ratio	CMRR	DC	70	85	-	dB
Power Supply Rejection Ratio	PSRR	DC	65	100	-	dB
Amplifier-to-Amplifier Coupling		f = 1 to 20kHz (Input referred)	-	-120	-	dB
T_A = -55°C to +125°C						
Input Offset Voltage	V_{IO}	(Note 5)	-	-	7	mV
Temperature Coefficient of Input Offset Voltage	$\propto V_{IO}$	R_S = 0Ω	-	7	-	µV/°C
Input Offset Current	I_{IO}	I_I+ - I_I-	-	-	100	nA
Temperature Coefficient of Input Offset Current	$\propto I_{IO}$		-	10	-	pA/°C
Input Bias Current	I_{IB}	I_I+ or I_I-	-	-	300	nA
Total Supply Current	I+	R_L = ∞ On all amplifiers	-	0.8	2	mA
Input Common Mode Voltage Range	V_{ICR}	V+ = 30V	0	-	V+ -2	V
Large Signal Voltage Gain	A_{OL}	R_L ≥ 2kΩ, V+ = 15V (For large V_O swing)	88	-	-	dB
OUTPUT VOLTAGE SWING						
High Level	V_{OH}	R_L = 2kΩ, V+ = 30V	26	-	-	V
		R_L = 10kΩ	27	28	-	V
Low Level	V_{OL}	R_L = 10kΩ	-	5	20	mV

Electrical Specifications Values Apply for Each Operational Amplifier. Supply Voltage (V+) = 5V, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	CA124 LIMITS			UNITS
			MIN	TYP	MAX	
OUTPUT CURRENT						
Source	I_O	$V_I+ = 1V_{DC}$, $V_I- = 0$, V+ = 15V	10	20	-	mA
Sink	I_O	$V_I- = 1V_{DC}$, $V_I+ = 0$, V+ = 15V	5	8	-	mA
Differential Input Voltage		(Note 2)	-	-	V+	V

NOTES:

1. This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$.
2. The maximum output current is approximately 40mA independent of the magnitude of V+. Continuous short circuits at V+ > 15V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V+ can cause overheating and eventual destruction of the device.
3. Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because the current is essentially constant, independent of the state of the output.
4. The input signal voltage and the input common mode voltage should not be allowed to go negative by more than 0.3V. The positive limit of the common mode voltage range is V+ - 1.5V, but either or both inputs can go to +32V without damage.
5. $V_O = 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common mode voltage range (0V to V+ - 1.5V).

Electrical Specifications Values Apply for Each Operational Amplifier. Supply Voltage (V+) = 5V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	CA224, CA324 LIMITS			UNITS
			MIN	TYP	MAX	
T_A = +25°C						
Input Offset Voltage	V_{IO}	(Note 3)	-	2	7	mV
Output Voltage Swing	V_{OPP}	$R_L = 2k\Omega$	0	-	V+ -1.5	V
Input Common Mode Voltage Range	V_{ICR}	(Note 2), V+ = 30V	0	-	V+ -1.5	V
Input Offset Current	I_{IO}	$I_I+ - I_I-$	-	5	50	nA
Input Bias Current	I_{IB}	I_I+ or I_I-, (Note 1)	-	45	250	nA
Output Current (Source)	I_O	$V_I+ = +1V$, $V_I- = 0V$, V+ = 15V	20	40	-	mA
Output Current (Sink)	I_O	$V_I+ = 0V$, $V_I- = 1V$, V+ = 15V	10	20	-	mA
		$V_I+ = 0V$, $V_I- = 1V$, $V_O = 200mV$	12	50	-	µA
Large Signal Voltage Gain	A_{OL}	$R_L \geq 2k\Omega$, V+ = 15V (For large V_O swing)	88	100	-	dB
Common Mode Rejection Ratio	CMRR	DC	65	70	-	dB
Power Supply Rejection Ratio	PSRR	DC	65	100	-	dB
Amplifier-to-Amplifier Coupling		f = 1 to 20kHz (Input referred)	-	-120	-	dB
T_A = -40°C to +85°C (CA224), T_A = 0°C to +70°C (CA324)						
Input Offset Voltage	V_{IO}	(Note 3)	-	-	9	mV
Temperature Coefficient of Input Offset Voltage	$\propto V_{IO}$	$R_S = 0\Omega$	-	7	-	µV/°C
Input Offset Current	I_{IO}	$I_I+ - I_I-$	-	-	150	nA

Electrical Specifications Values Apply for Each Operational Amplifier. Supply Voltage (V+) = 5V, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	CA224, CA324 LIMITS			UNITS
			MIN	TYP	MAX	
T_A = -40°C to +85°C (CA224), T_A = 0°C to +70°C (CA324) (Continued)						
Temperature Coefficient of Input Offset Current	$\propto I_{IO}$		-	10	-	pA/°C
Input Bias Current	I_{IB}	I_I+ or I_I-	-	-	500	nA
Total Supply Current	I+	$R_L = \infty$ On all amplifiers	-	0.8	2	mA
Input Common Mode Voltage Range	V_{ICR}	V+ = 30V	0	-	V+ -2	V
Large Signal Voltage Gain	A	$R_L \geq 2k\Omega$, V+ = 15V (For large V_O swing)	83	-	-	dB
OUTPUT VOLTAGE SWING						
High Level	V_{OH}	$R_L = 2k\Omega$, V+ = 30V	26	-	-	V
		$R_L = 10k\Omega$	27	28	-	V
Low Level	V_{OL}	$R_L = 10k\Omega$	-	5	20	mV
OUTPUT CURRENT						
Source	I_O	V_I+ = $1V_{DC}$, V_I- = 0, V+ = 15V	10	20	-	mA
Sink	I_O	V_I- = $1V_{DC}$, V_I+ = 0, V+ = 15V	5	8	-	mA
Differential Input Voltage		(Note 2)	-	-	V+	V

NOTES:

1. Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because the current is essentially constant, independent of the state of the output.
2. The input signal voltage and the input common mode voltage should not be allowed to go negative by more than 0.3V. The positive limit of the common mode voltage range is V+ - 1.5V, but either or both inputs can go to +32V without damage.
3. V_O = $1.4V_{DC}$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common mode voltage range (0V to V+ - 1.5V).

Electrical Specifications Values Apply for Each Operational Amplifier. Supply Voltage (V+) = 5V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LM2902 LIMITS			UNITS
			MIN	TYP	MAX	
T_A = -40°C to +85°C						
Input Offset Voltage	V_{IO}	(Note 3)	-	-	10	mV
Temperature Coefficient of Input Offset Voltage	$\propto V_{IO}$	$R_S = 0$	-	7	-	µV/°C
Input Offset Current	I_{IO}	I_I+ - I_I-	-	45	200	nA
Temperature Coefficient of Input Offset Current	$\propto I_{IO}$		-	10	-	pA/°C
Input Bias Current	I_{IB}	I_I+ or I_I-, (Note 1)	-	40	500	nA
Total Supply Current	I+	$R_L = \infty$ On all amplifiers	-	0.7	1.2	mA
		$R_L = \infty$, V+ = 26V	-	1.5	3	mA
Input Common Mode Voltage Range	V_{ICR}	V+ = 26V, (Note 2)	0	-	V+ -2	V
Large Signal Voltage Gain	A_{OL}	$R_L > 2k\Omega$, V+ = 15V (For large V_O swing)	83	-	-	dB

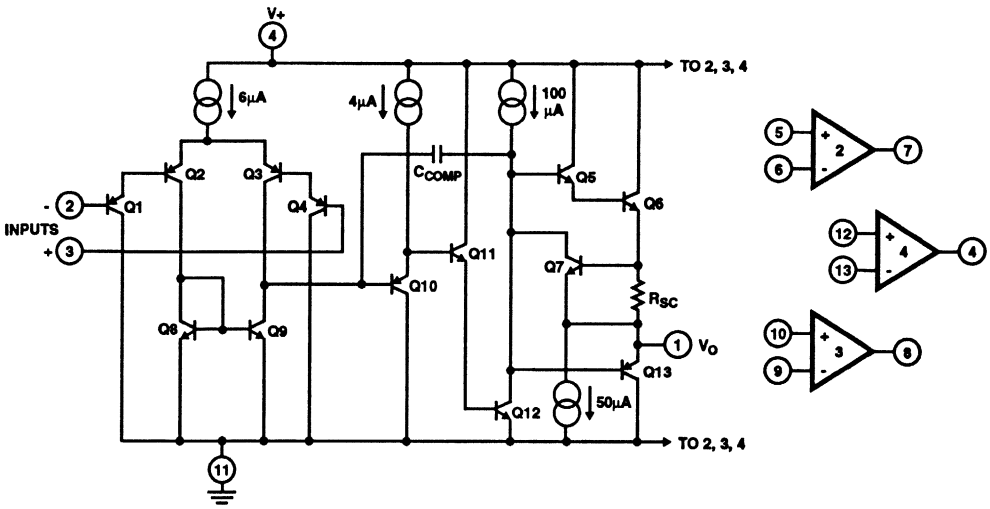
Electrical Specifications Values Apply for Each Operational Amplifier. Supply Voltage (V+) = 5V, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	LM2902 LIMITS			UNITS
			MIN	TYP	MAX	
OUTPUT VOLTAGE SWING						
High Level	V_{OH}	R_L = 2kΩ, V+ = 26V	22	-	-	V
		R_L = 10kΩ	23	28	-	V
Low Level	V_{OL}	R_L = 10kΩ	-	5	100	mV
OUTPUT CURRENT						
Source	I_O	V_{I+} = 1V_{DC}, V_{I-} = 0, V+ = 15V	10	20	-	mA
Sink	I_O	V_{I-} = 1V_{DC}, V_{I+} = 0, V+ = 15V	5	8	-	mA
Differential Input Voltage		(Note 2)	-	-	V+	V

NOTES:

1. Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because the current is essentially constant, independent of the state of the output.
2. The input signal voltage and the input common mode voltage should not be allowed to go negative by more than 0.3V. The positive limit of the common mode voltage range is V+ - 1.5V, but either or both inputs can go to +32V without damage.
3. V_O = 1.4V_{DC}, R_S = 0Ω with V+ from 5V to 30V; and over the full input common mode voltage range (0V to V+ - 1.5V).

Schematic Diagram (One of Four Operational Amplifiers)



Typical Performance Curves

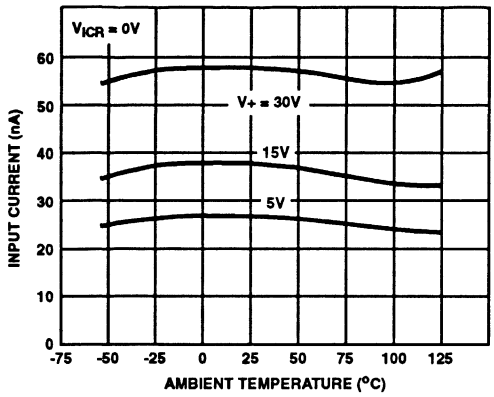


FIGURE 1. INPUT CURRENT vs AMBIENT TEMPERATURE

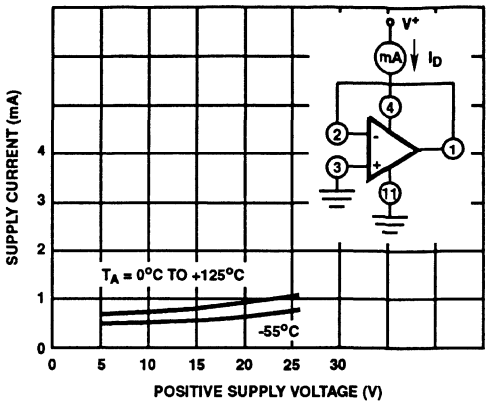


FIGURE 2. SUPPLY CURRENT vs SUPPLY VOLTAGE

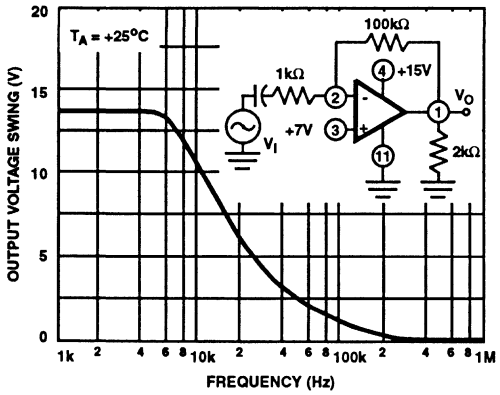


FIGURE 3. LARGE SIGNAL FREQUENCY RESPONSE

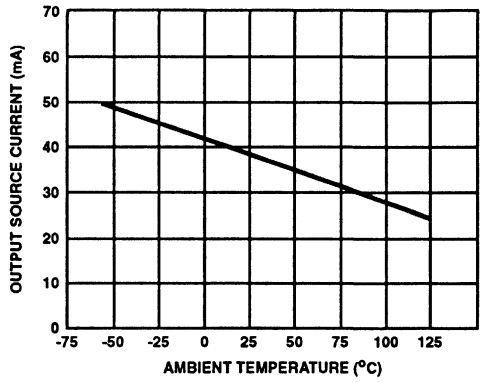


FIGURE 4. OUTPUT CURRENT vs AMBIENT TEMPERATURE

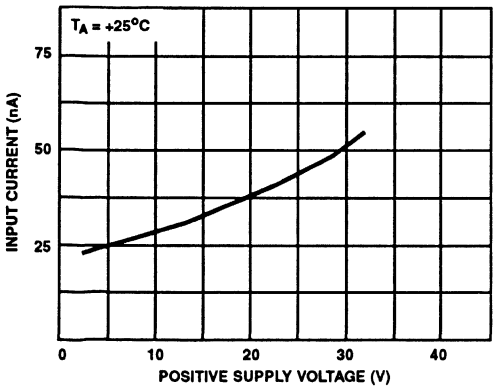


FIGURE 5. INPUT CURRENT vs SUPPLY VOLTAGE

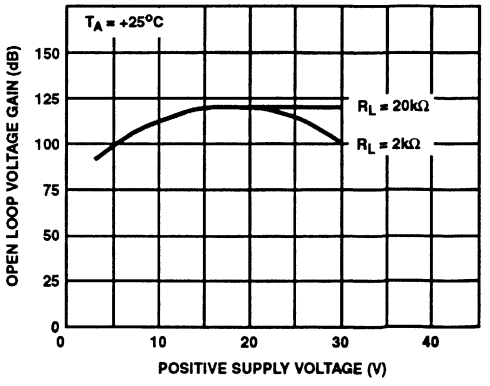


FIGURE 6. VOLTAGE GAIN vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

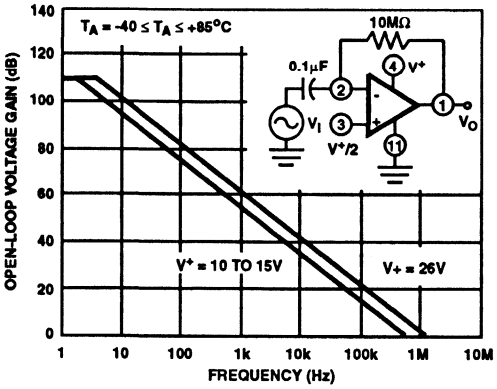


FIGURE 7. OPEN LOOP FREQUENCY RESPONSE

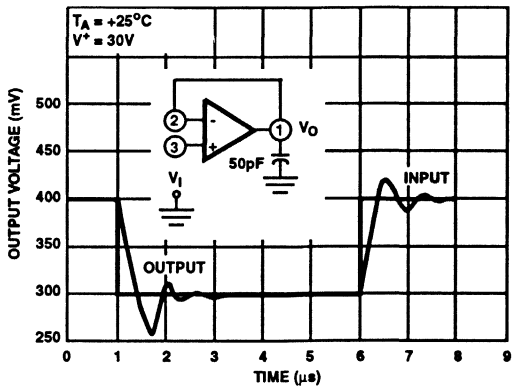


FIGURE 8. VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)

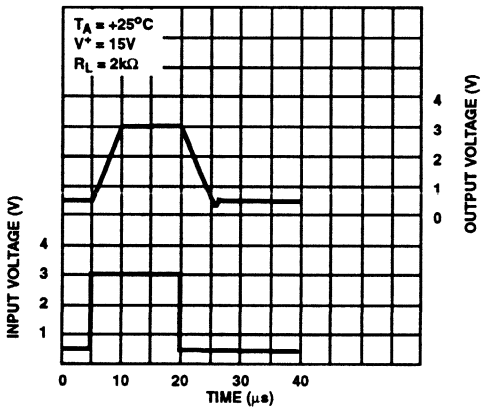


FIGURE 9. VOLTAGE FOLLOWER PULSE RESPONSE (LARGE SIGNAL)

HARRIS SEMICONDUCTOR

CA158, CA258 CA358, CA2904, LM358*, LM2904*

Dual Operational Amplifiers for Commercial Industrial, and Military Applications

March 1993

Features

- Internal Frequency Compensation for Unity Gain
- High DC Voltage Gain ..... 100dB (Typ.)
- Wide Bandwidth at Unity Gain ..... 1MHz (Typ.)
- Wide Power Supply Range:
  - Single Supply ..... 3 to 30V
  - Dual Supplies ..... ±1.5 to ±15V
- Low Supply Current ..... 1.5 mA (Typ.)
- Low Input Bias Current
- Low Input Offset Voltage and Current
- Input Common-Mode Voltage Range Includes Ground
- Differential Input Voltage Range Equal to V+ Range
- Large Output Voltage Swing ..... 0 to V+ -1.5V

Description

The CA158, CA158A, CA258, CA258A, CA358, CA358A and CA2904 types consist of two independent, high gain, internally frequency compensated operational amplifiers which are designed specifically to operate from a single power supply over a wide range of voltages. They may also be operated from split power supplies. The supply current is basically independent of the supply voltage over the recommended voltage range.

These devices are particularly useful in interface circuits with digital systems and can be operated from the single common $5V_{DC}$ power supply. They are also intended for transducer amplifiers, DC gain blocks and many other conventional op amp circuits which can benefit from the single power supply capability.

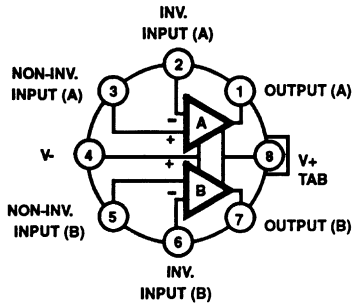
The CA158, CA158A, CA258, CA258A, CA358, CA358A, and CA2904 types are an equivalent to or a replacement for the industry types 158, 158A, 258, 258A, 358, 358A, and CA2904.

Ordering Information

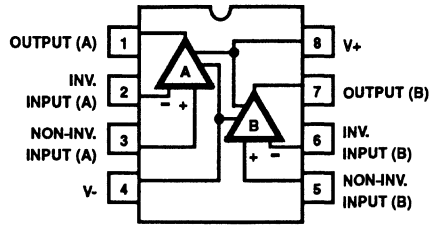
PART NUMBER	SUFFIX LETTERS	PACKAGE
CA158, A CA258, A CA358, A CA2904	E	8 Lead Plastic DIP
	M	8 Lead SOIC
CA158, A CA258, A CA358, A	T	8 Pin TO-5 Can with Standard Leads
	S	8 Pin TO-5 Can with Dual-In-Line Formed Leads

Pinouts

CA158, CA258, and CA358 (TO-5 CAN)
TOP VIEW



CA158, CA258, CA358, AND CA2904 (PDIP, SOIC)
TOP VIEW



* Technical Data on LM Branded types is identical to the corresponding CA Branded types.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1019.2

Absolute Maximum Ratings

Supply Voltage (Note 5)
- CA2904 ..... 26V or ±13V
- Other Types ..... 32V or ±16V

Differential Input Voltage (All Types) 32V
Input Voltage ..... -0.3V to V+V
Input Current (V_I < -0.3V) (Note 5) 50mA
Output Short Circuit Duration (V+ ≤ 15V) (Note 6) ..... Continuous
Power Dissipation
- Up to T_A = -55°C 630mW
- Above T_A = -55°C ..... Derate Linearly at 6.67 mW/°C

Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Values Apply for Each Operational Amplifier, Supply Voltage (V+) = 5V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	CA158A LIMITS MIN	CA158A LIMITS TYP	CA158A LIMITS MAX	UNITS
T_A = +25°C						
Input Offset Voltage	V_{IO}	(Note 3)	-	1	2	mV
Output Voltage Swing	V_{OPP}	R_L = 2kΩ	0	-	V+ -1.5	V
Input Common Mode Voltage Range	V_{ICR}	(Note 2), V+ = 30V	0	-	V+ -1.5	V
Input Offset Current	I_{IO}	I_I+ - I_I-	-	2	10	nA
Input Bias Current	I_{IB}	I_I+ or I_I-, (Note 1)	-	20	50	nA
Output Current (Source)	I_O	V_I+ = +1V, V_I- = 0V, V+ = 15V	20	40	-	mA
Output Current (Sink)	I_O	V_I+ = 0V, V_I- = 1V, V+ = 15V	10	20	-	mA
		V_I+ = 0V, V_I- = 1V, V_O = 200mV	12	50	-	µA
Short Circuit Output Current		R_L = 0Ω (to Ground) (Note 4)	-	40	60	mA
Large Signal Voltage Gain	A_{OL}	R_L ≥ 2kΩ, V+ = 15V (For large V_O swing)	50	100	-	V/mV
Common Mode Rejection Ratio	CMRR	DC	70	85	-	dB
Power Supply Rejection Ratio	PSRR	DC	65	100	-	dB
Amplifier-to-Amplifier Coupling		f = 1 to 20kHz (Input referred)	-	-120	-	dB
T_A = -55°C to +125°C						
Input Offset Voltage	V_{IO}	(Note 3)	-	-	4	mV
Temperature Coefficient of Input Offset Voltage	$\propto V_{IO}$	R_S = 0Ω	-	7	15	µV/°C
Input Offset Current	I_{IO}	I_I+ - I_I-	-	-	30	nA
Temperature Coefficient of Input Offset Current	$\propto I_{IO}$		-	10	200	pA/°C
Input Bias Current	I_{IB}	I_I+ or I_I-	-	40	100	nA
Input Common Mode Voltage Range	V_{ICR}	V+ = 30V (Note 2)	0	-	V+ -2	V

Electrical Specifications Values Apply for Each Operational Amplifier, Supply Voltage (V+) = 5V, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	CA158A LIMITS			UNITS
			MIN	TYP	MAX	
Supply Current	I+	$R_L = \infty$ On all amplifiers	-	0.7	1.2	mA
		$R_L = \infty$, V+ = 30V	-	1.5	3	mA

NOTES:

1. Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.
2. The input signal voltages and the input common mode voltage should not be allowed to go negative by more than 0.3V. The positive limit of the common mode voltage range is V+ - 1.5V, but either or both inputs can go to +32V without damage.
3. $V_O = 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common mode voltage range (0V to V+ - 1.5V).
4. The maximum output current is approximately 40mA independent of the magnitude of V+. Continuous short circuits at V+ > 15V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.
5. This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3VDC.
6. The maximum output current is approximately 40mA independent of the magnitude of V+. Continuous short circuits at V+ > 15V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

Electrical Specifications Values Apply for Each Operational Amplifier, Supply Voltage (V+) = 5V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	CA258A LIMITS			UNITS
			MIN	TYP	MAX	
T_A = +25°C						
Input Offset Voltage	V_{IO}	(Note 3)	-	1	3	mV
Output Voltage Swing	V_{OPP}	$R_L = 2k\Omega$	0	-	V+ -1.5	V
Input Common Mode Voltage Range	V_{ICR}	(Note 2), V+ = 30V	0	-	V+ -1.5	V
Input Offset Current	I_{IO}	$I_I+ - I_I-$	-	2	15	nA
Input Bias Current	I_{IB}	I_I+ or I_I-, (Note 1)	-	40	80	nA
Output Current (Source)	I_O	V_I+ = +1V, V_I- = 0V, V+ = 15V	20	40	-	mA
Output Current (Sink)	I_O	V_I+ = 0V, V_I- = 1V, V+ = 15V	10	20	-	mA
		V_I+ = 0V, V_I- = 1V, V_O = 200mV	12	50	-	µA
Short Circuit Output Current		$R_L = 0\Omega$ (to Ground) (Note 4)	-	40	60	mA
Large Signal Voltage Gain	A_{OL}	$R_L \geq 2k\Omega$, V+ = 15V (For large V_O swing)	50	100	-	V/mV
Common Mode Rejection Ratio	CMRR	DC	70	85	-	dB
Power Supply Rejection Ratio	PSRR	DC	65	100	-	dB
Amplifier-to-Amplifier Coupling		f = 1 to 20kHz (Input referred)	-	-120	-	dB
T_A = -25°C to +85°C						
Input Offset Voltage	V_{IO}	(Note 3)	-	-	4	mV
Temperature Coefficient of Input Offset Voltage	$\propto V_{IO}$	$R_S = 0\Omega$	-	7	15	µV/°C
Input Offset Current	I_{IO}	$I_I+ - I_I-$	-	-	30	nA

Electrical Specifications Values Apply for Each Operational Amplifier, Supply Voltage (V+) = 5V, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	CA258A LIMITS			UNITS
			MIN	TYP	MAX	
Temperature Coefficient of Input Offset Current	$\propto I_{IO}$		-	10	200	pA/°C
Input Bias Current	I_{IB}	I_I+ or I_I-	-	40	100	nA
Input Common Mode Voltage Range	V_{ICR}	V+ = 30V (Note 2)	0	-	V+ -2	V
Supply Current	I+	$R_L = \infty$ On all amplifiers	-	0.7	1.2	mA
		$R_L = \infty$, V+ = 30V	-	1.5	3	mA

NOTES:

1. Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.
2. The input signal voltages and the input common mode voltage should not be allowed to go negative by more than 0.3V. The positive limit of the common mode voltage range is V+ - 1.5V, but either or both inputs can go to +32V without damage.
3. $V_O = 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common mode voltage range (0V to V+ - 1.5V).
4. The maximum output current is approximately 40mA independent of the magnitude of V+. Continuous short circuits at V+ > 15V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

Electrical Specifications Values Apply for Each Operational Amplifier, Supply Voltage (V+) = 5V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	CA358A LIMITS			UNITS
			MIN	TYP	MAX	
T_A = +25°C						
Input Offset Voltage	V_{IO}	(Note 3)	-	2	3	mV
Output Voltage Swing	V_{OPP}	$R_L = 2k\Omega$	0	-	V+ -1.5	V
Input Common Mode Voltage Range	V_{ICR}	(Note 2), V+ = 30V	0	-	V+ -1.5	V
Input Offset Current	I_{IO}	$I_I+ - I_I-$	-	5	30	nA
Input Bias Current	I_{IB}	I_I+ or I_I-, (Note 1)	-	45	100	nA
Output Current (Source)	I_O	V_I+ = +1V, V_I- = 0V, V+ = 15V	20	40	-	mA
Output Current (Sink)	I_O	V_I+ = 0V, V_I- = 1V, V+ = 15V	10	20	-	mA
		V_I+ = 0V, V_I- = 1V, V_O = 200mV	12	50	-	µA
Short Circuit Output Current		$R_L = 0\Omega$ (to Ground) (Note 4)	-	40	60	mA
Large Signal Voltage Gain	A_{OL}	$R_L \geq 2k\Omega$, V+ = 15V (For large V_O swing)	25	100	-	V/mV
Common Mode Rejection Ratio	CMRR	DC	65	85	-	dB
Power Supply Rejection Ratio	PSRR	DC	65	100	-	dB
Amplifier-to-Amplifier Coupling		f = 1 to 20kHz (Input referred)	-	-120	-	dB
T_A = 0 to +70°C						
Input Offset Voltage	V_{IO}	(Note 3)	-	-	5	mV
Temperature Coefficient of Input Offset Voltage	$\propto V_{IO}$	$R_S = 0\Omega$	-	7	20	µV/°C
Input Offset Current	I_{IO}	$I_I+ - I_I-$	-	-	75	nA
Temperature Coefficient of Input Offset Current	$\propto I_{IO}$		-	10	300	pA/°C

Electrical Specifications Values Apply for Each Operational Amplifier, Supply Voltage (V+) = 5V, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	CA358A LIMITS			UNITS
			MIN	TYP	MAX	
Input Bias Current	I_{IB}	I_I+ or I_I-	-	40	200	nA
Input Common Mode Voltage Range	V_{ICR}	V+ = 30V (Note 2)	0	-	V+ -2	V
Supply Current	I+	$R_L = \infty$ On all amplifiers	-	0.7	1.2	mA
		$R_L = \infty$, V+ = 30V	-	1.5	3	mA

NOTES:

1. Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.
2. The input signal voltages and the input common mode voltage should not be allowed to go negative by more than 0.3V. The positive limit of the common mode voltage range is V+ - 1.5V, but either or both inputs can go to +32V without damage.
3. $V_O = 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common mode voltage range (0V to V+ - 1.5V).
4. The maximum output current is approximately 40mA independent of the magnitude of V+. Continuous short circuits at V+ > 15V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

Electrical Specifications Values Apply for Each Operational Amplifier, Supply Voltage (V+) = 5V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS CA158, CA258			UNITS
			MIN	TYP	MAX	
T_A = +25°C						
Input Offset Voltage	V_{IO}	(Note 3)	-	2	5	mV
Output Voltage Swing	V_{OPP}	$R_L = 2k\Omega$	0	-	V+ -1.5	V
Input Common Mode Voltage Range	V_{ICR}	(Note 2), V+ = 30V	0	-	V+ -1.5	V
Input Offset Current	I_{IO}	I_I+ - I_I-	-	3	30	nA
Input Bias Current	I_{IB}	I_I+ or I_I-, (Note 1)	-	45	150	nA
Output Current (Source)	I_O	V_I+ = +1V, V_I- = 0V, V+ = 15V	20	40	-	mA
Output Current (Sink)	I_O	V_I+ = 0V, V_I- = 1V, V+ = 15V	10	20	-	mA
		V_I+ = 0V, V_I- = 1V, V_O = 200mV	12	50	-	µA
Short Circuit Output Current		$R_L = 0\Omega$ (to Ground) (Note 4)	-	40	60	mA
Large Signal Voltage Gain	A_{OL}	$R_L \geq 2k\Omega$, V+ = 15V (For large V_O swing)	50	100	-	V/mV
Common Mode Rejection Ratio	CMRR	DC	70	85	-	dB
Power Supply Rejection Ratio	PSRR	DC	65	100	-	dB
Amplifier-to-Amplifier Coupling		f = 1 to 20kHz (Input referred)	-	-120	-	dB
T_A = -55°C to +125°C (CA158); T_A = -25°C to +85°C (CA258)						
Input Offset Voltage	V_{IO}	(Note 3)	-	-	7	mV
Temperature Coefficient of Input Offset Voltage	$\propto V_{IO}$	$R_S = 0\Omega$	-	7	-	µV/°C
Input Offset Current	I_{IO}	I_I+ - I_I-	-	-	100	nA
Temperature Coefficient of Input Offset Current	$\propto I_{IO}$		-	10	-	pA/°C

Electrical Specifications Values Apply for Each Operational Amplifier, Supply Voltage (V+) = 5V, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS CA158, CA258			UNITS
			MIN	TYP	MAX	
Input Bias Current	I_{IB}	I_I+ or I_I-	-	40	300	nA
Input Common Mode Voltage Range	V_{ICR}	V+ = 30V (Note 2)	0	-	V+ -2	V
Supply Current	I+	$R_L = \infty$ On all amplifiers	-	0.7	1.2	mA
		$R_L = \infty$, V+ = 30V	-	1.5	3	mA

NOTES:

1. Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.
2. The input signal voltages and the input common mode voltage should not be allowed to go negative by more than 0.3V. The positive limit of the common mode voltage range is V+ - 1.5V, but either or both inputs can go to +32V without damage.
3. $V_O = 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common mode voltage range (0V to V+ - 1.5V).
4. The maximum output current is approximately 40mA independent of the magnitude of V+. Continuous short circuits at V+ > 15V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

Electrical Specifications Values Apply for Each Operational Amplifier, Supply Voltage (V+) = 5V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	CA358 LIMITS			UNITS
			MIN	TYP	MAX	
T_A = +25°C						
Input Offset Voltage	V_{IO}	(Note 3)	-	2	7	mV
Output Voltage Swing	V_{OPP}	$R_L = 2k\Omega$	0	-	V+ -1.5	V
Input Common Mode Voltage Range	V_{ICR}	(Note 2), V+ = 30V	0	-	V+ -1.5	V
Input Offset Current	I_{IO}	I_I+ - I_I-	-	5	50	nA
Input Bias Current	I_{IB}	I_I+ or I_I-, (Note 1)	-	45	250	nA
Output Current (Source)	I_O	V_I+ = +1V, V_I- = 0V, V+ = 15V	20	40	-	mA
Output Current (Sink)	I_O	V_I+ = 0V, V_I- = 1V, V+ = 15V	10	20	-	mA
		V_I+ = 0V, V_I- = 1V, V_O = 200mV	12	50	-	µA
Short Circuit Output Current		$R_L = 0\Omega$ (to Ground) (Note 4)	-	40	60	mA
Large Signal Voltage Gain	A_{OL}	$R_L \geq 2k\Omega$, V+ = 15V (For large V_O swing)	25	100	-	V/mV
Common Mode Rejection Ratio	CMRR	DC	65	70	-	dB
Power Supply Rejection Ratio	PSRR	DC	65	100	-	dB
Amplifier-to-Amplifier Coupling		f = 1 to 20kHz (Input referred)	-	-120	-	dB
T_A = 0 to +70°C						
Input Offset Voltage	V_{IO}	(Note 3)	-	-	9	mV
Temperature Coefficient of Input Offset Voltage	$\propto V_{IO}$	$R_S = 0\Omega$	-	7	-	µV/°C
Input Offset Current	I_{IO}	I_I+ - I_I-	-	-	150	nA
Temperature Coefficient of Input Offset Current	$\propto I_{IO}$		-	10	-	pA/°C

Electrical Specifications Values Apply for Each Operational Amplifier, Supply Voltage (V+) = 5V, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	CA358 LIMITS			UNITS
			MIN	TYP	MAX	
Input Bias Current	I_{IB}	I_I+ or I_I-	-	40	500	nA
Input Common Mode Voltage Range	V_{ICR}	V+ = 30V (Note 2)	0	-	V+ -2	V
Supply Current	I+	$R_L = \infty$ On all amplifiers	-	0.7	1.2	mA
		$R_L = \infty$, V+ = 30V	-	1.5	3	mA

NOTES:

1. Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.
2. The input signal voltages and the input common mode voltage should not be allowed to go negative by more than 0.3V. The positive limit of the common mode voltage range is V+ - 1.5V, but either or both inputs can go to +32V without damage.
3. $V_O = 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common mode voltage range (0V to V+ - 1.5V).
4. The maximum output current is approximately 40mA independent of the magnitude of V+. Continuous short circuits at V+ > 15V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

Electrical Specifications Values Apply for Each Operational Amplifier, Supply Voltage (V+) = 5V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	CA2904 LIMITS			UNITS
			MIN	TYP	MAX	
T_A = +25°C						
Input Offset Voltage	V_{IO}	(Note 3)	-	2	7	mV
Output Voltage Swing	V_{OPP}	R_L = 10kΩ	0	-	V+ -1.5	V
Input Common Mode Voltage Range	V_{ICR}	(Note 2), V+ = 30V	0	-	V+ -1.5	V
Input Offset Current	I_{IO}	$I_I+ - I_I-$	-	5	50	nA
Input Bias Current	I_{IB}	I_I+ or I_I-, (Note 1)	-	45	250	nA
Output Current (Source)	I_O	V_I+ = +1V, V_I- = 0V, V+ = 15V	20	40	-	mA
Output Current (Sink)	I_O	V_I+ = 0V, V_I- = 1V, V+ = 15V	10	20	-	mA
Short Circuit Output Current		R_L = 0Ω (to Ground) (Note 4)	-	40	60	mA
Large Signal Voltage Gain	A_{OL}	$R_L \geq 2k\Omega$, V+ = 15V (For large V_O swing)	-	100	-	V/mV
Common Mode Rejection Ratio	CMRR	DC	50	70	-	dB
Power Supply Rejection Ratio	PSRR	DC	50	100	-	dB
Amplifier-to-Amplifier Coupling		f = 1 to 20kHz (Input referred)	-	-120	-	dB
T_A = -40°C to +85°C						
Input Offset Voltage	V_{IO}	(Note 3)	-	-	10	mV
Temperature Coefficient of Input Offset Voltage	$\propto V_{IO}$	$R_S = 0\Omega$	-	7	-	µV/°C
Input Offset Current	I_{IO}	$I_I+ - I_I-$	-	45	200	nA
Temperature Coefficient of Input Offset Current	$\propto I_{IO}$		-	10	-	pA/°C
Input Bias Current	I_{IB}	I_I+ or I_I-	-	40	500	nA

Electrical Specifications Values Apply for Each Operational Amplifier, Supply Voltage (V+) = 5V, Unless Otherwise Specified **(Continued)**

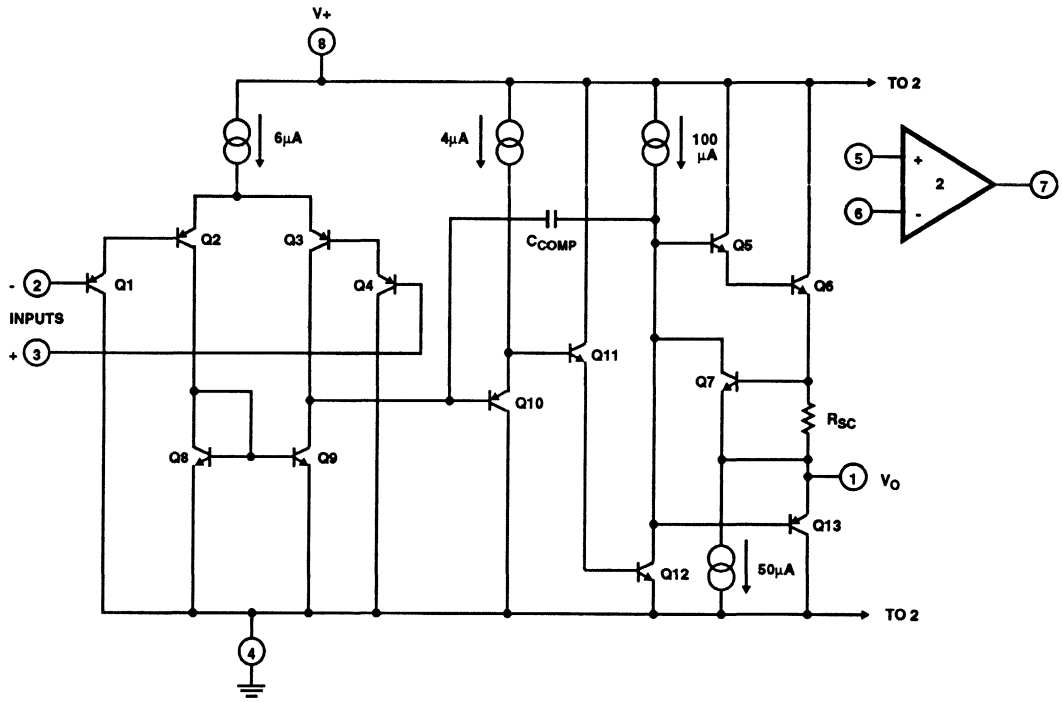
PARAMETERS	SYMBOL	TEST CONDITIONS	CA2904 LIMITS			UNITS
			MIN	TYP	MAX	
Input Common Mode Voltage Range	V_{ICR}	V+ = 30V (Note 2)	0	-	V+ -2	V
Supply Current	I+	R_L = ∞ On all amplifiers	-	0.7	1.2	mA
		R_L = ∞, V+ = 30V	-	1.5	3	mA

NOTES:

1. Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.
2. The input signal voltages and the input common mode voltage should not be allowed to go negative by more than 0.3V. The positive limit of the common mode voltage range is V+ - 1.5V, but either or both inputs can go to +32V without damage.
3. V_O = 1.4V_{DC}, R_S = 0Ω with V+ from 5V to 30V; and over the full input common mode voltage range (0V to V+ - 1.5V).
4. The maximum output current is approximately 40mA independent of the magnitude of V+. Continuous short circuits at V+ > 15V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

Schematic Diagram

ONE OF TWO OPERATIONAL AMPLIFIERS



Typical Performance Curves

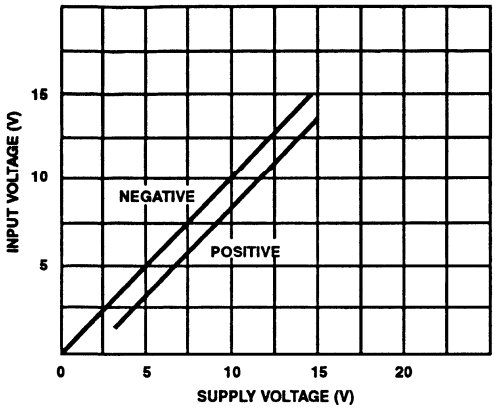


FIGURE 1. INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

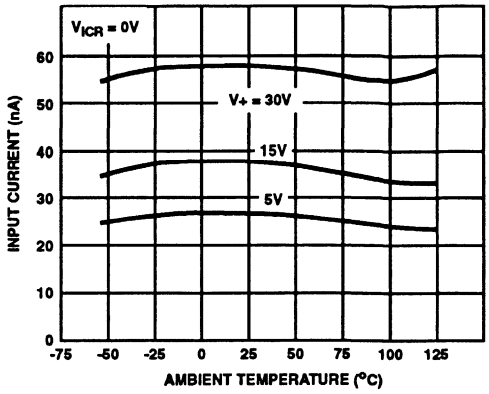


FIGURE 2. INPUT CURRENT vs AMBIENT TEMPERATURE

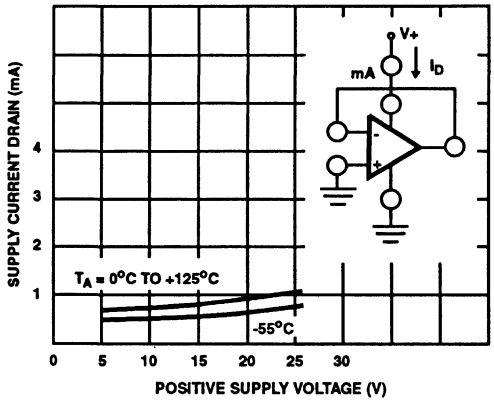


FIGURE 3. SUPPLY CURRENT DRAIN vs SUPPLY VOLTAGE

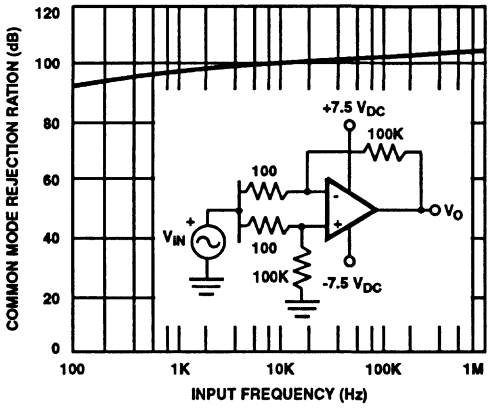


FIGURE 4. COMMON MODE REJECTION RATIO vs INPUT FREQUENCY

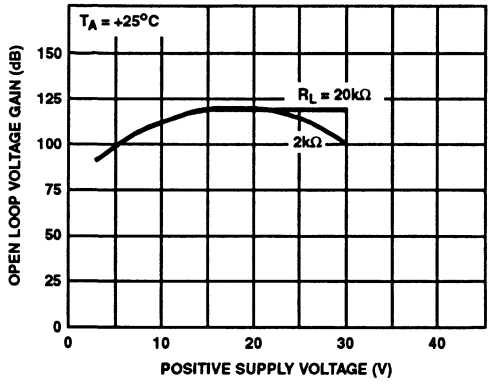


FIGURE 5. VOLTAGE GAIN vs SUPPLY VOLTAGE

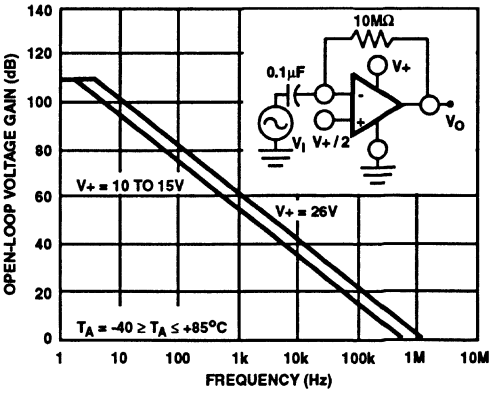


FIGURE 6. OPEN-LOOP FREQUENCY RESPONSE

Typical Performance Curves (Continued)

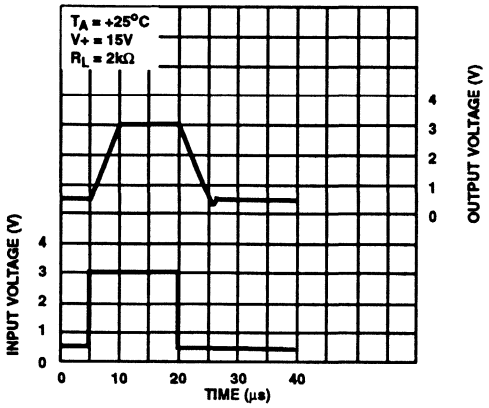


FIGURE 7. VOLTAGE FOLLOWER PULSE RESPONSE (LARGE SIGNAL)

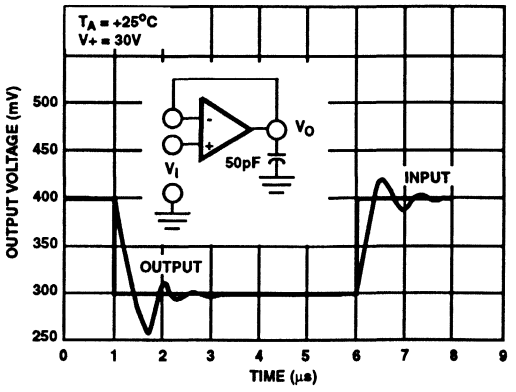


FIGURE 8. VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)

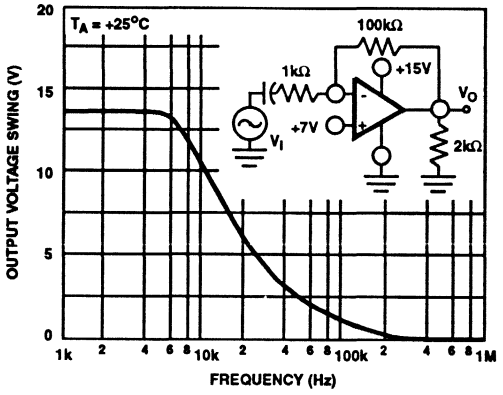


FIGURE 9. LARGE-SIGNAL FREQUENCY RESPONSE

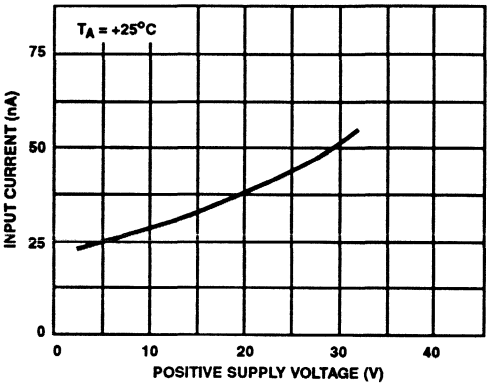


FIGURE 10. INPUT CURRENT vs SUPPLY VOLTAGE

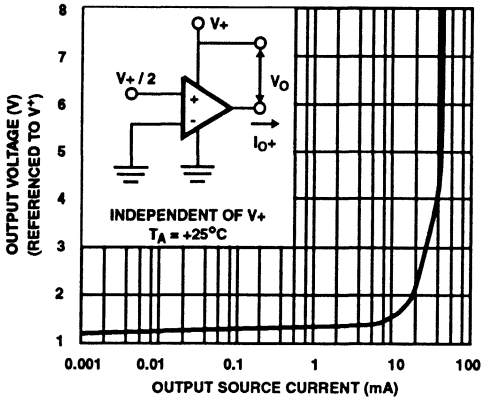


FIGURE 11. OUTPUT SOURCE CURRENT CHARACTERISTICS

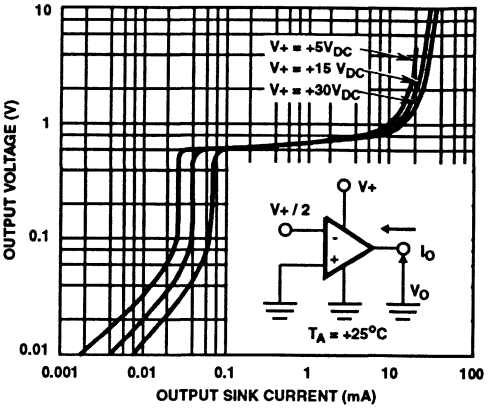


FIGURE 12. OUTPUT SINK CURRENT CHARACTERISTICS

Typical Performance Curves (Continued)

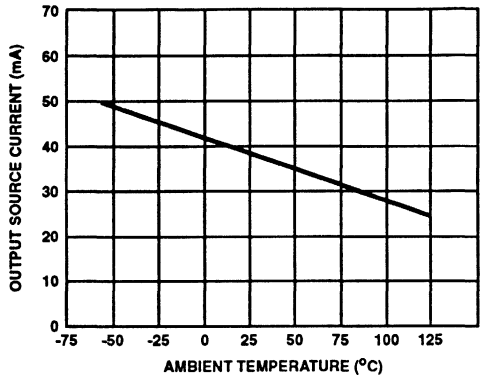
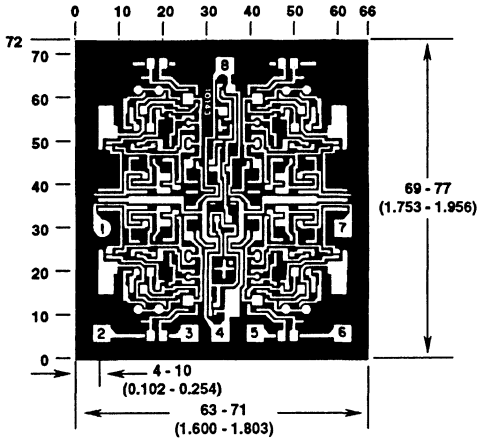


FIGURE 13. OUTPUT CURRENT vs AMBIENT TEMPERATURE

Metallization Mask Layout



Dimensions in parentheses are in millimeters and derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

HARRIS SEMICONDUCTOR

CA741, CA1458, CA1558, LM741*, LM1458*, LM1558*

High Gain Single and Dual Operational Amplifiers for Military, Industrial and Commercial Applications

March 1993

Features

- Input Bias Current (All Types) 500nA (Max.)
- Input Offset Current (All Types) 200nA (Max.)

Applications

- Comparator
- DC Amplifier
- Integrator or Differentiator
- Multivibrator
- Summing Amplifier
- Narrow Band or Band Pass Filter

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
CA741E	-55°C to +125°C	8 Lead Plastic DIP
CA741CE	0°C to +70°C	8 Lead Plastic DIP
CA1458E	0°C to +70°C	8 Lead Plastic DIP
CA1558E	-55°C to +125°C	8 Lead Plastic DIP
CA741T	-55°C to +125°C	8 Pin Can
CA741CT	0°C to +70°C	8 Pin Can
CA1458T	0°C to +70°C	8 Pin Can
CA1558T	-55°C to +125°C	8 Pin Can

NOTE: All types in any package style can be operated over the temperature range of -55°C to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0°C to +70°C.

Description

The CA1458, CA1558 (dual types); CA741C, CA741 (single types); high-gain operational amplifiers for use in military, industrial, and commercial applications.

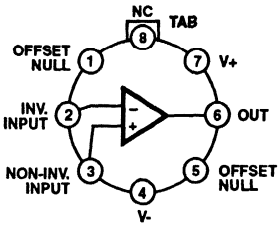
These monolithic silicon integrated circuit devices provide output short circuit protection and latch-free operation. These types also feature wide common mode and differential mode signal ranges and have low offset voltage nulling capability when used with an appropriately valued potentiometer. A 10kΩ potentiometer is used for offset nulling types CA741C, CA741 (See Figure 4); and types CA1458, CA1558, have no specific terminals for offset nulling. Each type consists of a differential input amplifier that effectively drives a gain and level shifting stage having a complementary emitter follower output.

The manufacturing process make it possible to produce IC operational amplifiers with low burst ("popcorn") noise characteristics. The CA741 gives limit specifications for burst noise in the data bulletin, File Number 530. Contact your Sales Representative for information pertinent to other operational amplifier types that meet low burst noise specifications.

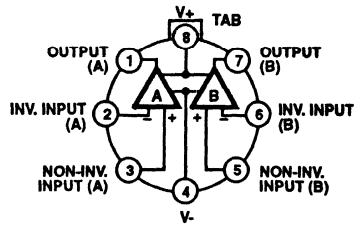
2 OPERATIONAL AMPLIFIERS

Pinouts

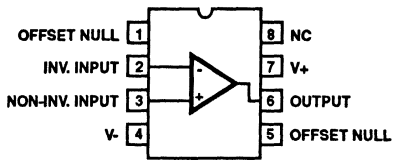
CA741, CA741C (TO-5 CAN)
TOP VIEW



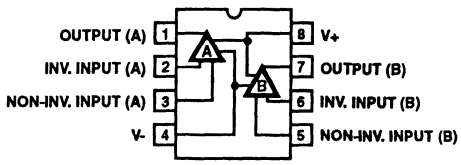
CA1458, CA1558 (TO-5 CAN)
TOP VIEW



CA741, CA741C (PDIP)
TOP VIEW



CA1458, CA1558 (PDIP)
TOP VIEW



* Technical Data on LM Branded types is identical to the corresponding CA Branded types.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 531.2

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals)
- CA741C, CA1458 (Note 3) 36V
- CA741, CA1558 (Note 3) 44V

Differential Input Voltage 30V
Input Voltage (Note 2) ..... ±15V
Offset Terminal to V- Terminal Voltage (CA741C, CA741) ....±0.5V
Output Short Circuit Duration ..... Indefinite
Power Dissipation
- Up to +70°C (CA741C) 500mW
- Up to +75°C (CA741) 500mW
- Up to +30°C (CA1558) 680mW
- Up to +25°C (CA1458) 680mW

For Temperatures exceeding those indicated above ..... Derate Linearly 6.67mW/°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
- CA741, CA1558 ..... -55°C to +125°C
- CA741C, CA1458 ..... 0°C to +70°C (Note 4)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications Typical Values Intended Only for Design Guidance, V± = ±15V

PARAMETERS	SYMBOL	TEST CONDITIONS	TYPICAL VALUE (ALL TYPES)	UNITS
Input Capacitance	C_I		1.4	pF
Offset Voltage Adjustment Range			±15	mV
Output Resistance	R_O		75	Ω
Output Short Circuit Current			25	mA
Transient Response Rise Time	t_R	Unity Gain, V_I = 20mV, R_L = 2kΩ, $C_L \leq$ 100pF	0.3	µs
Overshoot	O.S.		5.0	%
Slew Rate (Closed Loop)	SR	$R_L \geq$ 2kΩ	0.5	V/µs

Electrical Specifications For Equipment Design, V± = ±15V

PARAMETERS	SYMBOL	TEST CONDITIONS	TEMPERATURE	LIMITS CA741C, CA1458 (NOTE 1) MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{IO}	$R_S \leq$ 10kΩ	+25°C	-	2	6	mV
			0°C to +70°C	-	-	7.5	mV
Input Offset Current	I_{IO}		+25°C	-	20	200	nA
			0°C to +70°C	-	-	300	nA
Input Bias Current	I_{IB}		+25°C	-	80	500	nA
			0°C to +70°C	-	-	800	nA
Input Resistance	R_I			0.3	2	-	MΩ
Open Loop Differential Voltage Gain	A_{OL}	$R_L \geq$ 2kΩ, V_O = ±10V	+25°C	20,000	200,000	-	V/V
			0°C to +70°C	15,000	-	-	V/V
Common Mode Input Voltage Range	V_{ICR}		+25°C	±12	±13	-	V
Common Mode Rejection Ratio	CMRR	$R_S \leq$ 10kΩ	+25°C	70	90	-	dB
Supply Voltage Rejection Ratio	PSRR	$R_S \leq$ 10kΩ	+25°C	-	30	150	µV/V

Electrical Specifications For Equipment Design, V± = ±15V **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	TEMPERATURE	LIMITS CA741C, CA1458 (NOTE 1) MIN	TYP	MAX	UNITS
Output Voltage Swing	V_{OPP}	$R_L \geq 10k\Omega$	+25°C	±12	±14	-	V
		$R_L \geq 2k\Omega$	+25°C	±10	±13	-	V
			0°C to +70°C	±10	±13	-	V
Supply Current	I±		+25°C	-	1.7	2.8	mA
Device Dissipation	P_D		+25°C	-	50	85	mW

NOTE: 1. Values Apply for Each Section of the Dual Amplifiers

Electrical Specifications For Equipment Design, V± = ±15V

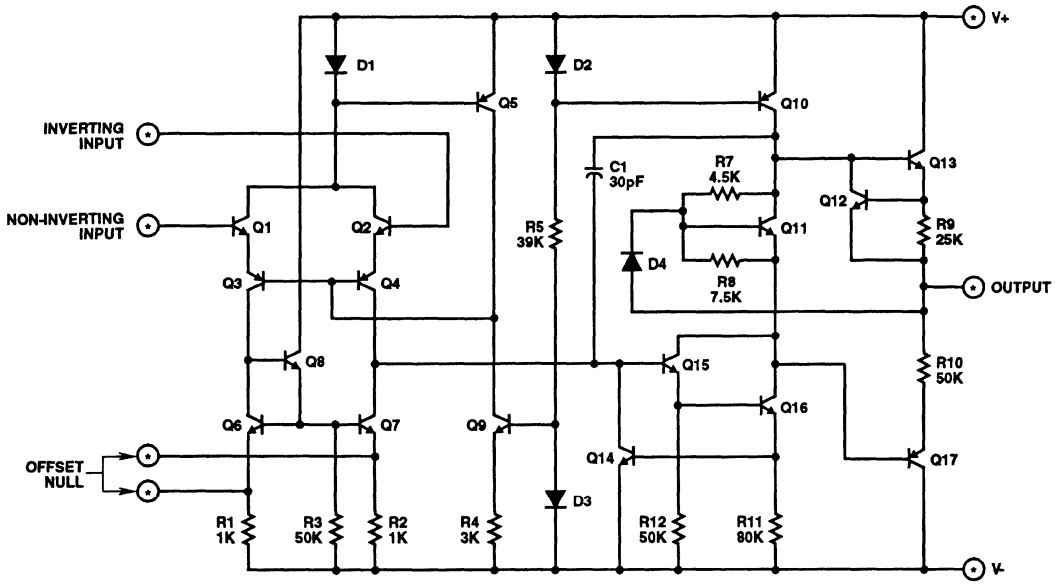
PARAMETERS	SYMBOL	TEST CONDITIONS	TEMPERATURE	LIMITS CA741, CA1558 (NOTE 1) MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{IO}	$R_S \leq 10k\Omega$	+25°C	-	1	5	mV
			-55°C to +125°C	-	1	6	mV
Input Offset Current	I_{IO}		+25°C	-	20	200	nA
			-55°C	-	85	500	nA
			+125°C	-	7	200	nA
Input Bias Current	I_{IB}		+25°C	-	80	500	nA
			-55°C	-	300	1500	nA
			+125°C	-	30	500	nA
Input Resistance	R_I		-	0.3	2	-	MΩ
Open Loop Differential Voltage Gain	A_{OL}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	+25°C	50,000	200,000	-	V/V
			-55°C to +125°C	25,000	-	-	V/V
Common Mode Input Voltage Range	V_{ICR}		-55°C to +125°C	±12	±13	-	V
Common Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$	-55°C to +125°C	70	90	-	dB
Supply Voltage Rejection Ratio	PSRR	$R_S \leq 10k\Omega$	-55°C to +125°C	-	30	150	µV/V
Output Voltage Swing	V_{OPP}	$R_L \geq 10k\Omega$	-55°C to +125°C	±12	±14	-	V
		$R_L \geq 2k\Omega$	-55°C to +125°C	±10	±13	-	V
Supply Current	I±		+25°C	-	1.7	2.8	mA
			-55°C	-	2	3.3	mA
			+125°C	-	1.5	2.5	mA
Device Dissipation	P_D		+25°C	-	50	85	mW
			-55°C	-	60	100	mW
			+125°C	-	45	75	mW

NOTES:

1. Values Apply for Each Section of the Dual Amplifiers
2. If supply voltage is less than ±15V, the Absolute Maximum Input Voltage is equal to the Supply Voltage
3. Voltage values apply for each of the dual operational amplifiers
4. All types in any package style can be operated over the temperature range of -55°C to +125°C, although the published limits for certain electrical specification apply only over the temperature range of 0°C to +70°C

Schematic Diagram

CA741C, CA741 AND FOR EACH AMPLIFIER OF THE CA1458 AND CA1558



* See Functional Diagram for Terminal Numbers of Respective Type Numbers.

NOTE: All Resistance Values are in Ω

Typical Performance Curves

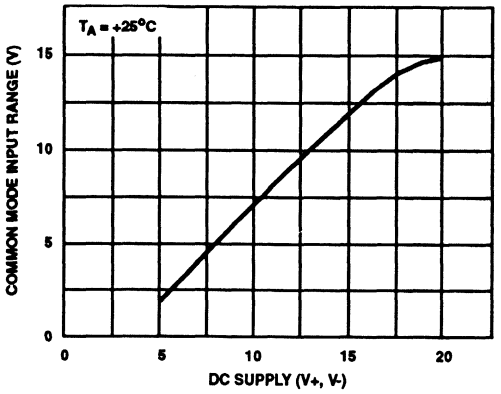


FIGURE 1. COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE FOR ALL TYPES

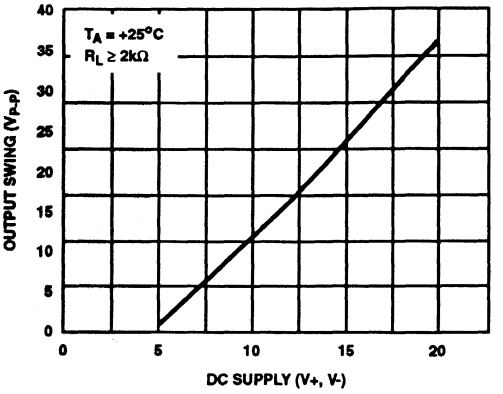


FIGURE 2. OUTPUT VOLTAGE vs SUPPLY VOLTAGE FOR ALL TYPES

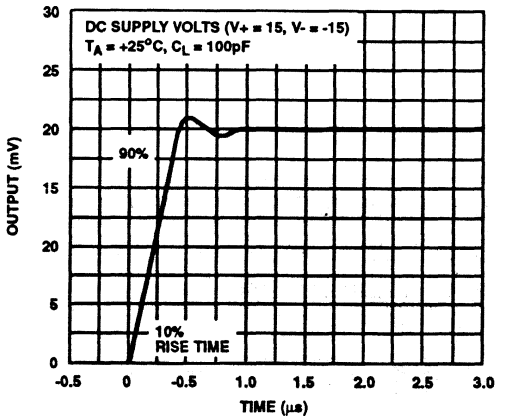


FIGURE 3. OUTPUT VOLTAGE vs TRANSIENT RESPONSE TIME FOR CA741C AND CA741

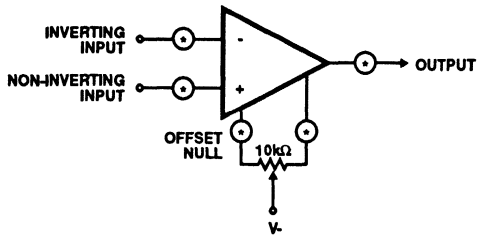


FIGURE 4. OFFSET VOLTAGE NULL CIRCUIT FOR CA741C AND CA741

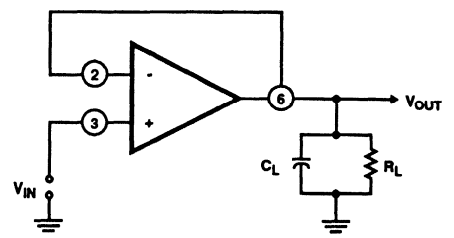
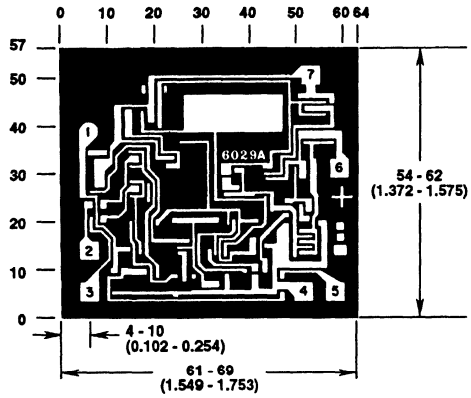


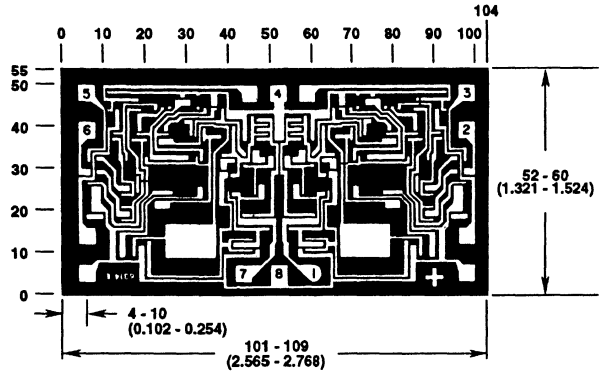
FIGURE 5. TRANSIENT RESPONSE TEST CIRCUIT FOR ALL TYPES

Metallization Mask Layout

CA741CH



CA1458H



NOTE: Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

HARRIS SEMICONDUCTOR

CA3020

Multipurpose Wide-Band Power Amps Military, Industrial and Commercial Equipment at Frequency Up to 8MHz

March 1993

Features

- High Power Output Class B Amplifier
  - CA3020 ..... 0.5W Typ. at V_{CC} = +9V
  - CA3020A ..... 1.0W Typ. at V_{CC} +12V
- Wide Frequency Range ... Up to 8MHz With Resistive Loads
- High Power Gain ..... 75dB Typ.
- Single Power Supply For Class B Operation With Transformer
  - CA3020 ..... 3V to 9V
  - CA3020A ..... 3V to 12V
- Built-In Temperature-Tracking Voltage Regulator Provides Stable Operation Over -55°C to +125°C Temperature Range

Applications

- AF Power Amplifiers For Portable and Fixed Sound and Communications Systems
- Servo-Control Amplifiers
- Wide-Band Linear Mixers
- Video Power Amplifiers
- Transmission-Line Driver Amplifiers (Balanced and Unbalanced)
- Fan-In and Fan-Out Amplifiers For Computer Logic Circuits
- Lamp-Control Amplifiers
- Motor-Control Amplifiers
- Power Multivibrators
- Power Switches
- Companion Application Note, AN-5766, "Application of CA3020 and CA3020A Integrated Circuit Multipurpose Wide-Band Power Amplifiers"

Description

The CA3020 and CA3020A are integrated-circuit, multistage, multipurpose, wide-band power amplifiers on a single monolithic silicon chip. They employ a highly versatile and stable direct coupled circuit configuration featuring wide frequency range, high voltage and power gain, and high power output. These features plus inherent stability over a wide temperature range make the CA3020 and CA3020A extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

The CA3020 and CA3020A are particularly suited for service as class B power amplifiers. The CA3020A can provide a maximum power output of 1W from a 12VDC supply with a typical power gain of 75dB. The CA3020 provides 0.5W power output from a 9V supply with the same power gain.

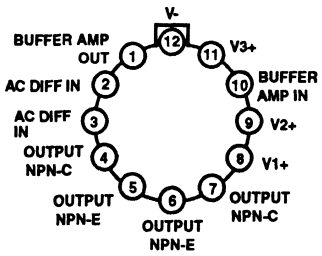
These types are supplied in hermetically sealed TO-5 style 12 lead packages.

Ordering Information

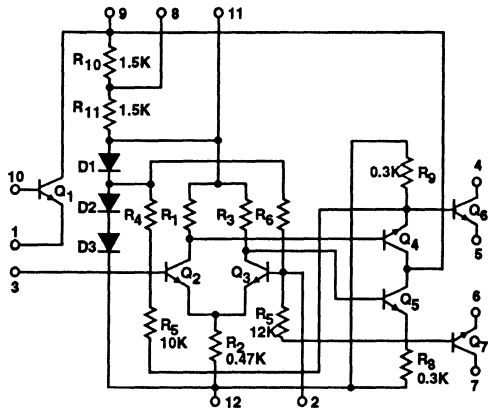
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3020	-55°C to +125°C	12 Pin Can
CA3020A	-55°C to +125°C	12 Pin Can

Pinout

CA3020, CA3020A
(CAN)
TOP VIEW



Schematic Diagram



The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as 30%.

Harris reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 339.2

Absolute Maximum Ratings

Power Dissipation
- Without Heat Sink
  - At T_A = +25°C 1W
  - Above T_A = +25°C ..... Derate Linearly 6.7mW/°C
- With Heat Sink
  - At T_C = +25°C 2W
  - At T_C = +25°C to T_C = +55°C 2W
  - Above T_C = +55°C ..... Derate Linearly 16.7 mW/°C

Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Storage Operating Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Maximum Voltage Ratings T_A = +25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical Terminal 1 with respect to Terminal 12 is 0V to +10V.

TERM NO.	1	2	3	4	5	6	7	8	9	10	11	12
1		Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 5 0 -10/-12	+3 Note 1	Note 4	+10 0
2			Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	+2 -2
3				Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	+2 -2
4					Note 5 +18/+25 0	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 5 +18/+25 0
5						Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	+3 Note 2
6							Note 5 0 -18/-25	Note 4	Note 4	Note 4	Note 4	+3 Note 2
7								Note 4	Note 4	Note 4	Note 4	Note 5 +18/+25 0
8									Note 3	Note 4	Note 4	Note 3 0
9										+10 0	Note 1 0	+10/+12 0
10											Note 4	+10 0
11												Note 4
12												Ref. Sub- strate

Maximum Current Ratings

TERM NO.	I_{IN} mA	I_{OUT} mA
1	-	20
2	-	-
3	-	-
4	300	-
5	-	300
6	-	300
7	300	-
8	-	-
9	20	-
10	1	-
11	20	-
12	-	-

NOTES:
1. This voltage is established by the maximum current rating.
2. The emitters of Q6 and Q7 may be returned to a negative voltage supply through emitter resistors. Current into terminal No. 9 should not be exceeded and the total device dissipation should not be exceeded.
3. Terminal No. 8 may be connected to terminals No. 9, 11, or 12.
4. Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.
5. Higher value is for CA3020A.

Specifications CA3020, CA3020A

Electrical Specifications T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS: CIRCUIT & PROCEDURE FIGURE	TEST CONDITIONS: DC SUPPLY VOLTAGE V_{CC1}	TEST CONDITIONS: DC SUPPLY VOLTAGE V_{CC2}	LIMITS CA3020 MIN	LIMITS CA3020 TYP	LIMITS CA3020 MAX	LIMITS CA3020A MIN	LIMITS CA3020A TYP	LIMITS CA3020A MAX	UNITS
Collector-to-Emitter Breakdown Voltage, Q_6 and Q_7 at 10mA	$V_{(BR)CER}$	1 (Note 1)	-	-	18	-	-	25	-	-	V
Collector-to-Emitter Breakdown Voltage, Q_1 at 0.1mA	$V_{(BR)CEO}$	-	-	-	10	-	-	10	-	-	V
Idle Currents, Q_6 and Q_7	I_4 IDLE I_7 IDLE	7	9.0	2.0	-	5.5	-	-	5.5	-	mA
Peak Output Currents, Q_6 and Q_7	I_4PK I_7PK	7	9.0	2.0	140	-	-	180	-	-	mA
Cutoff Currents, Q_6 and Q_7	I_4 CUTOFF I_7 CUTOFF	7	9.0	2.0	-	-	1.0	-	-	1.0	mA
Differential Amplifier Current Drain	I_{CC1}	7	9.0	9.0	6.3	9.4	12.5	6.3	9.4	12.5	mA
Total Current Drain	I_{CC1} + I_{CC2}	7	9.0	9.0	8.0	21.5	35.0	14.0	21.5	30.0	mA
Differential Amplifier Input Terminal Voltages	V_2 V_3	7	9.0	2.0	-	1.11	-	-	1.11	-	V
Regulator Terminal Voltage	V_{11}	7	9.0	2.0	-	2.35	-	-	2.35	-	V
Q, Cutoff (Leakage) Currents: Collector-to-Emitter	I_{CEO}	-	10.0	-	-	-	100	-	-	100	µA
Emitter-to-Base	I_{EBO}		3.0	-	-	-	0.1	-	-	0.1	µA
Collector-to-Base	I_{CBO}		3.0	-	-	-	0.1	-	-	0.1	µA
Forward Current Transfer Ratio, Q_1 at 3mA	h_{FE1}	-	6.0	-	30	75	-	30	75	-	
Bandwidth at -3dB Point	BW	8	6.0	6.0	-	8	-	-	8	-	MHz
Maximum Power Output	$P_{O(MAX)}$	9	6.0	6.0	200	300 (Note 1)	-	200	300 (Note 1)	-	mW
			9.0	9.0	400	550 (Note 1)	-	400	550 (Note 1)	-	mW
			9.0	12.0	-	-	-	800	1000 (Note 2)	-	mW
Sensitivity for P_{OUT} = 400mW	e_{IN}	9	9.0	9.0	-	35 (Note 1)	55	-	-	-	mV
Sensitivity for P_{OUT} = 800mW	e_{IN}	9	9.0	12.0	-	-	-	-	50 (Note 2)	100	mV
Input Resistance - Terminal 3 to Ground	R_{IN3}	10	6.0	6.0	-	1000	-	-	1000	-	Ω
Junction-to-Case Thermal to Resistance	θ_{JC}	-	-	-	-	-	60	-	-	60	°C/W

NOTES:

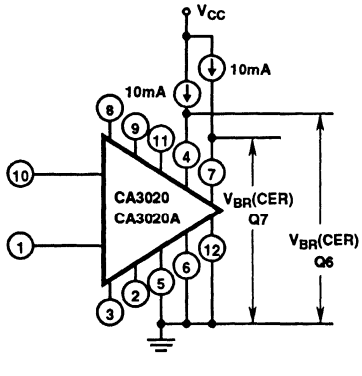
1. R_{CC} = 130Ω
2. R_{CC} = 200Ω

Typical Performance Data (Note 1) A heat sink is recommended for high ambient temperature operation.

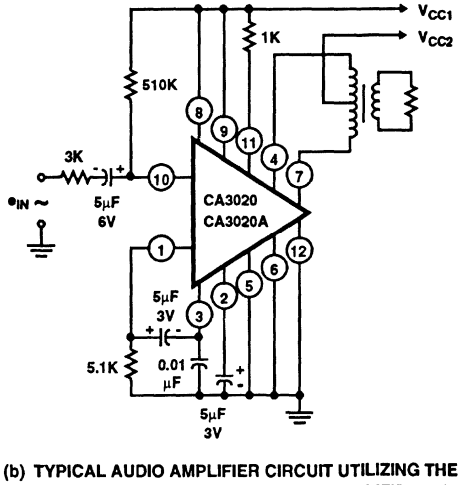
PARAMETERS		SYMBOL	CA3020	CA3020A	UNITS
Power Supply Voltage		V_{CC1}	9.0	9.0	V
		V_{CC2}	9.0	12.0	V
Zero Signal Current	Differential Amplifier	I_{CC1}	15	15	mA
	Output Amplifier	I_{CC2}	24	24	mA
Maximum Signal Current	Differential Amplifier	I_{CC1}	16	16.6	mA
	Output Amplifier	I_{CC2}	125	140	mA
Maximum Power Output at THD = 10%		PO	550	1000	mW
Sensitivity		e_{IN}	35	45	mV
Power Gain		G_P	75	75	dB
Input Resistance		R_{IN}	55	55	kΩ
Efficiency		η	45	55	%
Signal-to-Noise Ratio		S/N	70	66	dB
THD at 150mW Level			3.1	3.3	%
Test Signal Frequency from 600Ω Generator			1000	1000	Hz
Equivalent Collector-to-Collector Load Resistance		R_{CC}	130	200	Ω

NOTE:

1. Refer to Figures 7 through 11 for measurement and symbol information.

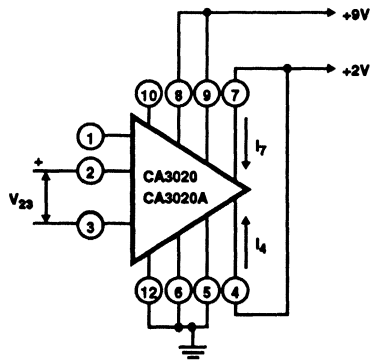


(a) COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE (Q6 AND Q7) CIRCUIT

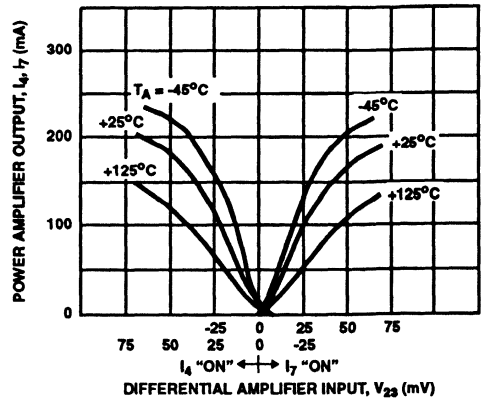


(b) TYPICAL AUDIO AMPLIFIER CIRCUIT UTILIZING THE CA3020 OR CA3020A AS AN AUDIO PREAMPLIFIER AND CLASS B POWER AMPLIFIER

FIGURE 1.

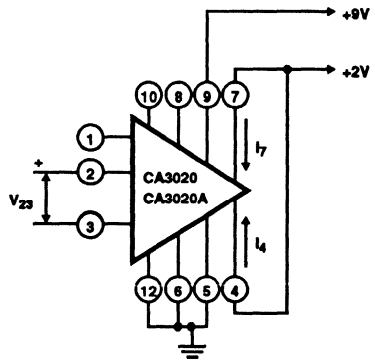


(a) TEST SETUP

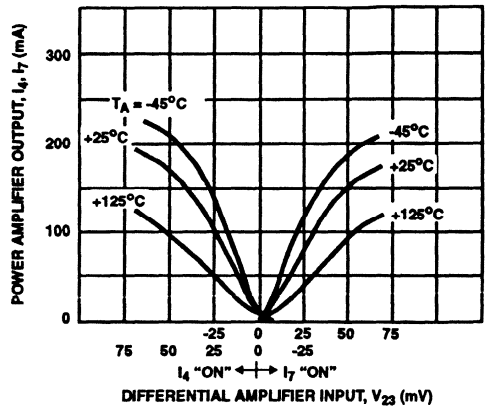


(b) CHARACTERISTICS WITH R_{10} SHORTED OUT

FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

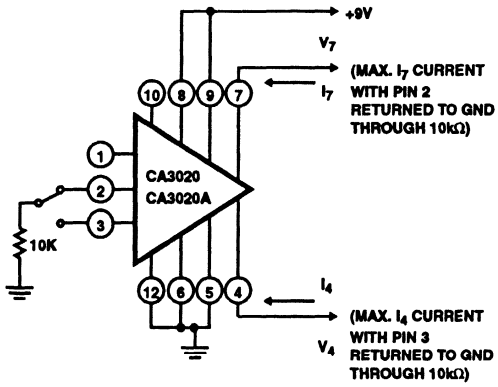


(a) TEST SETUP

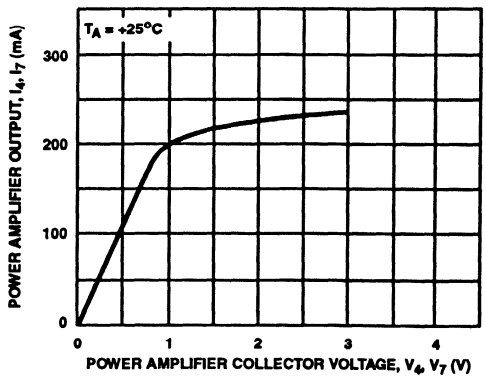


(b) CHARACTERISTIC WITH R_{10} IN CIRCUIT

FIGURE 3. TYPICAL TRANSFER CHARACTERISTICS

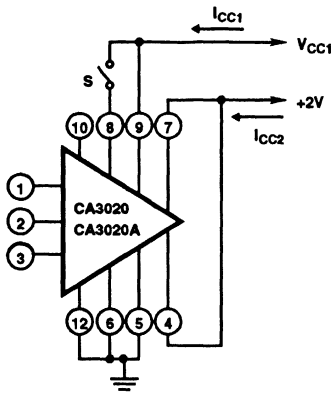


(a) TEST SETUP

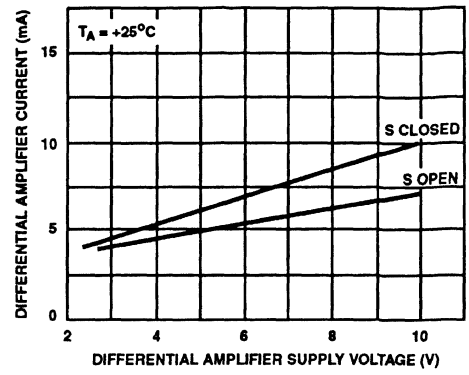


(b) CHARACTERISTIC

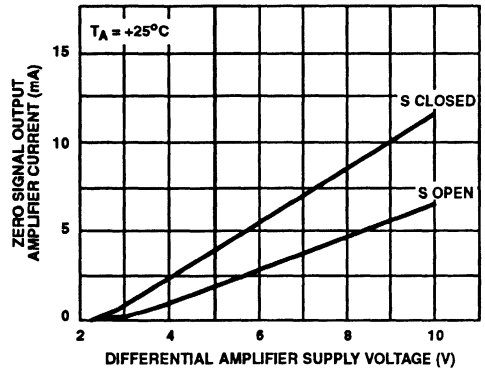
FIGURE 4. "MINIMUM DRIVE" TYPICAL CURRENT-VOLTAGE SATURATION CURVE



(a) TEST SETUP

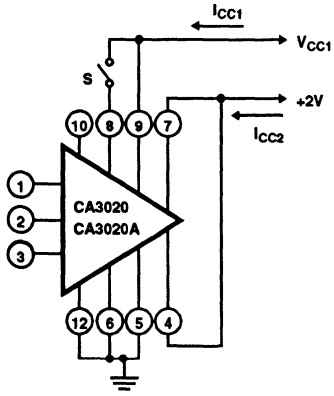


(b) DIFFERENTIAL AMPLIFIER CHARACTERISTICS

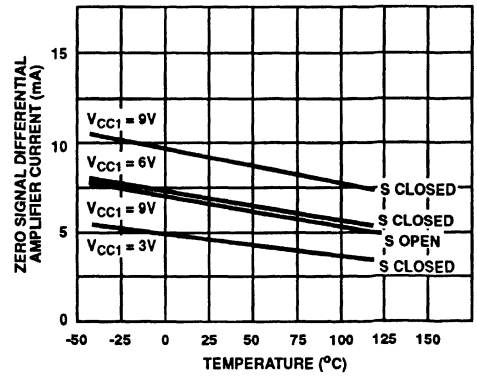


(c) OUTPUT AMPLIFIER CHARACTERISTICS

FIGURE 5. ZERO SIGNAL AMPLIFIER CURRENT vs DIFFERENTIAL AMPLIFIER SUPPLY VOLTAGE

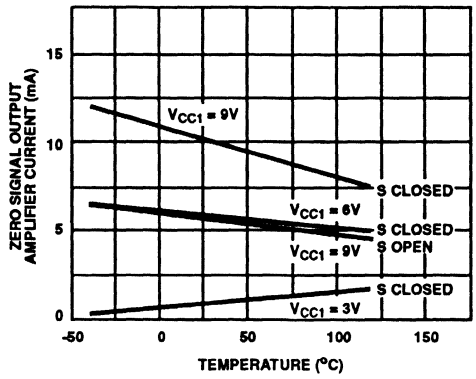


(a) TEST SETUP



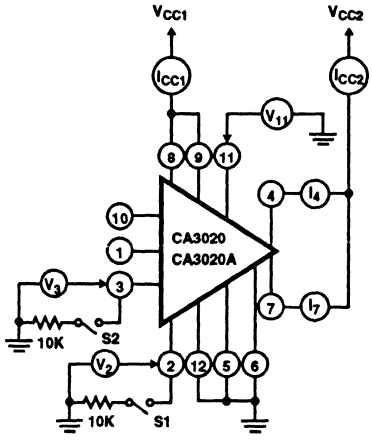
(b) DIFFERENTIAL AMPLIFIER CHARACTERISTICS

FIGURE 6. ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE



(c) OUTPUT AMPLIFIER CHARACTERISTICS

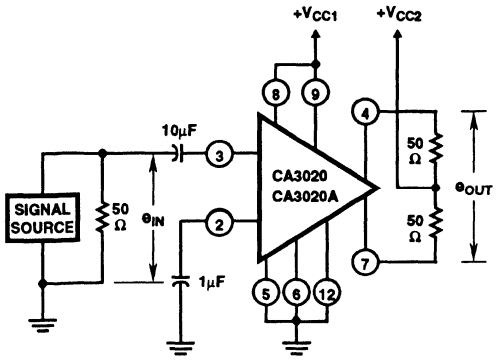
FIGURE 6. ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE (Continued)



CURRENTS OR VOLTAGES	S1	S2
I_4 -IDLE	OPEN	OPEN
I_7 -IDLE	OPEN	OPEN
I_4 -PEAK	OPEN	CLOSE
I_7 -PEAK	CLOSE	OPEN
I_4 -CUTOFF	CLOSE	OPEN
I_7 -CUTOFF	OPEN	CLOSE

CURRENTS OR VOLTAGES	S1	S2
I_{CC1}	OPEN	OPEN
I_{CC2}	OPEN	OPEN
V_2	OPEN	OPEN
V_3	OPEN	OPEN
V_{11}	OPEN	OPEN

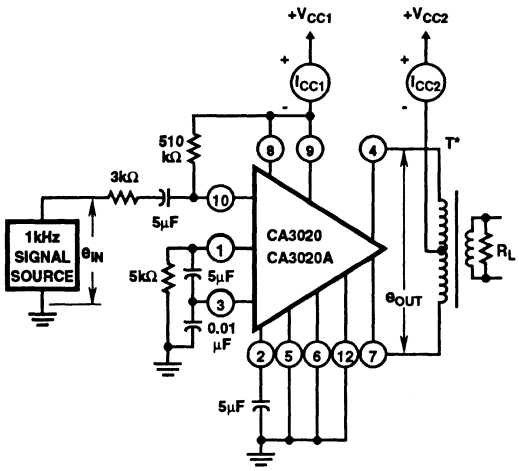
FIGURE 7. STATIC CURRENT AND VOLTAGE TEST CIRCUIT



PROCEDURES:

1. Apply desired value of V_{CC1} and V_{CC2}
2. Apply 1kHz input signal and adjust for e_{IN} = 5mV (rms)
3. Record the resulting value of e_{OUT} in dB (reference value)
4. Vary input-signal frequency, keeping e_{IN} constant at 5mV, and record frequencies above and below 1kHz at which e_{OUT} decreases 3dB below reference value
5. Record bandwidth as frequency range between -3dB points

FIGURE 8. MEASUREMENT OF BANDWIDTH AT -3dB POINTS



*T: PUSH-PULL OUTPUT TRANSFORMER; LOAD RESISTANCE (R_L) SHOULD BE SELECTED TO PROVIDE INDICATED COLLECTOR-TO-COLLECTOR LOAD IMPEDANCE (R_{CC})

PROCEDURES:

Zero-Signal DC Current Drain

1. Apply desired value of V_{CC1} and V_{CC2} and reduce e_{IN} to 0V
2. Record resulting values of I_{CC1} and I_{CC2} in mA as Zero-Signal DC Current Drain

Maximum-Signal DC Current Drain, Maximum Power Output, Circuit Efficiency, Sensitivity, and Transducer Power Gain

1. Apply desired value of V_{CC1} and V_{CC2} and adjust e_{IN} to the value at which the Total Harmonic Distortion in the output of the amplifier = 10%
2. Record resulting value of I_{CC1} and I_{CC2} in mA as Maximum Signal DC Current Drain
3. Determine resulting amplifier power output in watts and record as Maximum Power Output (P_{OUT})
4. Calculate Circuit Efficiency (η) in % as follows:

$$\eta = 100\frac{P_{OUT}}{V_{CC1}I_{CC1} + V_{CC2}I_{CC2}}$$

where P_{OUT} is in watts, V_{CC1} and V_{CC2} are in volts, and I_{CC1} and I_{CC2} are in amperes.

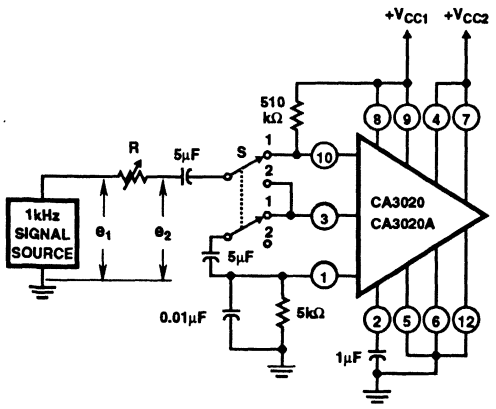
5. Record value of e_{IN} in mV (rms) required in Step 1 as Sensitivity (e_{IN})
6. Calculate Transducer Power Gain (G_p) in dB as follows:

$$G_p = 10\log_{10}\frac{P_{OUT}}{P_{IN}}$$

$$\text{where } P_{IN}\,(\text{in mW}) = \frac{e_{IN}^2}{3000 + R_{IN(10)}**}$$

**See Figure 10 for definition of $R_{IN(10)}$

FIGURE 9. MEASUREMENTS OF ZERO-SIGNAL DC CURRENT DRAIN, MAXIMUM-SIGNAL DC CURRENT DRAIN, MAXIMUM POWER OUTPUT, CIRCUIT EFFICIENCY, SENSITIVITY, AND TRANSDUCER POWER GAIN



PROCEDURES:

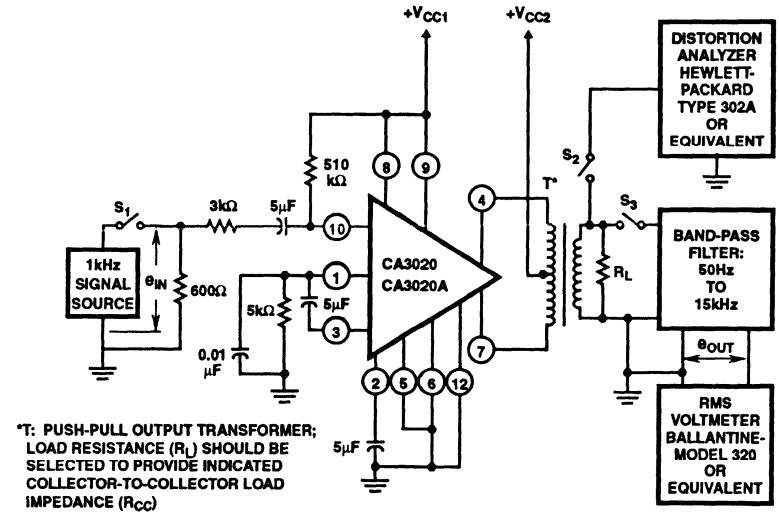
Input Resistance Terminal 10 to Ground (R_{IN10})

1. Apply desired value of V_{CC1} and V_{CC2} and set S in Position 1
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as R_{IN10}

Input Resistance Terminal 3 to Ground (R_{IN3})

1. Apply desired value of V_{CC1} and V_{CC2} set S in Position 2
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as R_{IN3}

FIGURE 10. MEASUREMENT OF INPUT RESISTANCE



*T: PUSH-PULL OUTPUT TRANSFORMER; LOAD RESISTANCE (R_L) SHOULD BE SELECTED TO PROVIDE INDICATED COLLECTOR-TO-COLLECTOR LOAD IMPEDANCE (R_{CC})

PROCEDURES:

Signal-to-Noise Ratio

1. Close S_1 and S_3; open S_2
2. Apply desired values of V_{CC1} and V_{CC2}
3. Adjust e_{IN} for an amplifier output of 150mW and resulting value of E_{OUT} in dB as e_{OUT1} (reference value)
4. Open S_1 and record resulting value of e_{OUT} in dB as e_{OUT2}
5. Signal-to-Noise Ratio $(S/N) = 20\log_{10}\frac{e_{OUT1}}{e_{OUT2}}$

Total Harmonic Distortion

1. Close S1 and S2; open S3
2. Apply desired values of V_{CC1} and V_{CC2}
3. Adjust e_{IN} for desired level amplifier output power
4. Record Total Harmonic Distortion (THD) in %

FIGURE 11. MEASUREMENT OF SIGNAL-TO-NOISE RATIO AND TOTAL HARMONIC DISTORTION

HARRIS SEMICONDUCTOR

CA3060

Operational Transconductance Amplifier Arrays

March 1993

Features

- Low Power Consumption as Low as 100mW Per Amplifier
- Independent Biasing for Each Amplifier
- High Forward Transconductance
- Programmable Range of Input Characteristics
- Low Input Bias and Input Offset Current
- High Input and Output Impedance
- No Effect on Device Under Output Short-Circuit Conditions
- Zener Diode Bias Regulator

Applications

- For Low Power Conventional Operational Amplifier Applications
- Active Filters
- Comparators
- Gyrators
- Mixers
- Modulators
- Multiplexers
- Multipliers
- Strobing and Gating Functions
- Sample and Hold Functions

Description

The CA3060 monolithic integrated circuit consists of an array of three independent Operational Transconductance Amplifiers.* This type of amplifier has the generic characteristics of an operational voltage amplifier with the exception that the forward gain characteristic is best described by transconductance rather than voltage gain (open-loop voltage gain is the product of the transconductance and the load resistance, g_mR_L). When operated into a suitable load resistor and with provisions for feedback, these amplifiers are well suited for a wide variety of operational-amplifier and related applications. In addition, the extremely high output impedance makes these types particularly well suited for service in active filters.

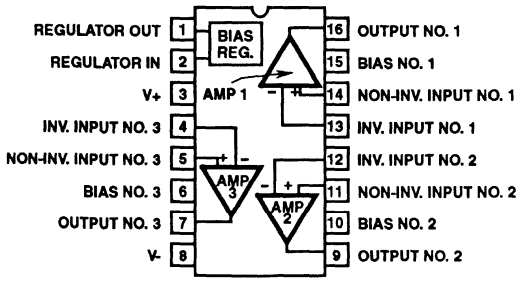
The three amplifiers in the CA3060 are identical push-pull Class A types which can be independently biased to achieve a wide range of characteristics for specific application. The electrical characteristics of each amplifier are a function of the amplifier bias current (I_{ABC}). This feature offers the system designer maximum flexibility with regard to output current capability, power consumption, slew rate, input resistance, input bias current, and input offset current. The linear variation of the parameters with respect to bias and the ability to maintain a constant dc level between input and output of each amplifier also makes the CA3060 suitable for a variety of nonlinear applications such as mixers, multipliers, and modulators.

In addition, the CA3060 incorporates a unique Zener diode regulator system that permits current regulation below supply voltages normally associated with such systems.

* Generic applications of the OTA are described in AN-6668. For improved input operating ranges, refer to CA3080 and CA3280 data bulletins (File Nos. 475 and 1174) and application notes AN-6668 and AN-6818.

Pinout

CA3060
(PDIP)
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3060E	-40°C to +85°C	16 Lead Plastic DIP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **537.2**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals)..... 36V (±18V)
Input Voltage..... V+ to V-
Differential Input Voltage (each amplifier)..... 5V
Input Current (each amplifier) .....±1mA
Amplifier Bias Current (each amplifier).....2mA
Bias Regulator Input Current .....-5mA
Output Short Circuit Duration (Note 3)..... Indefinite
Junction Temperature..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.)..... +300°C

Operating Conditions

Storage Temperature Range.....-65°C to +150°C
Operating Temperature Range .....-40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C, V+ = 15V, V- = -15V

PARAMETERS	SYMBOL	LIMITS AMPLIFIER BIAS CURRENT I_{ABC} = 1µA			I_{ABC} = 10µA			I_{ABC} = 100µA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (See Figure 1)	V_{IO}	-	1	-	-	1	-	-	1	5	mV
Input Offset Current (See Figure 2)	I_{IO}	-	3	-	-	30	-	-	250	1000	nA
Input Bias Current (See Figures 3, 4)	I_{IB}	-	33	-	-	300	-	-	2500	5000	nA
Peak Output Current (See Figures 5, 6)	I_{OM}	-	2.3	-	-	26	-	150	240	-	µA
Peak Output Voltage (See Figure 7)											
Positive	V_{OM+}	-	13.6	-	-	13.6	-	12	13.6	-	V
Negative	V_{OM-}	-	14.7	-	-	14.7	-	12	14.7	-	V
Amplifier Supply Current (each amplifier) (See Figures 8, 9)	I_A	-	8.5	-	-	85	-	-	850	1200	µA
Power Consumption (each amplifier)	P	-	0.26	-	-	2.6	-	-	26	36	mW
Input Offset Voltage Sensitivity (Note 1)											
Positive	$\Delta V_{IO}/\Delta V+$	-	1.5	-	-	2	-	-	2	150	µV/V
Negative	$\Delta V_{IO}/\Delta V-$	-	20	-	-	20	-	-	30	150	µV/V
Amplifier Bias Voltage (Note 2, See Figure 10)	V_{ABC}	-	0.54	-	-	0.60	-	-	0.66	-	V
DYNAMIC CHARACTERISTICS (At 1kHz, Unless Specified Otherwise)											
Forward Transconductance (large signal) (See Figures 11, 12)	g21	-	1.55	-	-	18	-	30	102	-	mmho
Common Mode Rejection Ratio	CMRR	-	110	-	-	110	-	70	90	-	dB
Common Mode Input Voltage Range	V_{ICR}	+12 to -12	+13 to -14	-	+12 to -12	+13 to -14	-	+12 to -12	+13 to -14	-	V
DYNAMIC CHARACTERISTICS (At 1kHz, Unless Specified Otherwise) Continued											
Slew Rate (test circuit) (See Figure 17)	SR	-	0.1	-	-	1	-	-	8	-	V/µs
Open Loop (g_{21}) Bandwidth (See Figure 13)	BW_{OL}	-	20	-	-	45	-	-	110	-	kHz

Electrical Specifications T_A = +25°C, V+ = 15V, V- = -15V **(Continued)**

PARAMETERS	SYMBOL	LIMITS AMPLIFIER BIAS CURRENT I_{ABC} = 1μA MIN	TYP	MAX	I_{ABC} = 10μA MIN	TYP	MAX	I_{ABC} = 100μA MIN	TYP	MAX	UNITS
Input Impedance Components											
Resistance (See Figure 14)	R_I	-	1600	-	-	170	-	10	20	-	kΩ
Capacitance at 1MHz	C_I	-	2.7	-	-	2.7	-	-	2.7	-	pF
Output Impedance Components											
Resistance (See Figure 15)	R_O	-	200	-	-	20	-	-	2	-	MΩ
Capacitance at 1MHz	C_O	-	4.5	-	-	4.5	-	-	4.5	-	pF
ZENER BIAS REGULATOR CHARACTERISTICS (At T_A = +25°C, I_2 = 0.1mA)											
Voltage (See Figure 16)	V_Z	Temperature Coefficient = 3mV/°C			6.2	6.7	7.9				V
Impedance	Z_Z				-	200	300				Ω

NOTES:

1. Conditions for Input Offset Voltage Sensitivity
   a. Bias current derived from the regulator with an appropriate resistor connected from Terminal 1 to the bias terminal on the amplifier under test V+ is reduced to +13V for V+ sensitivity and V- is reduced to -13V for V- sensitivity.

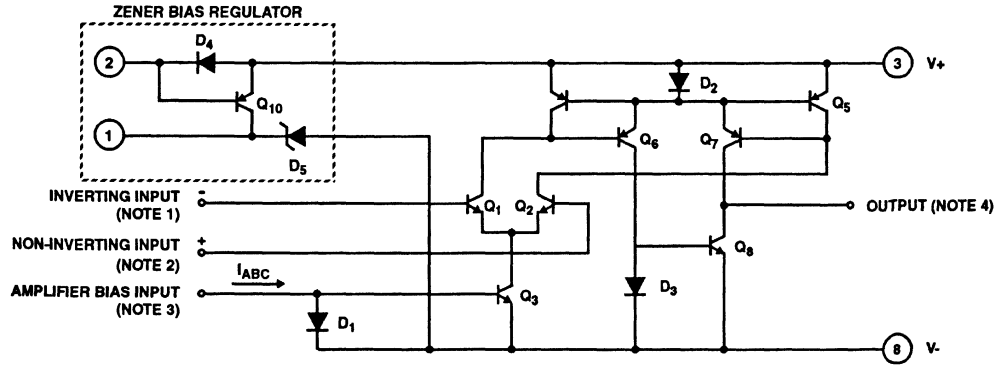
   b. V+ Sensitivity in $\mu V/V = \frac{V_{Offset} - V_{Offset}\ \text{for +13V and -15V Supplies}}{1V}$

   V- Sensitivity in $\mu V/V = \frac{V_{Offset} - V_{Offset}\ \text{for -13V and +15V Supplies}}{1V}$

2. Temperature Coefficient; -2.2mV/°C (at V_{ABC} = 0.54, I_{ABC} = 1μA); -2.1mV/°C (at V_{ABC} = 0.060V, I_{ABC} = 10μA); -1.9mV/°C (at V_{ABC} = 0.66V, I_{ABC} = 100μA)
3. Short circuit may be applied to ground or to either supply

Schematic Diagram

BIAS REGULATOR AND ONE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER



NOTES:

1. Inverting Input of Amplifiers 1, 2 and 3 is on Terminals 13, 12 and 4, respectively.
2. Non-inverting Input of Amplifiers 1, 2 and 3 is Terminals 14, 11 and 5, respectively.
3. Amplifier Bias Current of Amplifiers 1, 2 and 3 is on Terminals 15, 10 and 6, respectively.
4. Output of Amplifiers 1, 2 and 3 is on Terminals 16, 9 and 7, respectively.

Typical Performance Curves

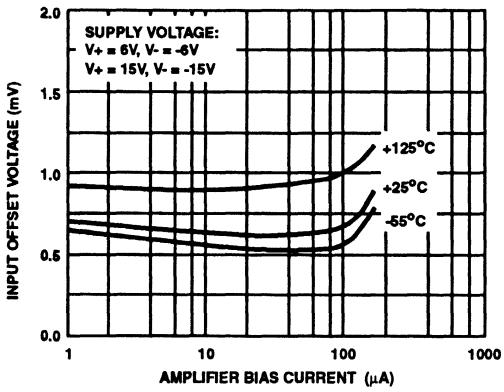


FIGURE 1. INPUT OFFSET VOLTAGE vs AMPLIFIER BIAS CURRENT

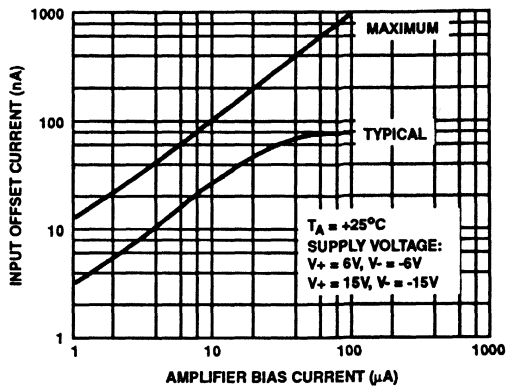


FIGURE 2. INPUT OFFSET CURRENT vs AMPLIFIER BIAS CURRENT

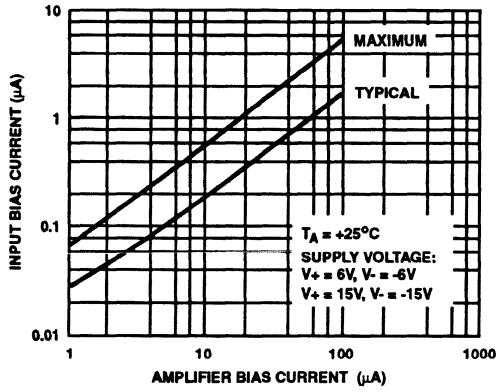


FIGURE 3. INPUT BIAS CURRENT vs AMPLIFIER BIAS CURRENT

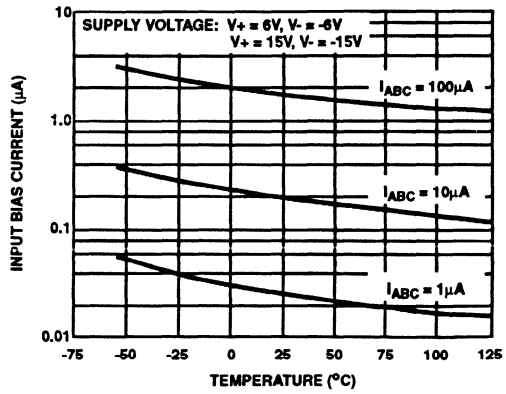


FIGURE 4. INPUT BIAS CURRENT vs AMBIENT TEMPERATURE

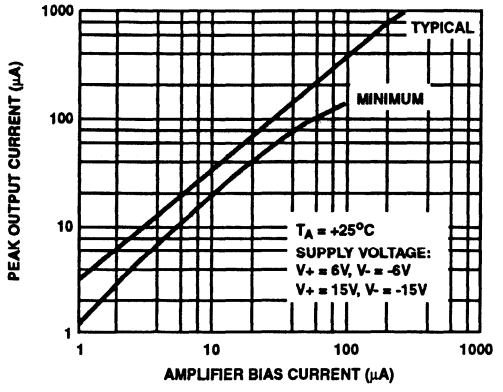


FIGURE 5. PEAK OUTPUT CURRENT vs AMPLIFIER BIAS CURRENT

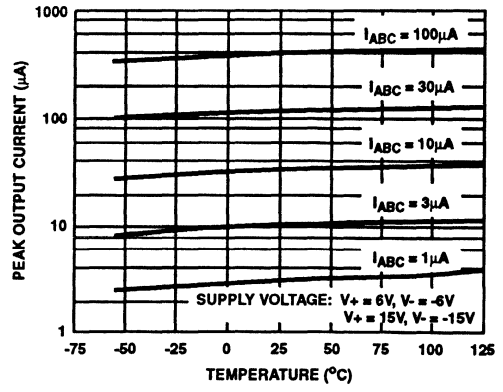


FIGURE 6. PEAK OUTPUT CURRENT vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

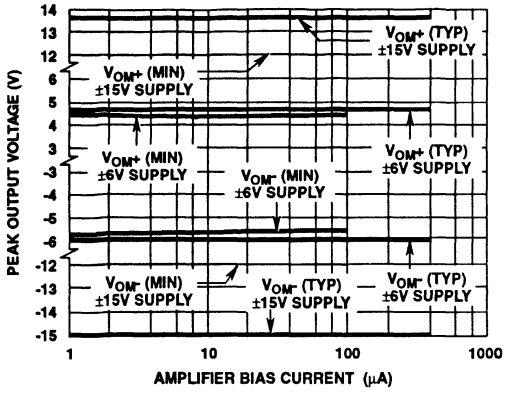


FIGURE 7. PEAK OUTPUT VOLTAGE vs AMPLIFIER BIAS CURRENT

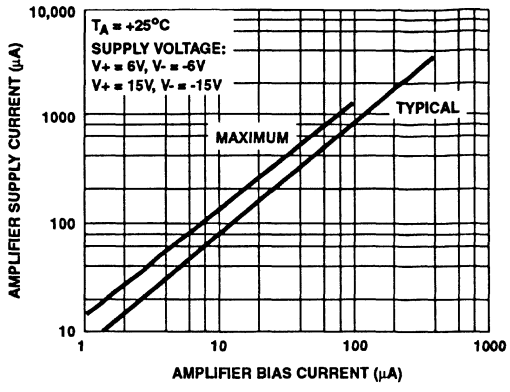


FIGURE 8. AMPLIFIER SUPPLY CURRENT (EACH AMPLIFIER) vs AMPLIFIER BIAS CURRENT

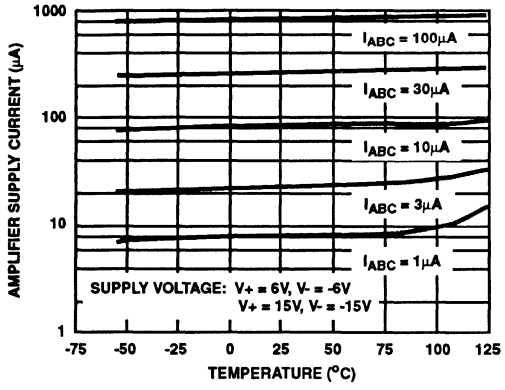


FIGURE 9. AMPLIFIER SUPPLY CURRENT (EACH AMPLIFIER) vs AMBIENT TEMPERATURE

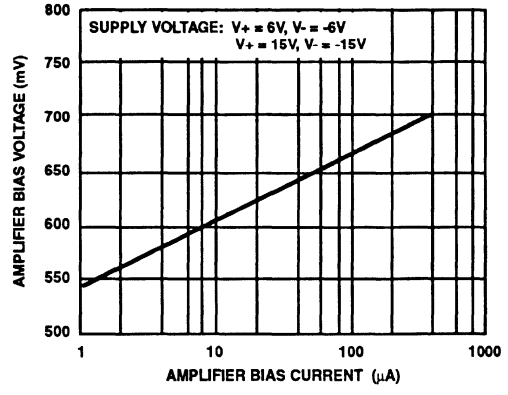


FIGURE 10. AMPLIFIER BIAS VOLTAGE vs AMPLIFIER BIAS CURRENT

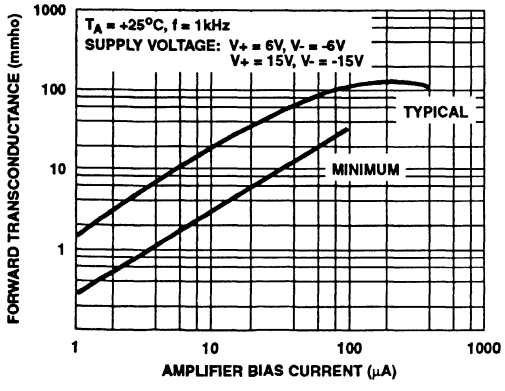


FIGURE 11. FORWARD TRANSCONDUCTANCE vs AMPLIFIER BIAS CURRENT

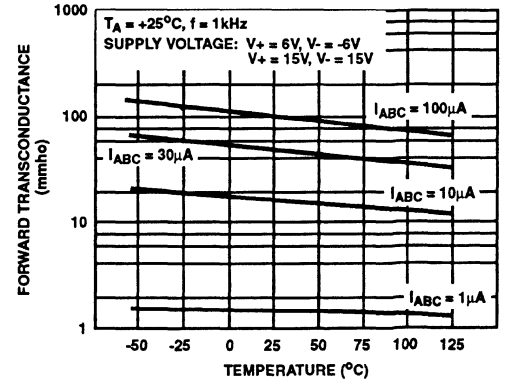


FIGURE 12. FORWARD TRANSCONDUCTANCE vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

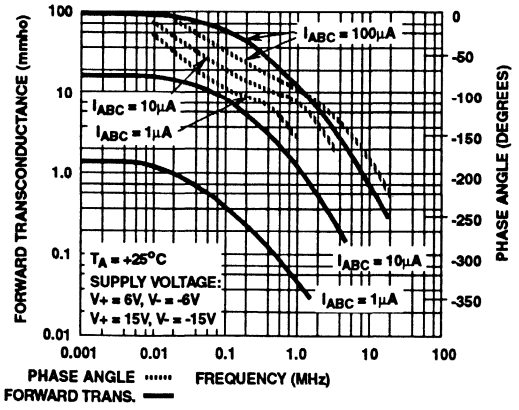


FIGURE 13. FORWARD TRANSCONDUCTANCE vs FREQUENCY

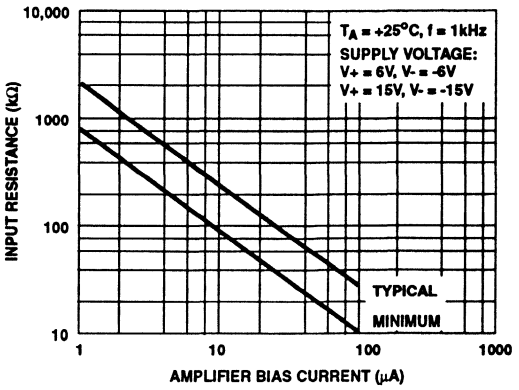


FIGURE 14. INPUT RESISTANCE vs AMPLIFIER BIAS CURRENT

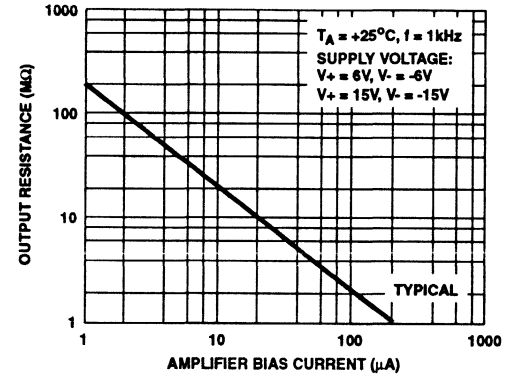


FIGURE 15. OUTPUT RESISTANCE vs AMPLIFIER BIAS CURRENT

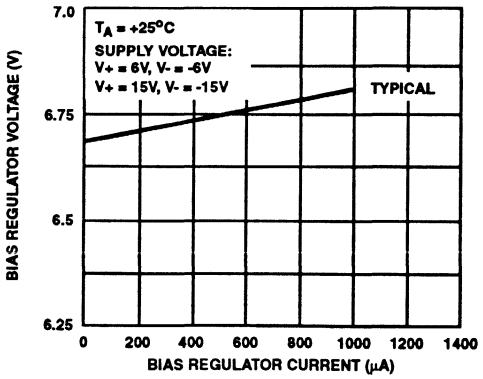
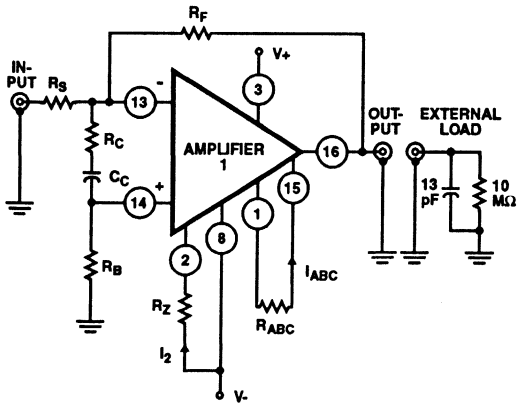


FIGURE 16. BIAS REGULATOR VOLTAGE vs BIAS REGULATOR CURRENT



V_Z is measured between Terminal 1 and 8

V_{ABC} is measured between Terminals 15 and 8

$$R_Z = \frac{[(V+) - (V-) - 0.7]}{I_2}, \quad R_{ABC} = \frac{V_Z - V_{ABC}}{I_{ABC}}$$

Supply Voltage: For both ±6V and ±15V

TYPICAL SLEW RATE TEST CIRCUIT PARAMETERS

I_{ABC}	SLEW RATE	I_2	R_{ABC}	R_S	R_F	R_B	R_C	C_C
μA	V/μs	μA	Ω	Ω	Ω	Ω	Ω	μF
100	8	200	62k	100k	100k	51k	100	0.02
10	1	200	620k	1M	1M	510k	1k	0.005
1	0.1	2	6.2M	10M	10M	5.1M	∞	0

FIGURE 17. SLEW RATE TEST CIRCUIT FOR AMPLIFIER 1 OF CA3060

Operating Considerations

The CA3060 consists of three operational amplifiers similar in form and application to conventional operational amplifiers but sufficiently different from the standard operational amplifier (op amp) to justify some explanation of their characteristics. The amplifiers incorporated in the CA3060 are best described by the term Operational Transconductance Amplifier (OTA). The characteristics of an ideal OTA are similar to those of an ideal op amp except that the OTA has an extremely high output impedance. Because of this inherent characteristics the output signal is best defined in terms of current which is proportional to the difference between the voltages of the two input terminals. Thus, the transfer characteristics is best described in terms of transconductance rather than voltage gain. Other than the difference given above, the characteristics tabulated are similar to those of any typical op amp.

The OTA circuitry incorporated in the CA3060 (Figure 18) provides the equipment designer with a wider variety of circuit arrangements than does the standard op amp; because as the curves indicate, the user may select the optimum circuit conditions for a specific application simply by varying the bias conditions of each amplifier. If low power consumption, low bias, and low offset current, or high input impedance are primary design requirements, then low current operating conditions may be selected. On the other hand, if operation into a moderate load impedance is the primary consideration, then higher levels of bias may be used.

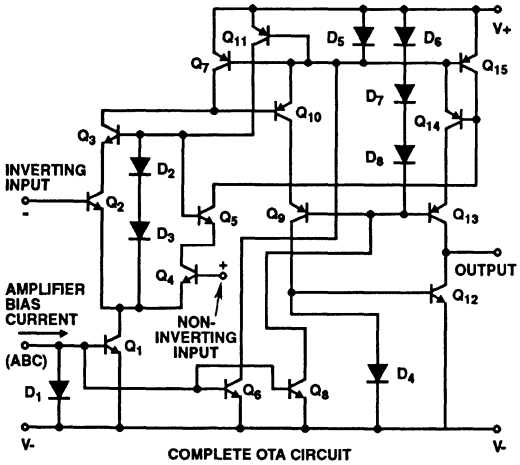


FIGURE 18. COMPLETE SCHEMATIC DIAGRAM SHOWING BIAS REGULATOR AND ONE OF THE THREE OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS

Bias Consideration for Op Amp Applications

The operational transconductance amplifiers allow the circuit designer to select and control the operating conditions of the circuit merely by the adjustment of the amplifier bias current I_{ABC}. This enables the designer to have complete control over transconductance, peak output current and total power consumption independent of supply voltage.

In addition, the high output impedance makes these amplifiers ideal for applications where current summing is involved.

The design of a typical operation amplifier circuit (Figure 19) would proceed as follows:

Circuit Requirements
Closed Loop Voltage Gain = 10 (20dB)
Offset Voltage Adjustable to Zero
Current Drain as Low as Possible
Supply Voltage = ±6V
Maximum Input Voltage = ±50mV
Input Resistance = 20kΩ
Load Resistance = 20kΩ
Device: CA3060

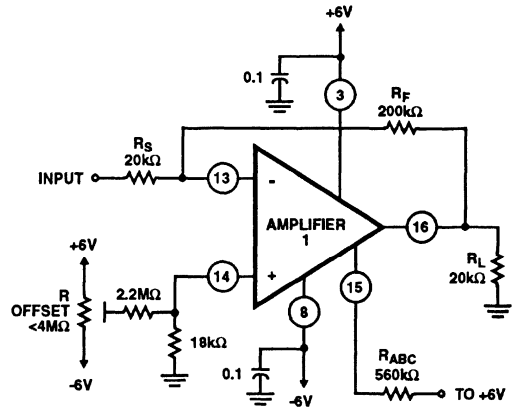


FIGURE 19. 20dB AMPLIFIER USING THE CA3060

Calculation

1. **Required Transconductance g21.** Assume that the open loop gain A_{OL} must be at least ten times the closed loop gain. Therefore, the forward transconductance required is given by:

   $g_{21} = A_{OL}/R_L$
   $= 100/18k\Omega$
   $\cong 5.5mmho$
   (R_L = 20kΩ in parallel with 200kΩ ≅ 18kΩ)

2. **Selection of Suitable Amplifier Bias Current.** The amplifier bias current is selected from the minimum value curve of transconductance (Figure 11) to assure that the amplifier will provide sufficient gain. For the required g_{21} of 5.5mmho an amplifier bias current I_{ABC} of 20μA is suitable.

3. **Determination of Output Swing Capability.** For a loop gain of 10 the output swing is ±0.5V and the peak load current 25μA. However, the amplifier must also supply the necessary current through the feedback resistor and for R_S = 20kΩ than R_F = 200kΩ if A_{OL} = 10. Therefore, the feedback loading = 0.5/200kΩ = 2.5μA.

   The total amplifier current output requirements are, therefore, ±27.5μA. Referring to the data given in Figure 5, we see that for an amplifier bias current of 20μA the amplifier output current is ±40μA. This is obviously adequate and it is not necessary to change the amplifier bias current I_{ABC}.

4. **Calculation of Bias Resistance.** For minimum supply current drain the amplifier bias current I_{ABC} should be fed directly from the supplies and not from the bias regulator. The value of the resistor R_{ABC} may be directly calculated using Ohm's law.

$$R_{ABC} = \frac{V_{SUP} - V_{ABC}}{I_{ABC}}$$

$$R_{ABC} = \frac{12 - 0.63}{20 \times 10^{-6}}$$

$$= 568.5k\Omega \text{ or } \cong 560k\Omega$$

5. **Calculation of Offset Adjustment Circuit.** In order to reduce the loading effect of the offset adjustment circuit on the power supply, the offset control should be arranged to provide the necessary offset current. The source resistance of the non-inverting input is made equal to the source resistance of the inverting input.

$$\text{i.e. } \frac{20 \times 200 \times 10^{6}\Omega}{220 \times 10^{3}} \cong 18k\Omega$$

Because the maximum offset voltage is 5mV and an additional increment due to the offset current (Figure 2) flowing through the source resistance (i.e. 200 x 10^{-9} x 18 x 10^{3} volts), therefore, the Offset Voltage Range = 5mV + 3.6mV = ±8.6mV. The current necessary to provide this offset is

$$\frac{8.6 \times 10^{-3}}{18 \times 10^{3}} \text{ or } 0.48\mu A$$

With a supply voltage of ±6V, this current can be provided by a 10MΩ resistor. However, the stability of such a resistor is often questionable and a more realistic value of 2.2MΩ was used in the final circuit.

Other Considerations

Capacitance Effects

The CA3060 is designed to operate at such low power level that high impedance circuits must be employed. In designing such circuits, particularly feedback amplifiers, stray circuit capacitance must always be considered because of its adverse effect on frequency response and stability. For example a 10kΩ load with a stray capacitance of 15pF has a time constant of 1MHz. Figure 20 illustrates how a 10kΩ 15pF load modifies the frequency characteristic.

Capacitive loading also has an effect on slew rate; because the peak output current is established by the amplifier bias current, I_{ABC} (Figure 5), the maximum slew rate is limited to the maximum rate at which the capacitance can be charged by the I_{OM}. Therefore, SR = dV/dt = I_{OM}/C_L, where C_L is the total load capacitance including strays. This relationship is shown graphically in Figure 21. When measuring slew rate for this data bulletin, care was taken to keep the total capacitive loading to 13pF.

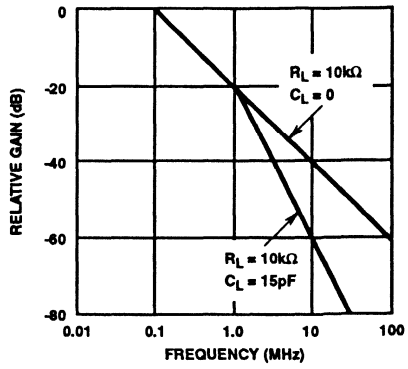
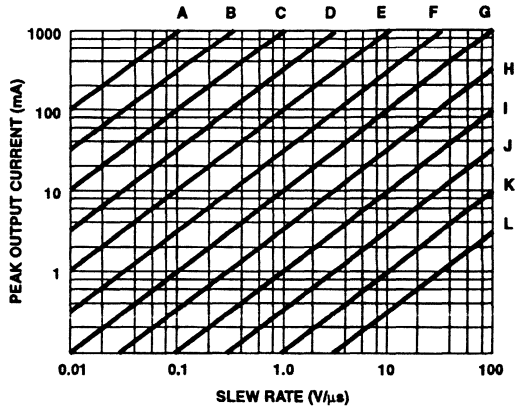


FIGURE 20. EFFECT OF CAPACITIVE LOADING ON FREQUENCY RESPONSE



A. C_L = 10,000pF
B. C_L = 3,000pF
C. C_L = 1000pF
D. C_L = 300pF
E. C_L = 100pF
F. C_L = 30pF
G. C_L = 10pF
H. C_L = 3pF
I. C_L = 1pF
J. C_L = 0.3pF
K. C_L = 0.1pF
L. C_L = 0.03pF

FIGURE 21. EFFECT OF LOAD CAPACITANCE ON SLEW RATE

Phase Compensation

In many applications phase compensation will not be required for the amplifiers of the CA3060. When needed, compensation may easily be accomplished by a simple RC network at the input of the amplifier as shown in Figure 17. The values given in Figure 17 provide stable operation for the critical unity gain condition, assuming that capacitive loading on the output is 13pF or less. Input phase compensation is recommended in order to maintain the highest possible slew rate.

In applications such as integrators, two OTAs may be cascaded to improve current gain. Compensation is best accomplished in this case with a shunt capacitor at the output of the first amplifier. The high gain following compensation assures a high slew rate.

Applications

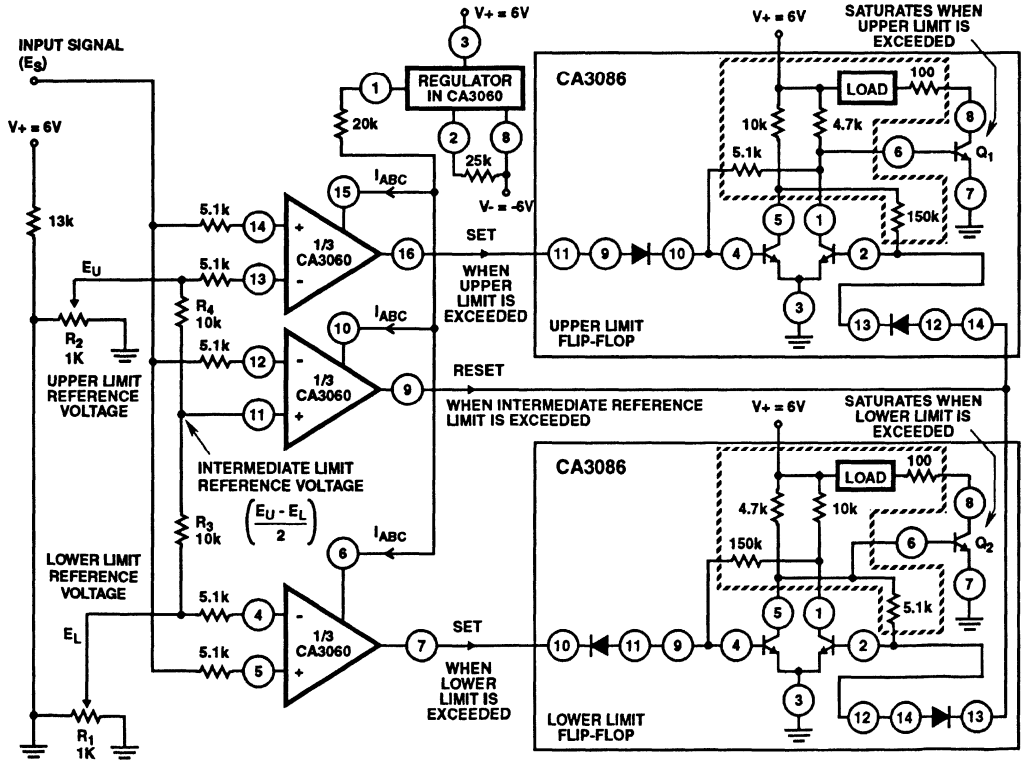
Having determined the operating points of the CA3060 amplifiers, they can now function in the same manner as conventional op amps, and thus, are well suited for most op amp applications, including inverting and non-inverting amplifiers, integrators, differentiators, summing amplifiers etc.

Tri-Level Comparator

Tri-level comparator circuits are an ideal application for the CA3060 since it contains the requisite three amplifiers. A tri-level comparator has three adjustable limits. If either the upper lower limit is exceeded, the appropriate output is activated until the input signal returns to a selected intermediate limit. Tri-level comparators are particularly suited to many industrial control applications.

Circuit Description

Figure 23 shows the block diagram of a tri-level comparator using the CA3060. Two of the three amplifiers are used to compare the input signal with the upper limit and lower limit reference voltages. The third amplifier is used to compare the input signal with a selected value of intermediate limit reference voltage. By appropriate selection of resistance ratios this intermediate limit may be set to any voltage between the upper limit and lower limit values. The output of the upper limit and lower limit comparator sets the corresponding upper or lower limit flip-flop. The activated flip-flop retains its state until the third comparator (intermediate limit) in the CA3060 initiates a reset function, thereby indicating that the signal voltage has returned to the intermediate limit selected. The flip-flops employ two CA3086 transistor array ICs, with circuitry to provide separate "SET" and "POSITIVE OUTPUT" terminals.



NOTES: 1. Items in dashed boxes are external to the CA3086. All resistance values are in Ω.

2. $E_S > E_U = Q_1\,(ON), Q_2\,(OFF)$

$E_S < E_L = Q_2\,(ON), Q_1\,(OFF)$

$E_S < \frac{E_U - E_L}{2} = Q_1\,(OFF), Q_2\,(OFF)$

FIGURE 22. TRI-LEVEL COMPARATOR CIRCUIT

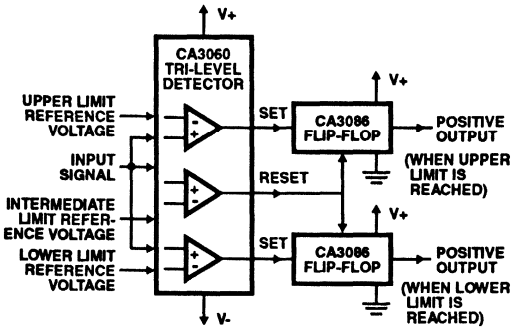


FIGURE 23. FUNCTIONAL BLOCK DIAGRAM OF A TRI-LEVEL COMPARATOR

The circuit diagram of a tri-level comparator appears in Figure 22. Power is provided for the CA3060 via terminal 3 and 8 by ±6V supplies and the built-in regulator provides amplifier bias current (I_{ABC}) to the three amplifiers via terminal 1. Lower limit and upper limit reference voltages are selected by appropriate adjustment of potentiometers R_1 and R_2, respectively. When resistors R_3 and R_4 are equal in value (as shown), the intermediate limit reference voltage is automatically established at a value midway between the lower limit and upper limit values. Appropriate variation of resistors R_3 and R_4 permits selection of other values of intermediate limit voltage. Input signal (E_S) is applied to the three comparators via terminals 5, 12 and 14. The "SET" output lines trigger the appropriate flip-flop whenever the input signal reaches a limit value. When the input signal returns to an intermediate value, the common flip-flop "RESET" line is energized. The loads in the circuits, shown in Figure 22 are 5V, 25mA lamps.

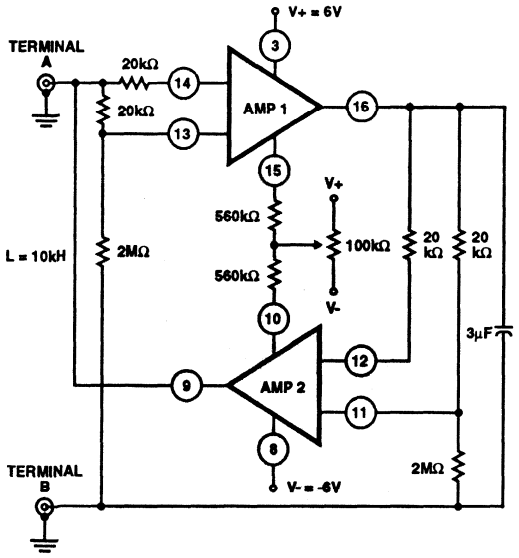


FIGURE 24. TWO OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS OF THE CA3060 CONNECTED AS A GYRATOR IN AN ACTIVE FILTER CIRCUIT

Active Filters - Using the CA3060 as a Gyrator

The high output impedance of the OTAs makes the CA3060 ideally suited for use as a gyrator in active filter applications. Figure 24 shows two OTAs of the CA3060 connected as a gyrator in an active filter circuit. The OTAs in this circuit can make a 3μF capacitor function as a floating 10kH inductor across Terminals A and B. The measured Q of 13 (at a frequency of 1Hz) of this inductor compares favorably with a calculated Q of 16. The 20kΩ to 2MΩ attenuators in this circuit extend the dynamic range of the OTA by a factor of 100. The 100kΩ potentiometer, across V+ and V-, tunes the inductor by varying the g21 of the OTAs, thereby changing the gyration resistance.

Three Channel Multiplexer

Figure 25 shows a schematic of a three channel multiplexer using a single CA3060 and a 3N153 MOSFET as a buffer and power amplifier.

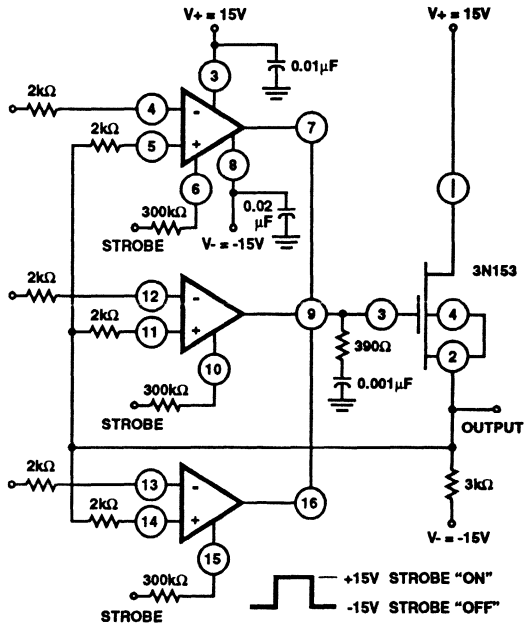


FIGURE 25. THREE CHANNEL MULTIPLEXER

When the CA3060 is connected as a high input impedance voltage follower, and strobe "ON", each amplifier is activated and the output swings to the level of the input of the amplifier. The cascade arrangement of each CA3060 amplifier with the MOSFET provides an open loop voltage gain in excess of 100dB, thus assuring excellent accuracy in the voltage follower mode with 100% feedback. Operation at ±6V is also possible with several minor changes. First, the resistance in series with the amplifier bias current (I_{ABC}) terminal of each amplifier should be decreased to maintain 100μA of strobe "ON" current at this lower supply voltage. Second, the drain resistance for the MOSFET should be

decreased to maintain the same value of source current. The low cost dual gate protected MOSFET, 40841 type, may be used when operating at the low supply voltage.

The phase compensation network consists of a single 390Ω resistor and a 1000pF capacitor, located at the interface of the CA3060 output and the MOSFET gate. The bandwidth of the system is 1.5MHz and the slew rate is 0.3V/μs. The system slew rate is directly proportional to the value of the phase compensation capacitor. Thus, with higher gain settings where lower values of phase compensation capacitors are possible, the slew rate is proportionally increased.

Non-Linear Applications

AM Modulator (Two Quadrant Multiplier)

Figure 26 shows Amplifier 3 of the CA3060 used in an AM modulator or two quadrant multiplier circuit. When modulation is applied to the amplifier bias input, Terminal B, and the carrier frequency to the differential input, Terminal A, the waveform, shown in Figure 26 is obtained. Figure 26 is a result of adjusting the input offset control to balance the circuit so that no modulation can occur at the output without a carrier input. The linearity of the modulator is indicated by the solid trace of the superimposed modulating frequency. The maximum depth of modulation is determined by the ratio of the peak input modulating voltage to V-.

The two quadrant multiplier characteristic of this modulator is easily seen if modulation and carrier are reversed as shown in Figure 26. The polarity of the output must follow that of the differential input; therefore, the output is positive only during, the positive half cycle of the modulation and negative only in the second half cycle. Note, that both the input and output signals are referenced to ground. The output signal is zero when either the differential input or I_{ABC} are zero.

Four Quadrant Multiplier

The CA3060 is also useful as a four quadrant multiplier. A block diagram of such a multiplier, utilizing Amplifiers 1, 2 and 3 is shown in Figure 27 and a typical circuit is shown in Figure 28. The multiplier consists of a single CA3060 and, as in the two quadrant multiplier, exhibits no level shift between input and output. In Figure 27, Amplifier 1 is connected as an inverting amplifier for the X-input signal. The output current of Amplifier 1 is calculated as follows:

$$I_O(1) = [-V_X]\,[g_{21}(1)] \qquad \text{Equation 3}$$

Amplifier 2 is a non-inverting amplifier so that

$$I_O(2) = [+V_X]\,[g_{21}(2)] \qquad \text{Equation 4}$$

Because the amplifier output impedances are high, the load current is the sum of the two output currents, for an output voltage

$$V_O = V_X R_L\,[g_{21}(2) - g_{21}(1)] \qquad \text{Equation 5}$$

The transconductance is approximately proportional to the amplifier bias current; therefore, by varying the bias current the g21 is also controlled. Amplifier 2 bias current is proportional to the Y-input signal and is expressed as

$$I_{ABC(2)} \approx \frac{(V\text{-}) + V_Y}{R_1} \qquad \text{Equation 6}$$

Hence,

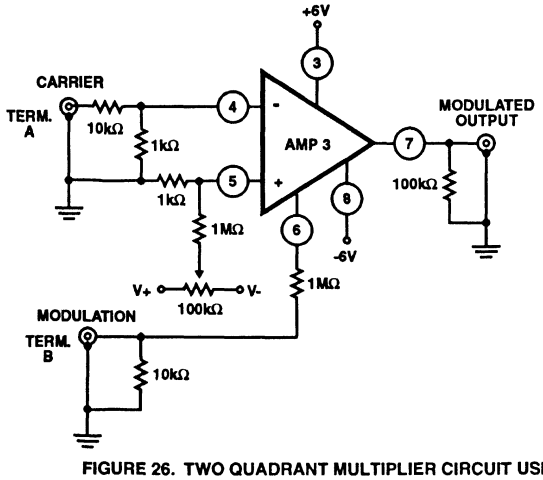
$$g_{21}(2) \approx k\,[(V\text{-}) + V_Y] \qquad \text{Equation 7}$$

Bias for Amplifier 1 is derived from the output of Amplifier 3 which is connected as a unity gain inverting amplifier. $I_{ABC(1)}$, therefore, varies inversely with V_Y. And by the same reasoning as above

$$g_{21}(1) \approx k\,[(V\text{-}) - V_Y] \qquad \text{Equation 8}$$

Combining Equations 5, 7 and 8 yields:

$$V_O \approx V_X \bullet k \bullet R_L\,\{[(V\text{-}) + V_Y] - [(V\text{-}) - V_Y]\} \text{ or } V_O \approx 2kR_L V_X V_Y$$



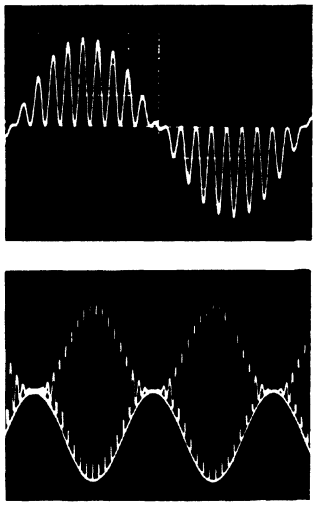


FIGURE 26. TWO QUADRANT MULTIPLIER CIRCUIT USING THE CA3060 WITH ASSOCIATED WAVEFORMS

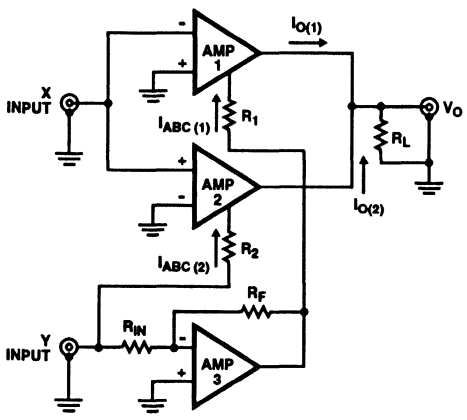


FIGURE 27. FOUR QUADRANT MULTIPLIER

Figure 28 shows the actual circuit including all the adjustments associated with differential input and an adjustment for equalizing the gains of Amplifiers 1 and 2. Adjustment of the circuit is quite simple. With both the X and Y voltages at zero, connect Terminal 10 to Terminal 8. This procedure disables Amplifier 2 and permits adjusting the offset voltage of Amplifier 1 to zero by means of the 100kΩ potentiometer. Next, remove the short between Terminal 10 and 8 and connect Terminal 15 to Terminal 8. This step disables Amplifier 1 and permits Amplifier 2 to be zeroed with the other potentiometer. With AC signals on both the X and Y inputs, R_3 and R_{11} are adjusted for symmetrical output signals. Figure 29 shows the output waveform with the multiplier adjusted. The voltage waveform in Figure 29a shows suppressed carrier modulation of 1kHz carrier with a triangular wave.

Figures 29b and 29c, respectively, show the squaring of a triangular wave and a sine wave. Notice that in both cases the output is always positive and returns to zero after each cycle.

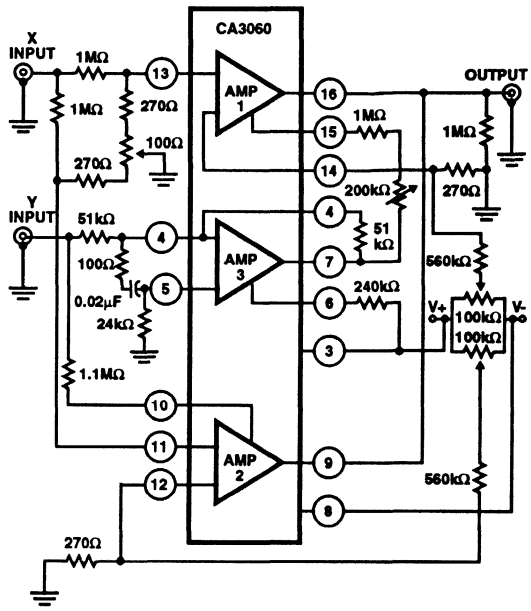
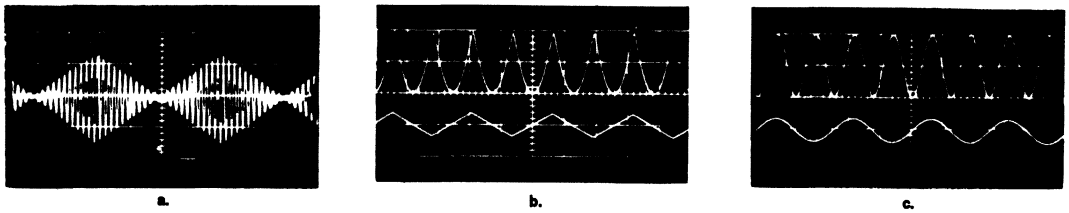


FIGURE 28. TYPICAL FOUR QUADRANT MULTIPLIER CIRCUIT



a. b. c.

FIGURE 29. VOLTAGE WAVEFORMS OF FOUR QUADRANT MULTIPLIER CIRCUIT

HARRIS SEMICONDUCTOR

CA3078

March 1993

Micropower Operational Amplifier

Features

- **Low Standby Power..... As Low As 700nW**
- **Wide Supply Voltage Range.....±0.75V to ±15V**
- **High Peak Output Current..... 6.5mA min.**
- **Adjustable Quiescent Current**
- **Output Short Circuit Protection**

Applications

- **Portable Electronics**
- **Medical Electronics**
- **Instrumentation**
- **Telemetry**
- **Intrusion Alarms**

Description

The CA3078 and CA3078A are high gain monolithic operational amplifiers which can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The CA3078 and CA3078A provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5V battery is a practical reality with these devices.

The CA3078A is a premium device having a supply voltage range of V± = 0.75V to V± = 15V. The CA3078 has the same lower supply voltage limit but the upper limit is V+ = +6V and V- = -6V.

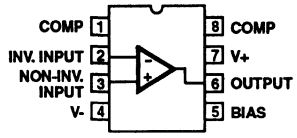
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3078AE	-55°C to +125°C	8 Lead Plastic DIP
CA3078AM	-55°C to +125°C	8 Lead SOIC
CA3078AM96	-55°C to +125°C	8 Lead SOIC*
CA3078AT	-55°C to +125°C	8 Pin Can
CA3078E	0°C to +70°C	8 Lead Plastic DIP
CA3078M	0°C to +70°C	8 Lead SOIC
CA3078M96	0°C to +70°C	8 Lead SOIC*
CA3078T	0°C to +70°C	8 Pin Can

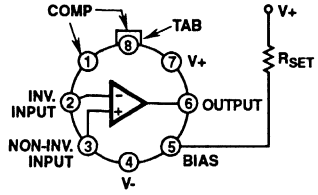
* Denotes Tape and Reel

Pinouts

CA3078 (PDIP, SOIC)
TOP VIEW



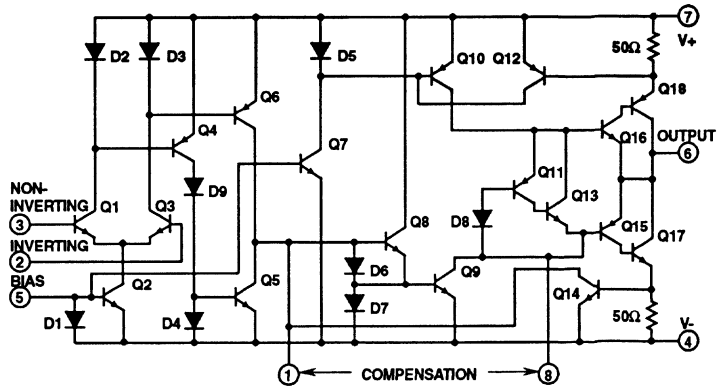
CA3078 (TO-5 CAN)
TOP VIEW



NOTE: Pin 4 is connected to case.

Schematic Diagram

CA3078 AND CA3078A



File Number **535.2**

Specifications CA3078, CA3078A

Absolute Maximum Ratings T_A = +25°C

Supply Voltage (Between V+ and V- Terminal)
- CA3078 ..... 14V
- CA3078A 36V

Differential Input Voltage 6V
Input Voltage ..... V+ to V-
Input Current 0.1mA
Output Short Circuit Duration (Note 1) ..... No Limitation
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
- CA3078 ..... 0°C to +70°C
- CA3078A ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications For Equipment Design

	TEST CONDITIONS			CA3078A LIMITS R_{SET} = 5.1MΩ					CA3078 LIMITS R_{SET} = 1MΩ					
				T_A = +25°C			T_A = -55°C to +125°C		T_A = +25°C			T_A = 0°C to +70°C		
SYMBOL	V+ and V-	R_S (kΩ)	R_L (kΩ)	MIN	TYP	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	UNITS
V_{IO}	±6V	≤10	-	-	0.70	3.5	-	4.5	-	1.3	4.5	-	5	mV
I_{IO}		-	-	-	0.50	2.5	-	5.0	-	6	32	-	40	nA
I_{IB}		-	-	-	7	12	-	50	-	60	170	-	200	nA
A_{OL}		-	≥10	92	100	-	90	-	88	92	-	86	-	dB
I_Q		-	-	-	20	25	-	45	-	100	130	-	150	µA
P_D		-	-	-	240	300	-	540	-	1200	1560	-	1800	µW
V_{OM}		-	≥10	±5.1	±5.3	-	±5	-	±5.1	±5.3	-	±5	-	V
V_{ICR}		≤10	-	-	-5.5 to +5.8	-	-5 to +5	-	-	-5.5 to +5.8	-	-5 to +5	-	V
CMRR		≤10	-	80	115	-	-	-	80	110	-	-	-	dB
I_{OM}+ or I_{OM}-		-	-	-	12	-	6.5	30	-	12	-	6.5	30	mA
$\Delta V_{IO}/\Delta V$+		≤10	-	76	105	-	-	-	76	93	-	-	-	µV/V
$\Delta V_{IO}/\Delta V$-		≤10	-	76	105	-	-	-	76	93	-	-	-	µV/V
				R_{SET} = 13MΩ										
V_{IO}	±15V	≤10	-	-	1.4	3.5	-	4.5	-	-	-	-	-	mV
A_{OL}		-	≥10	92	100	-	88	-	-	-	-	-	-	dB
I_Q		-	-	-	20	30	-	50	-	-	-	-	-	µA
P_D		-	-	-	600	750	-	1350	-	-	-	-	-	µW
V_{OM}		-	≥10	±13.7	±14.1	-	±13.5	-	-	-	-	-	-	V
CMRR		≤10	-	80	106	-	-	-	-	-	-	-	-	dB
I_{IB}		-	-	-	7	14	-	55	-	-	-	-	-	nA
I_{IO}		-	-	-	0.50	2.7	-	5.5	-	-	-	-	-	nA

NOTE:

1. Short circuit may be applied to ground or to either supply.

Electrical Specifications T_A = +25°C, Typical Values Intended Only for Design Guidance

SYMBOL	TYPICAL VALUES				UNITS
	CA3078A		CA3078		
	V+ = +1.3V, V- = -1.3V R_{SET} = 2MΩ	V+ = +0.75V, V- = -0.75V R_{SET} = 10MΩ	V+ = +1.3V, V- = -1.3V R_{SET} = 2MΩ	V+ = +0.75V, V- = -0.75V R_{SET} = 10MΩ	
V_{IO}	0.7	0.9	1.3	1.5	mV
I_{IO}	0.3	0.054	1.7	0.5	nA
I_{IB}	3.7	0.45	9	1.3	nA
A_{OL}	84	65	80	60	dB
I_Q	10	1	10	1	µA
P_D	26	1.5	26	1.5	µW
V_{OPP}	1.4	0.3	1.4	0.3	V
V_{ICR}	-0.8 to +1.1	-0.2 to +0.5	-0.8 to +1.1	-0.2 to +0.5	V
CMRR	100	90	100	90	dB
$I_{OM}\pm$	12	0.5	12	0.5	mA
$\Delta V_{IO}/\Delta V\pm$	20	50	20	50	µV/V

Electrical Specifications T_A = +25°C and V+ = +6V, V- = -6V, Typical Values Intended Only for Design Guidance

SYMBOL	TEST CONDITIONS	CA3078A		CA3078	UNITS
		R_{SET} = 5.1MΩ	R_{SET} = 1MΩ	R_{SET} = 1MΩ	
$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10k\Omega$	5	6	6	µV/°C
$\Delta I_{IO}/\Delta T_A$	$R_S \leq 10k\Omega$	6.3	70	70	pA/°C
BW_{OL}	3dB pt.	0.3	2	2	kHz
SR	See Figures 18, 19	0.027	0.04	0.04	V/µs
		0.5	1.5	1.5	V/µs
t_R	10% to 90% Rise Time	3	2.5	2.5	µs
R_I	-	7.4	1.7	0.87	MΩ
R_O	-	1	0.8	0.8	kΩ
e_N(10Hz)	R_S = 0	40	-	25	$nV/\sqrt{Hz}$
i_N(10Hz)	R_S = 1MΩ	0.25	-	1	$pA/\sqrt{Hz}$

Typical Performance Curves

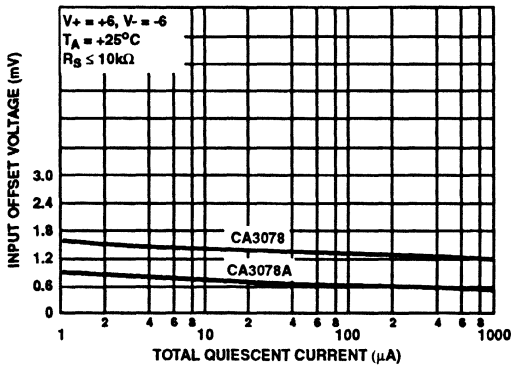


FIGURE 1. INPUT OFFSET VOLTAGE vs TOTAL QUIESCENT CURRENT

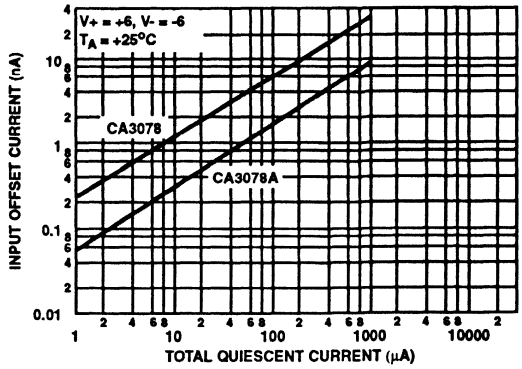


FIGURE 2. INPUT OFFSET CURRENT vs TOTAL QUIESCENT CURRENT

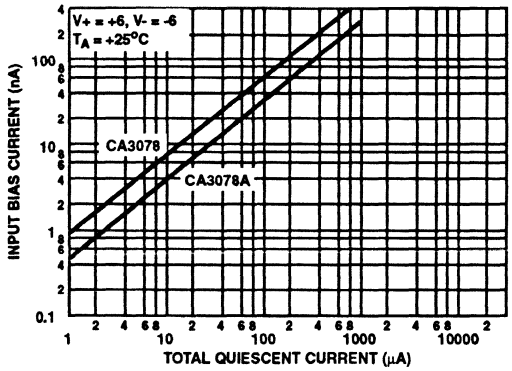


FIGURE 3. INPUT BIAS CURRENT vs TOTAL QUIESCENT CURRENT

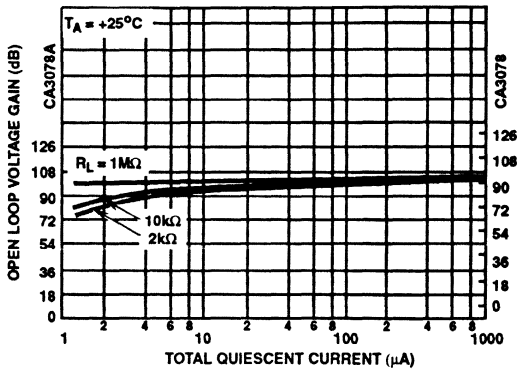


FIGURE 4. OPEN LOOP VOLTAGE GAIN vs TOTAL QUIESCENT CURRENT

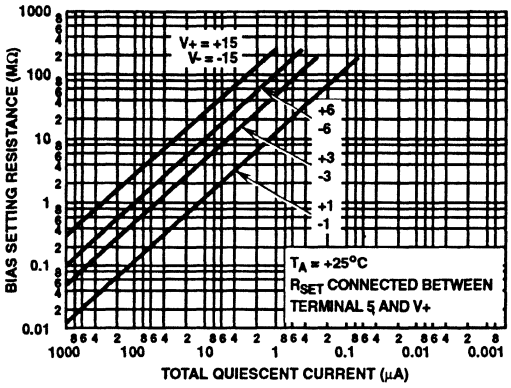


FIGURE 5. BIAS SETTING RESISTANCE vs TOTAL QUIESCENT CURRENT

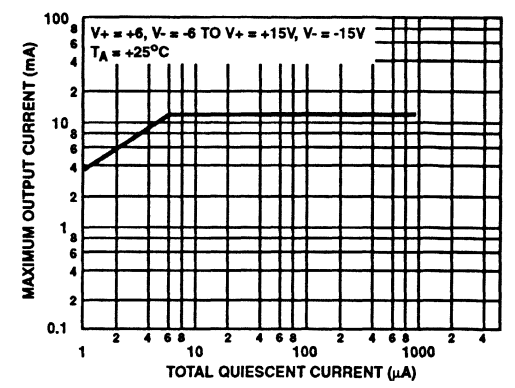


FIGURE 6. MAXIMUM OUTPUT CURRENT vs TOTAL QUIESCENT CURRENT

Typical Performance Curves (Continued)

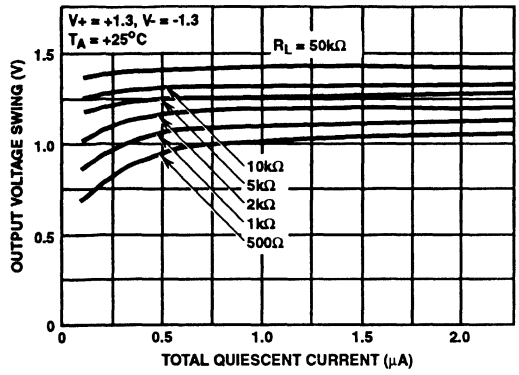


FIGURE 7. OUTPUT VOLTAGE SWING vs TOTAL QUIESCENT CURRENT

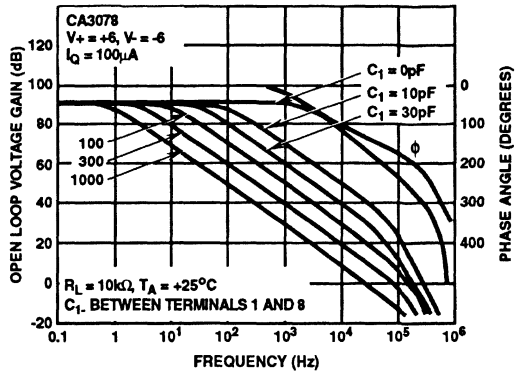


FIGURE 8. OPEN LOOP VOLTAGE GAIN vs FREQUENCY FOR CA3078

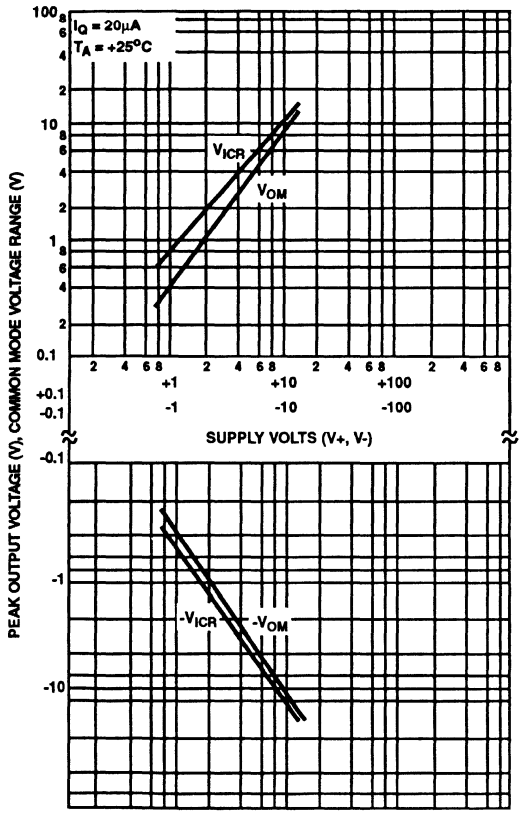


FIGURE 9. OUTPUT AND COMMON MODE VOLTAGE vs SUPPLY VOLTAGE

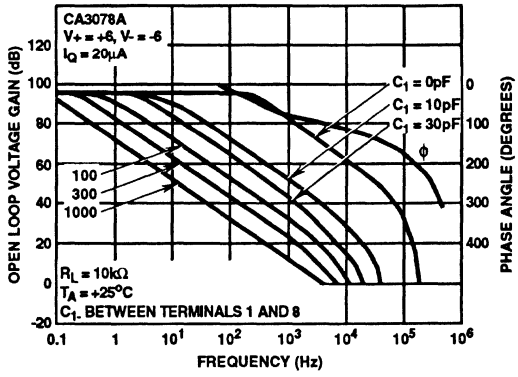


FIGURE 10. OPEN LOOP VOLTAGE GAIN vs FREQUENCY FOR CA3078A

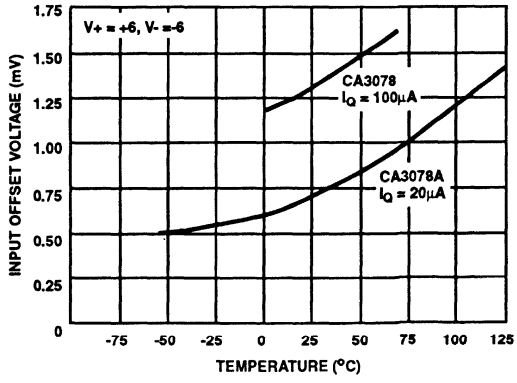


FIGURE 11. INPUT OFFSET VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

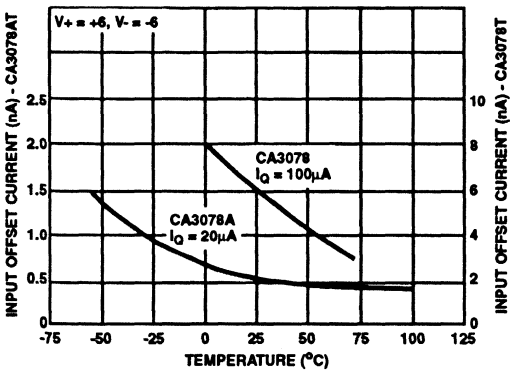


FIGURE 12. INPUT OFFSET CURRENT vs TEMPERATURE

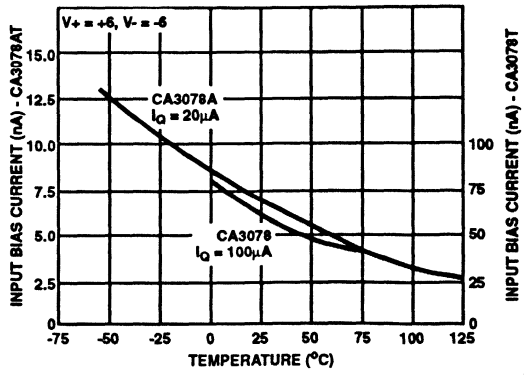


FIGURE 13. INPUT BIAS CURRENT vs TEMPERATURE

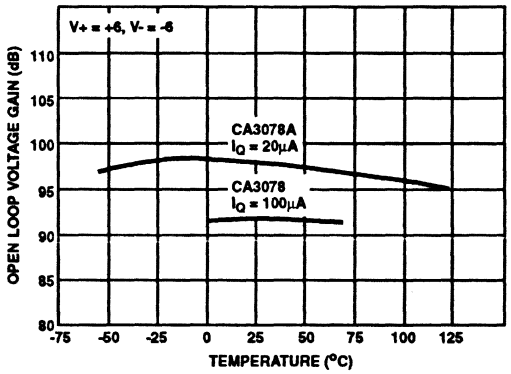


FIGURE 14. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

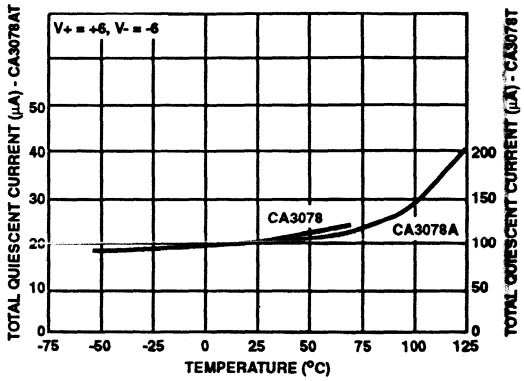


FIGURE 15. TOTAL QUIESCENT CURRENT vs TEMPERATURE

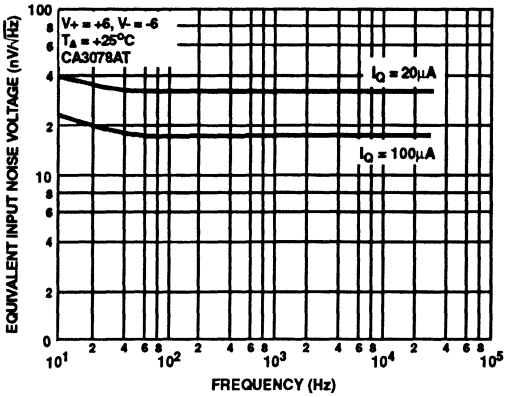


FIGURE 16. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

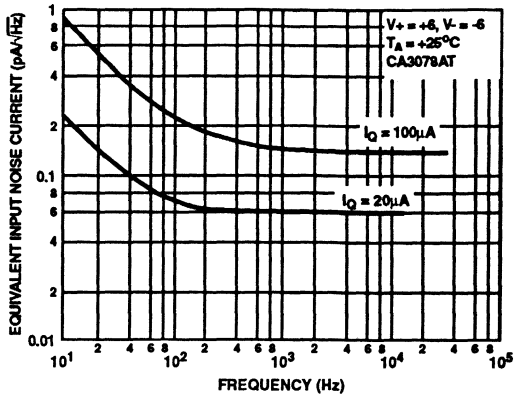
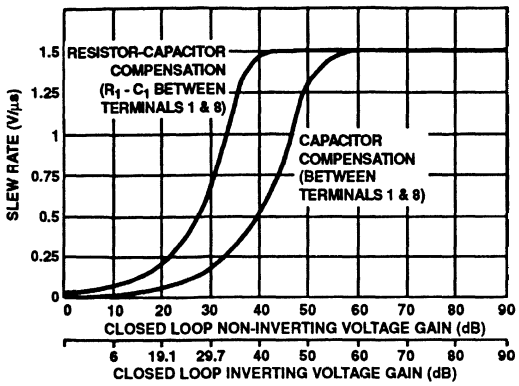


FIGURE 17. EQUIVALENT INPUT NOISE CURRENT vs FREQUENCY

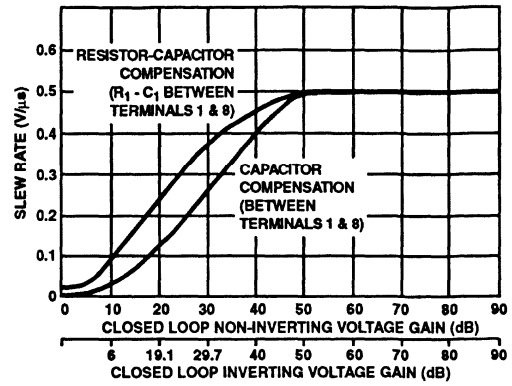
2 OPERATIONAL AMPLIFIERS

Typical Performance Curves (Continued)



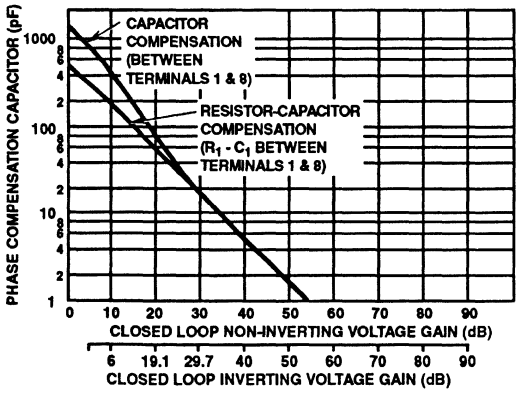
Supply Volts: V+ = +6, V- = -6
Quiescent Current (I_Q) = 100μA
Ambient Temperature (T_A) = +25°C
Load Impedance: R_L = 10kΩ, C_L = 100pF
Feedback Resistance (R_F) = 0.1MΩ
Output Voltage (V_{OPP}) = 10V
R_1 determined for transient response with 10% overshoot on a 100mV output signal ($R_1 \times C_1 = 2.5 \times 10^{-6}$)

FIGURE 18. SLEW RATE vs CLOSED LOOP GAIN FOR I_Q = 100μA - CA3078



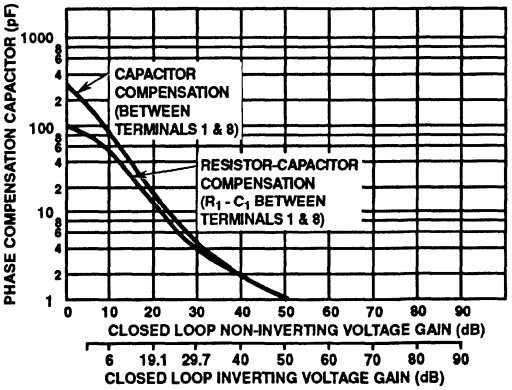
Supply Volts: V+ = +6, V- = -6
Quiescent Current (I_Q) = 20μA
Ambient Temperature (T_A) = +25°C
Load Impedance: R_L = 10kΩ, C_L = 100pF
Feedback Resistance (R_F) = 0.1MΩ
Output Voltage (V_{OPP}) = 10V
R_1 determined for transient response with 10% overshoot on a 100mV output signal ($R_1 \times C_1 = 2 \times 10^{-6}$)

FIGURE 19. SLEW RATE vs CLOSED LOOP GAIN FOR I_Q = 20μA - CA3078A



Supply Volts: V+ = +6, V- = -6
Quiescent Current (I_Q) = 100μA
Ambient Temperature (T_A) = +25°C
Load Impedance: R_L = 10kΩ, C_L = 100pF
Feedback Resistance (R_F) = 0.1MΩ
Output Voltage (V_{OPP}) = 100mV
R_1 determined for transient response with 10% overshoot on a 100mV output signal ($R_1 \times C_1 = 2.5 \times 10^{-6}$)

FIGURE 20. PHASE COMPENSATION CAPACITANCE vs CLOSED LOOP GAIN - CA3078



Supply Volts: V+ = +6, V- = -6
Quiescent Current (I_Q) = 20μA
Ambient Temperature (T_A) = +25°C
Load Impedance: R_L = 10kΩ, C_L = 100pF
Feedback Resistance (R_F) = 0.1MΩ
Output Voltage (V_{OPP}) = 100mV
R_1 determined for transient response with 10% overshoot on a 100mV output signal ($R_1 \times C_1 = 2 \times 10^{-6}$)

FIGURE 21. PHASE COMPENSATION CAPACITANCE vs CLOSED LOOP GAIN - CA3078A

TABLE 1. UNITY GAIN SLEW RATE vs COMPENSATION - CA3078 AND CA3078A

Supply Volts: V+ = +6, V- = -6, Output Voltage (V_O) = ±5V, Load Resistance (R_L) = 10kΩ, Transient Response: 10% overshoot for an output voltage of 100mV, Ambient Temperature (T_A) = +25°C

COMPENSATION TECHNIQUE	UNITY GAIN (INVERTING) FIGURE 22					UNITY GAIN (NON-INVERTING) FIGURE 23				
	R_1 kΩ	C_1 pF	R_2 kΩ	C_2 µF	SLEW RATE V/µs	R_1 kΩ	C_1 pF	R_2 kΩ	C_2 µF	SLEW RATE V/µs
CA3078 - I_Q = 100µA										
Single Capacitor	0	750	∞	0	0.0085	0	1500	∞	0	0.0095
Resistor & Capacitor	3.5	350	∞	0	0.04	5.3	500	∞	0	0.024
Input	∞	0	0.25	0.306	0.67	∞	0	0.311	0.45	0.67
CA3078A - I_Q = 20µA										
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor & Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	0.4

Operating Conditions

Compensation Techniques

The CA3078A and CA3078 can be phase compensated with one or two external components depending upon the closed loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from Terminal 1 to Terminal 8. Values of the resistor and capacitor required for compensation as a function of closed loop gain are shown in Figures 20 and 21. These curves represent the compensation necessary at quiescent currents of 100µA and 20µA, respectively, for a transient response with 10% overshoot. Figures 18 and 19 show the slew rates that can be obtained with the two different compensation techniques. Higher speeds can be achieved with input compensation, but this increases noise output. Compensation can also be accomplished with a single capacitor connected from Terminal 1 to Terminal 8, with speed being sacfificed for simplicity. Table 1 gives an indication of slew rates that can be obtained with various compensation techniques at quiescent currents of 100µA and 20µA.

Single Supply Operation

The CA3078A andCA3078 can operate from a single supply with a minimum total supply voltage of 1.5V. Figures 25 and 26 show the CA3078A or CA3078 in inverting and non-inverting 20dB amplifier configurations utilizing a 1.5V type "AA" cell for a supply. The total consumption for either circuit is approximately 675nW. The output voltage swing in this configuration is 300mVp-p with a 20kΩ load.

Test Circuits

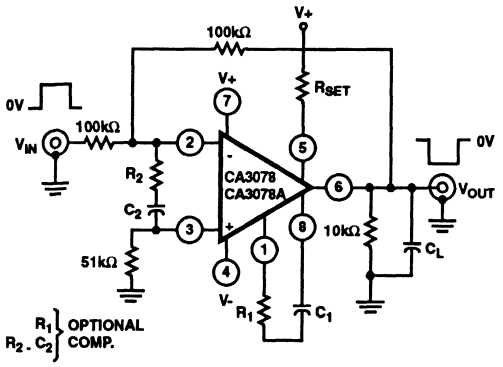


FIGURE 22. TRANSIENT RESPONSE AND SLEW RATE, UNITY GAIN (INVERTING) TEST CIRCUIT

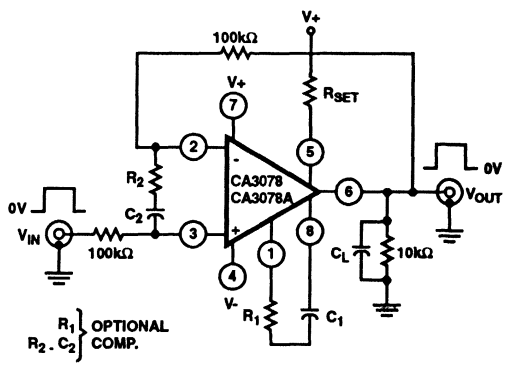
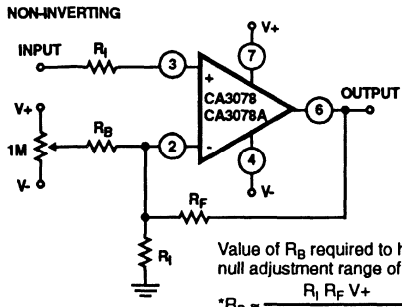


FIGURE 23. SLEW RATE, UNITY GAIN (NON-INVERTING) TEST CIRCUIT

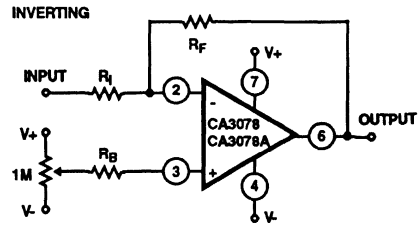
Test Circuits (Continued)



Value of R_B required to have a null adjustment range of ±7.5mV

$$*R_B \approx \frac{R_I R_F V+}{(R_I + R_F)\, 7.5 \times 10^{-3}}$$

assuming $R_B >> \frac{R_I R_F}{R_I + R_F}$



Value of R_B required to have a null adjustment range of ±7.5mV

$$R_B \approx \frac{R_I V+}{7.5 \times 10^{-3}}$$

assuming $R_B >> R_I$

FIGURE 24. OFFSET VOLTAGE NULL CIRCUITS

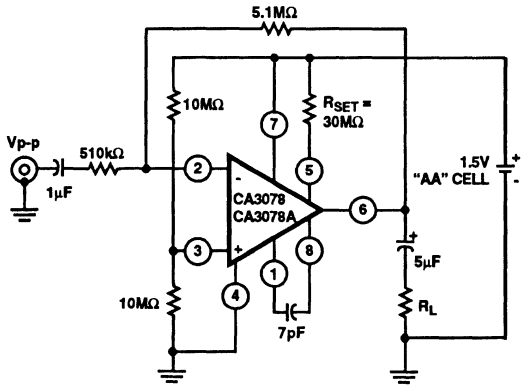


FIGURE 25. INVERTING 20dB AMPLIFIER CIRCUIT

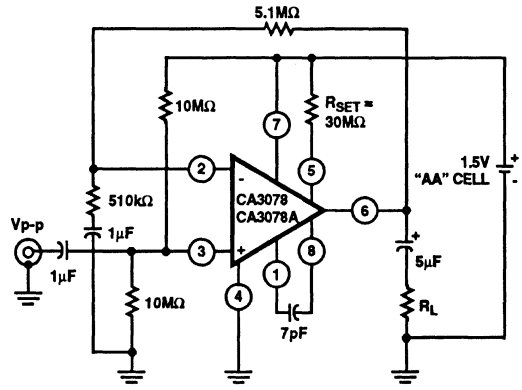


FIGURE 26. NON-INVERTING 20dB AMPLIFIER CIRCUIT

HARRIS SEMICONDUCTOR

CA3080

Operational Transconductance Amplifier (OTA)

April 1993

Features

- Slew Rate (Unity Gain, Compensated).....50V/ms
- Adjustable Power Consumption.....10μW to 30μW
- Flexible Supply Voltage Range ..... ±2V to ±15V
- Fully Adjustable Gain .....0 to gmR_L Limit
- Tight g_M Spread:
  - CA3080 ..... 2:1
  - CA3080A 1.6:1
- Extended g_M Linearity..... 3 Decades

Applications

- Sample and Hold
- Multiplexer
- Voltage Follower
- Multiplier
- Comparator

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
CA3080	0°C to +70°C	8 Pin Can
CA3080A	-55°C to +125°C	8 Pin Can
CA3080AE	-55°C to +125°C	8 Lead Plastic DIP
CA3080AM	-55°C to +125°C	8 Lead SOIC
CA3080AM96	-55°C to +125°C	8 Lead SOIC*
CA3080E	0°C to +70°C	8 Pin Can
CA3080M	0°C to +70°C	8 Lead SOIC
CA3080M96	0°C to +70°C	8 Lead SOIC*

* Denotes Tape and Reel

Description

The CA3080 and CA3080A types are Gatable-Gain Blocks which utilize the unique operational-transconductance-amplifier (OTA) concept described in Application Note ICAN-6668, "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

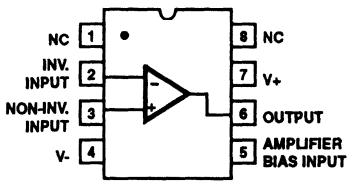
The CA3080 and CA3080A types have differential input and a single-ended, push-pull, class A output. In addition, these types have an amplifier bias input which may be used either for gating or for linear gain control. These types also have a high output impedance and their transconductance (g_M) is directly proportional to the amplifier bias current (I_{ABC}).

The CA3080 and CA3080A types are notable for their excellent slew rate (50V/μs), which makes them especially useful for multiplexer and fast unity-gain voltage followers. These types are especially applicable for multiplexer applications because power is consumed only when the devices are in the "ON" channel state.

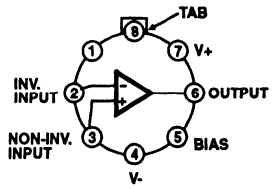
The CA3080A is rated for operation over the full military-temperature range (-55°C to +125°C) and its characteristics are specifically controlled for applications such as sample-hold, gain-control, multiplex, etc. Operational transconductance amplifiers are also useful in programmable power-switch applications, e.g., as described in Application Note AN6048, "Some Applications of a Programmable Power Switch/Amplifier" (CA3094, CA3094A, CA3094B).

Pinouts

CA3080 (PDIP, SOIC)
TOP VIEW

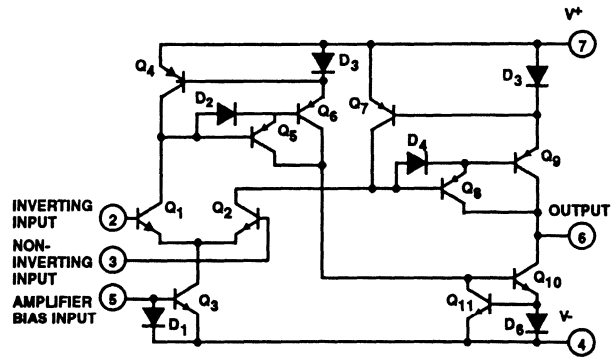


CA3080 (TO-5 CAN)
TOP VIEW



NOTE: Pin 4 is connected to case.

Schematic Diagram



File Number **475.2**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminal) 36V
Differential Input Voltage 5V
Input Voltage . . . . . V+ to V-
Input Signal Current 1mA
Amplifier Bias Current (I_{ABC}) 2mA
Power Dissipation 125mW
Output Short Circuit Duration (Note 1) . . . . . No Limitation
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Operating Temperature Range
CA3080 . . . . . 0°C to +70°C
CA3080A . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

For Equipment Design, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3080 LIMITS			UNITS
		V+ = 15V, V- = -15V I_{ABC} = 500µA	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}		-	0.4	5	mV
		T_A = 0 to +70°C	-	-	6	mV
Input Offset Current	I_{IO}		-	0.12	0.6	µA
Input Bias Current	I_I		-	2	5	µA
		T_A = 0 to +70°C	-	-	7	µA
Forward Transconductance (Large Signal)	g_M		6700	9600	13000	µmho
		T_A = 0 to +70°C	5400	-	-	µmho
Peak Output Current	I_{OM}	R_L = 0Ω	350	500	650	µA
		R_L = 0Ω, T_A = 0 to +70°C	300	-	-	µA
Peak Output Voltage: Positive	V_{+OM}	R_L = ∞	12	13.5	-	V
Negative	V_{-OM}	R_L = ∞	-12	-14.4	-	V
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V+$		-	-	150	µV/V
Negative	$\Delta V_{IO}/\Delta V-$		-	-	150	µV/V
Common-Mode Rejection Ratio	CMRR		80	110	-	dB
Common-Mode Input-Voltage	V_{ICR}		12 to -12	13.6 to -14.6	-	V
Input Resistance	R_I		10	26	-	kΩ

NOTE:

1. Short circuit may be applied to ground or to either supply.

Specifications CA3080, CA3080A

Electrical Specifications Typical Values Intended Only for Design Guidance, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS V+ = 15V, V- = -15V I_{ABC} = 500µA	CA3080 TYP	UNITS
Input Offset Voltage	V_{IO}	I_{ABC} = 5µA	0.3	mV
Input Offset Voltage Change	ΔV_{IO}	I_{ABC} = 500µA to I_{ABC} = 5µA	0.2	mV
Peak Output Current	I_{OM}	I_{ABC} = 5µA	5	µA
Peak Output Voltage:		I_{ABC} = 5µA		
Positive	V_{+OM}		13.8	V
Negative	V_{-OM}		-14.5	V
Magnitude of Leakage Current		I_{ABC} = 0, V_{TP} = 0	0.08	nA
		I_{ABC} = 0, V_{TP} = 36V	0.3	nA
Differential Input Current		I_{ABC} = 0, V_{DIFF} = 4V	0.008	nA
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate:	SR			
Maximum (Uncompensated)			75	V/µs
Unity Gain (Compensated)			50	V/µs
Open-Loop Bandwidth	BW_{OL}		2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		15	MΩ
Input-to-Output Capacitance	C_{I-O}	f = 1 MHz	0.024	pF
Propagation Delay	t_{PHL}, t_{PLH}	I_{ABC} = 500µA	45	ns

Electrical Specifications For Equipment Design, T_A = +25°C, Unless Otherwise Indicated

PARAMETERS	SYMBOL	TEST CONDITIONS V+ = 15V, V- = -15V I_{ABC} = 500µA	CA3080A LIMITS MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{IO}	I_{ABC} = 5µA	-	0.3	2	mV
			-	0.4	2	mV
		T_A = -55 to +125°C	-	-	5	mV
Input Offset Voltage Change	ΔV_{IO}	I_{ABC} = 500µA to I_{ABC} = 5µA	-	0.1	3	mV
Input Offset Current	I_{IO}		-	0.12	0.6	µA
Input Bias Current	I_I		-	2	5	µA
		T_A = -55°C to +125°C	-	-	15	µA
Forward Transconductance (Large Signal)	g_M		7700	9600	12000	µmho
		T_A = -55°C to +125°C	4000	-	-	µmho
Peak Output Current	I_{OM}	I_{ABC} = 5µA, R_L = 0Ω	3	5	7	µA
		R_L = 0Ω	350	500	650	µA
		R_L = 0Ω, T_A = -55°C to +125°C	300	-	-	µA

Electrical Specifications For Equipment Design, T_A = +25°C, Unless Otherwise Indicated **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS V+ = 15V, V- = -15V I_{ABC} = 500µA	CA3080A LIMITS MIN	TYP	MAX	UNITS
Peak Output Voltage:		I_{ABC} = 5µA, R_L = ∞				
Positive	V_{+OM}		12	13.8	-	V
Negative	V_{-OM}		-12	-14.5	-	V
Positive	V_{+OM}	R_L = ∞	12	13.5	-	V
Negative	V_{-OM}		-12	-14.4	-	V
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity:						
Positive	$\Delta V_{IO}/\Delta V^+$		-	-	150	µV/V
Negative	$\Delta V_{IO}/\Delta V^-$		-	-	150	µV/V
Magnitude of Leakage Current		I_{ABC} = 0, V_{TP} = 0	-	0.08	5	nA
		I_{ABC} = 0, V_{TP} = 36V	-	0.3	5	nA
Differential Input Current		I_{ABC} = 0, V_{DIFF} = 4V	-	0.008	5	nA
Common-Mode Rejection Ratio	CMRR		80	110	-	dB
Common-Mode Input-Voltage Range	V_{ICR}		12 to -12	13.6 to -14.6	-	V
Input Resistance	R_I		10	26	-	kΩ

Electrical Specifications Typical Values Intended Only for Design Guidance, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS V+ = 15V, V- = -15V I_{ABC} = 500µA	CA3080A TYP	UNITS
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate:				
Maximum (Uncompensated)	SR		75	V/µs
Unity Gain (Compensated)			50	V/µs
Open-Loop Bandwidth	BW_{OL}		2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		15	MΩ
Input-to-Output Capacitance	C_{I-O}	f = 1 MHz	0.024	pF
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	I_{ABC} = 100µA, T_A = -55°C to +125°C	3.0	µV/°C
Propagation Delay	t_{PHL}, t_{PLH}	I_{ABC} = 500µA	45	ns

Typical Performance Curves

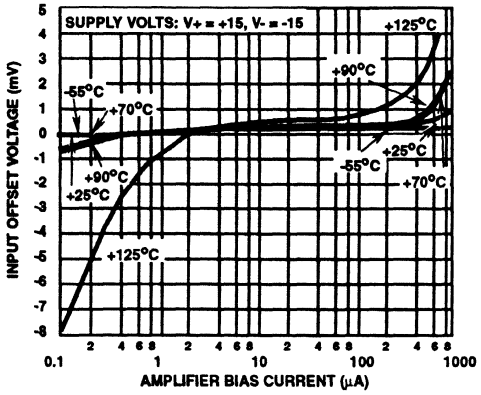


FIGURE 1. INPUT OFFSET VOLTAGEvs AMPLIFIER BIAS CURRENT

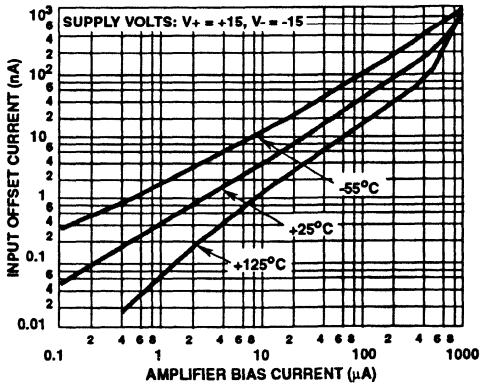


FIGURE 2. INPUT OFFSET CURRENT vs AMPLIFIER BIAS CURRENT

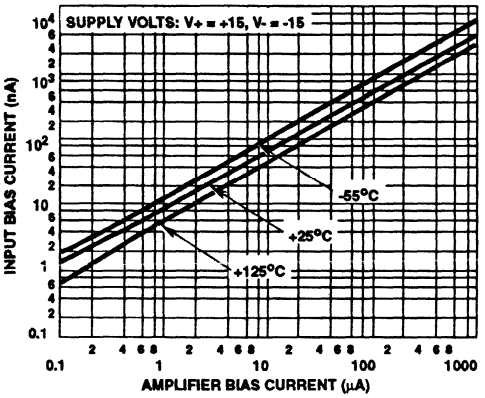


FIGURE 3. INPUT BIAS CURRENT vs AMPLIFIER BIAS CURRENT

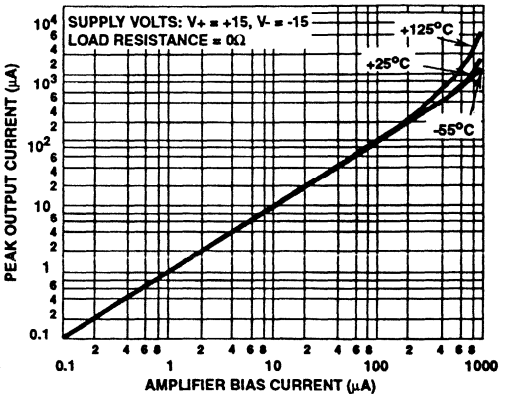


FIGURE 4. PEAK OUTPUT CURRENT vs AMPLIFIER BIAS CURRENT

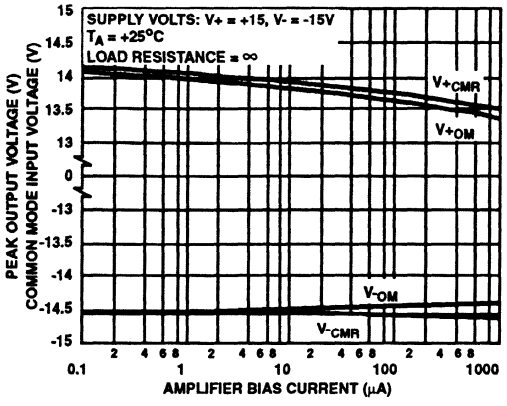


FIGURE 5. PEAK OUTPUT VOLTAGE vs AMPLIFIER BIAS CURRENT

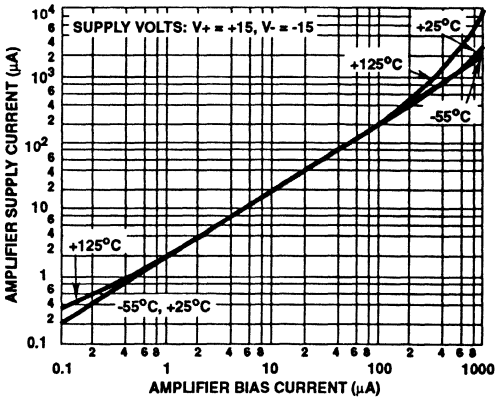


FIGURE 6. AMPLIFIER SUPPLY CURRENT vs AMPLIFIER BIAS CURRENT

Typical Performance Curves (Continued)

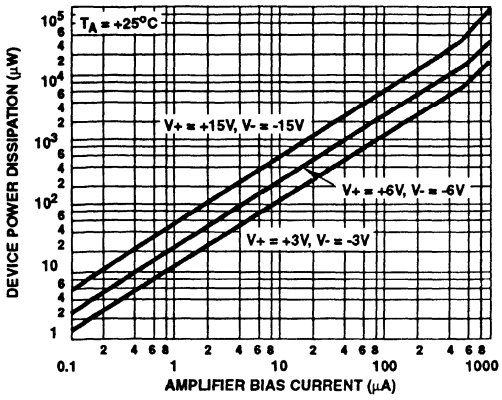


FIGURE 7. TOTAL POWER DISSIPATION vs AMPLIFIER BIAS CURRENT

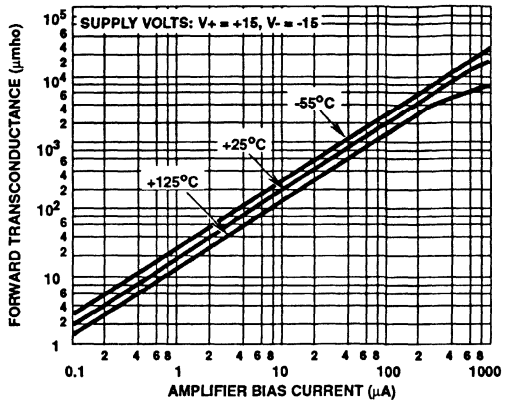


FIGURE 8. TRANSCONDUCTANCE vs AMPLIFIER BIAS CURRENT

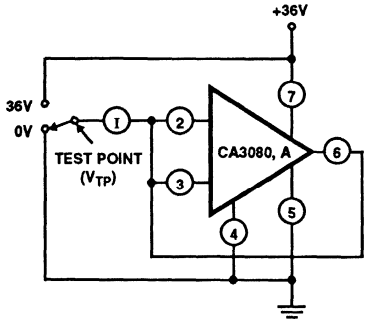


FIGURE 9. LEAKAGE CURRENT TEST CIRCUIT

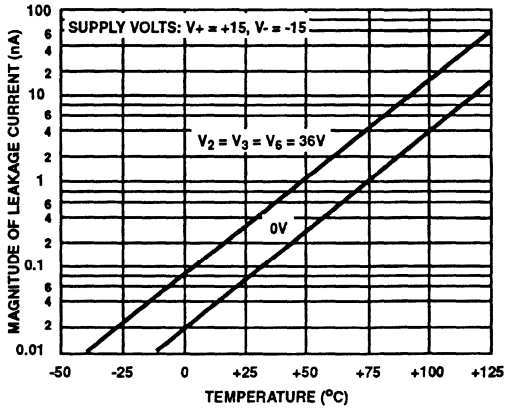


FIGURE 10. LEAKAGE CURRENT vs TEMPERATURE

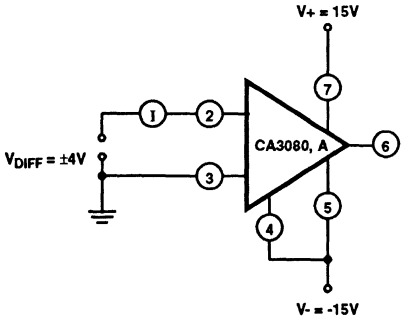


FIGURE 11. DIFFERENTIAL INPUT CURRENT TEST CIRCUIT

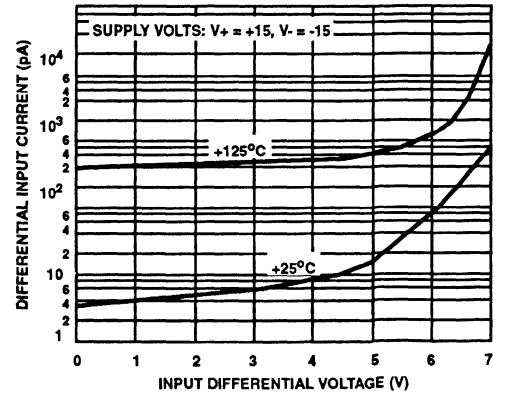


FIGURE 12. INPUT CURRENT vs INPUT DIFFERENTIAL VOLTAGE

Typical Performance Curves (Continued)

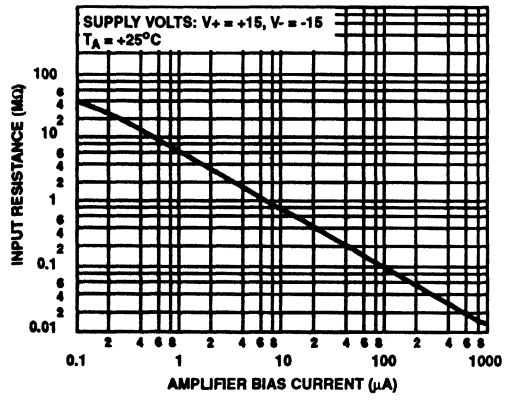


FIGURE 13. INPUT RESISTANCE vs AMPLIFIER BIAS CURRENT

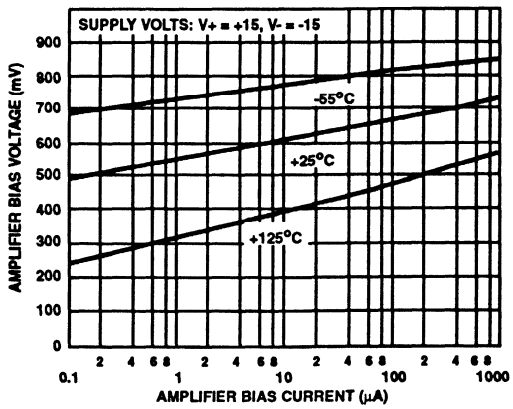


FIGURE 14. AMPLIFIER BIAS VOLTAGE vs AMPLIFIER BIAS CURRENT

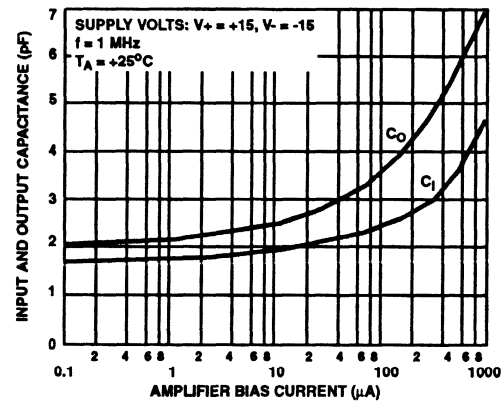


FIGURE 15. INPUT AND OUTPUT CAPACITANCE vs AMPLIFIER BIAS CURRENT

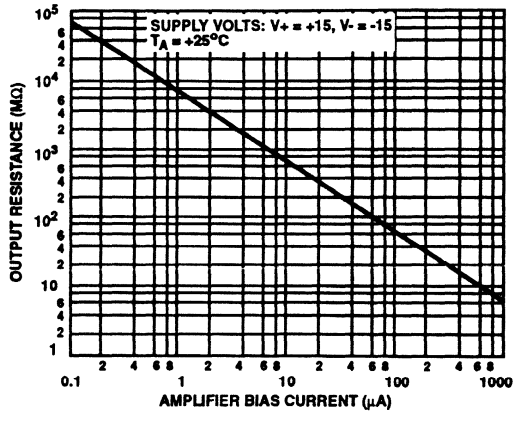


FIGURE 16. OUTPUT RESISTANCE vs AMPLIFIER BIAS CURRENT

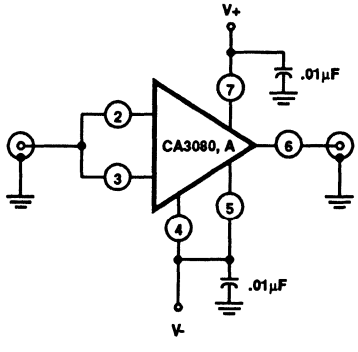


FIGURE 17. INPUT-TO-OUTPUT CAPACITANCE TEST CIRCUIT

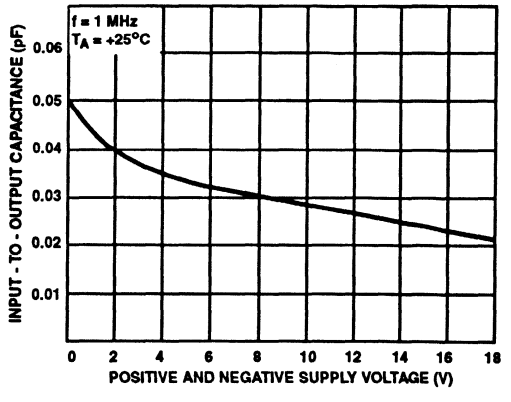


FIGURE 18. INPUT-TO-OUTPUT CAPACITANCE vs SUPPLY VOLTAGE

Applications

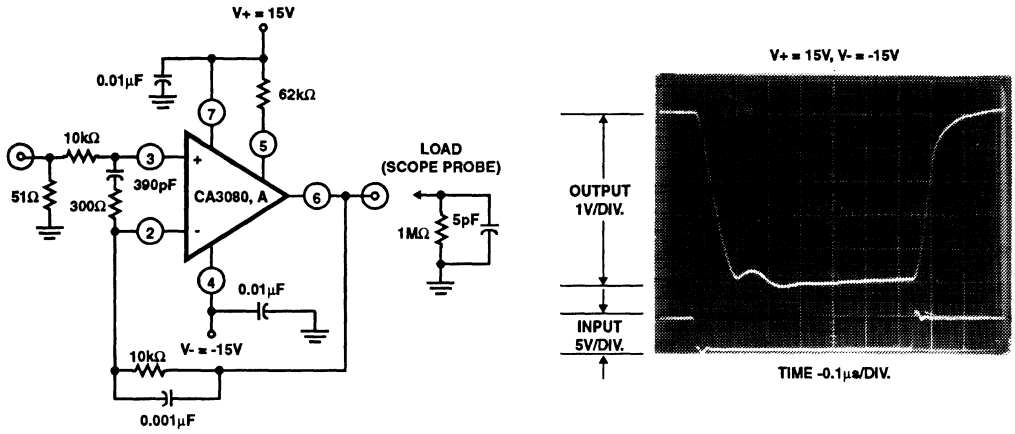


FIGURE 19. SCHEMATIC DIAGRAM OF THE CA3080 AND CA3080A IN A UNITY-GAIN VOLTAGE FOLLOWER CONFIGURATION AND ASSOCIATED WAVEFORM

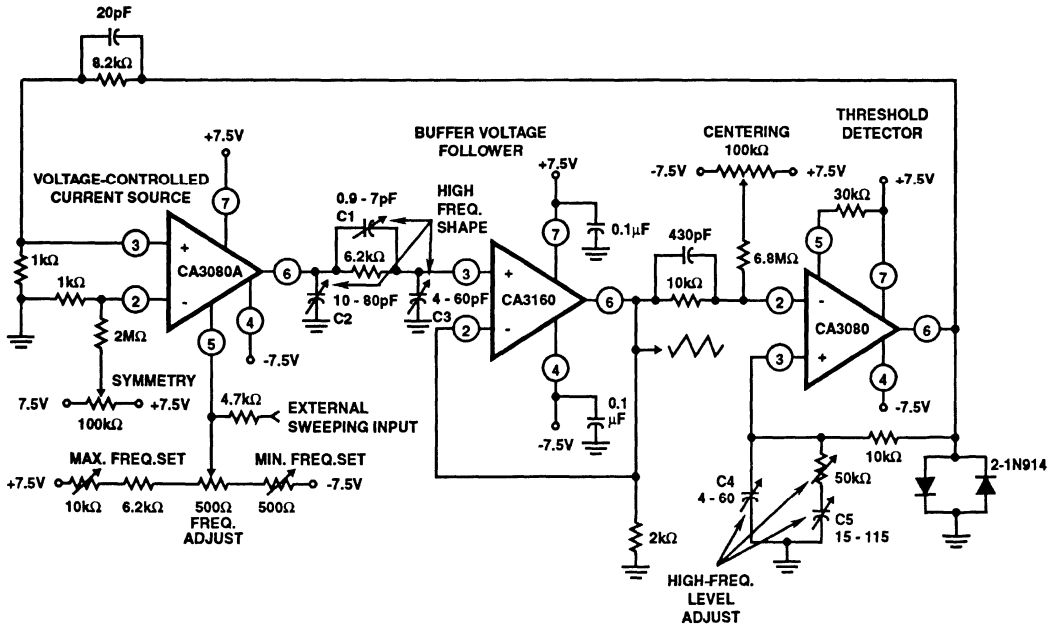
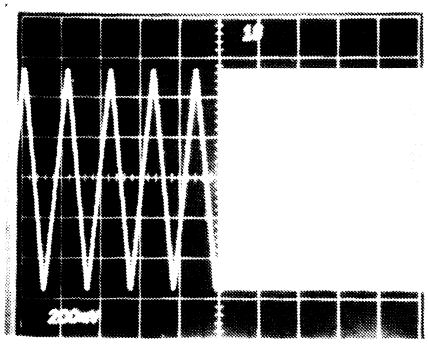
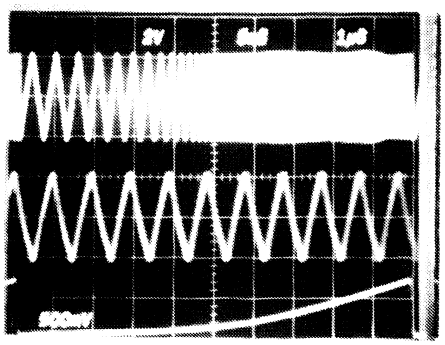


FIGURE 20. 1,000,000/1 SINGLE-CONTROL FUNCTION GENERATOR - 1MHz TO 1Hz

Applications (Continued)



(a) Two-Tone Output Signal From The Function Generator. A Square-Wave Signal Modulates The External Sweeping Input to Produce 1Hz and 1MHz, Showing the 1,000,000/1 Frequency Range of the Function Generator.



(b) Triple-Trace of the Function Generator Sweeping to 1MHz. The Bottom Trace is the Sweeping Signal and the Top Trace is the Actual Generator Output. The Center Trace Displays the 1MHz signal Via Delayed Oscilloscope Triggering of the Upper Swept Output Signal

FIGURE 21. FUNCTION GENERATOR DYNAMIC CHARACTERISTICS WAVEFORMS

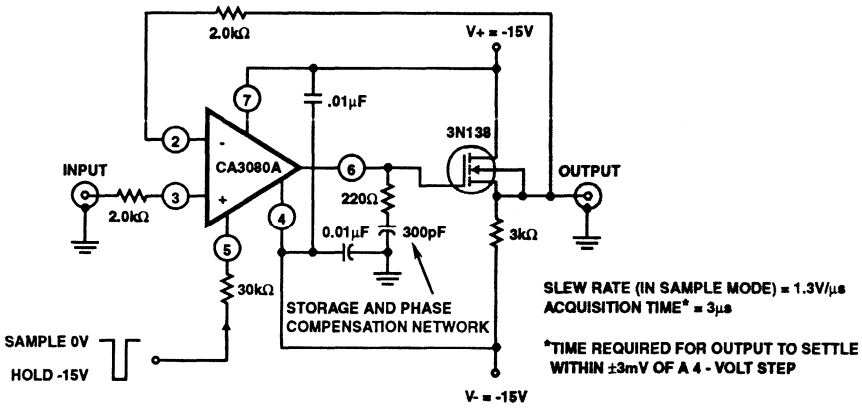


FIGURE 22. SCHEMATIC DIAGRAM OF THE CA3080A IN A SAMPLE-HOLD CONFIGUREATION

Applications (Continued)

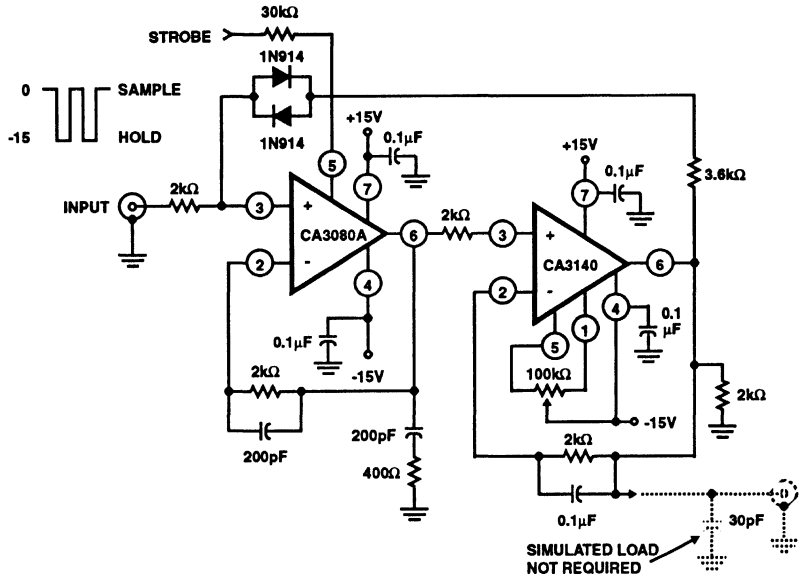
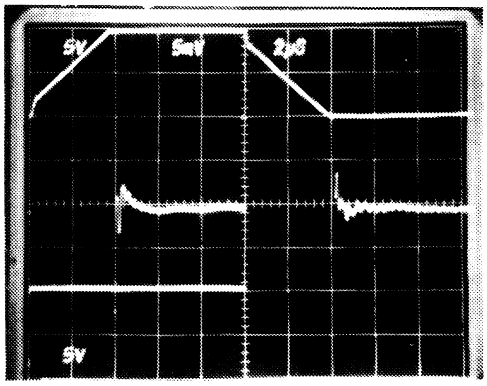


FIGURE 23. SAMPLE AND HOLD CIRCUIT



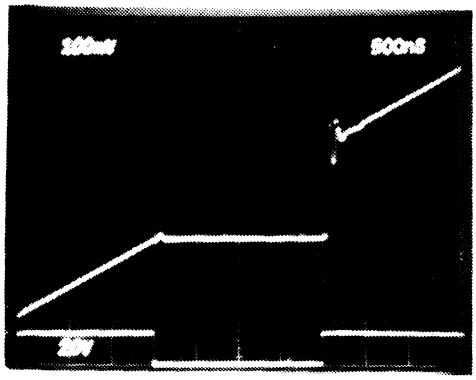
Top Trace: Output Signal (5V/Div. and 2μs/Div.)

Bottom Trace: Input Signal (5V/Div. and 2μs/Div.)

Center Trace: Difference of Input and Output Signals Through Tektronix Amplifier 7A13 (5mV/Div. and 2μs/Div.)

FIGURE 24. LARGE SIGNAL RESPONSE AND SETTLING TIME FOR CIRCUIT SHOWN IN FIGURE 23

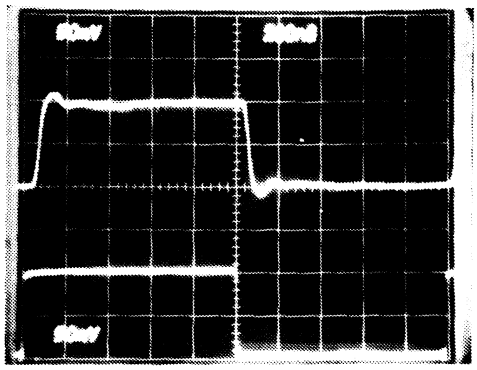
Applications (Continued)



Top Trace: System Output (100mV/Div. and 500ns/Div.)

Bottom Trace: Sampling Signal (20V/Div. and 500ns/Div.)

FIGURE 25. SAMPLING RESPONSE FOR CIRCUIT SHOWN IN FIGURE 23



Top Trace: Output (50mV/Div. and 200ns/Div.)

Bottom Trace: Input (50mV/Div. and 200ns/Div.)

FIGURE 26. INPUT AND OUTPUT RESPONSE FOR CIRCUIT SHOWN IN FIGURE 23

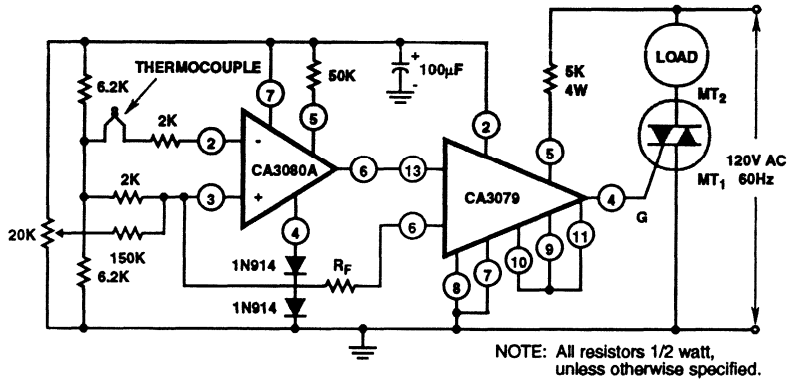


FIGURE 27. THERMOCOUPLE TEMPERATURE CONTROL WITH CA3079 ZERO VOLTAGE SWITCH AS THE OUTPUT AMPLIFIER

Applications (Continued)

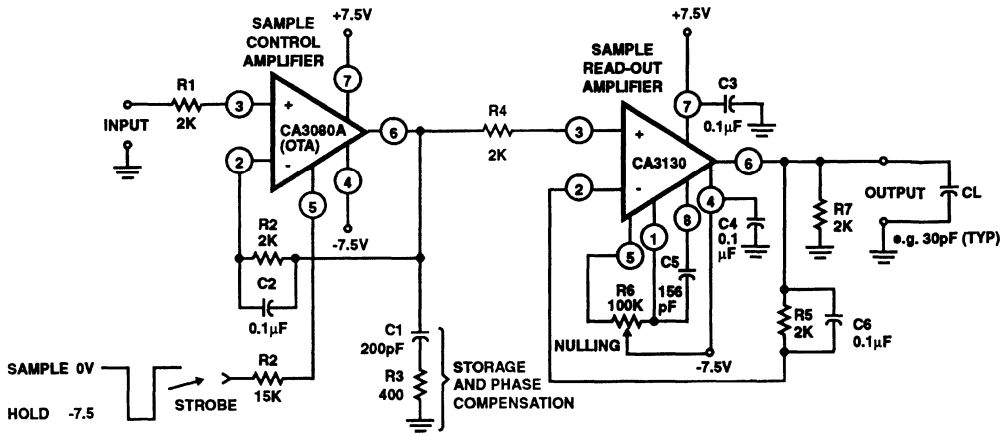
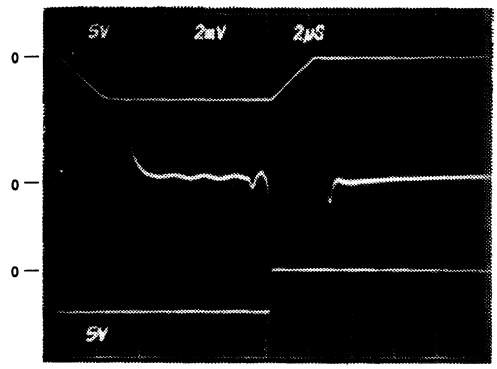


FIGURE 28. SCHEMATIC DIAGRAM OF THE CA3080A IN A SAMPLIE-HOLD CIRCUIT WITH BIMOS OUTPUT AMPLIFIER

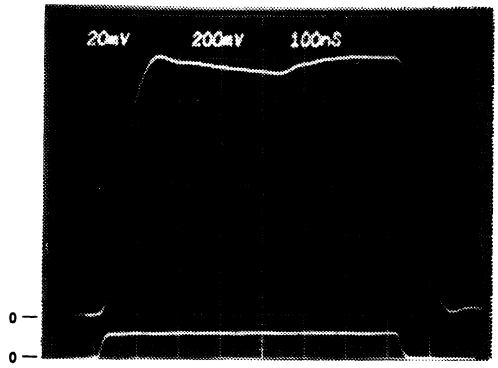


Top Trace: Output (5V/Div. and 2μs/Div.)

Center Trace: Differential Comparison of Input and Output (2mV/Div. and 2μs/Div.)

Bottom Trace: Input (5V/Div. and 2μs/Div.)

FIGURE 29. LARGE-SIGNAL RESPONSE FOR CIRCUIT SHOWN IN FIGURE 28



Top Trace: Output (20mV/Div. and 100ns/Div.)

Bottom Trace: Input (200mV/Div. and 100ns/Div.)

FIGURE 30. SMALL-SIGNAL RESPONSE FOR CIRCUIT SHOWN IN FIGURE 28

Applications (Continued)

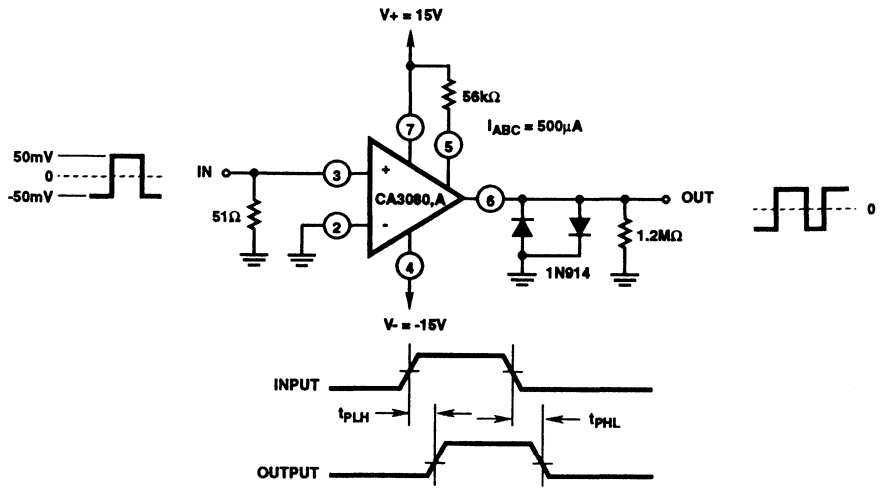


FIGURE 31. PROPAGATION DELAY TEST CIRCUIT AND ASSOCIATED WAVEFORMS

HARRIS SEMICONDUCTOR

CA3094

Programmable Power Switch/Amplifier for Control and General Purpose Applications

March 1993

Features

- CA3094T, S, E, M for Operation Up to 24V
- CA3094AT, S, E, M for Operation Up to 36V
- CA3094BT, S, M for Operation Up to 44V
- Designed for Single or Dual Power Supply
- Programmable: Strobing, Gating, Squelching, AGC Capabilities
- Can Deliver 3W (Average) or 10W (Peak) to External Load (in Switching Mode)
- High Power, Single Ended Class A Amplifier will Deliver Power Output of 0.6W (1.6W Device Dissipation)
- Total Harmonic Distortion (THD) at 0.6W in Class A Operation 1.4% (Typ.)

Applications

- Error Signal Detector: Temperature Control with Thermistor Sensor; Speed Control for Shunt Wound DC Motor
- Over Current, Over Voltage, Over Temperature Protectors
- Dual Tracking Power Supply with CA3085
- Wide Frequency Range Oscillator
- Analog Timer
- Level Detector
- Alarm Systems
- Voltage Follower
- Ramp Voltage Generator
- High Power Comparator
- Ground Fault Interrupter (GFI) Circuits

Description

The CA3094 is a differential input power control switch/amplifier with auxiliary circuit features for ease of programmability. For example, an error or unbalance signal can be amplified by the CA3094 to provide an on-off signal or proportional control output signal up to 100mA. This signal is sufficient to directly drive high current thyristors, relays, dc loads, or power transistors. The CA3094 has the generic characteristics of the CA3080 operational amplifier directly coupled to an integral Darlington power transistor capable of sinking or driving currents up to 100mA.

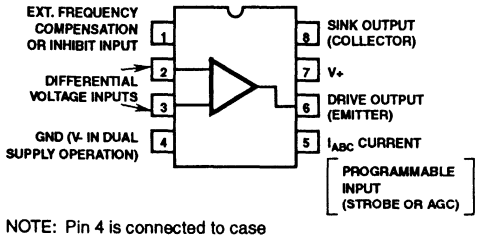
The gain of the differential input stage is proportional to the amplifier bias current (I_{ABC}), permitting programmable variation of the integrated circuit sensitivity with either digital and/or analog programming signals. For example, at an I_{ABC} of 100mA, a 1mV change at the input will change the output from 0 to 100mA (typical).

The CA3094 is intended for operation up to 24V and is especially useful for timing circuits, in automotive equipment, and in other applications where operation up to 24V is a primary design requirement (see Figures 28, 29 and 30 in Applications Section). The CA3094 and CA3094B are like the CA3094 but are intended for operation up to 36V and 44V, respectively (single or dual supply).

These types are available in 8 lead TO-5 style packages with standard leads ("T" suffix) and with dual-in-line formed leads "DIL-CAN" ("S" suffix). Type CA3094 is also available in an 8 lead dual-in-line plastic package "MINI-DIP" ("E" suffix), Small Outline Pakcage ("M" suffix), and in chip form ("H" suffix).

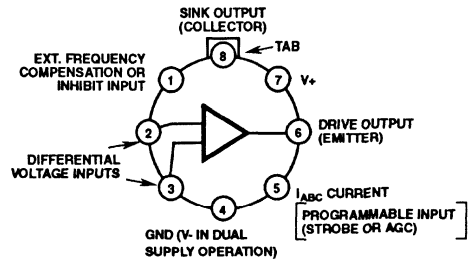
Pinouts

CA3094
(PDIP, SOIC)
TOP VIEW



NOTE: Pin 4 is connected to case

CA3094
(TO-5 CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **598.2**

Specifications CA3094, CA3094A, CA3094B

Absolute Maximum Ratings

Dual Supply Voltage
- CA3094 ..... ±12V
- CA3094A ..... ±18V
- CA3094B ..... ±22V

Single Supply Voltage
- CA3094 ..... 24V
- CA3094A 36V
- CA3094B 44V

Differential Input Voltage (Term. 2 and 3) Note 1 ..... 5V
DC Input Voltage ..... V+ to V-
Input Current (Term. 2 and 3) ..... ±1mA
Amplifier Bias Current (Term. 5) 2mA
Output Current 300mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C for Equipment Design. Single Supply V+ = 30V, Dual Supply V+ = 15V, V- = -15V, I_{ABC} = 100µA Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
INPUT PARAMETERS						
Input Offset Voltage	V_{IO}	T_A = +25°C	-	0.4	5.0	mV
		T_A = 0°C to +70°C	-	-	7.0	mV
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	Change in V_{IO} between I_{ABC} = 100µA and I_{ABC} = 5µA	-	1	8.0	mV
Input Offset Current	I_{IO}	T_A = +25°C	-	0.02	0.2	µA
		T_A = 0°C to +70°C	-	-	0.3	µA
Input Bias Current	I_I	T_A = +25°C	-	0.2	0.50	µA
		T_A = 0°C to +70°C	-	-	0.70	µA
Device Dissipation	P_D	I_{OUT} = 0mA	8	10	12	mW
Common Mode Rejection Ratio	CMRR		70	110	-	dB
Common Mode Input Voltage Range	V_{ICR}	V+ = 30V (High)	27	28.8	-	V
		V- = 0V (Low)	1.0	0.5	-	V
		V+ = 15V	12	13.8	-	V
		V- = -15V	-14	-14.5	-	V
Unity Gain Bandwidth	f_T	I_C = 7.5mA, V_{CE} = 15V, I_{ABC} = 500µA	-	30	-	MHz
Open Loop Bandwidth at -3dB Point	BW_{OL}	I_C = 7.5mA, V_{CE} = 15V, I_{ABC} = 500µA	-	4	-	kHz
Total Harmonic Distortion (Class A Operation)	THD	P_D = 220mW	-	0.4	-	%
		P_D = 600mW	-	1.4	-	%
Amplifier Bias Voltage (Terminal 5 to Terminal 4)	V_{ABC}		-	0.68	-	V
Input Offset Voltage Temperature Coefficient	$\Delta V_{IO}/\Delta T$		-	4	-	µV/°C
Power Supply Rejection	$\Delta V_{IO}/\Delta V$		-	15	150	µV/V

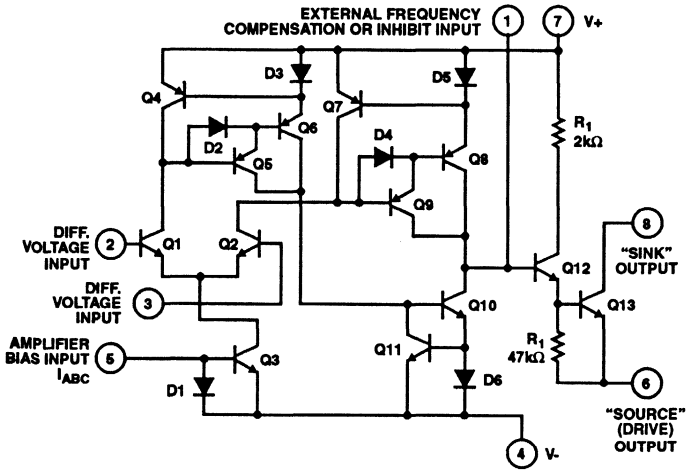
Electrical Specifications T_A = +25°C for Equipment Design. Single Supply V+ = 30V, Dual Supply V+ = 15V, V- = -15V, I_{ABC} = 100µA Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
INPUT PARAMETERS (Continued)						
1/F Noise Voltage	E_N	f = 10Hz, I_{ABC} = 50µA	-	18	-	$nV/\sqrt{Hz}$
1/F Noise Current	I_N	f = 10Hz, I_{ABC} = 50µA	-	1.8	-	$pA/\sqrt{Hz}$
Differential Input Resistance	R_I	I_{ABC} = 20µA	0.50	1.0	-	MΩ
Differential Input Capacitance	C_I	f = 1MHz, V+ = 30V	-	2.6	-	pF
OUTPUT PARAMETERS (Differential Input Voltage = 1V)						
Peak Output Voltage (Terminal 6)		V+ = 30V, R_L = 2kΩ to GND				
With Q13 "ON"	V+OM		26	27	-	V
With Q13 "OFF"	V-OM		-	0.01	0.05	V
Peak Output Voltage (Terminal 6)		V+ = 15V, V- = -15V, R_L = 2kΩ to -15V				
Positive	V+OM		11	12	-	V
Negative	V-OM		-	-14.99	-14.95	V
Peak Output Voltage (Terminal 8)		V+ = 30V, R_L = 2kΩ to 30V				
With Q13 "OFF"	V+OM		29.95	29.99	-	V
With Q13 "ON"	V-OM		-	0.040	-	V
Peak Output Voltage (Terminal 8)		V+ = 15V, V- = -15V, R_L = 2kΩ to 15V				
Positive	V+OM		14.95	14.99	-	V
Negative	V-OM		-	-14.96	-	V
Collector-to-Emitter Saturation Voltage (Terminal 8)	$V_{CE(SAT)}$	V+ = 30V, I_C = 50mA, Terminal 6 Grounded	-	0.17	0.80	V
Output Leakage Current (Terminal 6 to Terminal 4)		V+ = 30V	-	2	10	µA
Composite Small Signal Current Transfer Ratio (Beta) (Q12 and Q13)	h_{FE}	V+ = 30V, V_{CE} = 5V, I_C = 50mA	16,000	100,000	-	
Output Capacitance		f = 1MHz, All remaining Terminals Tied to Terminal 4				
Terminal 6	C_O		-	5.5	-	pF
Terminal 8	C_O		-	17	-	pF
TRANSFER PARAMETERS						
Voltage Gain	A	V+ = 30V, I_{ABC} = 100µA, ΔV_{OUT} = 20V, R_L = 2kΩ	20,000	100,000	-	V/V
			86	100	-	dB
Forward Transconductance to Terminal 1	g_M		1650	2200	2750	µmhos
Slew Rate (Open Loop)	SR	I_{ABC} = 500µA, R_L = 2kΩ				
Positive Slope			-	500	-	V/µs
Negative Slope			-	50	-	V/µs
Unity Gain (Non-Inverting Compensated)		I_{ABC} = 500µA, R_L = 2kΩ	-	0.70	-	V/µs

NOTE:

1. Exceeding this voltage rating will not damage the device unless the peak input signal current (1mA) is also exceeded.

Schematic Diagram



OUTPUT MODE	OUTPUT TERM	INPUTS	
		INV	NON-INV
"Source"	6	2	3
"Sink"	8	3	2

Typical Performance Curves

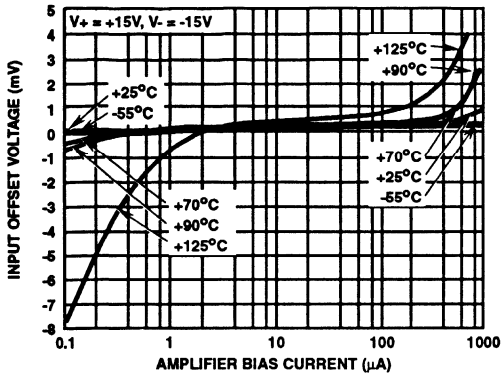


FIGURE 1. INPUT OFFSET VOLTAGE vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

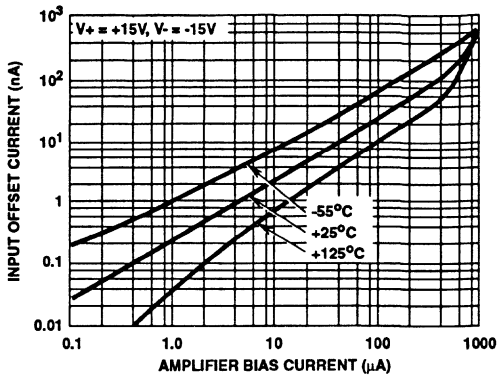


FIGURE 2. INPUT OFFSET CURRENT vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

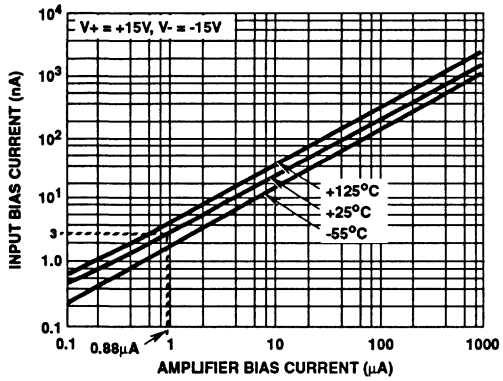


FIGURE 3. INPUT BIAS CURRENT vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

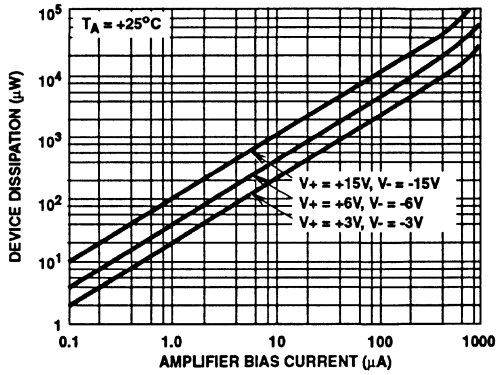


FIGURE 4. DEVICE DISSIPATION vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

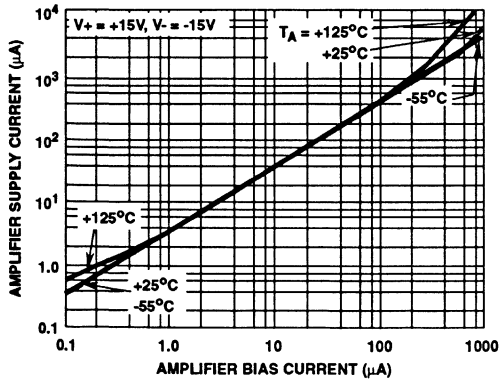


FIGURE 5. AMPLIFIER SUPPLY CURRENT vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

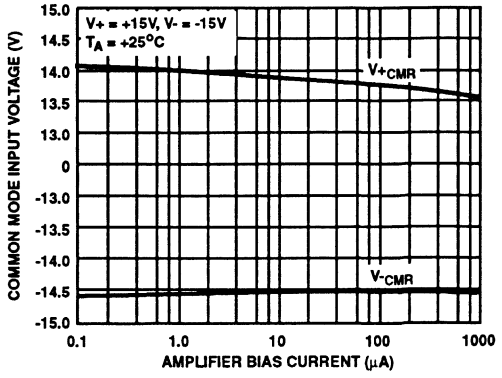


FIGURE 6. COMMON MODE INPUT VOLTAGE vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

Typical Performance Curves (Continued)

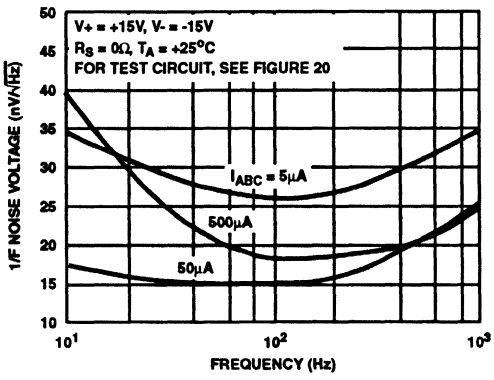


FIGURE 7. 1/F NOISE VOLTAGE vs FREQUENCY

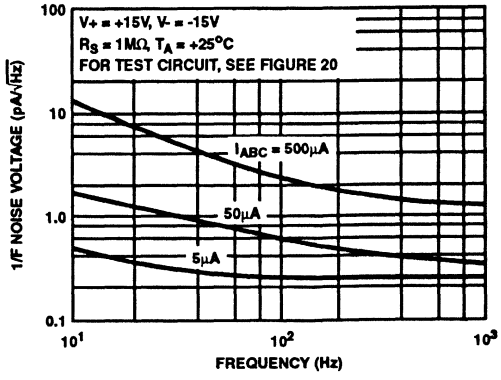


FIGURE 8. 1/F NOISE CURRENT vs FREQUENCY

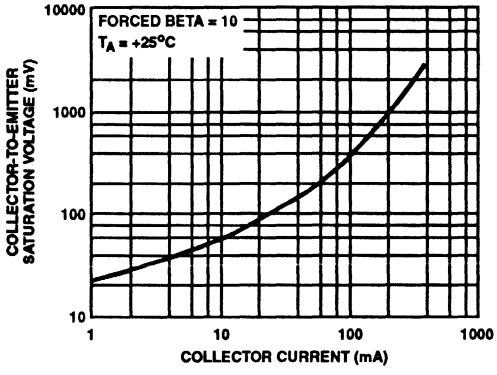


FIGURE 9. COLLECTOR EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT OF OUTPUT TRANSISTOR Q13

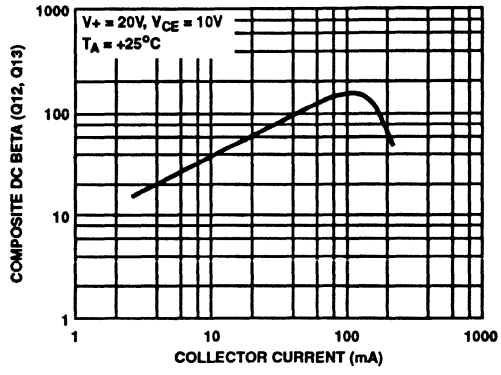


FIGURE 10. COMPOSITE DC BETA vs COLLECTOR CURRENT OF DARLINGTON CONNECTED OUTPUT TRANSISTORS (Q12, Q13)

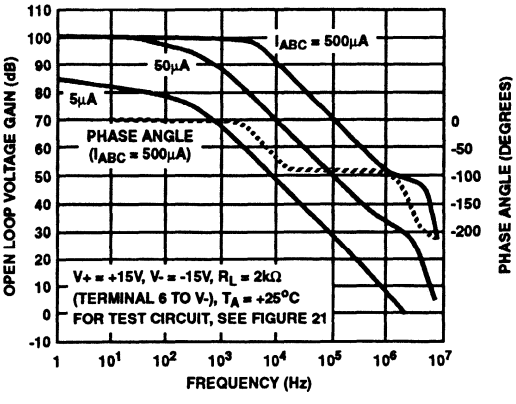


FIGURE 11. OPEN LOOP VOLTAGE GAIN vs FREQUENCY

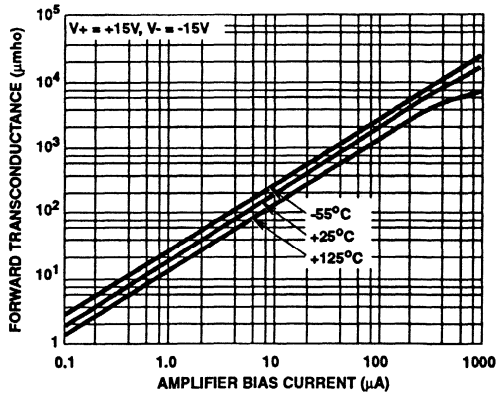


FIGURE 12. FORWARD TRANSCONDUCTANCE vs AMPLIFIER BIAS CURRENT

Typical Performance Curves (Continued)

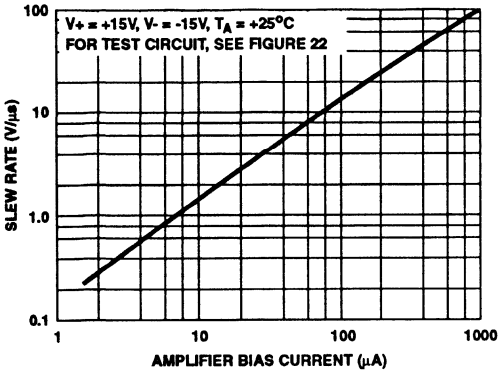


FIGURE 13. SLEW RATE vs AMPLIFIER BIAS CURRENT

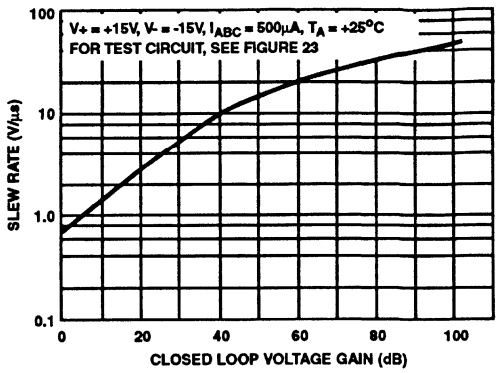


FIGURE 14. SLEW RATE vs CLOSED LOOP VOLTAGE GAIN

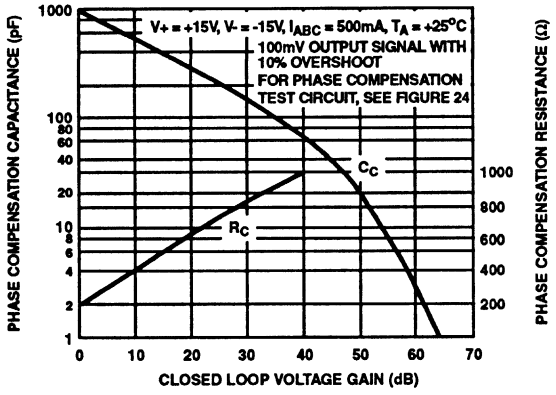


FIGURE 15. PHASE COMPENSATION CAPACITANCE AND RESISTANCE vs CLOSED LOOP VOLTAGE GAIN

Operating Considerations

The "Sink" Output (Terminal 8) and the "Drive" Output (Terminal 6) of the CA3094 are not inherently current (or power) limited. Therefore, if a load is connected between Terminal 6 and Terminal 4 (V- or Ground), it is important to connect a current limiting resistor between Terminal 8 and Terminal 7 (V+) to protect transistor Q13 under shorted load conditions. Similarly, if a load is connected between Terminal 8 and Terminal 7 (V+), the current limiting resistor should be connected between Terminal 6 and Terminal 4 or ground. In circuit applications where the emitter of the output transistor is not connected to the most negative potential in the system, it is recommended that a 100Ω current limiting resistor be inserted between Terminal 7 and the V+ supply.

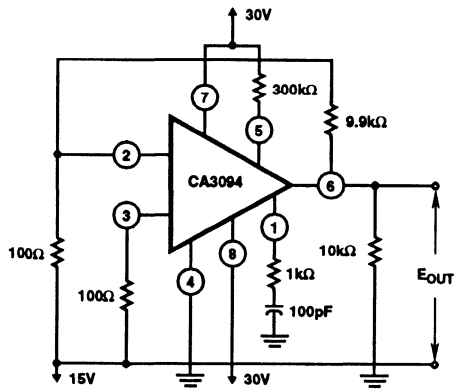
Test Circuits

1/F Noise Measurement Circuit

When using the CA3094, A, or B audio amplifier circuits, it is frequently necessary to consider the noise performance of the device. Noise measurements are made in the circuit shown in Figure 20. This circuit is a 30dB, non-inverting amplifier with emitter follower output and phase compensation from Terminal 2 to ground. Source resistors (R_S) are set to 0Ω or 1MΩ for E noise and I noise measurements, respectively. These measurements are made at frequencies of 10Hz, 100Hz and 1kHz with a 1Hz measurement bandwidth. Typical values for 1/f noise at 10Hz and 50μA I_{ABC} are

$E_N = 18nV/\sqrt{Hz}$ and $I_N = 1.8pA/\sqrt{Hz}$.

Test Circuits



NOTES:

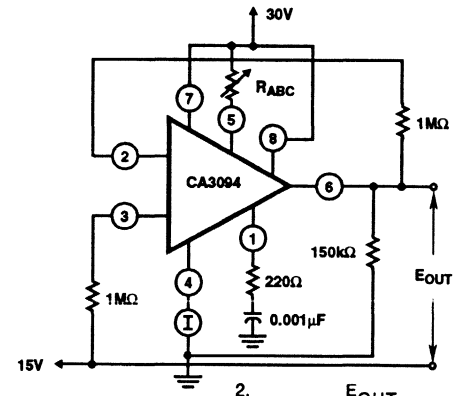
1. Input Offset Voltage: $V_{IO} = \frac{E_{OUT}}{100}$
2. For Power Supply Rejection Test: (1) vary V+ by -2V; then (2) vary V- by +2V
3. Equations:

   (1) V+ Rejection $= \frac{E_0OUT - E_1OUT}{200}$

   (2) V- Rejection $= \frac{E_0OUT - E_2OUT}{200}$
4. Power Supply Rejection: $(dB) = 20\log\frac{1}{V_{Rejection}*}$

* Maximum Reading of Step 1 or Step 2

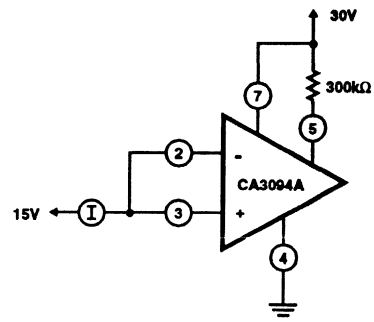
FIGURE 16. INPUT OFFSET VOLTAGE AND POWER SUPPLY REJECTION TEST CIRCUIT



NOTES:

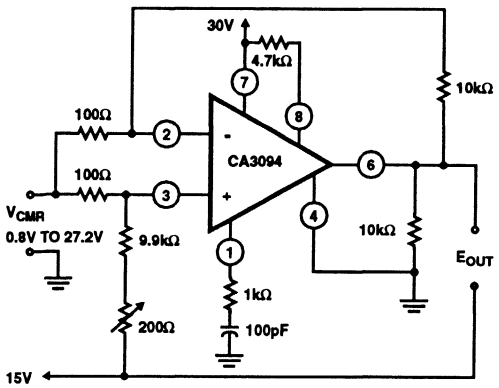
1. $P_{DISSIPATION} = (V+)(I)$
2. $I_{OS} = \frac{E_{OUT}}{10^6 \frac{VOLTS}{AMPS}}$

FIGURE 17. INPUT OFFSET CURRENT TEST CIRCUIT



NOTE: $I_I = \frac{I}{2}$

FIGURE 18. INPUT BIAS CURRENT TEST CIRCUIT

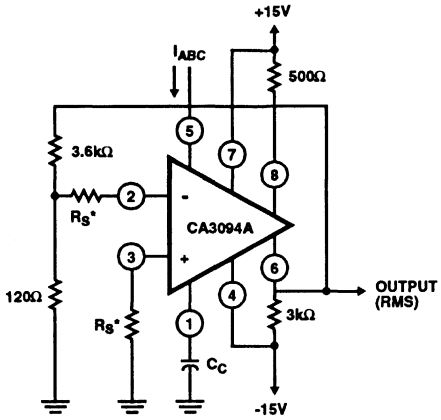


NOTES:

1. $CMRR = \left|\frac{100 \times 26V}{E_{2OUT} - E_{1OUT}}\right|$
2. Input Voltage Range for CMRR = 1V to 27V
3. $CMRR\ (dB) = 20\log\left|\frac{100 \times 26V}{E_{2OUT} - E_{1OUT}}\right|$

FIGURE 19. COMMON MODE RANGE AND REJECTION RATIO TEST CIRCUIT

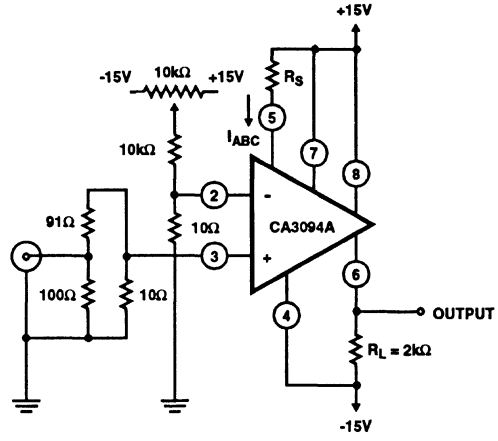
Test Circuits (Continued)



I_{ABC} (μA)	C_{COMP} (pF)
5	0
50	50
500	500

NOTES:
1. R_S* = 1MΩ (1/F Noise Current Test)
2. R_S = 0Ω (1/F Noise Voltage Test)

FIGURE 20. 1/F NOISE TEST CIRCUIT



R_S (Ω)	I_{ABC} (μA)
56K	500
560K	50
56M	5

FIGURE 21. OPEN LOOP GAIN vs FREQUENCY TEST CIRCUIT

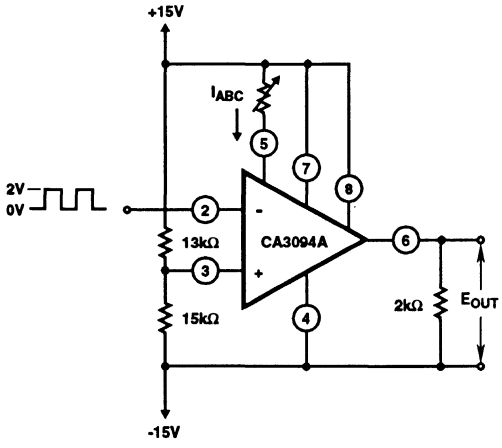


FIGURE 22. OPEN LOOP SLEW RATE vs I_{ABC} TEST CIRCUIT

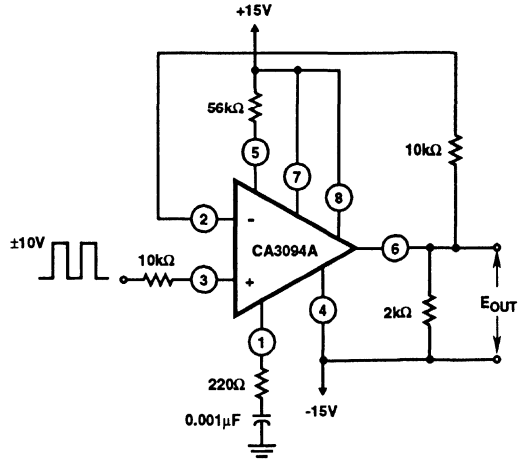
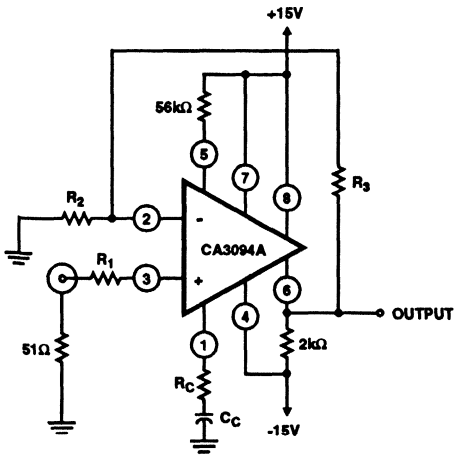


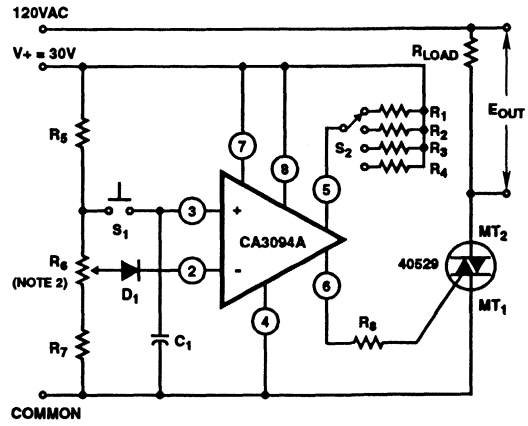
FIGURE 23. SLEW RATE vs NON-INVERTING UNITY GAIN TEST CIRCUIT

Test Circuits (Continued)



CLOSED LOOP GAIN (dB)	R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)
0	10	∞	10
20	10	1	10
40	1	0.1	10

FIGURE 24. PHASE COMPENSATION TEST CIRCUIT



NOTES:

1. $C_1 = 0.5\mu F$
   $D_1 = 1N914$
   $R_1 = 0.51M\Omega$ = 3 min.
   $R_2 = 5.1M\Omega$ = 30 min.
   $R_3 = 22M\Omega$ = 2 hrs.
   $R_4 = 44M\Omega$ = 4 hrs.
   $R_5 = 1.5k\Omega$
   $R_6 = 50k\Omega$
   $R_7 = 5.1k\Omega$
   $R_8 = 1.5k\Omega$
2. Potentiometer required for initial time set to permit device interconnecting. Time variation with temperature < 0.3%/°C.

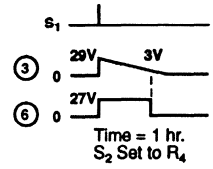


FIGURE 25. PRESETTABLE ANALOG TIMER

Typical Applications

For Additional Application Information, refer to Application Note ICAN-6048 "Some Applications of a Programmable Power/Switch Amplifier IC".

Design Considerations

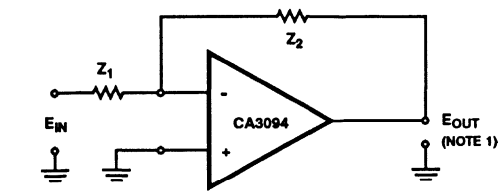
The selection of the optimum amplifier bias current (I_{ABC}) depends on:

1. The Desired Sensitivity - The higher the I_{ABC}, the higher the sensitivity, i.e., a greater drive current capability at the output for a specific voltage change at the input.
2. Required Input Resistance - The lower the I_{ABC}, the higher the input resistance.

If the desired sensitivity and required input resistance are not known and are to be experimentally determined, or the anticipated equipment design is sufficiently flexible to tolerate a wide range of these parameters, it is recommended that the equipment designer begin his calculations with an I_{ABC} of 100μA, since the CA3094 is characterized at this value of amplifier bias current.

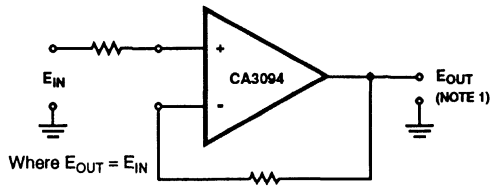
The CA3094 is extremely versatile and can be used in a wide variety of applications.

Typical Applications



Where $\frac{E_{OUT}}{E_{IN}} = f\left(\frac{Z_2}{Z_1}\right)$ depends on the characteristics of Z1 and Z2

(a)

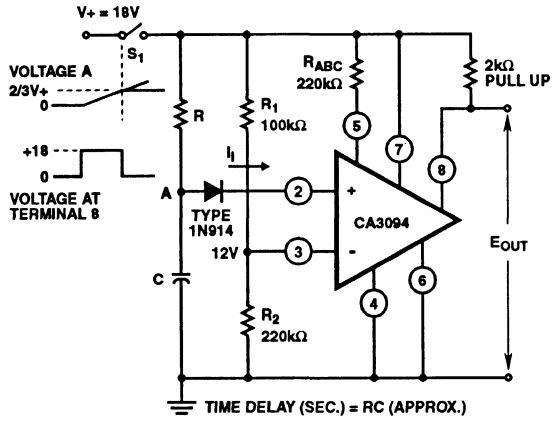


(b)

NOTE: 1. In single-ended output operation, the CA3094 may require a pull up or pull down resistor

FIGURE 26. APPLICATION OF THE CA3094: (a) AS AN INVERTING OP AMP AND (b) IN A NON-INVERTING MODE, AS A FOLLOWER

FIGURE 27. RC TIMER



Problem: To calculate the maximum value of R required to switch a 100mA output current comparator

Given: $I_{ABC} = 5\mu A$, $R_{ABC} = 3.6M\Omega \approx \frac{18V}{5\mu A}$

$I_I = 500nA$ at $I_{ABC} = 100\mu A$ (from Figure 3)

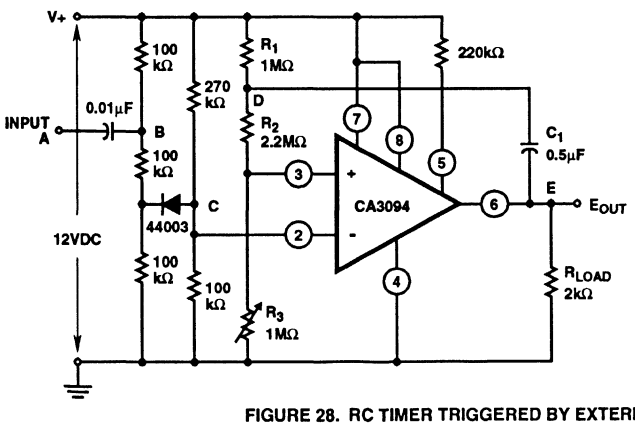
$I_I = 5\mu A$ can be determined by drawing a line on Figure 3 through $I_{ABC} = 100\mu A$ and $I_B = 500nA$ parallel to the typical $T_A = +25°C$ curve.

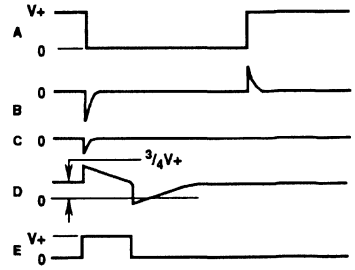
Then: $I_I = 33nA$ at $I_{ABC} = 5\mu A$

$$R_{MAX} = \frac{18V - 12V}{33nA} = 180M\Omega \text{ at } T_A = +25°C$$

$$R_{MAX} = 180M\Omega \times 2/3^* = 120M\Omega \text{ at } T_A = -55°C$$

* Ratio of I_I at $T_A = +25°C$ to I_I at $T_A = -55°C$ for any given value of I_{ABC}



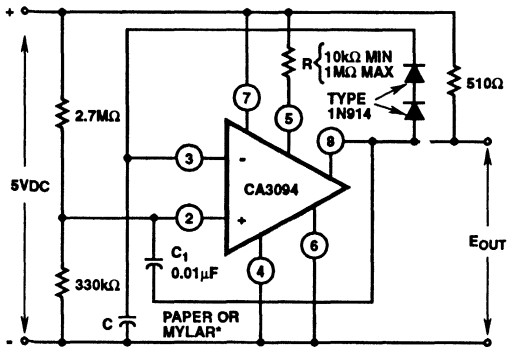


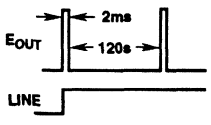
On a negative going transient at input (A), a negative pulse at C will turn "on" the CA3094, and the output (E) will go from a low to a high level.

At the end of the time constant determined by C1, R1, R2, R3, the CA3094 will return to the "off" state and the output will be pulled low by R_{LOAD}. This condition will be independent of the interval when input (A) returns to a high level.

FIGURE 28. RC TIMER TRIGGERED BY EXTERNAL NEGATIVE PULSE

Typical Applications (Continued)





NOTES:

1. R = 1MΩ, C = 1μF
2. Time Constant: t ≈ RC x 120
3. Pulse Width: ω ≈ K(C_1/C)

* Trademark E.I. Dupont de Nemours

FIGURE 29. FREE RUNNING PULSE GENERATOR

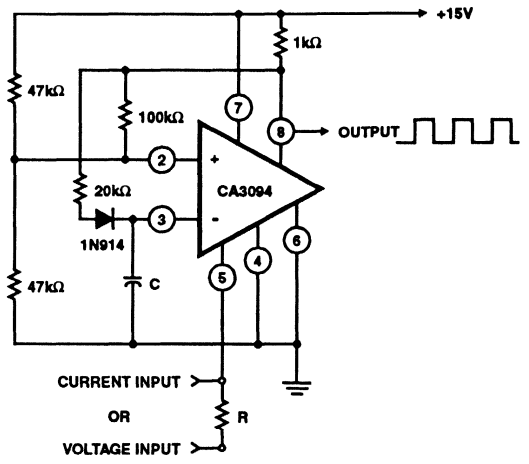


FIGURE 30. CURRENT OR VOLTAGE CONTROLLED OSCILLATOR

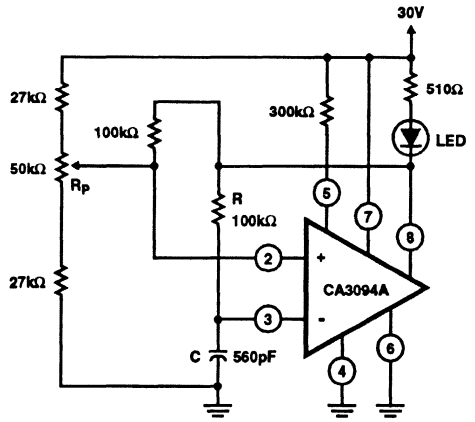
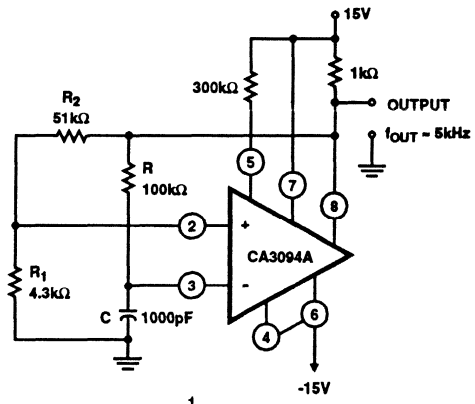


FIGURE 31. SINGLE SUPPLY ASTABLE MULTIVIBRATOR

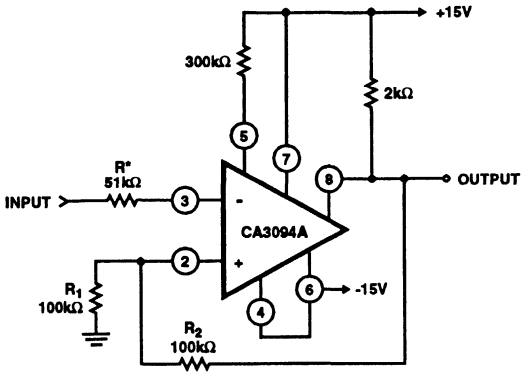


NOTE: $f_{OUT} = \frac{1}{2RC \ln\left(\frac{2R_1}{R_2} + 1\right)}$

If: $R_2 = 3.08R_1$, $f_{OUT} = \frac{1}{RC}$

FIGURE 32. DUAL SUPPLY ASTABLE MULTIVIBRATOR

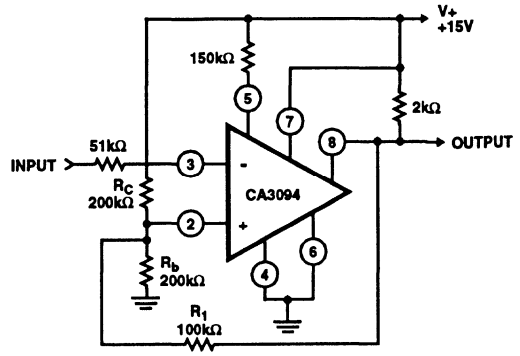
Typical Applications (Continued)



NOTES:

1. $R^* = \frac{R_1 R_2}{R_1 + R_2}$
2. $\pm\text{Threshold} = [\pm\text{Supply}]\left[\frac{R_1}{R_1 + R_2}\right]$

(a) Dual Supply

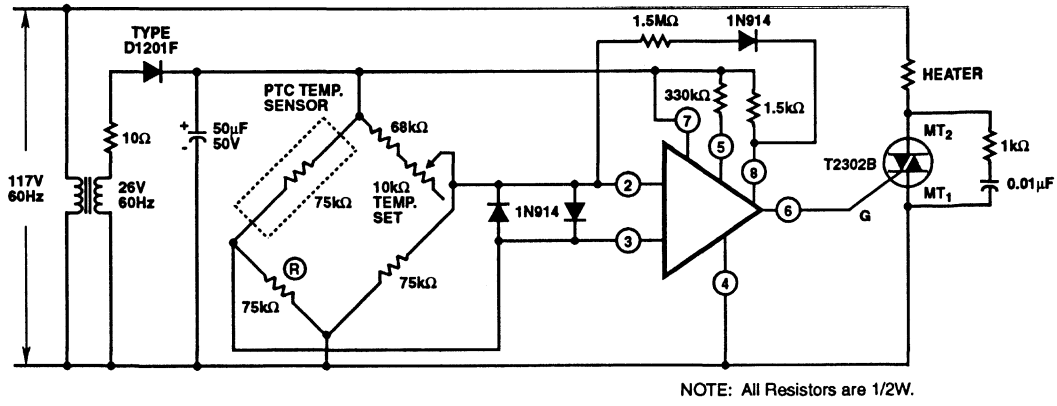


NOTES:

1. Upper Threshold $= [V+]\left[\frac{R_b}{\left(\frac{R_1 R_a}{R_1 + R_a}\right) + R_b}\right]$
2. Lower Threshold $= [V+]\left[\frac{\frac{R_1 R_b}{R_1 + R_b}}{\left(\frac{R_1 R_b}{R_1 + R_b}\right) + R_a}\right]$

(b) Single Supply

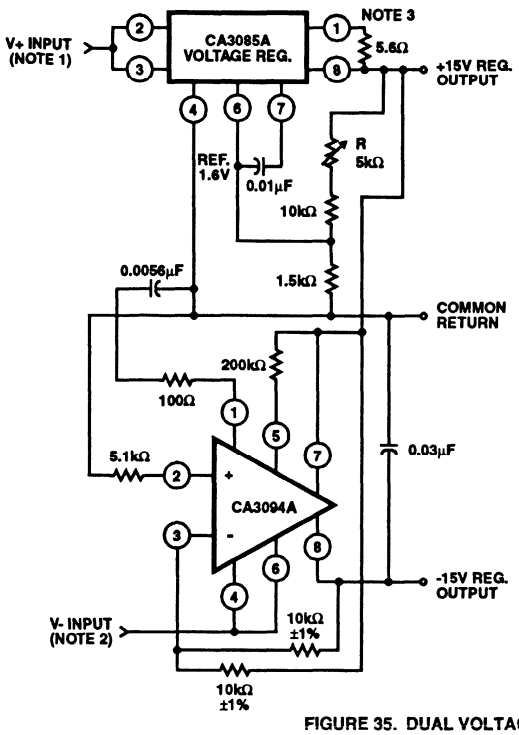
FIGURE 33. COMPARATORS (THRESHOLD DETECTORS) DUAL AND SINGLE SUPPLY TYPES



NOTE: All Resistors are 1/2W.

FIGURE 34. TEMPERATURE CONTROLLER

Typical Applications (Continued)



NOTES:

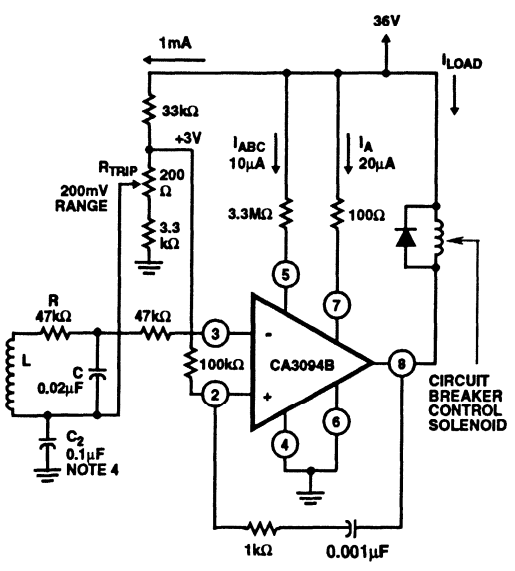
1. V+ Input Range = 19V to 30V for 15V output
2. V- Input Range = -16V to -30V for -15V output
3. Max I_{OUT} = ±100mA
4. Regulation:

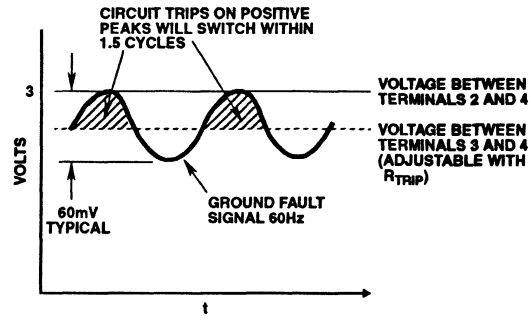
$$\text{Max Line} = \frac{\Delta V_{OUT}}{[V_{OUT}(\text{Initial})]\,\Delta V_{IN}} \times 100 = 0.075\%/V$$

$$\text{Max. Load} = \frac{\Delta V_{OUT}}{V_{OUT}(\text{Initial})} \times 100 = 0.075\%\ V_{OUT}$$

(IL from 1mA to 50mA)

FIGURE 35. DUAL VOLTAGE TRACKING REGULATOR



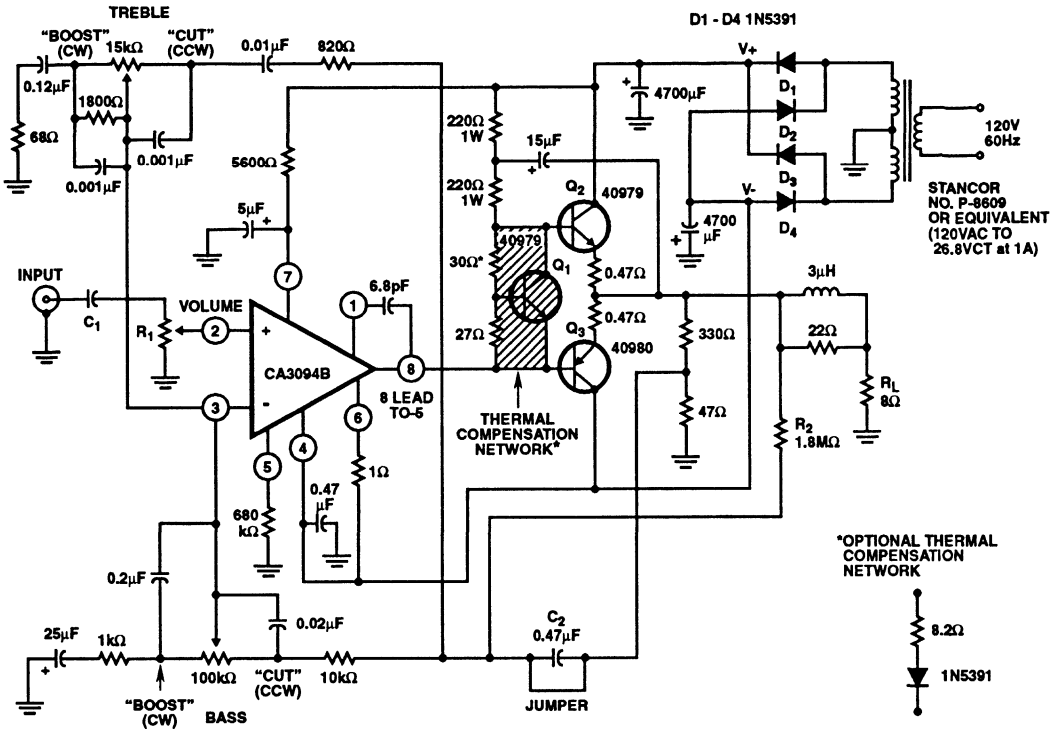


NOTES:

1. Differential current sensor provides 60mV signal = 5mA of unbalance (Trip) current
2. All Resistors are 1/2 Watt, ±10%
3. RC selected for 3dB point at 200Hz
4. C_2 = AC by-pass
5. Offset adj. included in R_{TRIP}
6. Input impedance from 2 to 3 = 800kΩ
7. With no input signal Terminal 8 (output) at 36V

FIGURE 36. GROUND FAULT INTERRUPTER (GFI) AND WAVEFORMS PERTINENT TO GROUND FAULT DETECTOR

Typical Applications (Continued)



TYPICAL PERFORMANCE DATA
For 12W Audio Amplifier Circuit

Power Output (8Ω load, Tone Control set at "Flat")	
Music (at 5% THD, regulated supply)	15W
Continuous (at 0.2% IMD, 60Hz and 2kHz mixed in a 4:1 ratio, unregulated supply) See Figure 8 in AN6048	12W
Total Harmonic Distortion	
At 1W, unregulated supply	0.05%
At 12W, unregulated supply	0.57%
Voltage Gain	40dB
Hum and Noise (below continuous power output)	83dB
Input Resistance	250kΩ
Tone Control Range	See Figure 9 in AN6048

NOTES:

1. For standard input: Short C_2; $R_1 = 250k\Omega$, $C_1 = 0.047\mu F$; remove R_2
2. For ceramic cartridge input: $C_1 = 0.0047\mu F$, $R_1 = 2.5M\Omega$, remove jumper from C_2; leave R_2

FIGURE 37. 12W AUDIO AMPLIFIER CIRCUIT FEATURING TRUE COMPLEMENTARY SYMMETRY OUTPUT STAGE WITH CA3094 IN DRIVER STAGE

HARRIS SEMICONDUCTOR

CA3100

March 1993

Wideband Operational Amplifier

Features

- High Open Loop Gain at Video Frequencies ..... 42dB (Typ.) at 1MHz
- High Unity Gain Crossover Frequency (f_T) ..... 38MHz (Typ.)
- Wide Power Bandwidth V_O = 18Vp-p ..... 1.2MHz(Typ.)
- High Slew Rate
  - 20dB Amplifier ..... 70V/μs (Typ.)
  - Unity Gain Amplifier..... 25V/μs (Typ.)
- Fast Settling Time ..... 0.6μs (Typ.)
- High Output Current..... ±15mA Min.
- Single Capacitor Compensation
- Offset Null Terminals

Applications

- Video Amplifiers
- Fast Peak Detectors
- Meter Driver Amplifiers
- High Frequency Feedback Amplifiers
- Video Pre-Drivers
- Oscillators
- Multivibrators
- Voltage Controlled Oscillator
- Fast Comparators

Description

The CA3100 is a large signal wideband, high speed operational amplifier which has a unity gain cross over frequency (f_T) of approximately 38MHz and an open loop, 3dB corner frequency of approximately 110kHz. It can operate at a total supply voltage of from 14V to 36V (±7V to ±18V when using split supplies) and can provide at least $18V_{P-P}$ and $30mA_{P-P}$ at the output when operating from ±15V supplies. The CA3100 can be compensated with a single external capacitor and has DC offset adjust terminals for those applications requiring offset null. (See Figure 14).

The CA3100 circuit contains both bipolar and PMOS transistors on a single monolithic chip..

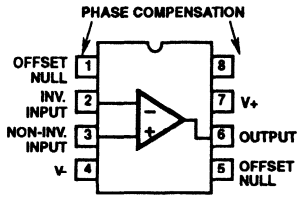
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3100E	-45°C to +85°C	8 Lead Plastic DIP
CA3100M	-45°C to +85°C	8 Lead SOIC
CA3100M96	-45°C to +85°C	8 Lead SOIC*
CA3100T	-55°C to +125°C	8 Pin Can

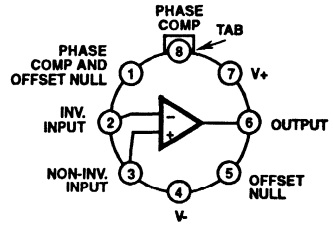
* Denotes Tape and Reel

Pinouts

CA3100
(PDIP, SOIC)
TOP VIEW



CA3100
(CAN)
TOP VIEW



File Number 625.2

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 36V
Differential Input Voltage 12V
Input Voltage to Ground (Note 1) . . . . . ±15V
Offset Terminal to V- Terminal Voltage . . . . . ±0.5V
Output Current (Note 2) 50mA
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Operating Temperature Range:
E and M Types . . . . . -40°C to +85°C
S and T Types . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications, at T_A = +25°C, Supply Voltage (V+, V-) = ±15V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
STATIC						
Input Offset Voltage	V_{IO}	V_O = 0 ± 0.1V	-	±1	±5	mV
Input Bias Current	I_{IB}	V_O = 0 ± 1V	-	0.7	2	µA
Input Offset Current	I_{IO}	V_O = 0 ± 1V	-	±0.05	±0.4	µA
Low Frequency Open Loop Voltage Gain (Note 3)	A_{OL}	V_O = ± 1V Peak, f = 1 kHz	56	61	-	dB
Common Mode Input Voltage Range	V_{ICR}	CMRR ≥ 76dB	±12	+14 -13	-	V
Common Mode Rejection Ratio	CMRR	V_I Common Mode = ± 12V	76	90	-	dB
Maximum Output Voltage Positive	V_{OM+}	Differential Input Voltage = 0 ± 0.1V, R_L = 2kΩ	+9	+11	-	V
Negative	V_{OM-}		-9	-11	-	V
Maximum Output Current Positive	I_{OM+}	Differential Input Voltage = 0 + 0.1V, R_L = 250Ω	+15	+30	-	mA
Negative	I_{OM-}		-15	-30	-	mA
Supply Current	I+	V_O = 0 ± 0.1V, R_L ≥ 10kΩ	-	8.5	10.5	mA
Power Supply Rejection Ratio	PSRR	ΔV+ = ± 1V, ΔV- = ± 1V	60	70	-	dB
DYNAMIC						
Unity-Gain Crossover Frequency	f_T	C_C = 0, V_O = 0.3V_{P-P}	-	38	-	MHz
1MHz Open-Loop Voltage Gain	A_{OL}	f = 1MHz, C_C = 0, V_O = 10V_{P-P}	36	42	-	dB
Slew Rate 20dB Amplifier	SR	A_V = 10, C_C = 0, V_I = 1V (Pulse)	50	70	-	V/µs
Follower Mode		A_V = 1, C_C = 10pF, V_I = 10V (Pulse)	-	25	-	V/µs
Power Bandwidth (Note 4) 20dB Amplifier	PBW	A_V = 10, C_C = 0, V_O = 18V_{P-P}	0.8	1.2	-	MHz
Follower Mode		A_V = 1, C_C = 10pF, V_O = 18V_{P-P}	-	0.4	-	MHz
Open Loop Differential Input Impedance	Z_I	F = 1MHz	-	30	-	kΩ
Open-Loop Output Impedance	Z_O	F = 1MHz	-	110	-	Ω

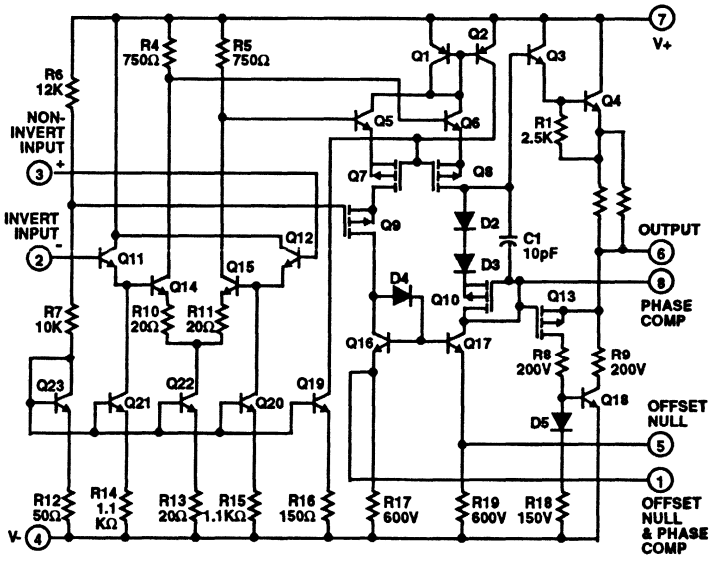
Electrical Specifications, at T_A = +25°C, Supply Voltage (V+, V-) = ±15V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
DYNAMIC (Continued)						
Wideband Noise Voltage Referred to Input	e_N (Total)	BW = 1MHz, R_S = 1kΩ	-	8	-	μV_{RMS}
Settling Time (To Within ±50 mV of 9V Output Swing)	t_S	R_L = 2kΩ, C_L = 20pF	-	0.6	-	µs

NOTES:

1. If the supply voltage is less than ± 15V, the maximum input voltage to ground is equal to the supply voltage.
2. CA3100 does not contain circuitry to protect against short circuits in the output.
3. Low frequency dynamic characteristic.
4. Power Bandwidth = $\frac{\text{Slew Rate}}{\pi V_{OP-P}}$

Schematic Diagram



Typical Performance Curves

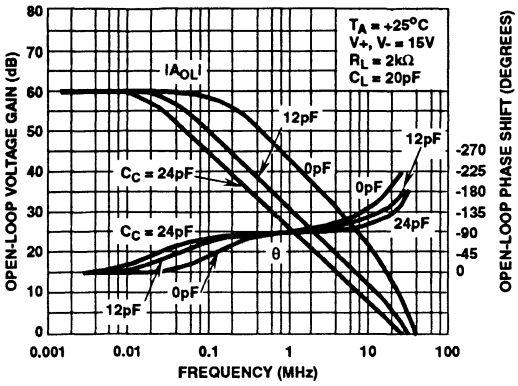


FIGURE 1. OPEN-LOOP GAIN, OPEN-LOOP PHASE SHIFT vs FREQUENCY

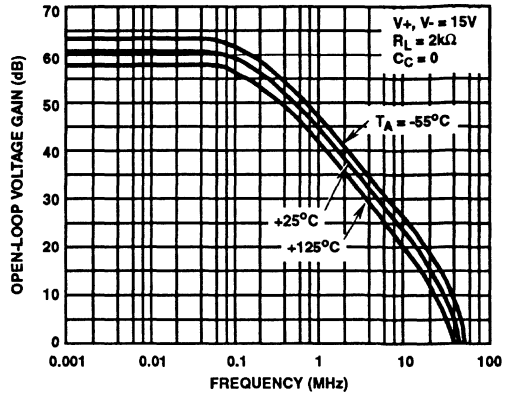


FIGURE 2. OPEN-LOOP GAIN vs FREQUENCY

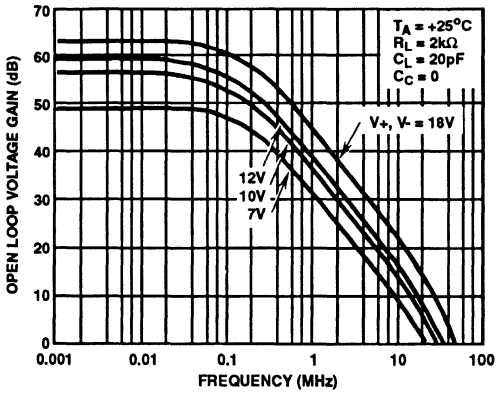


FIGURE 3. OPEN LOOP GAIN vs FREQUENCY

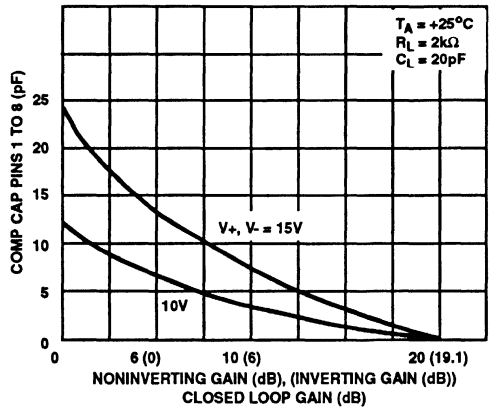


FIGURE 4. REQUIRED COMPENSATION CAPACITANCE vs CLOSED LOOP GAIN

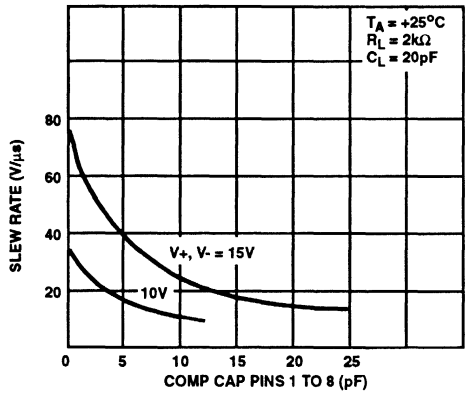


FIGURE 5. SLEW RATE vs COMPENSATION CAPACITANCE

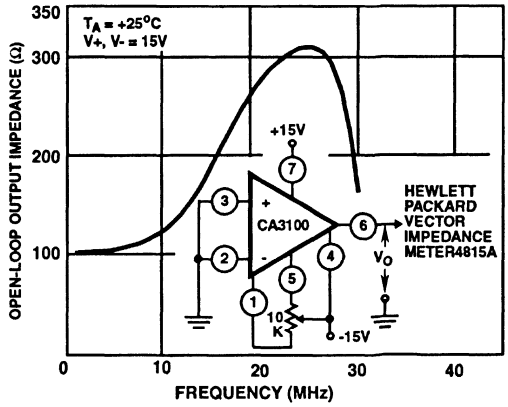


FIGURE 6. TYPICAL OPEN LOOP OUTPUT IMPEDANCE vs FREQUENCY

Typical Performance Curves (Continued)

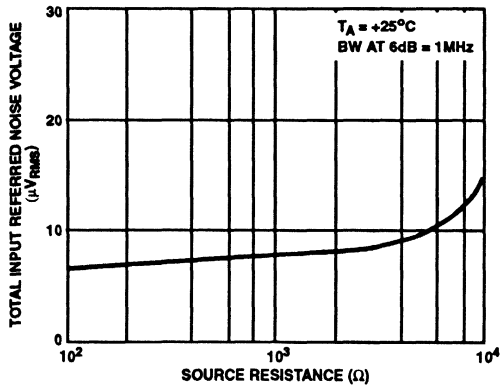


FIGURE 7. WIDEBAND INPUT NOISE VOLTAGE vs SOURCE RESISTANCE

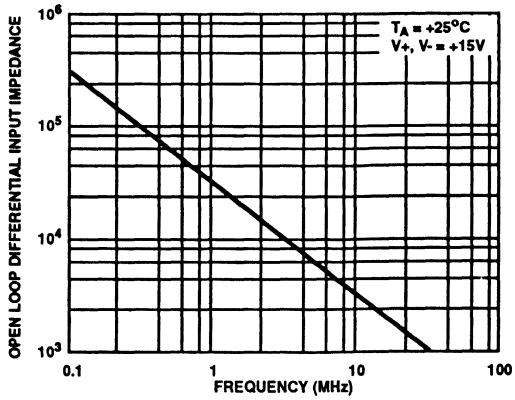


FIGURE 8. TYPICAL OPEN-LOOP DIFFERENTIAL INPUT IMPEDANCE vs FREQUENCY

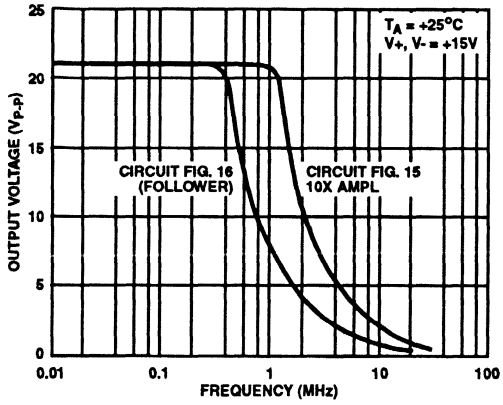


FIGURE 9. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

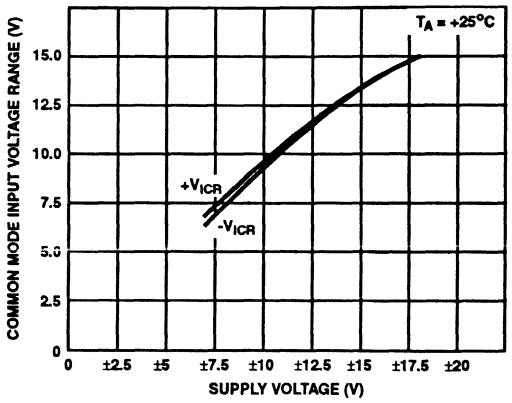


FIGURE 10. COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

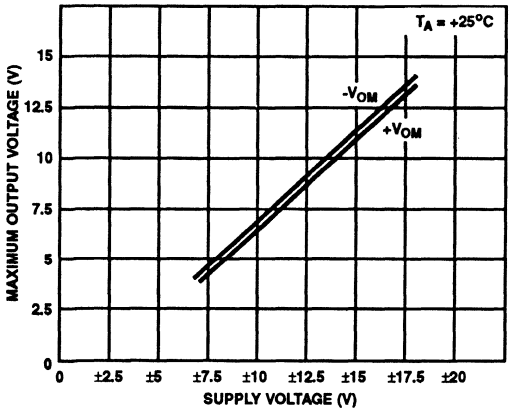


FIGURE 11. MAXIMUM OUTPUT VOLTAGE vs SUPPLY VOLTAGE

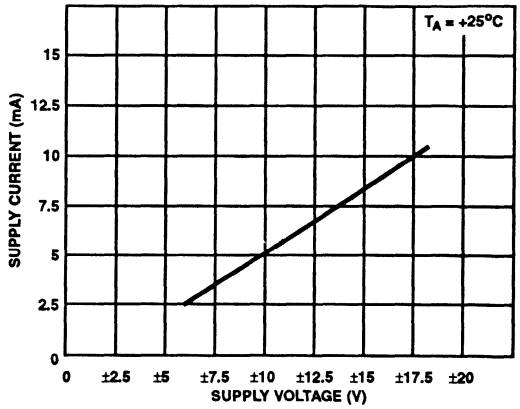


FIGURE 12. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

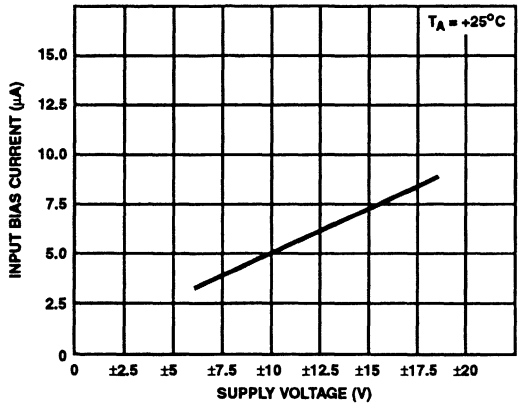


FIGURE 13. INPUT BIAS CURRENT vs SUPPLY VOLTAGE

Test Circuits

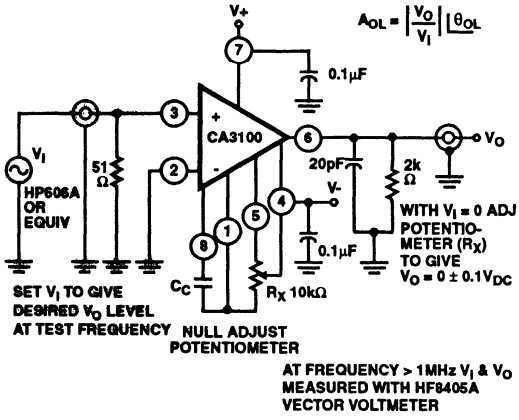


FIGURE 14. OPEN-LOOP VOLTAGE GAIN TEST CIRCUIT AND OFFSET ADJUST CIRCUIT

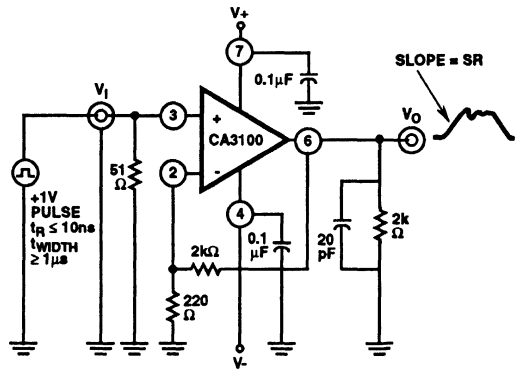


FIGURE 15. SLEW RATE IN 10X AMPLIFIER TEST CIRCUIT

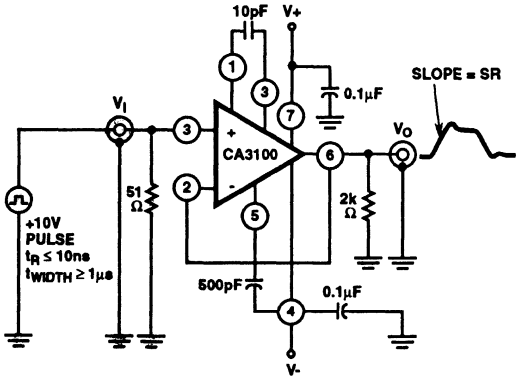


FIGURE 16. FOLLOWER SLEW RATE TEST CIRCUIT

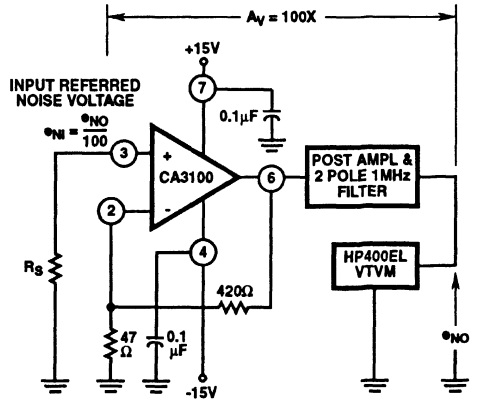


FIGURE 17. WIDEBAND INPUT NOISE VOLTAGE TEST CIRCUIT

Test Circuits (Continued)

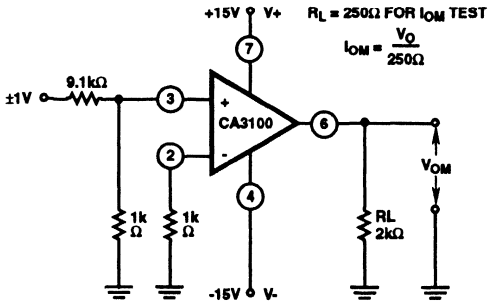


FIGURE 18. OUTPUT VOLTAGE SWING (V_{OM}), OUTPUT CURRENT SWING (I_{OM}) TEST CIRCUIT

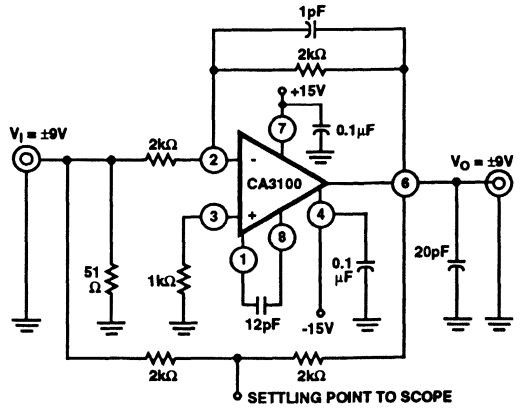


FIGURE 19. SETTLING TIME TEST CIRCUIT

Typical Applications

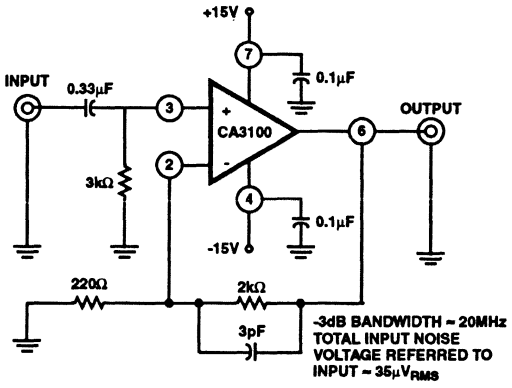


FIGURE 20. 20dB VIDEO AMPLIFIER

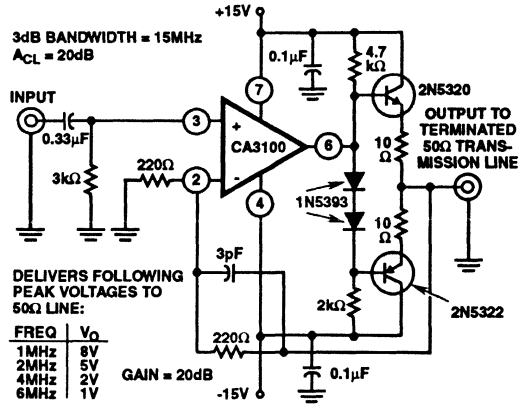


FIGURE 21. 20dB VIDEO LINE DRIVER

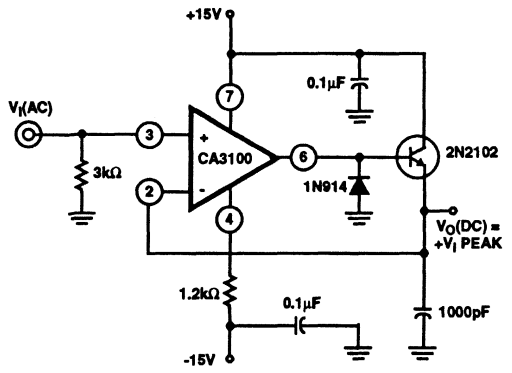


FIGURE 22. FAST POSITIVE PEAK DETECTOR

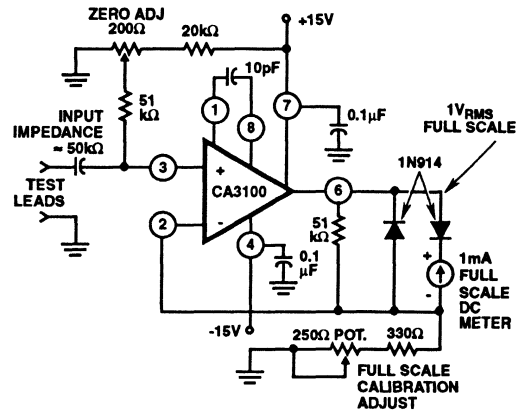


FIGURE 23. 1MHz METER-DRIVER AMPLIFIER

HARRIS SEMICONDUCTOR

CA3130

BiMOS Operational Amplifier with MOSFET Input/CMOS Output

April 1993

Features

- MOSFET Input Stage Provides:
  - Very High Z_I = 1.5 TΩ (1.5 x 10^{12}Ω) Typ.
  - Very Low I_I = 5pA Typ. at 15V Operation
    = 2pA Typ. at 5V Operation
- Ideal for Single-Supply Applications
- Common-Mode Input-Voltage Range Includes Negative Supply Rail; Input Terminals can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or both) Supply Rails

Applications

- Ground-Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long-Duration Timers/Monostables
- High-Input-Impedance Comparators (Ideal Interface with Digital CMOS)
- High-Input-Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single-Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to Zero Volts)
- Peak Detectors
- Single-Supply Full-Wave Precision Rectifiers
- Photo-Diode Sensor Amplifiers

Description

CA3130A and CA3130 are integrated-circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

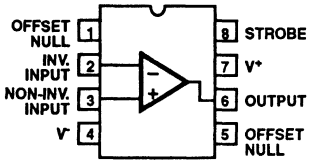
A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions can also made to permit strobing of the output stage.

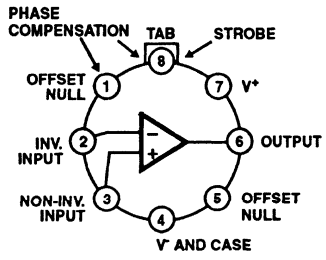
The CA3130A offers superior input characteristics over those of the CA3130.

Pinouts

CA3130, CA3130A
(PDIP, SOIC)
TOP VIEW



CA3130, CA3130A
(CAN)
TOP VIEW



Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
CA3130AE	-55°C to +125°C	8 Lead PDIP
CA3130AM	-55°C to +125°C	8 Lead SOIC
CA3130AM96	-55°C to +125°C	8 Lead SOIC*
CA3130AT	-55°C to +125°C	8 Pin CAN
CA3130BT	-55°C to +125°C	8 Pin CAN
CA3130E	-55°C to +125°C	8 Lead PDIP
CA3130M	-55°C to +125°C	8 Lead SOIC
CA3130M96	-55°C to +125°C	8 Lead SOIC*
CA3130T	-55°C to +125°C	8 Pin CAN

* Denotes Tape and Reel

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **817.2**

Absolute Maximum Ratings

DC Supply Voltage (Between V^+ And V^- Terminals) 16V
Differential-Mode Input Voltage 8V
DC Input Voltage ..... (V^+ +8 V) to (V^- -0.5V)
Input-Terminal Current 1mA
Device Dissipation:
  Without Heat Sink-
    Up To 55°C ..... 630 mW
    Above 55°C ..... Derate Linearly 6.67 mW/°C
  With Heat Sink-
    Up To 90°C 1W
    Above 90°C ..... Derate Linearly 16.7 mW/°C.
Output Short-Circuit Duration (Note 1) ..... Indefinite
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range (All Types) ..... -55°C to +125°C
Storage Temperature Range(All Types) ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, V+ = 15V, V- = 0V (Unless Otherwise Specified)

PARAMETERS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS
			CA3130A			CA3130			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$\|V_{IO}\|$	V± = ±7.5V	-	2	5	-	8	15	mV
Input Offset Current	$\|I_{IO}\|$	V± = ±7.5V	-	0.5	20	-	0.5	30	pA
Input Current	I_I	V± = ±7.5V	-	5	30	-	5	50	pA
Large-Signal Voltage Gain	A_{OL}	V_O = 10 Vp-p, R_L = 2kΩ	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common-Mode Rejection Ratio	CMRR		80	90	-	70	90	-	dB
Common-Mode Input Voltage Range	V_{ICR}		0	-0.5 to 12	10	0	-0.5 to 12	10	V
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V\pm$	V± = ±7.5V	-	32	150	-	32	320	µV/V
Maximum Output Voltage	$V_{OM}+$	At R_L = 2kΩ	12	13.3	-	12	13.3	-	V
	$V_{OM}-$	At R_L = 2kΩ	-	0.002	0.01	-	0.002	0.01	V
	$V_{OM}+$	At R_L = 2kΩ	14.99	15	-	14.99	15	-	V
	$V_{OM}-$	At R_L = 2kΩ	-	0	0.01	-	0	0.01	V
Maximum Output Current	$I_{OM}+$ (Source) at V_O = 0V		12	22	45	12	22	45	mA
	$I_{OM}-$ (Sink) at V_O = 15V		12	20	45	12	20	45	mA
Supply Current	I+	V_O = 7.5V, R_L = ∞	-	10	15	-	10	15	mA
	I+	V_O = 0V, R_L = ∞	-	2	3	-	2	3	mA
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	10	-	-	10	-	µV/°C

NOTE:
1. Short circuit may be applied to ground or to either supply.

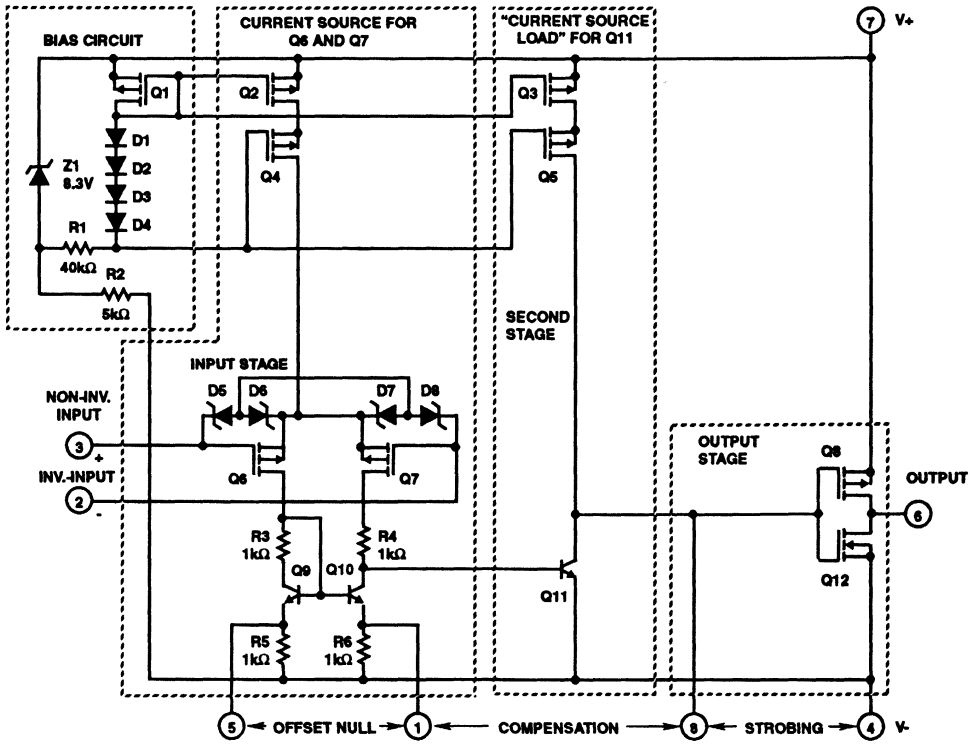
Electrical Specifications Typical Values Intended Only for Design Guidance, V+ = +7.5V, V- = -7.5V, T_A = +25°C (Unless Otherwise Specified)

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3130A, CA3130	UNITS
Input Offset Voltage Adjustment Range		10kΩ Across Terms. 4 and 5 or 4 and 1	±22	mV
Input Resistance	R_I		1.5	TΩ
Input Capacitance	C_I	f = 1MHz	4.3	pF
Equivalent Input Noise Voltage	e_N	BW = 0.2MHz, R_S = 1MΩ*	23	μV
Unity Gain Crossover Frequency	f_T	C_C = 0	15	MHz
		C_C = 47pF	4	MHz
Slew Rate:	SR			
Open Loop		C_C = 0	30	V/μs
Closed Loop		C_C = 56pF	10	V/μs
Transient Response:		C_C = 56pF, C_L = 25pF, R_L = 2kW (Voltage Follower)		
Rise Time	t_R		0.09	μs
Overshoot	OS		10	%
Settling Time (To <0.1%, V_{IN} = $4V_{P-P}$)	t_S		1.2	μs

* Although a 1MΩ source is used for this test, the equivalent input noise remains constant for values of R_S up to 10MΩ.

Electrical Specifications Typical Values Intended Only for Design Guidance, V+ = 5V, V- = 0V, T_A = +25°C (Unless Otherwise Specified)

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3130A	CA3130	UNITS
Input Offset Voltage	V_{IO}		2	8	mV
Input Offset Current	I_{IO}		0.1	0.1	pA
Input Current	I_I		2	2	pA
Common-Mode Rejection Ratio	CMRR		90	80	dB
Large-Signal Voltage Gain	A_{OL}	V_O = $4V_{P-P}$, R_L = 5kW	100	100	kV/V
			100	100	dB
Common-Mode Input Voltage Range	V_{ICR}		0 to 2.8	0 to 2.8	V
Supply Current	I+	V_O = 5V, R_L = ∞	300	300	μA
		V_O = 2.5V, R_L = ∞	500	500	μA
Power Supply Rejection Ratio	$\Delta V_{IO}/\Delta V+$		200	200	μV/V



NOTE: DIODES D5 THROUGH D8 PROVIDE GATE-OXIDE PROTECTION FOR MOSFET INPUT STAGE

FIGURE 1. SCHEMATIC DIAGRAM OF THE CA3130 SERIES

Circuit Description

Figure 2 is a block diagram of the CA3130 Series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Figure 2, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g.,when the amplifier output is used to drive CMOS digital circuits in Comparator applications).

Input Stages

The circuit of the CA3130 is shown in Figure 1. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000Ω potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascade-connected PMOS transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, including static electricity during handling for Q6 and Q7.

Second-Stage

Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascade-connected load resistance provided by

PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit

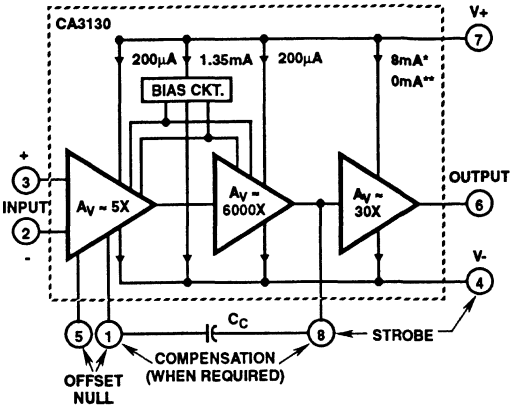
At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"* to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes nonconductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage

The output stage consists of a drain-loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Figure 5. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 percent accuracy levels, including the negative supply rail.

* For general information on the characteristics of CMOS transistor-pairs in linear-circuit applications, see File Number 619, data bulletin on CA3600E "CMOS Transistor Array".

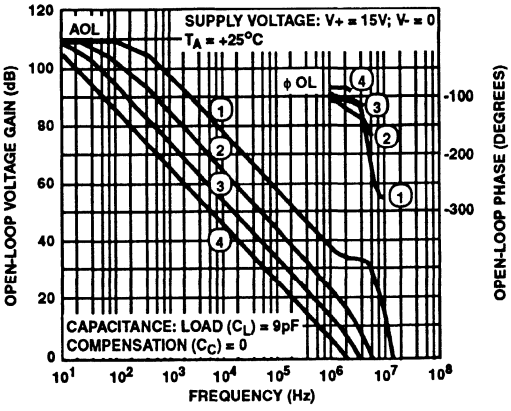


TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15V

*WITH INPUT TERMINALS BIASED SO THAT TERM. 6 POTENTIAL IS +7.5V ABOVE TERM. 4.

**WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.

FIGURE 2. BLOCK DIAGRAM OF THE CA3130 SERIES



1 = LOAD RESISTANCE (R_L) = ∞

2 = C_L = 30pF, C_C = 15pF, R_L = 2kΩ

3 = C_L = 30pF, C_C = 47pF, R_L = 2kΩ

4 = C_L = 30pF, C_C = 150pF, R_L = 2kΩ

FIGURE 3. OPEN-LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY

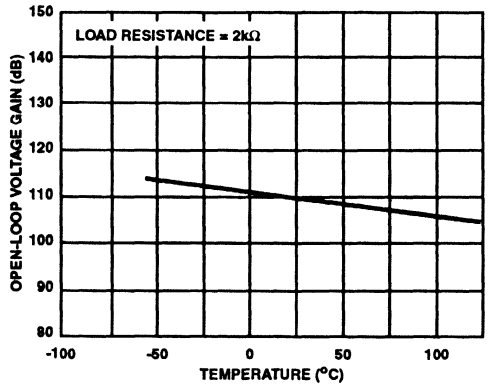


FIGURE 4. OPEN-LOOP GAIN vs TEMPERATURE

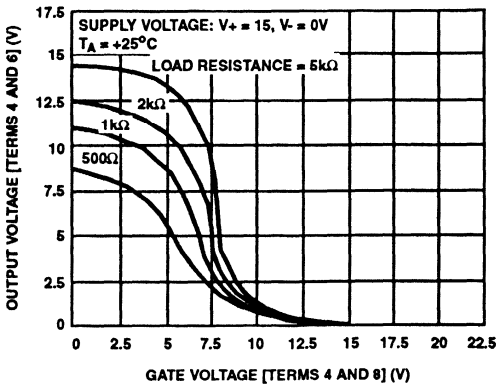


FIGURE 5. VOLTAGE TRANSFER CHARACTERISTICS OF CMOS OUTPUT STAGE

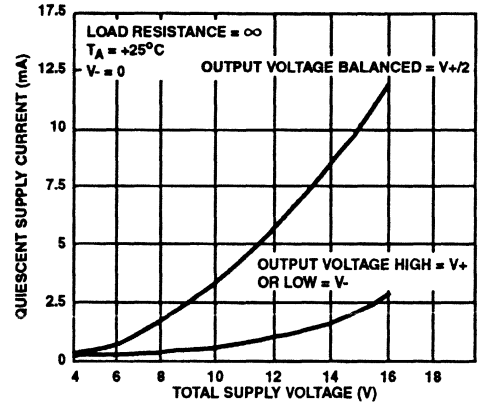


FIGURE 6. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

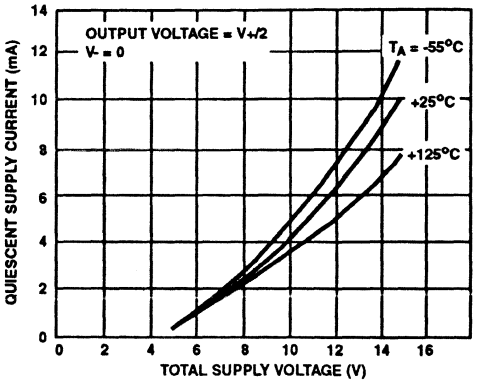


FIGURE 7. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

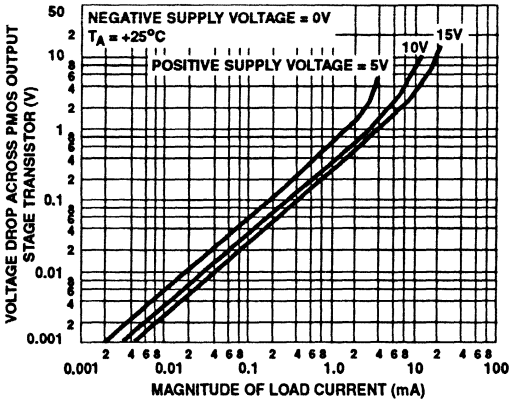


FIGURE 8. VOLTAGE ACROSS PMOS OUTPUT TRANSISTOR (Q8) vs LOAD CURRENT

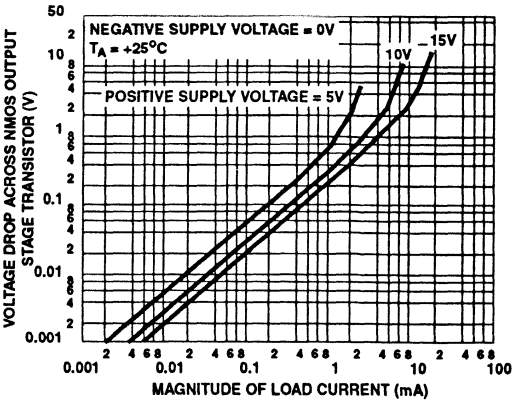


FIGURE 9. VOLTAGE ACROSS NMOS OUTPUT TRANSISTOR (Q12) vs LOAD CURRENT

Input Current Variation with Common Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3130 Series Op-Amps is typically 5pA at T_A = +25°C when terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Figure 10 contains data showing the variation of input current as a function of common-mode input voltage at T_A = +25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3130 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

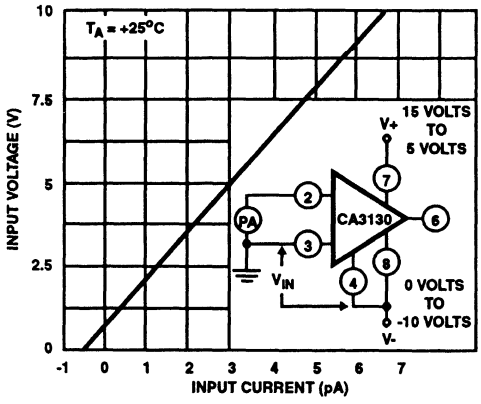


FIGURE 10. INPUT CURRENT vs COMMON-MODE VOLTAGE

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5pA at +25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op-amps with a junction-FET input stage, the leakage current approximately doubles for every +10°C increase in temperature. Figure 11 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

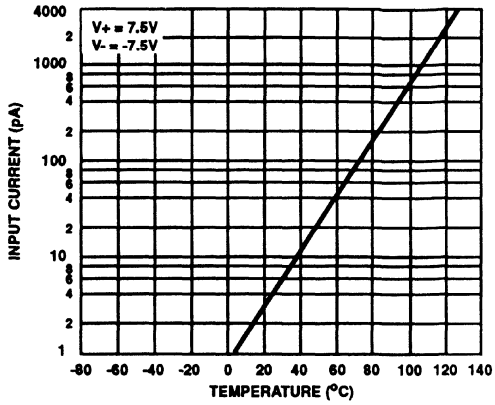


FIGURE 11. INPUT CURRENT vs AMBIENT TEMPERATURE

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs Device Operating Life

It is well known that the characteristics of a MOSFET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terms. 2 and 3. Figure 12 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices (TO-5 package) during life testing. At lower temperatures (TO-5 and plastic), for example at +85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

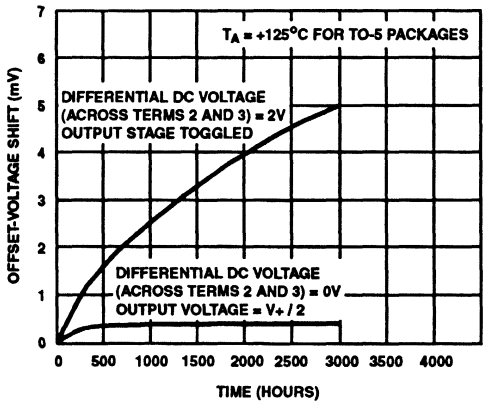
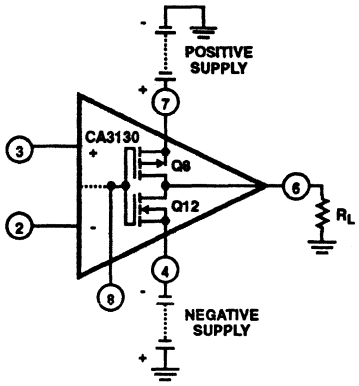
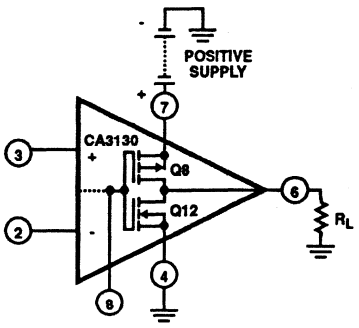


FIGURE 12. TYPICAL INCREMENTAL OFFSET-VOLTAGE SHIFT vs OPERATING LIFE



(A) DUAL POWER-SUPPLY OPERATION



(B) SINGLE POWER-SUPPLY OPERATION

FIGURE 13. CA3130 OUTPUT STAGE IN DUAL AND SINGLE POWER-SUPPLY OPERATION

Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single-and dual-supply service. Figures 13A and 13B show the CA3130 connected for both dual-and single-supply operation.

Dual-supply Operation: When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply Operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Figure 6 shows typical quiescent supply-current vs supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Figure 5). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Figure 6) even though the output stage is strobed off. Figure 13A shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$ by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Figure 13B. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Figure 8 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply voltages. Figure 5 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is on the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 23μV when the

test-circuit amplifier of Figure 14 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

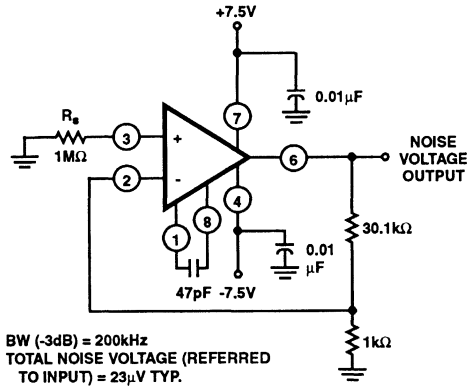


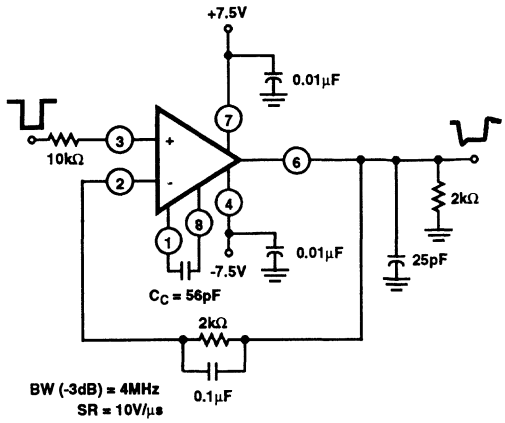
FIGURE 14. TEST-CIRCUIT AMPLIFIER (30-dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENTS

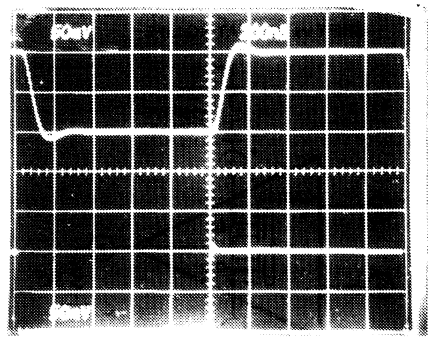
Typical Applications

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Figure 15 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

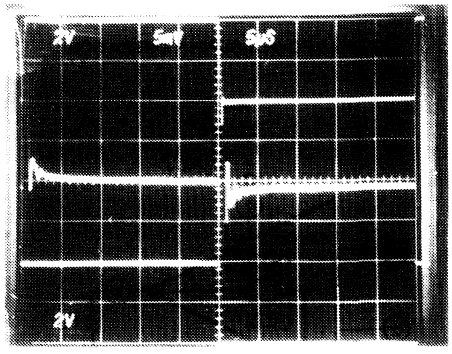
A voltage follower, operated from a single supply, is shown in Figure 16, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Figure 16A with input-signal ramping. The waveforms in Figure 16B show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Figure 16B also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.





Top Trace: Output
Bottom Trace: Input

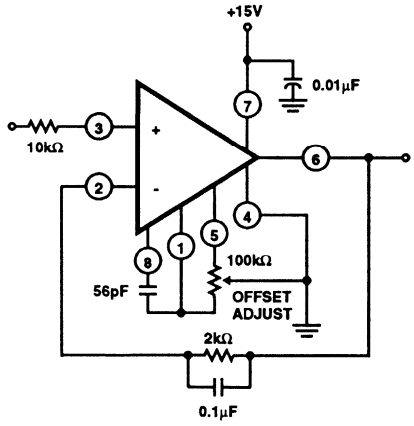
(A) SMALL-SIGNAL RESPONSE (50mV/DIV. AND 200ns/DIV.)

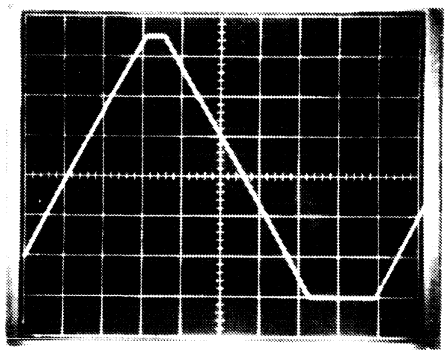


Top Trace: Output Signal (2V/DIV. and 5μs/DIV.)
Center Trace: Difference Signal (5mV/DIV. and 5μs/DIV.)
Bottom Trace: Input Signal (2V/DIV. and 5μs/DIV.)

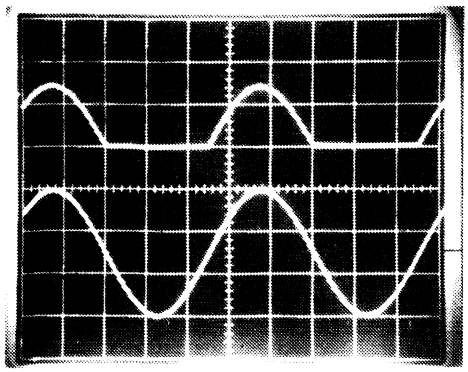
(B) INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME (MEASUREMENT MADE WITH TEKTRONIX 7A13 DIFFERENTIAL AMPLIFIER)

FIGURE 15. SPLIT-SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS





(A) OUTPUT-WAVEFORM WITH INPUT-SIGNAL RAMPING (2V/DIV. AND 500μs/DIV.)



Top Trace: Output (5V/DIV. and 200μs/DIV.)
Bottom Trace: Input Signal (5V/DIV. and 200μs/DIV.)

(B) OUTPUT WAVEFORM WITH GROUND-REFERENCE SINE-WAVE INPUT

FIGURE 16. SINGLE-SUPPLY VOLTAGE-FOLLOWER WITH ASSOCIATED WAVEFORMS. (e.g., FOR USE IN SINGLE-SUPPLY D/A CONVERTER; SEE FIGURE 9 IN AN6080)

9-Bit COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Figure 17 This system combines the concepts of multiple-switch CMOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op-amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10-volt logic levels are used in the circuit of Figure 17.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one percent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

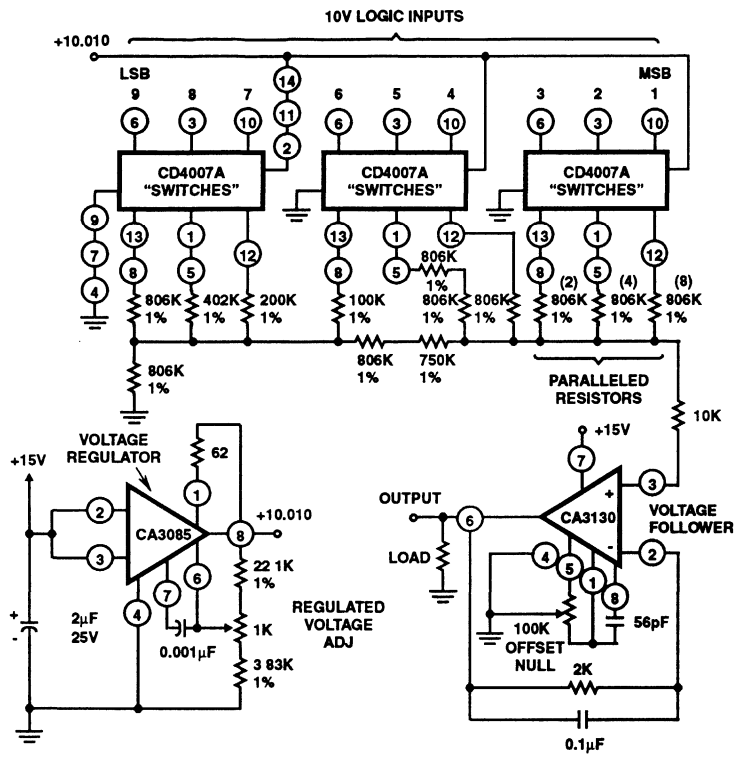
A single 15-volt supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

The absolute-value circuit using the CA3130 is shown in Figure 18. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to -R2/R1. When the equality of the two equations shown in Figure 18 is satisfied, the full-wave output is symmetrical.

Peak Detectors

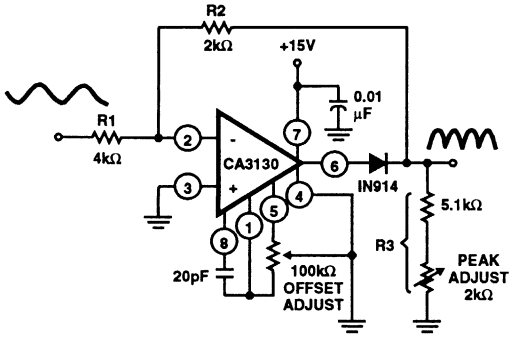
Peak-detector circuits are easily implemented with the CA3130, as illustrated in Figure 19 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in an active "pull-down" mode so that the intrinsic capacitance can be discharged more expeditiously.



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6 - 9	±1% ABS

ALL RESISTANCES IN OHMS

FIGURE 17. 18-9-BIT DAC USING CMOS DIGITAL SWITCHES AND CA3130

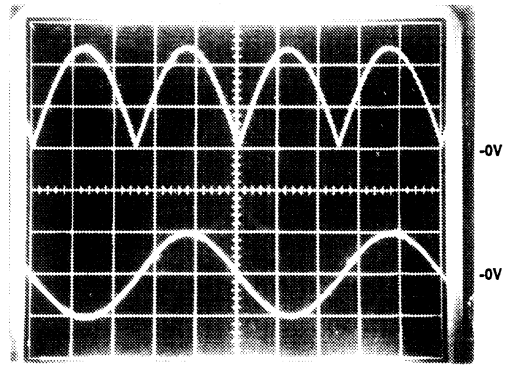


$$\text{Gain} = \frac{R_2}{R_1} = X = \frac{R_3}{R_1 + R_2 + R_3}$$

$$R_3 = R_1\left(\frac{X + X^2}{1 - X}\right)$$

$$\text{For } X = 0.5: \frac{2k\Omega}{4k\Omega} = \frac{R_2}{R_1}$$

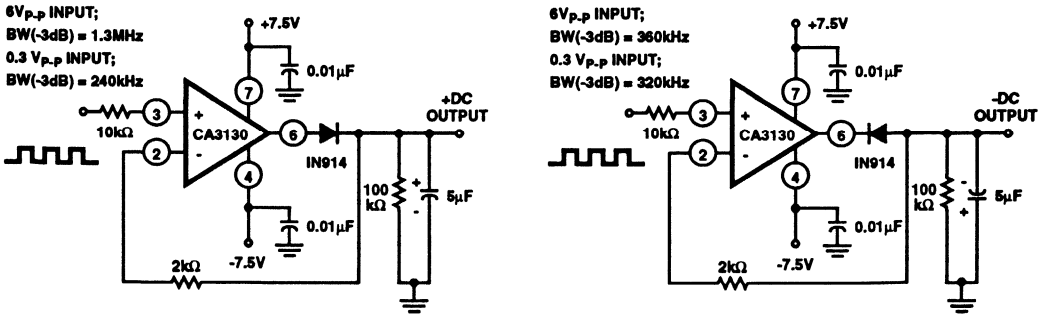
$$R_3 = 4k\Omega\left(\frac{0.75}{0.5}\right) = 6k\Omega$$



Top Trace: Output Signal (2V/div.)
Bottom Trace: Input Signal (10V/div.)
Time base on both traces: 0.2ms/div.

20Vp-p Input: BW(-3dB) = 230kHz, DC Output (Avg.) = 3.2V
1Vp-p Input: BW(-3dB) = 130kHz, DC Output (Avg.) = 160mV

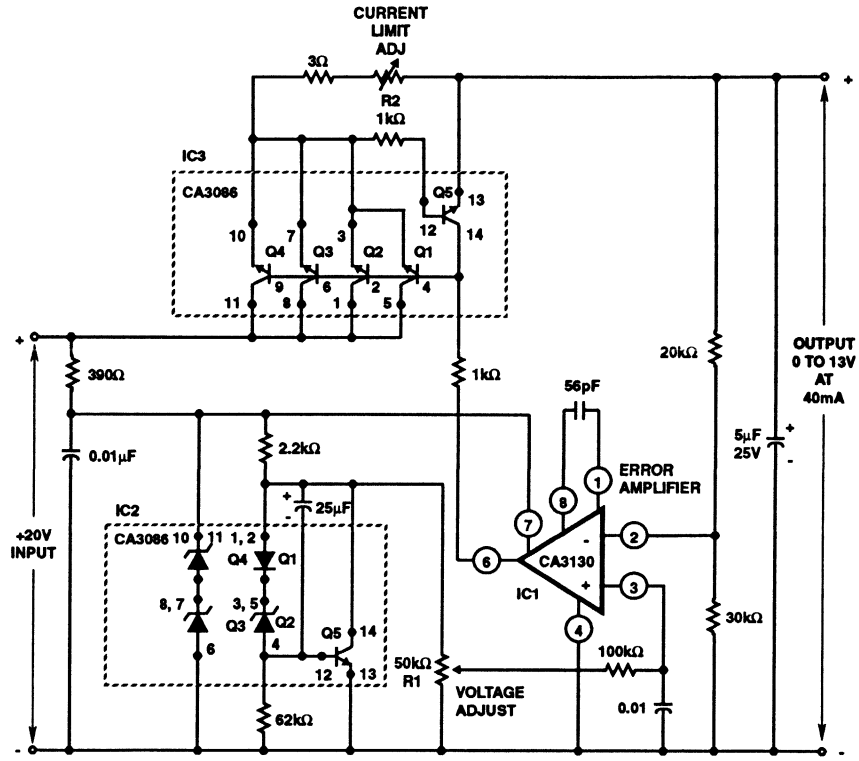
FIGURE 18. SINGLE-SUPPLY, ABSOLUTE-VALUE, IDEAL FULL-WAVE RECTIFIER WITH ASSOCIATED WAVEFORMS



(A) PEAK POSITIVE DETECTOR CIRCUIT

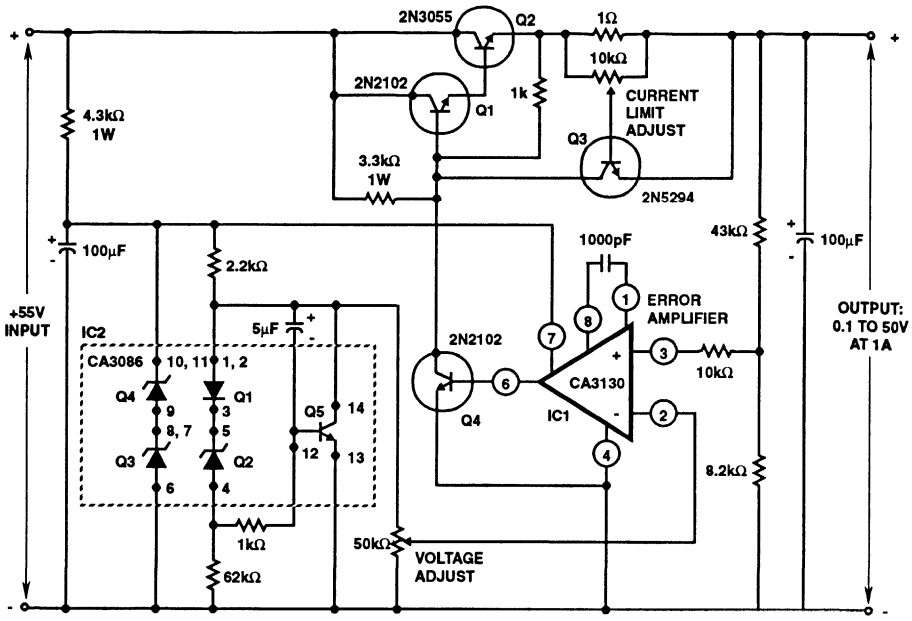
(B) PEAK NEGATIVE DETECTOR CIRCUIT

FIGURE 19. PEAK-DETECTOR CIRCUITS



REGULATION (NO LOAD TO FULL LOAD): < 0.01%
INPUT REGULATION: 0.02%/V
HUM AND NOISE OUTPUT: < 25µV UP TO 100kHz

FIGURE 20. VOLTAGE REGULATOR CIRCUIT (0 TO 13V AT 40mA)



REGULATION (NO LOAD TO FULL LOAD): < 0.005%
INPUT REGULATION: 0.01%/V
HUM AND NOISE OUTPUT: < 250μV RMS UP TO 100kHz

FIGURE 21. VOLTAGE REGULATOR CIRCUIT (0.1 TO 50V AT 1A)

Error-Amplifier in Regulated-Power Supplies

The CA3130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero. Figure 20 shows the schematic diagram of a 40mA power supply capable of providing regulated output voltage by continuous adjustment over the range from 0 to 13 volts. Q3 and Q4 in IC2 (a CA3086 transistor-array IC) function as zeners to provide supply-voltage for the CA3130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier. Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q5 in IC3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R2.

Figure 21 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Figure 22. Resistors R1 and R2 are used to bias the CA3130 to the mid-point of the supply-voltage and R3 is the feedback resistor. The pulse repetition rate is selected by positioning S1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

Function Generator

Figure 23 contains a schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)*, IC1, operated as a voltage-controlled current-source. The output, I_O, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA3130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

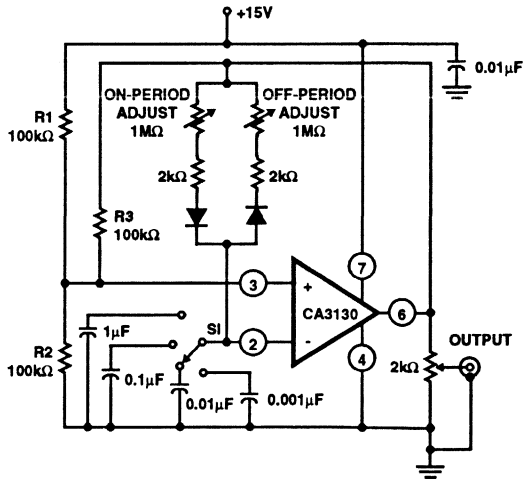
Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

Operation with Output-Stage Power-Booster

The current-sourcing and-sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit of Figure 24, three CMOS transistor-pairs in a single CA3600E* IC array are shown parallel connected with the output stage in the CA3130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15V operation. This arrangement boosts the current-handling capability of the CA3130 output stage by about 2.5X.

The amplifier circuit in Figure 24 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (-3dB) is 50 kHz.

* See File Number 619 for technical information.



FREQUENCY RANGE:

POSITION OF S1	PULSE PERIOD
0.001µF	4µs to 1ms
0.01µF	40µs to 10ms
0.1µF	0.4µs to 100ms
1µF	4µs to 1s

FIGURE 22. PULSE GENERATOR (ASTABLE MULTIVIBRATOR) WITH PROVISIONS FOR INDEPENDENT CONTROL OF "ON" AND "OFF" PERIODS.

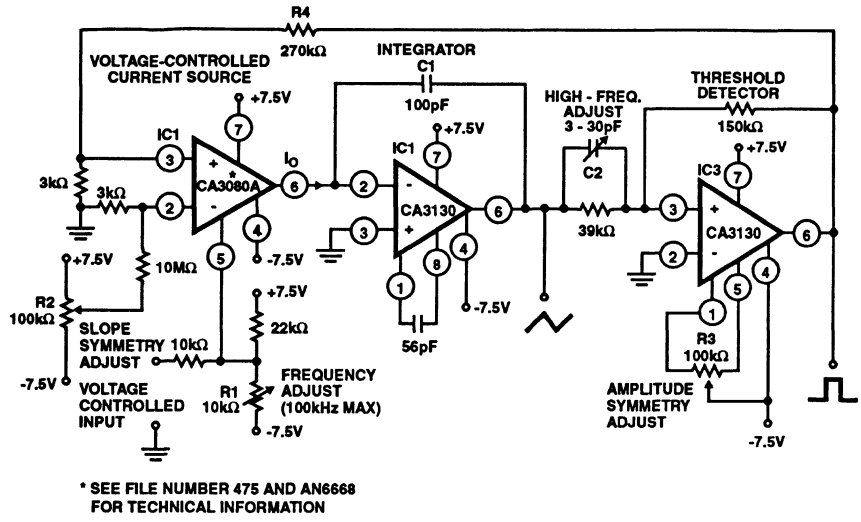


FIGURE 23. FUNCTION GENERATOR (FREQUENCY CAN BE VARIED 1,000,000/1 WITH A SINGLE CONTROL).

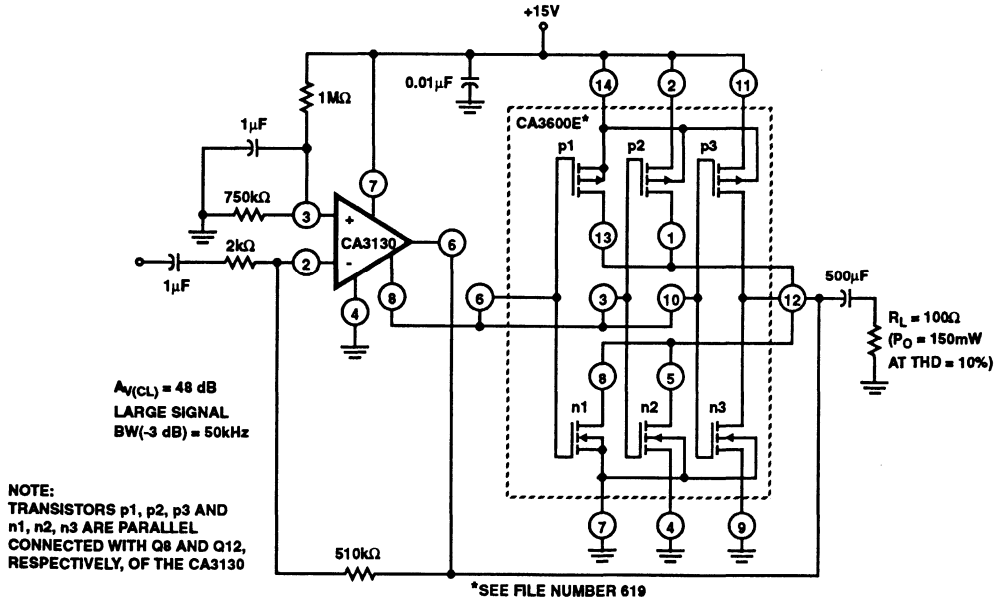


FIGURE 24. CMOS TRANSISTOR ARRAY (CA3600E) CONNECTED AS POWER BOOSTER IN THE OUTPUT STAGE OF THE CA3130.

HARRIS SEMICONDUCTOR

CA3140

BiMOS Operational Amplifier with MOSFET Input/Bipolar Output

April 1993

Features

- MOSFET Input Stage
  - Very High Input Impedance (Z_{IN}) -1.5TΩ (Typ.)
  - Very Low Input Current (I_I) -10pA (Typ.) at ±15V
  - Wide Common Mode Input Voltage Range (VICR) - Can be Swung 0.5V Below Negative Supply Voltage Rail
  - Output Swing Complements Input Common Mode Range
- Directly Replaces Industry Type 741 in Most Applications

Applications

- Ground-Referenced Single Supply Amplifiers in Automobile and Portable Instrumentation
- Sample and Hold Amplifiers
- Long Duration Timers/Multivibrators (μseconds-Minutes-Hours)
- Photocurrent Instrumentation
- Peak Detectors
- Active Filters
- Comparators
- Interface in 5V TTL Systems and Other Low Supply Voltage Systems
- All Standard Operational Amplifier Applications
- Function Generators
- Tone Controls
- Power Supplies
- Portable Instruments
- Intrusion Alarm Systems

Description

The CA3140A and CA3140 are integrated circuit operational amplifiers that combine the advantages of high voltage PMOS transistors with high voltage bipolar transistors on a single monolithic chip. Because of this unique combination of technologies, this device can now provide designers, for the first time, with the special performance features of the CA3130 CMOS operational amplifiers and the versatility of the 741 series of industry standard operational amplifiers.

The CA3140A and CA3140 BiMOS operational amplifiers feature gate protected MOSFET (PMOS) transistors in the input circuit to provide very high input impedance, very low input current, and high speed performance. The CA3140A and CA3140 operate at supply voltage from 4V to 36V (either single or dual supply). These operational amplifiers are internally phase compensated to achieve stable operation in unity gain follower operation, and additionally, have access terminal for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute for single supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load terminal short circuiting to either supply rail or to ground.

The CA3140 Series has the same 8-lead pinout used for the "741" and other industry standard op amps. The CA3140A and CA3140 are intended for operation at supply voltages up to 36V (±18V).

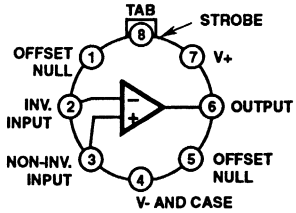
Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
CA3140AE	-55°C to +125°C	8 Lead Plastic DIP
CA3140AM	-55°C to +125°C	8 Lead SOIC
CA3140AS	-55°C to +125°C	8 Pin Can, Lead Formed
CA3140AT	-55°C to +125°C	8 Pin Can
CA3140BT	-55°C to +125°C	8 Pin Can
CA3140E	-55°C to +125°C	8 Lead Plastic DIP
CA3140M	-55°C to +125°C	8 Lead SOIC
CA3140M96	-55°C to +125°C	8 Lead SOIC*
CA3140T	-55°C to +125°C	8 Pin Can

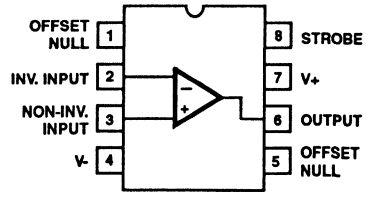
* Denotes Tape and Reel

Pinouts

CA3140 (TO-5 STYLE CAN)
TOP VIEW



CA3140 (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **975.2**

Absolute Maximum Ratings

DC Supply Voltage (Between V+ and V- Terminals) 36V
Differential Mode Input Voltage 8V
DC Input Voltage . . . . . (V+ +8V) To (V- -0.5V)
Input Terminal Current 1mA
Output Short Circuit Duration * . . . . . Indefinite
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

* Short circuit may be applied to ground or to either supply.

Operating Conditions

Operating Temperature Range (All Types) . . . . . -55°C to +125°C
Storage Temperature Range (All Types) . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V+ = +15V$, $V- = -15V$, $T_A = +25°C$

PARAMETERS	SYMBOL	TEST CONDITIONS		CA3140A	CA3140	UNITS
Input Offset Voltage Adjustment Resistor		Typical Value of Resistor Between Term. 4 and 5 or 4 and 1 to Adjust Max. V_{IO}		18	4.7	kΩ
Input Resistance	R_I			1.5	1.5	TΩ
Input Capacitance	C_I			4	4	pF
Output Resistance	R_O			60	60	Ω
Equivalent Wideband Input Noise Voltage (See Figure 35)	e_N	BW = 140kHz R_S = 1 MΩ		48	48	μV
Equivalent Input Noise Voltage (See Figure 7)	e_N	f = 1kHz	R_S = 100Ω	40	40	$nV/\sqrt{Hz}$
		f = 10 kHz		12	12	$nV/\sqrt{Hz}$
Short Circuit Current to Opposite Supply						
Source	$I_{OM}+$			40	40	mA
Sink	$I_{OM}-$			18	18	mA
Gain-Bandwidth Product, (See Figures 2 & 15)	f_T			4.5	4.5	MHz
Slew Rate, (See Figure 3)	SR			9	9	V/μs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low				220	220	μA
Transient Response:		R_L = 2kΩ C_L = 100pF				
Rise Time	t_R			0.08	0.08	μs
Overshoot (See Figure 34)	OS			10	10	%
Settling Time at 10 V_{p-p}, (See Figure 14)	t_S	R_L = 2kΩ C_L = 100pF Voltage Follower				
1mV				4.5	4.5	μs
10mV				1.4	1.4	μs

Specifications CA3140, CA3140A

Electrical Specifications For Equipment Design. At V+ = 15V, V- = 15V, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	LIMITS						UNITS
		CA3140A			CA3140			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$\|V_{IO}\|$	-	2	5	-	5	15	mV
Input Offset Current	$\|I_{IO}\|$	-	0.5	20	-	0.5	30	pA
Input Current	I_I	-	10	40	-	10	50	pA
Large Signal Voltage Gain (Note 1) (See Figures 1, 15)	A_{OL}	20	100	-	20	100	-	kV/V
		86	100	-	86	100	-	dB
Common Mode Rejection Ratio (See Figure 6)	CMRR	-	32	320	-	32	320	µV/V
		70	90	-	70	90	-	dB
Common Mode Input Voltage Range (See Figure 17)	V_{ICR}	-15	-15.5 to +12.5	12	-15	-15.5 to +12.5	11	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V_S$ (See Figure 8)	PSRR	-	100	150	-	100	150	µV/V
		76	80	-	76	80	-	dB
Max. Output Voltage (Note 2) (See Figures 10, 17)	V_{OM}+	+12	13	-	+12	13	-	V
	V_{OM}-	-14	-14.4	-	-14	-14.4	-	V
Supply Current (See Figure 4)	I+	-	4	6	-	4	6	mA
Device Dissipation	P_D	-	120	180	-	120	180	mW
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$		-	6	-	-	8	-	µV/° C

NOTES:

1. At V_O = $26V_{p-p}$, +12V, 14V and R_L = 2kΩ.
2. At R_L = 2kΩ.

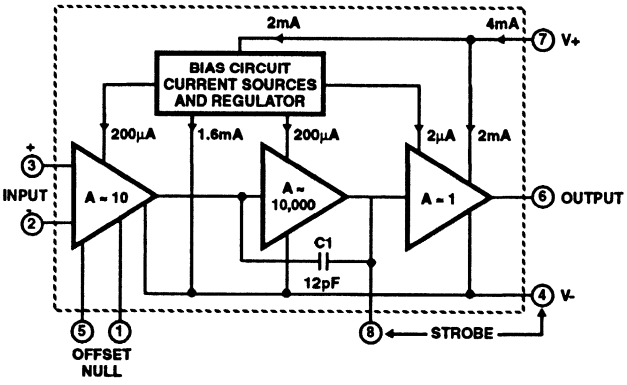
Electrical Specifications For Design Guidance. At V+ = 5 V, V- = 0V, T_A = +25°C

PARAMETERS	SYMBOL	CA3140A	CA3140	UNITS
Input Offset Voltage	$\|V_{IO}\|$	2	5	mV
Input Offset Current	$\|I_{IO}\|$	0.1	0.1	pA
Input Current	I_I	2	2	pA
Input Resistance	R_I	1	1	TΩ

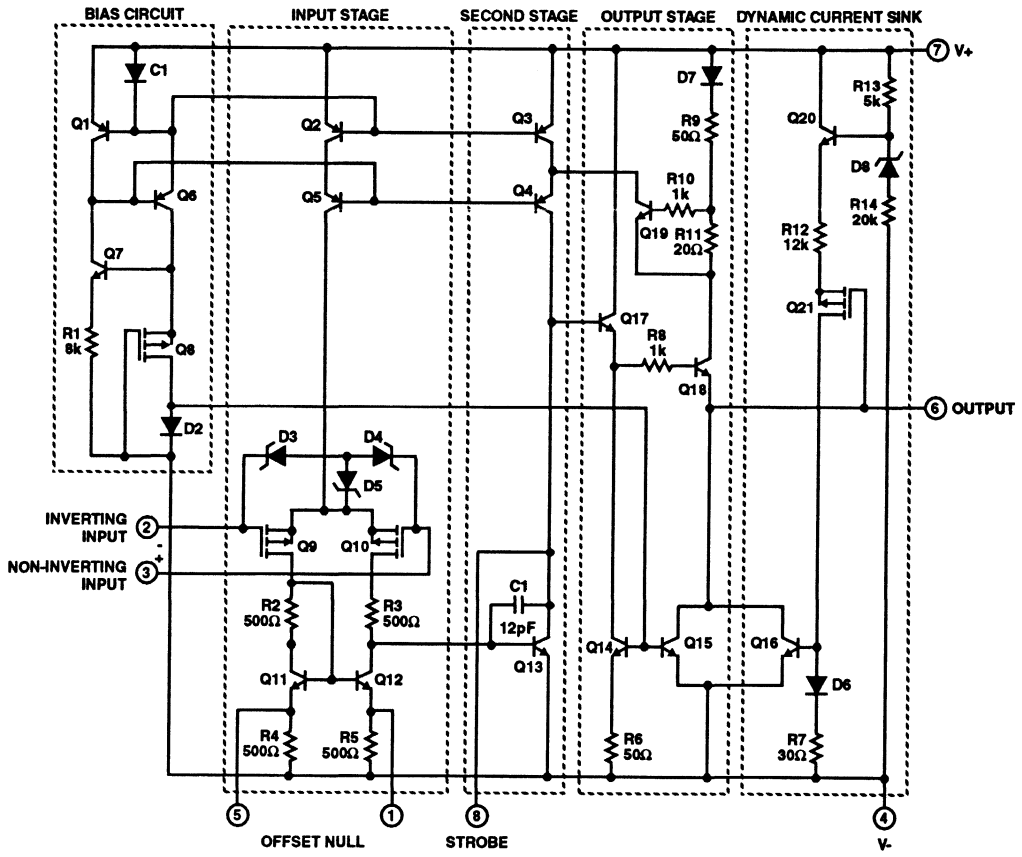
Electrical Specifications For Design Guidance. At V+ = 5 V, V- = 0V, T_A = +25°C **(Continued)**

PARAMETERS	SYMBOL	CA3140A	CA3140	UNITS
Large Signal Voltage Gain (See Figures 1, 15)	A_{OL}	100	100	kV/V
		100	100	dB
Common Mode Rejection Ratio,	CMRR	32	32	µV/V
		90	90	dB
Common Mode Input Voltage Range (See Figure 17)	V_{ICR}	-0.5	-0.5	V
		2.6	2.6	V
Power Supply Rejection Ratio	PSRR $\Delta V_{IO}/\Delta V_S$	100	100	µV/V
		80	80	dB
Maximum Output Voltage (See Figures 10, 17)	V_{OM}+	3	3	V
	V_{OM}-	0.13	0.13	V
Maximum Output Current:				
Source	IOM+	10	10	mA
Sink	I_{OM}-	1	1	mA
Slew Rate (See Figure 3)	SR	7	7	V/µs
Gain-Bandwidth Product (See Figure 2)	f_T	3.7	3.7	MHz
Supply Current (See Figure 4)	I+	1.6	1.6	mA
Device Dissipation	P_D	8	8	mW
Sink Current from Term. 8 to Term. 4 to Swing Output Low		200	200	µA

Block Diagram



Schematic Diagram



ALL RESISTANCE VALUES ARE IN Ω

Circuit Description

As shown in the block diagram, the input terminals may be operated down to 0.5V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant current flow circuits in the first and second stages. The CA3140 includes an on chip phase compensating capacitor that is sufficient for the unity gain voltage follower configuration.

Input Stages

The schematic diagram consists of a differential input stage using PMOS field-effect transistors (Q9, Q10) working into a mirror pair of bipolar transistors (Q11, Q12) functioning as load resistors together with resistors R2 through R5. The mirror pair transistors also function as a differential-to-single-ended converter to provide base current drive to the second stage bipolar transistor (Q13). Offset nulling, when desired, can be effected with a 10kΩ potentiometer connected across terminals 1 and 5 and with its slider arm connected to terminal 4. Cascode connected bipolar transistors Q2, Q5 are the constant current source for the input stage. The base biasing circuit for the constant current source is described subsequently. The small diodes D3, D4, D5 provide gate oxide protection against high voltage transients, e.g., static electricity.

Second Stage

Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q13 and its cascode connected load resistance provided by bipolar transistors Q3, Q4. On-chip phase compensation, sufficient for a majority of the applications is provided by C1. Additional Miller-Effect compensation (roll off) can be accomplished, when desired, by simply connecting a small capacitor between terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (terminal 4) by mechanical or electrical means, the output terminal 6 swings low, i.e., approximately to terminal 4 potential.

Output Stage

The CA3140 Series circuits employ a broad band output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q17, Q18) is established by transistors (Q14, Q15) whose base currents are "mirrored" to current flowing through diode D2 in the bias circuit section.

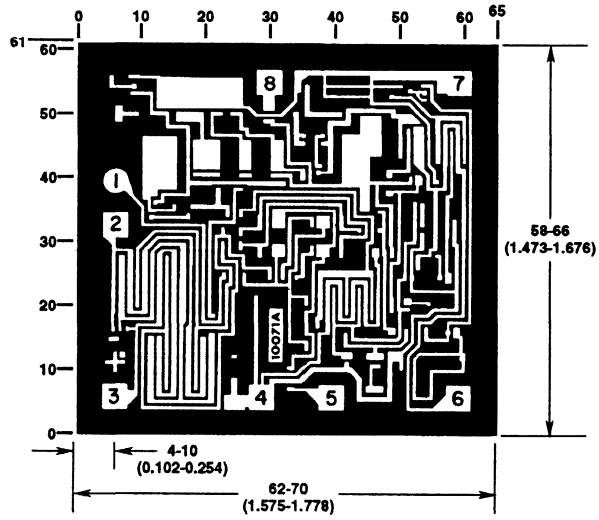
When the CA3140 is operating such that output terminal 6 is sourcing current, transistor Q18 functions as an emitter-follower to source current from the V+ bus (terminal 7), via D7, R9, and R11. Under these conditions, the collector potential of Q13 is sufficiently high to permit the necessary flow of base current to emitter follower Q17 which, in turn, drives Q18.

When the CA3140 is operating such that output terminal 6 is sinking current to the V- bus, transistor Q16 is the current sinking element. Transistor Q16 is mirror connected to D6, R7, with current fed by way of Q21, R12, and Q20. Transistor Q20, in turn, is biased by current flow through R13, zener D8, and R14. The dynamic current sink is controlled by voltage level sensing. For purposes of explanation, it is assumed that output terminal 6 is quiescently established at the potential midpoint between the V+ and V- supply rails. When output current sinking mode operation is required, the collector potential of transistor Q13 is driven below its quiescent level, thereby causing Q17, Q18 to decrease the output voltage at terminal 6. Thus, the gate terminal of PMOS transistor Q21 is displaced toward the V- bus, thereby reducing the channel resistance of Q21. As a consequence, there is an incremental increase in current flow through Q20, R12, Q21, D6, R7, and the base of Q16. As a result, Q16 sinks current from terminal 6 in direct response to the incremental change in output voltage caused by Q18. This sink current flows regardless of load; any excess current is internally supplied by the emitter-follower Q18. Short circuit protection of the output circuit is provided by Q19, which is driven into conduction by the high voltage drop developed across R11 under output short circuit conditions. Under these conditions, the collector of Q19 diverts current from Q4 so as to reduce the base current drive from Q17, thereby limiting current flow in Q18 to the short circuited load terminal.

Bias Circuit

Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R1. The function of the bias circuit is to establish and maintain constant current flow through D1, Q6, Q8 and D2. D1 is a diode connected transistor mirror connected in parallel with the base emitter junctions of Q1, Q2, and Q3. D1 may be considered as a current sampling diode that senses the emitter current of Q6 and automatically adjusts the base current of Q6 (via Q1) to maintain a constant current through Q6, Q8, D2. The base currents in Q2, Q3 are also determined by constant current flow D1. Furthermore, current in diode connected transistor Q2 establishes the currents in transistors Q14 and Q15.

Metallization Mask Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

Typical Performance Curves

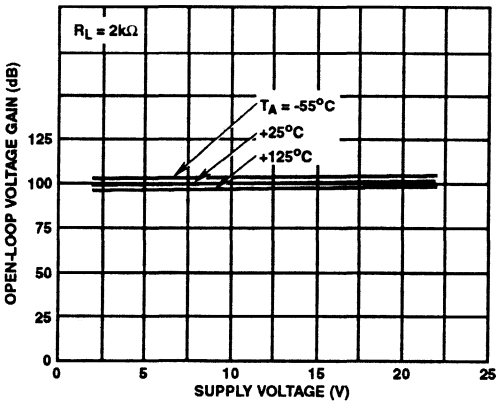


FIGURE 1. OPEN LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE AND TEMPERATURE

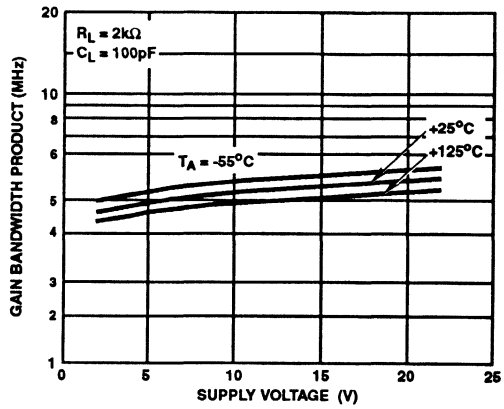


FIGURE 2. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE AND TEMPERATURE

Typical Performance Curves (Continued)

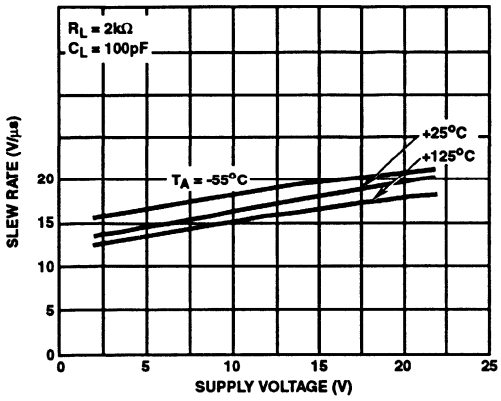


FIGURE 3. SLEW RATE vs SUPPLY VOLTAGE AND TEMPERATURE

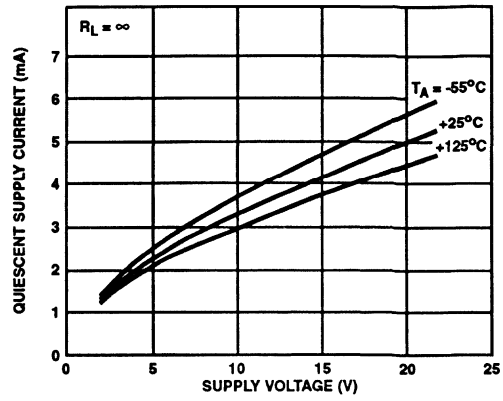


FIGURE 4. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE AND TEMPERATURE

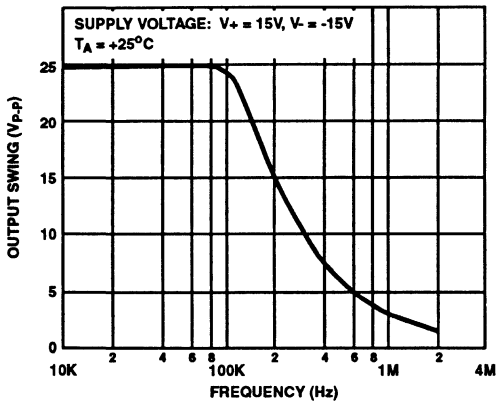


FIGURE 5. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

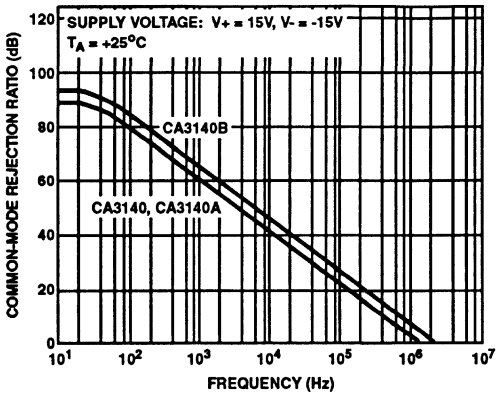


FIGURE 6. COMMON MODE REJECTION RATIO vs FREQUENCY

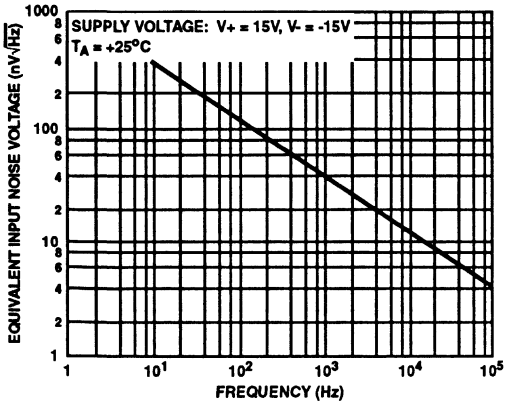


FIGURE 7. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

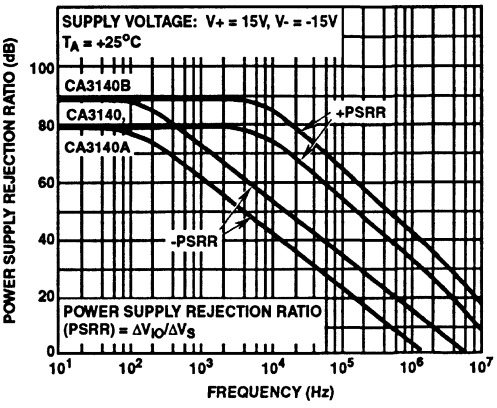


FIGURE 8. POWER SUPPLY REJECTION RATIO vs FREQUENCY

Applications Considerations

Wide dynamic range of input and output characteristics with the most desirable high input impedance characteristics is achieved in the CA3140 by the use of an unique design based upon the PMOS Bipolar process. Input common mode voltage range and output swing capabilities are complementary, allowing operation with the single supply down to 4V.

The wide dynamic range of these parameters also means that this device is suitable for many single supply applications, such as, for example, where one input is driven below the potential of terminal 4 and the phase sense of the output signal must be maintained – a most important consideration in comparator applications.

Output Circuit Considerations

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2V zener diode connected to terminal 8 as shown in Figure 9. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the CA3140. These voltages are independent of the operating supply voltage.

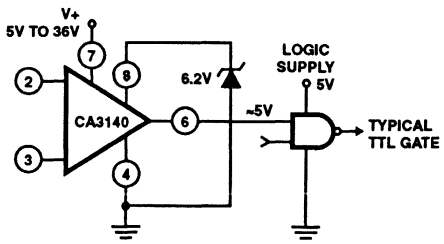


FIGURE 9. ZENER CLAMPING DIODE CONNECTED TO TERMINALS 8 AND 4 TO LIMIT CA3140 OUTPUT SWING TO TTL LEVELS

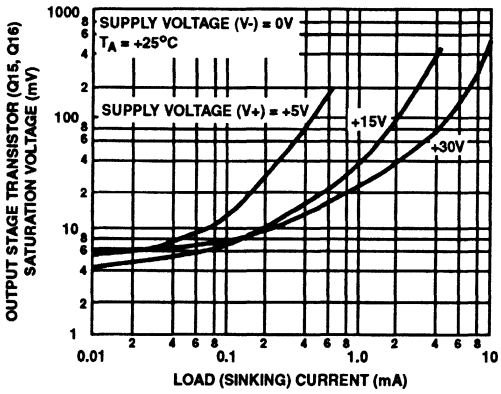


FIGURE 10. VOLTAGE ACROSS OUTPUT TRANSISTORS Q15 AND Q16 vs LOAD CURRENT

Figure 10 shows output current sinking capabilities of the CA3140 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level shifting circuitry usually associated with the 741 series of operational amplifiers.

Figure 13 shows some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

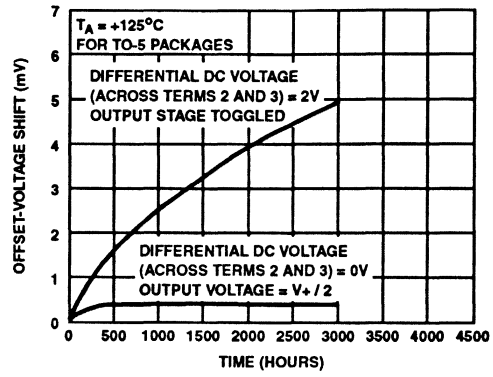


FIGURE 11. TYPICAL INCREMENTAL OFFSET VOLTAGE SHIFT vs OPERATING LIFE

Offset Voltage Nulling

The input offset voltage can be nulled by connecting a 10kΩ potentiometer between terminals 1 and 5 and returning its wiper arm to terminal 4, see Figure 12(A). This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Figure 12(B), to optimize its utilization range are given in the table "Electrical Specifications" shown in this bulletin.

An alternate system is shown in Figure 12(C). This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero Ω at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

Low Voltage Operation

Operation at total supply voltages as low as 4V is possible with the CA3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low voltage limitation occurs when the upper extreme of the input common mode voltage range extends down to the

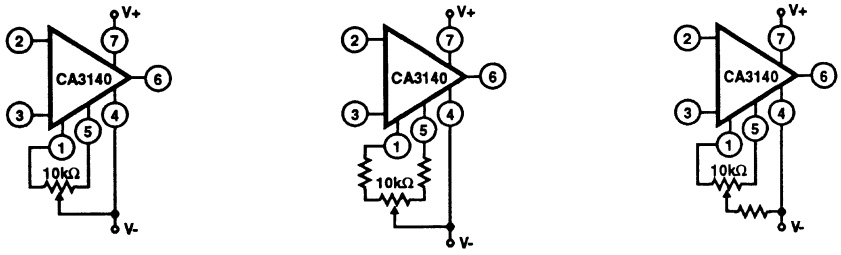


FIGURE 12. THREE OFFSET VOLTAGE NULLING METHODS

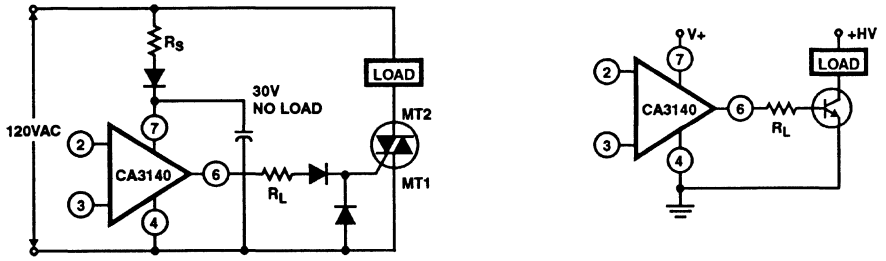


FIGURE 13. METHODS OF UTILIZING THE V_{CE}(SAT) SINKING CURRENT CAPABILITY OF THE CA3140 SERIES

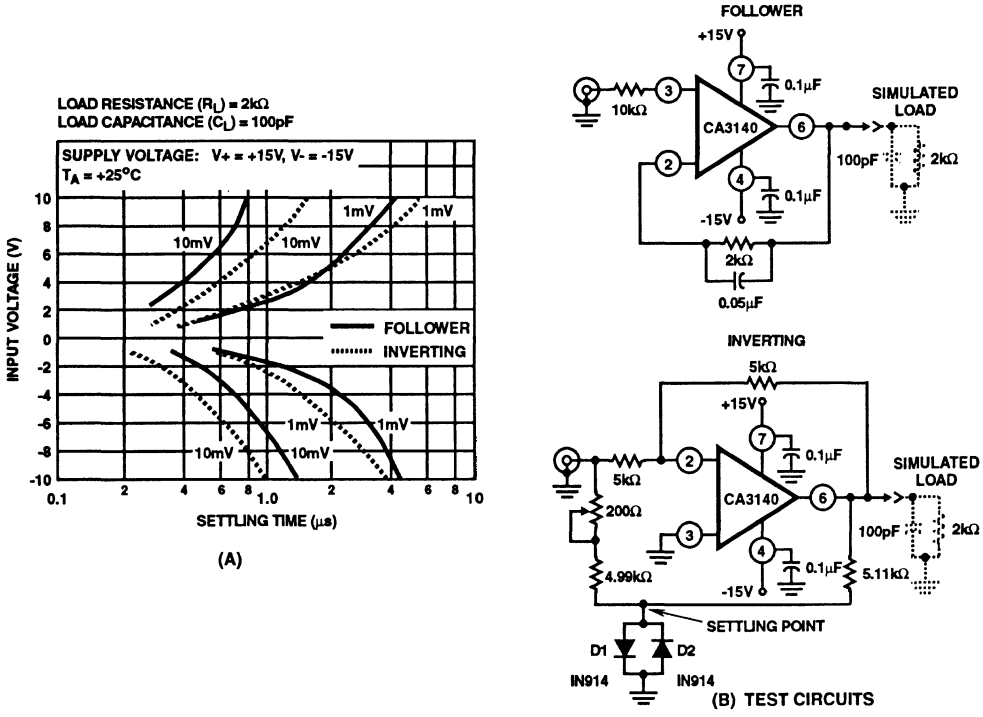


FIGURE 14. INPUT VOLTAGE vs SETTLING TIME

voltage at terminal 4. This limit is reached at a total supply voltage just below 4V. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Figure 17 shows these characteristics and shows that with 2V dual supplies, the lower extreme of the input common mode voltage range is below ground potential.

Bandwidth and Slew Rate

For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between terminals 1 and 8 can reduce the open loop -3dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Figure 14 shows the typical settling time required to reach 1mV or 10mV of the final value for various levels of large signal inputs for the voltage follower and inverting unity gain amplifiers. The exceptionally fast settling time characteristics are largely due to the high combination of high gain and wide bandwidth of the CA3140; as shown in Figure 15.

Input Circuit Considerations

As mentioned previously, the amplifier inputs can be driven below the terminal 4 potential, but a series current limiting resistor is recommended to limit the maximum input terminal current to less than 1mA to prevent damage to the input protection circuitry.

Moreover, some current limiting resistance should be provided between the inverting input and the output when the CA3140 is used as a unity gain voltage follower. This resistance prevents the possibility of extremely large input signal transients from forcing a signal through the input protection network and directly driving the internal constant current source which could result in positive feedback via the output terminal. A 3.9kΩ resistor is sufficient.

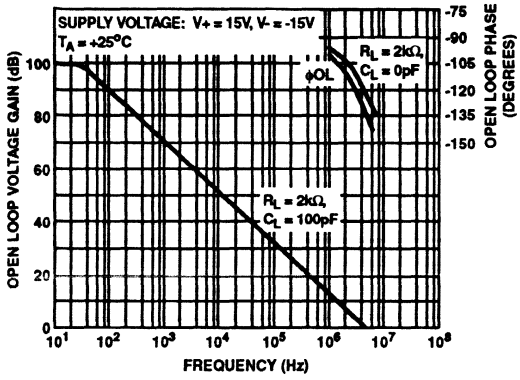


FIGURE 15. OPEN LOOP VOLTAGE GAIN AND PHASE vs FREQUENCY

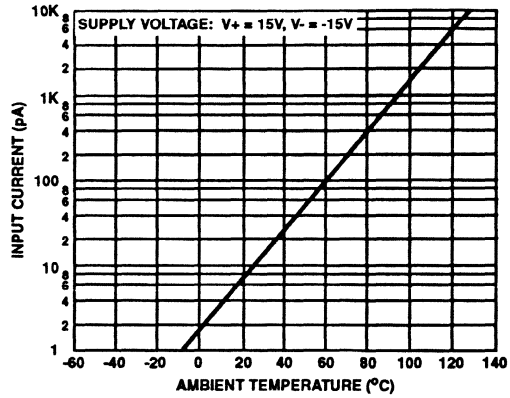


FIGURE 16. INPUT CURRENT vs AMBIENT TEMPERATURE

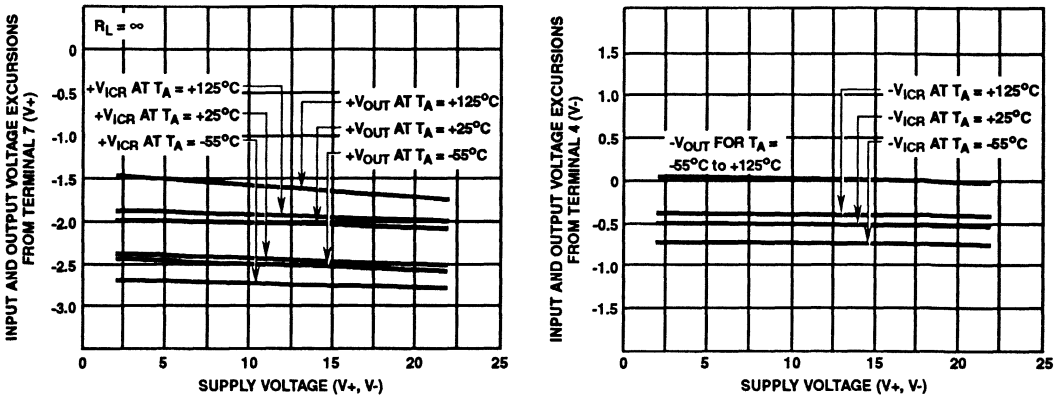


FIGURE 17. OUTPUT VOLTAGE SWING CAPABILITY AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE AND TEMPERATURE

The typical input current is in the order of 10pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Figure 16 shows typical input terminal current versus ambient temperature for the CA3140.

It is well known that MOSFET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Figure 11 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of +125°C (for TO-5); at lower temperatures (TO-5 and plastic), for example, at +85°C, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

Super Sweep Function Generator

A function generator having a wide tuning range is shown in Figure 18. The 1,000,000/1 adjustment range is accomplished by a single variable potentiometer or by an auxiliary sweeping signal. The CA3140 functions as a non-inverting readout amplifier of the triangular signal developed across the integrating capacitor network connected to the output of the CA3080A current source.

Buffered triangular output signals are then applied to a second CA3080 functioning as a high speed hysteresis switch. Output from the switch is returned directly back to the input of the CA3080A current source, thereby, completing the positive feedback loop

The triangular output level is determined by the four 1N914 level limiting diodes of the second CA3080 and the resistor divider network connected to terminal No. 2 (input) of the CA3080. These diodes establish the input trip level to this switching stage and, therefore, indirectly determine the amplitude of the output triangle.

Compensation for propagation delays around the entire loop is provided by one adjustment on the input of the CA3080. This adjustment, which provides for a constant generator amplitude output, is most easily made while the generator is sweeping. High frequency ramp linearity is adjusted by the single 7-to-6pF capacitor in the output of the CA3080A.

It must be emphasized that only the CA3080A is characterized for maximum output linearity in the current generator function.

Meter Driver and Buffer Amplifier

Figure 19 shows the CA3140 connected as a meter driver and buffer amplifier. Low driving impedance is required of the CA3080A current source to assure smooth operation of the Frequency Adjustment Control. This low-driving impedance requirement is easily met by using a CA3140 connected as a voltage follower. Moreover, a meter may be placed across the input to the CA3080A to give a logarithmic analog indication of the function generators frequency.

Analog frequency readout is readily accomplished by the means described above because the output current of the CA3080A varies approximately one decade for each 60mV change in the applied voltage, V_{ABC} (voltage between terminals 5 and 4 of the CA3080A of the function generator). Therefore, six decades represent 360mV change in V_{ABC}.

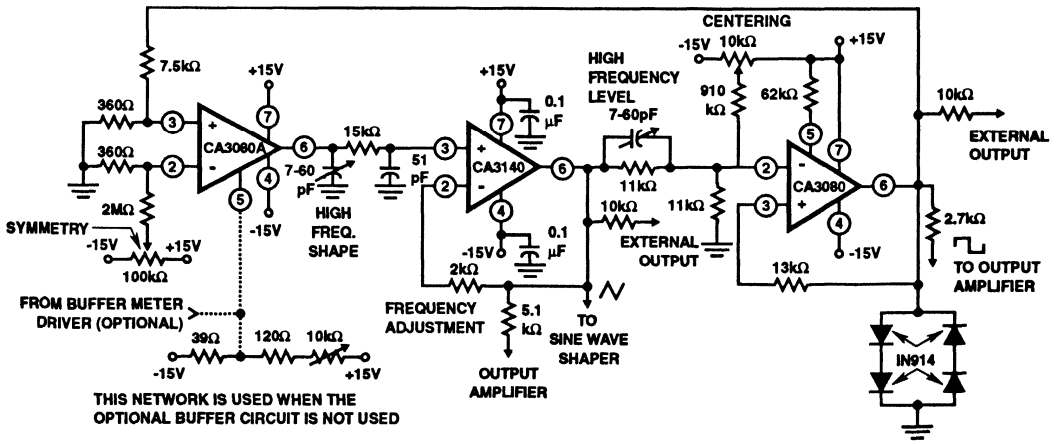
Now, only the reference voltage must be established to set the lower limit on the meter. The three remaining transistors from the CA3086 Array used in the sweep generator are used for this reference voltage. In addition, this reference generator arrangement tends to track ambient temperature variations, and thus compensates for the effects of the normal negative temperature coefficient of the CA3080A V_{ABC} terminal voltage.

Another output voltage from the reference generator is used to insure temperature tracking of the lower end of the Frequency Adjustment Potentiometer. A large series resistance simulates a current source, assuring similar temperature coefficients at both ends of the Frequency Adjustment Control.

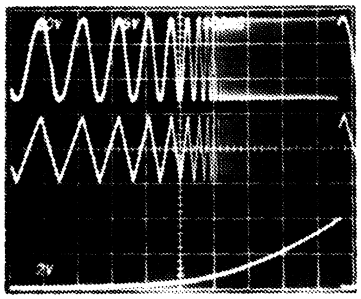
To calibrate this circuit, set the Frequency Adjustment Potentiometer at its low end. Then adjust the Minimum Frequency Calibration Control for the lowest frequency. To establish the upper frequency limit, set the Frequency Adjustment Potentiometer to its upper end and then adjust the Maximum Frequency Calibration Control for the maximum frequency. Because there is interaction among these controls, repetition of the adjustment procedure may be necessary. Two adjustments are used for the meter. The meter sensitivity control sets the meter scale width of each decade, while the meter position control adjusts the pointer on the scale with negligible effect on the sensitivity adjustment. Thus, the meter sensitivity adjustment control calibrates the meter so that it deflects $^1/_6$ of full scale for each decade change in frequency.

Sine Wave Shaper

The circuit shown in Figure 20 uses a CA3140 as a voltage follower in combination with diodes from the CA3019 Array to convert the triangular signal from the function generator to a sine-wave output signal having typically less than 2% THD. The basic zero crossing slope is established by the 10kΩ potentiometer connected between terminals 2 and 6 of the CA3140 and the 9.1kΩ resistor and 10kΩ potentiometer from terminal 2 to ground. Two break points are established by diodes D_1 through D_4. Positive feedback via D_5 and D_6 establishes the zero slope at the maximum and minimum levels of the sine wave. This technique is necessary because the voltage follower configuration approaches unity gain rather than the zero gain required to shape the sine wave at the two extremes.



(A) CIRCUIT

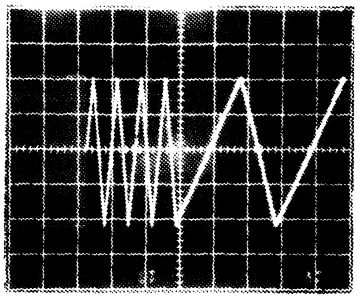


(B1) FUNCTION GENERATOR SWEEPING

Top Trace: Output at junction of 2.7Ω and 51Ω resistors 5V/Div and 500ms/Div

Center Trace: External output of triangular function generator 2V/Div and 500ms/Div

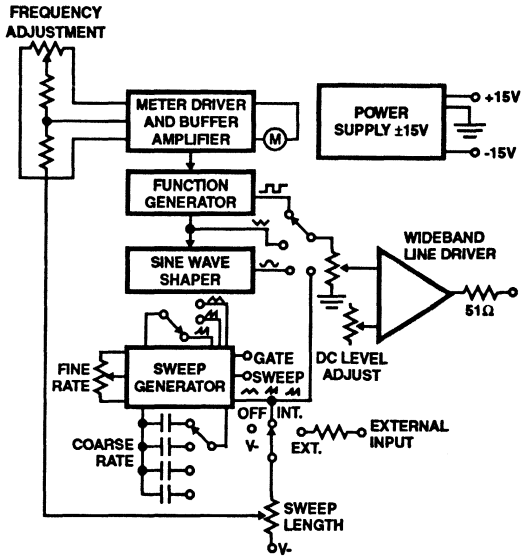
Bottom Trace: Output of "Log" generator; 10V/Div and 500ms/Div



(B2) FUNCTION GENERATOR WITH FIXED FREQUENCIES

1V/Div and 1sec/Div

Three tone test signals, highest frequency ≥0.5MHz. Note the slight asymmetry at the three second/cycle signal. This asymmetry is due to slightly different positive and negative integration from the CA3080A and from the pc board and component leakages at the 100pA level.



(C) INTERCONNECTIONS

FIGURE 18. FUNCTION GENERATOR

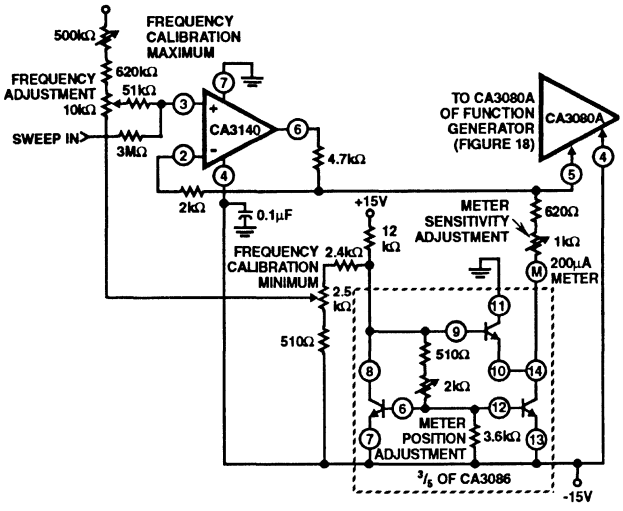


FIGURE 19. METER DRIVER AND BUFFER AMPLIFIER

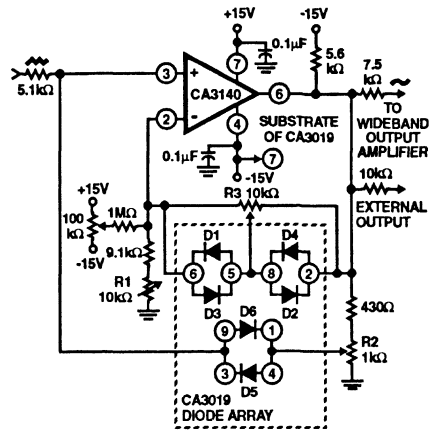


FIGURE 20. SINE WAVE SHAPER

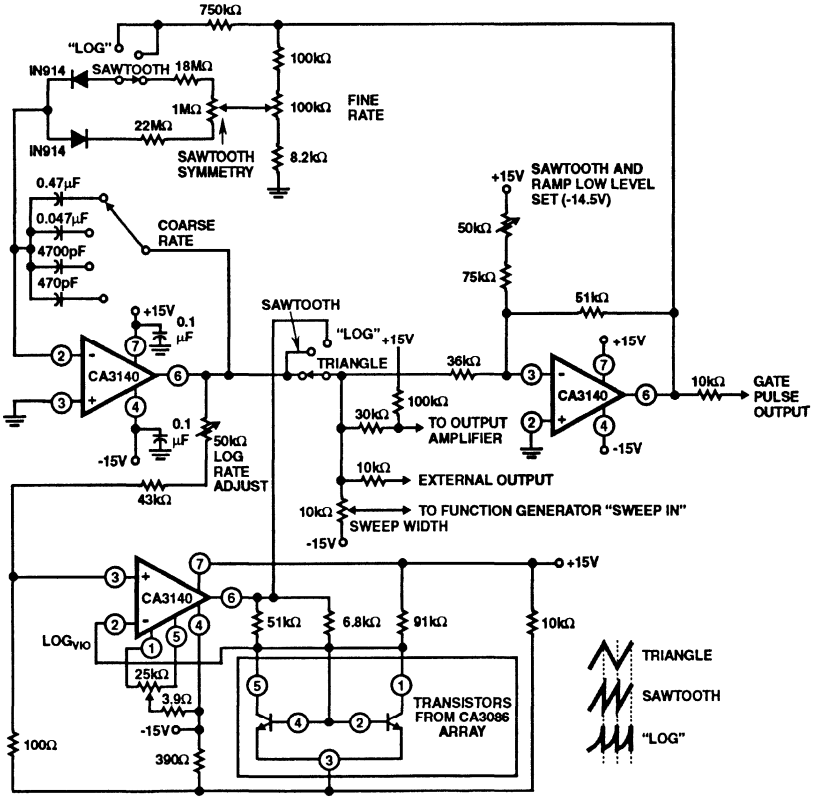


FIGURE 21. SWEEPING GENERATOR

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine wave generator. The initial slope is adjusted with the potentiometer R_1, followed by an adjustment of R_2. The final slope is established by adjusting R_3, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessary.

Sweeping Generator

Figure 21 shows a sweeping generator. Three CA3140's are used in this circuit. One CA3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third CA3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

Wideband Output Amplifier

Figure 22 shows a high slew rate, wideband amplifier suitable for use as a 50Ω transmission line driver. This circuit, when used in conjunction with the function generator and sine wave shaper circuits shown in Figures 18 and 20 provides 18V peak-to-peak output open circuited, or 9V peak-to-peak output when terminated in 50Ω. The slew rate required of this amplifier is 28V/μs (18V peak-to-peak x π x 0.5MHz).

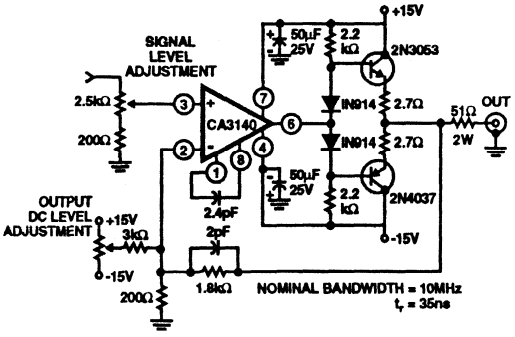


FIGURE 22. WIDEBAND OUTPUT AMPLIFIER

Power Supplies

High input impedance, common mode capability down to the negative supply and high output drive current capability are key factors in the design of wide range output voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0V to 24V.

Unlike many regulator systems using comparators having a bipolar transistor input stage, a high impedance reference voltage divider from a single supply can be used in connection with the CA3140 (see Figure 23).

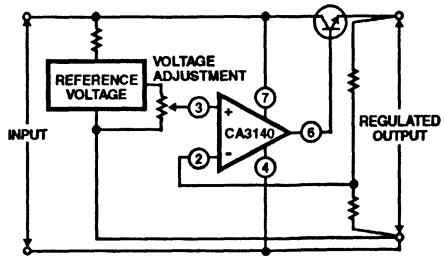


FIGURE 23. BASIC SINGLE SUPPLY VOLTAGE REGULATOR SHOWING VOLTAGE FOLLOWER CONFIGURATION

Essentially, the regulators, shown in Figures 24 and 25, are connected as non inverting power operational amplifiers with a gain of 3.2. An 8V reference input yields a maximum output voltage slightly greater than 25V. As a voltage follower, when the reference input goes to 0V the output will be 0V. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high I_{CBO} levels will also prevent the output voltage from reaching zero because there is a finite voltage drop (V_{CE}sat) across the output of the CA3140 (see Figure 10). This saturation voltage level may indeed set the lowest voltage obtainable.

The high impedance presented by terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the CA3140 in the event of unusual input or output transients on the supply rail.

Figures 24 and 25, show circuits in which a D2201 high speed diode is used for the current sensor. This diode was chosen for its slightly higher forward voltage drop characteristic, thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1A at 1V forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small signal reference amplifier in the proximity of the current sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode. In spite of those limitations, the current limiting point can easily be adjusted over the range from 10mA to 1A with a single adjustment potentiometer. If the temperature stability of the current limiting system is a serious consideration, the more usual current sampling resistor type of circuitry should be employed.

A power Darlington transistor (in a heat sink TO-3 case), is used as the series pass element for the conventional current limiting system, Figure 24, because high power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat sink VERSAWATT transistor is used as the series pass element in the fold back current system, Figure 25, since dissipation levels will only approach 10W. In this system, the D2201 diode is used for current sampling. Fold-

back is provided by the 3kΩ and 100kΩ divider network connected to the base of the current sensing transistor.

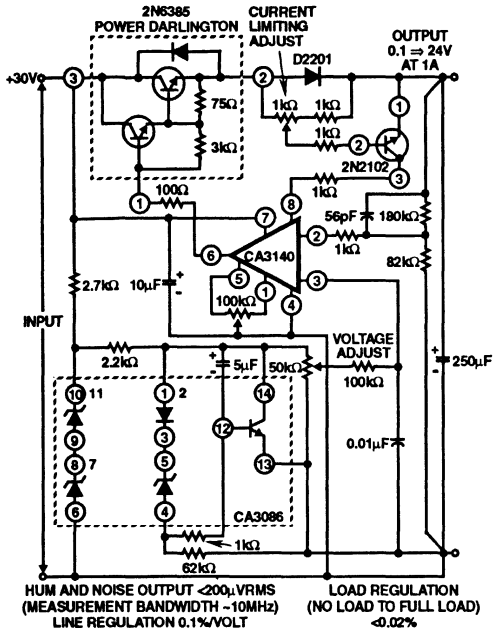


FIGURE 24. REGULATED POWER SUPPLY

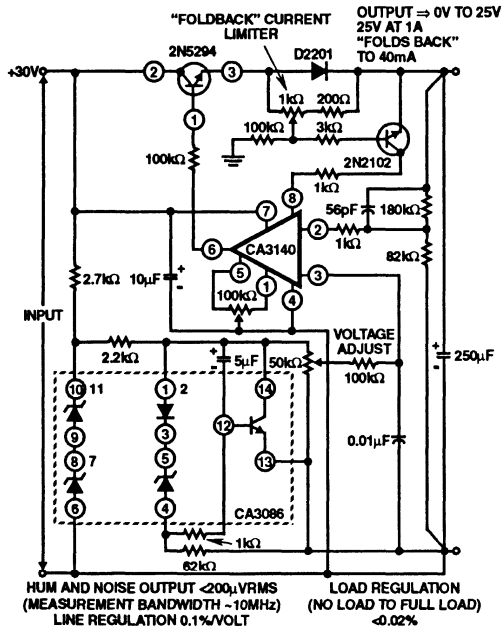
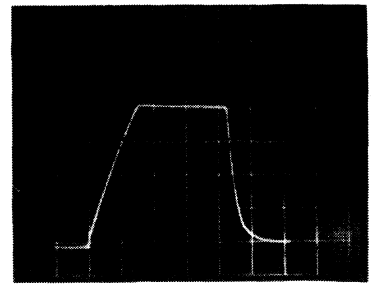


FIGURE 25. REGULATED POWER SUPPLY WITH "FOLDBACK" CURRENT LIMITING

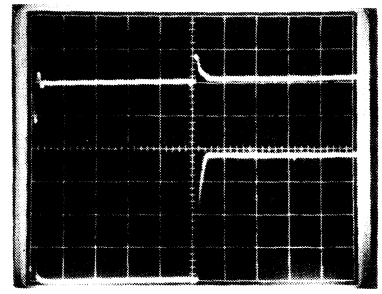
Both regulators, Figures 24 and 25, provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200μV as read with a meter having a 10MHz bandwidth.

Figure 28 (a) shows the turn ON and turn OFF characteristics of both regulators. The slow turn on rise is due to the slow rate of rise of the reference voltage. Figure 26 (B) shows the transient response of the regulator with the switching of a 20Ω load at 20V output.



(A) SUPPLY TURN-ON AND TURNOFF CHARACTERISTICS

5V/Div and -1s/Div



(B) TRANSIENT RESPONSE

Top Trace: Output voltage
200mV/Div and 5μs/Div

Bottom Trace: Collector of load switching transistor, load = 1A
5V/Div and 5μs/Div

FIGURE 26. WAVEFORMS OF DYNAMIC CHARACTERISTICS OF POWER SUPPLY CURRENTS SHOWN IN FIGURES 24 AND 25

Tone Control Circuits

High slew rate, wide bandwidth, high output voltage capability and high input impedance are all characteristics required of tone control amplifiers. Two tone control circuits that exploit these characteristics of the CA3140 are shown in Figures 27 and 28.

The first circuit, shown in Figure 28, is the Baxandall tone control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the CA3140 makes possible the use of low-cost, low-value, small size capacitors, as well as reduced load of the driving stage.

Bass treble boost and cut are ±15dB at 100Hz and 10kHz, respectively. Full peak-to-peak output is available up to at least 20kHz due to the high slew rate of the CA3140. The amplifier gain is 3dB down from its "flat" position at 70kHz.

Figure 27 shows another tone control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from terminal No. 3 to ground. A detailed analysis of this circuit is given in "An IC Operational TransconductanceAmplifier (OTA) With Power Capability" by L. Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No. 3, August, 1972.

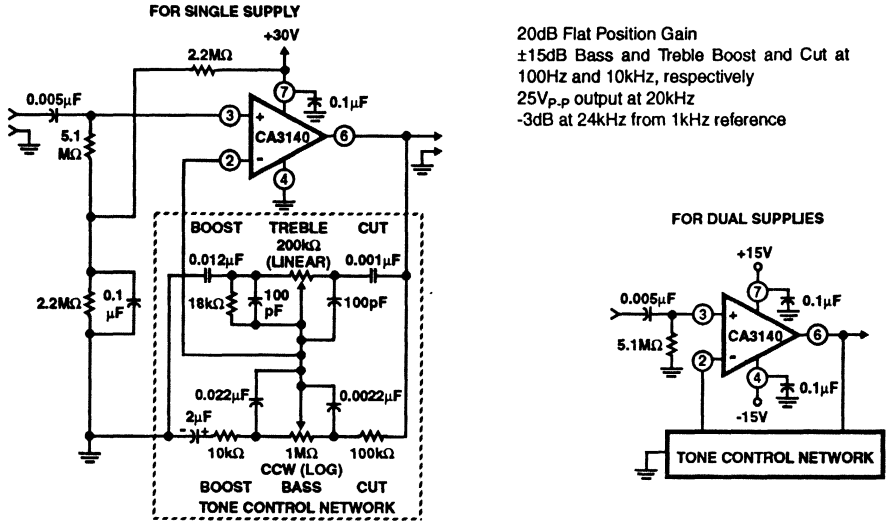


FIGURE 27. TONE CONTROL CIRCUIT USING CA3130 SERIES (20dB MIDBAND GAIN)

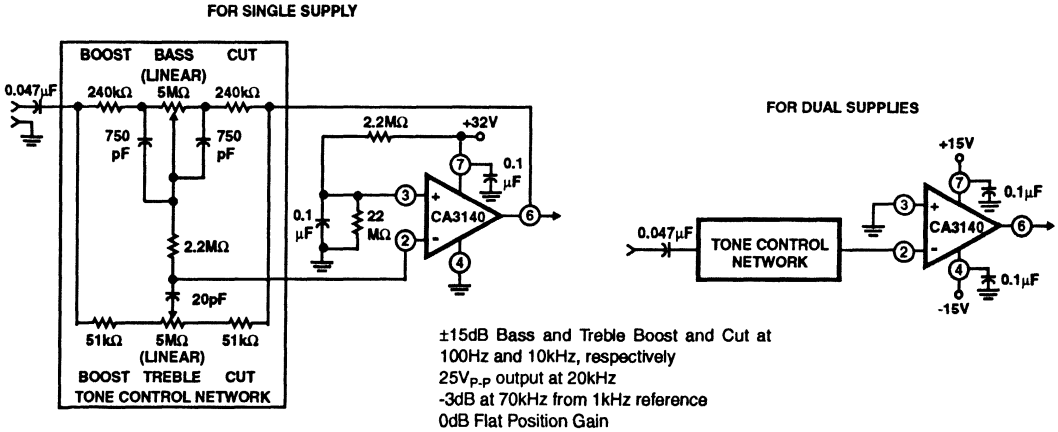
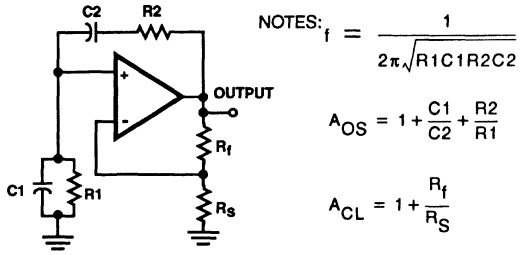


FIGURE 28. BAXANDALL TONE CONTROL CIRCUIT USING CA3140 SERIES

Wien Bridge Oscillator

Another application of the CA3140 that makes excellent use of its high input impedance, high slew rate, and high voltage qualities is the Wien Bridge sine wave oscillator. A basic Wien Bridge oscillator is shown in Figure 29. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency equation reduces to the familiar $f = {}^1/_2 \pi$ RC and the gain required for oscillation, A_{OSC} is equal to 3. Note that if C_2 is increased by a factor of four and R_2 is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus permitting a potentially higher operating frequency closer to the gain bandwidth product of the CA3140.



NOTES: $f = \frac{1}{2\pi\sqrt{R1C1R2C2}}$

$A_{OS} = 1 + \frac{C1}{C2} + \frac{R2}{R1}$

$A_{CL} = 1 + \frac{R_f}{R_S}$

FIGURE 29. BASIC WIEN BRIDGE OSCILLATOR CIRCUIT USING AN OPERATIONAL AMPLIFIER

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, R_S, is commonly replaced with some variable resistance element. Thus, through some control means, the value of R_S is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance is made to increase as the output amplitude is increased are a few of the elements often utilized.

Figure 30 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor (R_f of Figure 29). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1µF polycarbonate capacitors and 22MΩ for the frequency determining network, the operating frequency is 0.007Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of 180kHz will reach a slew rate of approximately 9V/µs when its amplitude is 16V peak-to-peak.

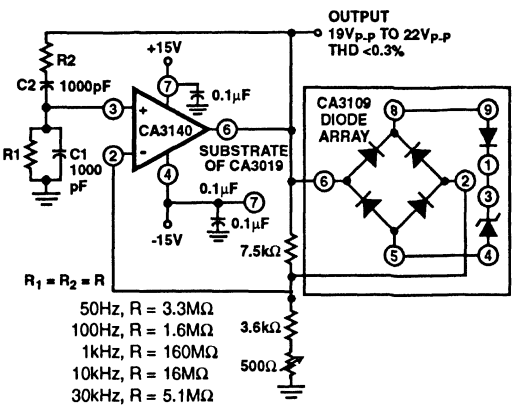


FIGURE 30. WIEN BRIDGE OSCILLATOR CIRCUIT USING CA3140 SERIES

Simple Sample-and-Hold System

Figure 31 shows a very simple sample-and-hold system using the CA3140 as the readout amplifier for the storage capacitor. The CA3080A serves as both input buffer amplifier and low feed-through transmission switch.* System offset nulling is accomplished with the CA3140 via its offset nulling terminals. A typical simulated load of 2kΩ and 30pF is shown in the schematic.

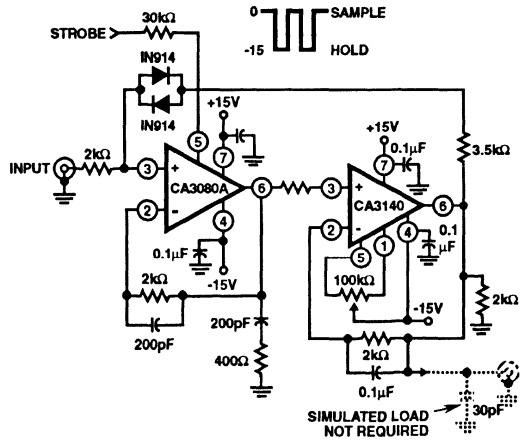


FIGURE 31. SAMPLE AND HOLD CIRCUIT

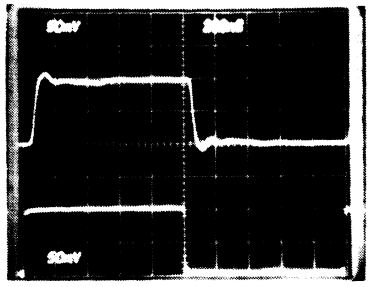
In this circuit, the storage compensation capacitance (C_1) is only 200pF. Larger value capacitors provide longer "hold" periods but with slower slew rates. The slew rate

$$\frac{dv}{dt} = \frac{i}{c} = 0.5mA/200pF = 2.5V/\mu s$$

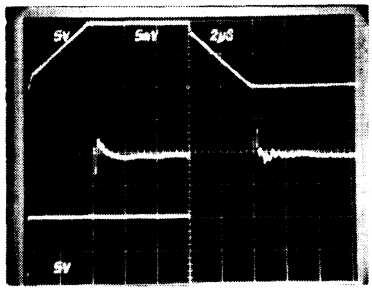
* ICAN-6668 "Applications of the CA3080 and CA 3080A High Performance Operational Transconductance Amplifiers".

Pulse "droop" during the hold interval is 170pA/200pF which is = 0.85µV/µs; (i.e., 170pA/200pF). In this case, 170pA

represents the typical leakage current of the CA3080A when strobed off. If C_1 were increased to 2000 pF, the "hold-droop" rate will decrease to 0.085μV/μs, but the slew rate would decrease to 0.25V/μs. The parallel diode network connected between terminal 3 of the CA3080A and terminal 6 of the CA3140 prevents large input signal feedthrough across the input terminals of the CA3080A to the 200pF storage capacitor when the CA3080A is strobed off. Figure 32 shows dynamic characteristic waveforms of this sample-and-hold system.

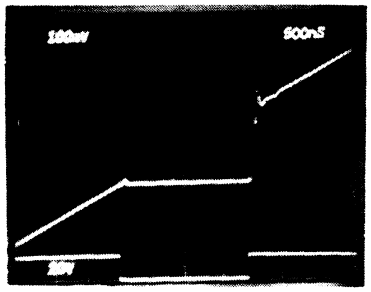


Top Trace: Output; 50mV/Div and 200ns/Div
Bottom Trace: Input; 50mV/Div and 200ns/Div



LARGE SIGNAL RESPONSE AND SETTLING TIME

Top Trace: Output Signal; 5V/Div and 2μs/Div
Center Trace: Difference of Input and Output Signals through Tektronix Amplifier 7A13; 5mV/Div and 2μs/Div
Bottom Trace: Input Signal; 5V/Div and 2μs/Div



SAMPLING RESPONSE

Top Trace: Output; 100mV/Div and 500ns/Div
Bottom Trace: Input; 20V/Div and 500ns/Div

FIGURE 32. SAMPLE AND HOLD SYSTEM DYNAMIC CHARACTERISTICS WAVEFORMS

Current Amplifier

The low input terminal current needed to drive the CA3140 makes it ideal for use in current amplifier applications such as the one shown in Figure 33.* In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R2/R1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100nA, with values shown, the load current presented to the supply will be 100μA; a much easier current to measure in many systems.

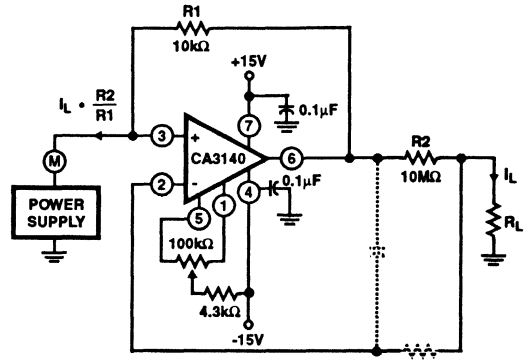


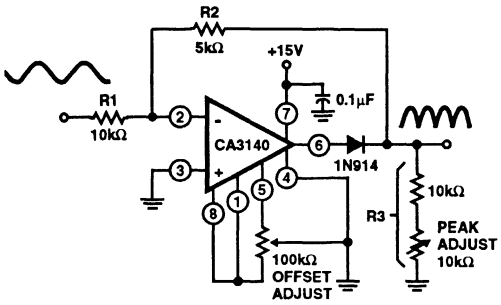
FIGURE 33. BASIC CURRENT AMPLIFIER FOR LOW CURRENT MEASUREMENT SYSTEMS

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output load capacitance and the potential oscillation in this situation. Essentially, the necessary high frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

Figure 34 shows a single supply, absolute value, ideal full-wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative going excursion of the input signal, the CA3140 functions as a normal inverting amplifier with a gain equal to -R2/R1. When the equality of the two equations shown in Figure 34 is satisfied, the full wave output is symmetrical.

* "Operational Amplifiers Design and Applications", J. G. Graeme, McGraw-Hill Book Company, page 308 - "Negative Immittance Converter Circuits".



$$GAIN = \frac{R2}{R1} = X = \frac{R3}{R1+R2+R3}$$

$$R3 = \left(\frac{X+X^2}{1-X}\right) R1$$

$$FOR\ X = 0.5\ \frac{5k\Omega}{10k\Omega} = \frac{R2}{R1}$$

$$R3 = 10k\Omega\left(\frac{0.75}{0.5}\right) = 15k\Omega$$

20Vp-p Input BW(-3dB) = 290kHz, DC Output (Avg) = 3.2V

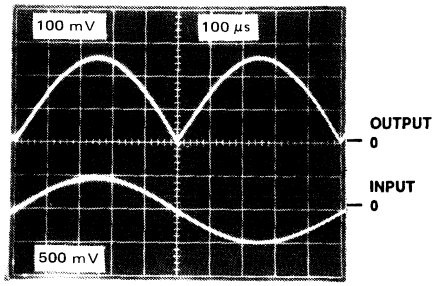


FIGURE 34. SINGLE SUPPLY, ABSOLUTE VALUE, IDEAL FULL WAVE RECTIFIER WITH ASSOCIATED WAVEFORMS

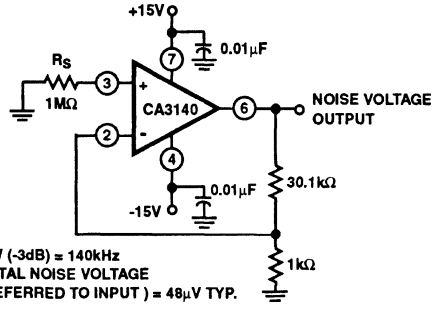
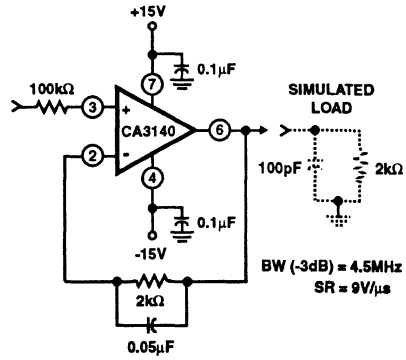
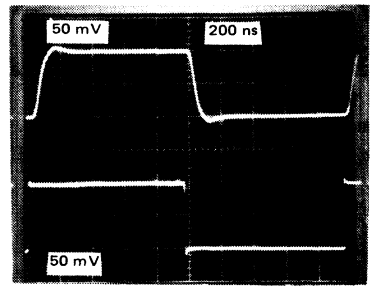


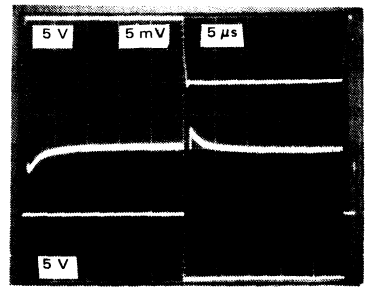
FIGURE 35. TEST CIRCUIT AMPLIFIER (30dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENT





(A) SMALL SIGNAL RESPONSE
50mV/Div and 200ns/Div

Top Trace: Output; 50mV/Div and 200ns/Div
Bottom Trace: Input; 50mV/Div and 200ns/Div



(B) INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME
(measurement made with Tektronix 7A13 differential amplifier)

Top Trace: Output Signal; 5V/Div and 5μs/Div
Center Trace: Difference Signal; 5mV/Div and 5μs/Div
Bottom Trace: Input Signal; 5V/Div and 5μs/Div

FIGURE 36. SPLIT SUPPLY VOLTAGE FOLLOWER TEST CIRCUIT AND ASSOCIATED WAVEFORMS

HARRIS SEMICONDUCTOR

CA3160

BiMOS Operational Amplifiers with MOSFET Input/CMOS Output

March 1993

Features

- MOSFET Input Stage Provides:
  - Very High Z_I = 1.5TΩ (1.5 x 10^{12}Ω) (Typ.)
  - Very Low I_I = 5pA Typ. at 15V Operation
    = 2pA Typ. at 5V Operation
- Common-Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can Be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample Hold Amplifiers
- Long Duration Timers/Monostables
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single Supply D/A Converter)
- Wien-Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers

Description

The CA3160A and CA3160 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA3160 series are frequency compensated versions of the popular CA3130 series.

Gate protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common-mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute in single supply applications.

A complementary symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10mV of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3160 Series circuits operate at supply voltages ranging from 5V to 16V, or ±2.5V to ±8V when using split supplies, and have terminals for adjustment of offset voltage for applications requiring offset null capability. Terminal provisions are also made to permit strobing of the output stage.

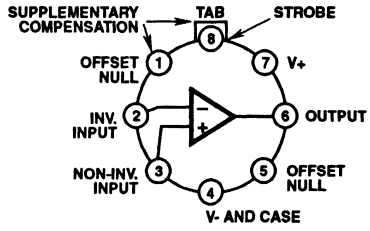
The CA3160A offers superior input characteristics over those of the CA3160.

Ordering Information

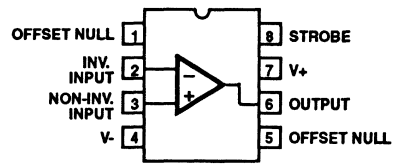
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3160AE	-55°C to +125°C	8 Lead Plastic DIP
CA3160AT	-55°C to +125°C	8 Pin TO-5 Can
CA3160E	-55°C to +125°C	8 Lead Plastic DIP
CA3160T	-55°C to +125°C	8 Pin TO-5 Can

Pinouts

CA3160
(TO-5 CAN)
TOP VIEW



CA3160
(PDIP)
TOP VIEW



NOTE: CA3160 Series devices have an on-chip frequency compensation network. Supplementary phase compensation or frequency roll-off (if desired) can be connected externally between terminals 1 and 8

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **976.1**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) . . . . . +16.0V
Differential Mode Input Voltage 8V
Input Voltage . . . . . (V+ +8V) to (V- -0.5V)
Input Current 1mA
Output Short Circuit Duration (Note 1) . . . . . Indefinite
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Temperature Range:
Operating (All Types) . . . . . -55°C to +125°C
Storage (All Types) . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications at T_A = +25°C, V+ = 15V, V- = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	LIMITS						UNITS
		CA3160A			CA3160			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage, V± = ±7.5V	$\|V_{IO}\|$	-	2	5	-	6	15	mV
Input Offset Current, V± = ±7.5V	$\|I_{IO}\|$	-	0.5	20	-	0.5	30	pA
Input Current, V± = ±7.5V	I_I	-	5	30	-	5	50	pA
Large-Signal Voltage Gain	A_{OL}	50	320	-	50	320	-	kV/V
V_O = 10V_{P-P}, R_L = 2kΩ		94	110	-	94	110	-	dB
Common-Mode Rejection Ratio	CMRR	80	95	-	70	90	-	dB
Common-Mode Input-Voltage Range	V_{ICR}	0	-0.5 to 12	10	0	-0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V\pm$, V± = ±7.5V	PSRR	-	32	150	-	32	320	µV/V
Maximum Output Voltage								
At R_L = 2kΩ	$V_{OM}+$	12	13.3	-	12	13.3	-	V
	$V_{OM}-$	-	0.002	0.01	-	0.002	0.01	V
At R_L = ∞	$V_{OM}+$	14.99	15	-	14.99	15	-	V
	$V_{OM}-$	-	0	0.01	-	0	0.01	V
Maximum Output Current:								
(Source) at V_O = 0V	$I_{OM}+$	12	22	45	12	22	45	mA
(Sink) at V_O = 15V	$I_{OM}-$	12	20	45	12	20	45	mA
Supply Current V_O = 7.5V, R_L = ∞	I+	-	10	15	-	10	15	mA
V_O = 0V, R_L = ∞ (Note 2)		-	2	3	-	2	3	mA
Input Offset Voltage Temperature Drift, $\Delta V_{IO}/\Delta T$		-	6	-	-	8	-	µV/°C

Specifications CA3160, CA3160A

Typical Values Intended Only for Design Guidance V+ = +7.5V, -V = -7.5V, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS		CA3160/CA3160A	UNITS
Input Offset Voltage Adjustment Range		10kΩ Across Terminals 4 and 5 or Terminals 4 and 1		±22	mV
Input Resistance	R_I			1.5	TΩ
Input Capacitance	C_I	f = 1MHz		4.3	pF
Equivalent Input Noise Voltage	e_N	BW = 0.2 MHz	R_S = 1 MΩ	40	μV
			R_S = 10MΩ	50	μV
Equivalent Input Noise Voltage	e_N	R_S = 100Ω	1kHz	72	$nV\sqrt{Hz}$
			10kHz	30	$nV\sqrt{Hz}$
Unity Gain Crossover Frequency	f_T			4	MHz
Slew Rate:	SR			10	V/μs
Transient Response, Rise Time	t_R	C_L = 25pF, R_L = 2kΩ, (Voltage Follower)		0.09	μs
Overshoot	OS			10	%
Settling Time (to <0.1%, V_{IN} = $4V_{P-P}$)	t_S			1.8	μs

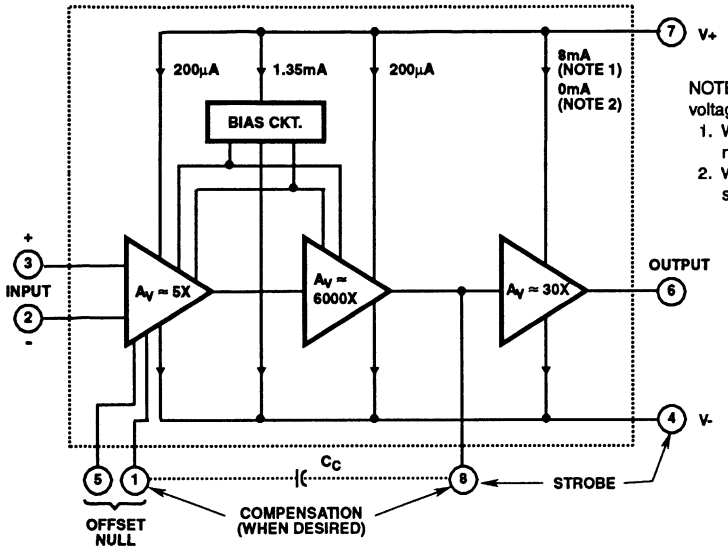
Typical Values Intended Only For Design Guidance V+ = +5V, V- = 0V, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	CA3160A	CA3160	UNITS
Input Offset Voltage	V_{IO}		2	6	mV
Input Offset Current	I_{IO}		0.1	0.1	pA
Input Current	I_I		2	2	pA
Common-Mode Rejection Ratio	CMRR		90	80	dB
Large Signal Voltage Gain	A_{OL}	V_O = $4V_{P-P}$, R_L = 5kΩ	100	100	kV/V
			100	100	dB
Common-Mode Input Voltage Range	V_{ICR}		0 to 2.8	0 to 2.8	V
Supply Current	I+	V_O = 5V, R_L = ∞	300	300	μA
		V_O = 2.5V, R_L = ∞	500	500	μA
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V+$	200	200	μV/V

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. I_{CC} typically increases by 1.5mA/MHz during operation.

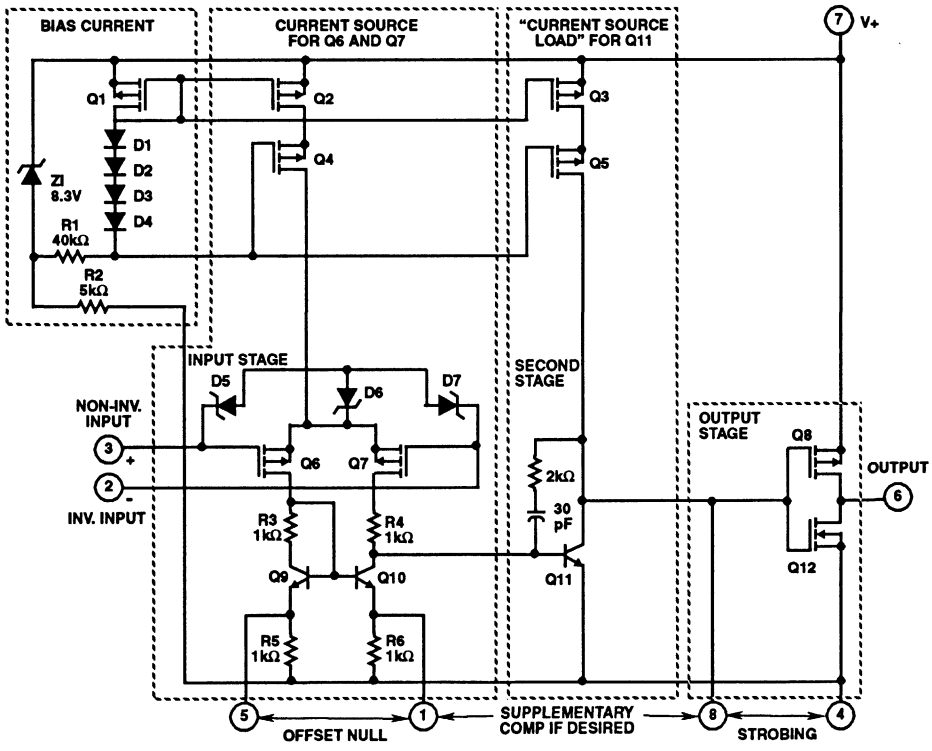
Block Diagram



NOTE: Total supply voltage (for indicated voltage gains) = 15V

1. With input terminals biased so that Terminal 6 potential is +7.5V above terminal 4.
2. With output terminal driven to either supply rail.

Schematic Diagram



NOTE: Diodes D5 Through D7 Provide Gate Oxide Protection For MOSFET Input Stage

Performance Curves

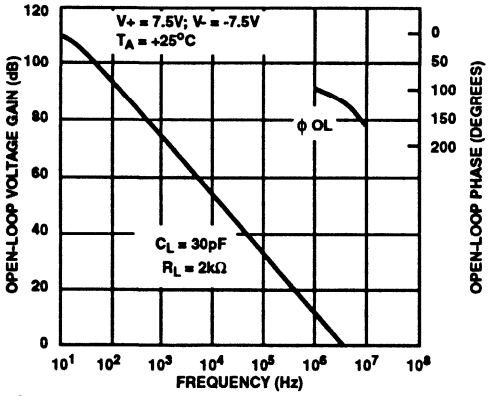


FIGURE 1. OPEN LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY

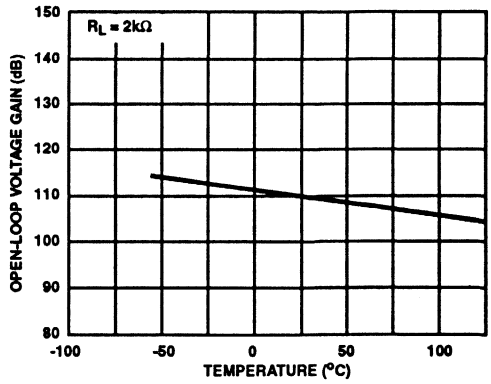


FIGURE 2. OPEN LOOP GAIN vs TEMPERATURE

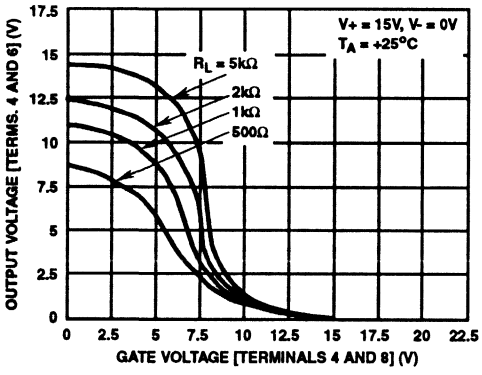


FIGURE 3. VOLTAGE TRANSFER CHARACTERISTICS OF COS/MOS OUTPUT STAGE

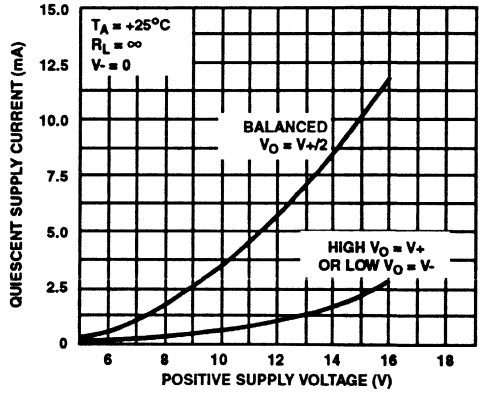


FIGURE 4. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

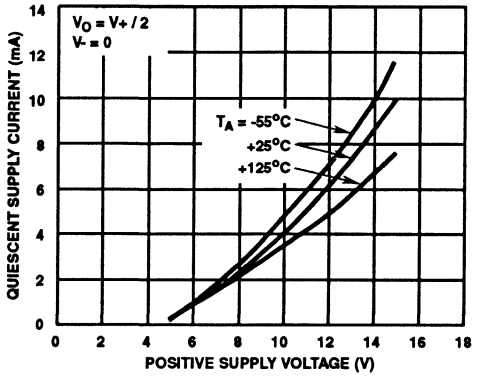


FIGURE 5. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

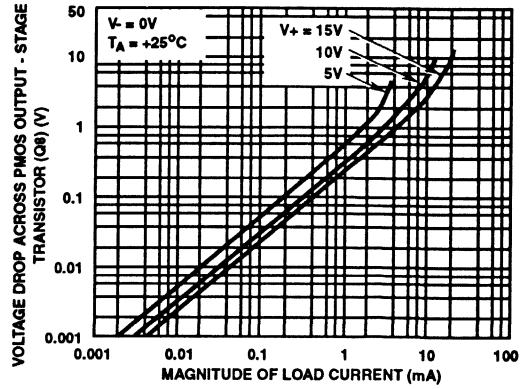


FIGURE 6. VOLTAGE ACROSS PMOS OUTPUT TRANSISTOR (Q8) vs LOAD CURRENT

Performance Curves (Continued)

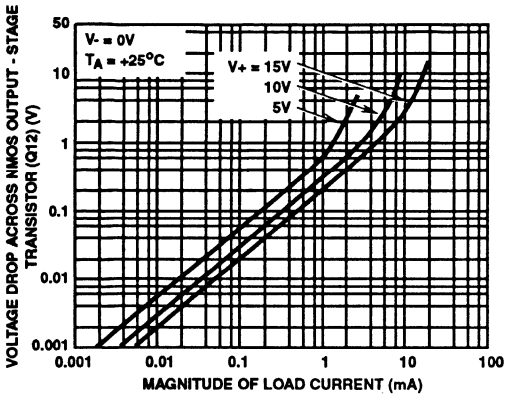


FIGURE 7. VOLTAGE ACROSS NMOS OUTPUT TRANSISTOR (Q12) vs LOAD CURRENT

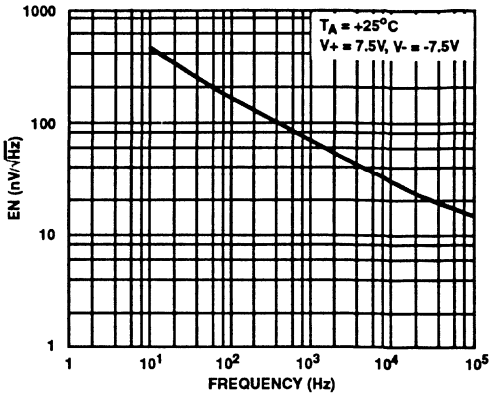


FIGURE 8. EQUIVALENT NOISE VOLTAGE vs FREQUENCY

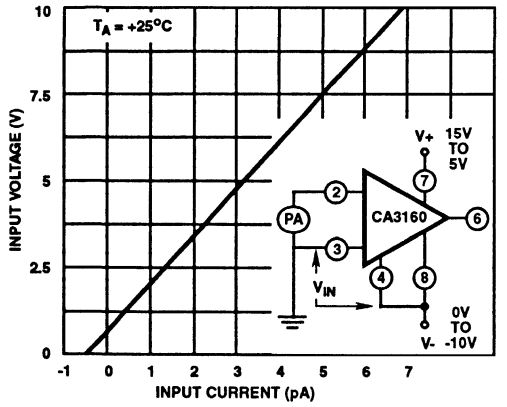


FIGURE 9. INPUT CURRENT vs COMMON MODE VOLTAGE

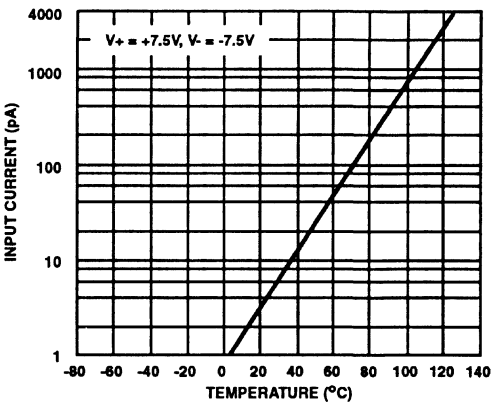


FIGURE 10. INPUT CURRENT vs AMBIENT TEMPERATURE

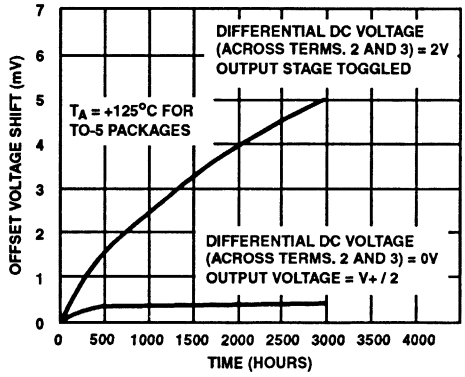


FIGURE 11. TYPICAL INCREMENTAL OFFSET VOLTAGE SHIFT vs OPERATING LIFE

Circuit Description

Refer to the Block Diagram of the CA3160 series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3160 series circuits are ideal for single supply operation. Three class A amplifier stages, having the individual gain capability and current consumption shown in the Block Diagram provide the total gain of the CA3160. A biasing circuit provides two potentials for common use in the first and second stages. Terminals 8 and 1 can be used to supplement the internal phase compensation network if additional phase compensation or frequency roll-off is desired. Terminals 8 and 4 can also be used to strobe the output stage into a low quiescent current state. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply-rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive MOS digital circuits in comparator applications).

Input Stages - The circuit of the CA3160 is shown in the Schematic Diagram. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000Ω potentiometer across Terminals 1 and 5 and the potentiometer slider arm to Terminal 4. Cascode-connected PMOS transistors Q2, Q4, are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D7 provide gate-oxide protection against high-voltage transients, including static electricity during handling for Q6 and Q7.

Second-Stage - Most of the voltage gain in the CA3160 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is described later. Miller Effect compensation (roll off) is accomplished by means of the 30pF capacitor and 2kΩ resistor connected between the base and collector of transistor Q11. These internal components provide sufficient compensation for unity gain operation in most applications. However, additional compensation, if desired, may be used between Terminals 1 and 8.

Bias-Source Circuit - At total supply voltages, somewhat above 8.3V, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3V across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5V for PMOS transistors Q4 and Q5 with respect to Terminal 7. A potential of about 2.2V is developed across diode-connected PMOS transistor Q1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected" to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200μA current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3V, zener diode Z1 becomes nonconductive and the potential, developed across series-connected R1, D1 - D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3V. Operation at total supply voltages below about 4.5V results in seriously degraded performance.

Output Stage - The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Figure 3. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01% accuracy levels, including the negative supply rail.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000Ω potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input Current Variation with Common Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3160 Series Op-Amps is typically 5pA at T_A = +25°C when Terminals 2 and 3 are at a common-mode potential of +7.5V with respect to negative supply Terminal 4. Figure 9 contains data showing the variation of input current as a function of common-mode input voltage at T_A = +25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1pA, provided the common-mode input voltage does not exceed 2V. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors.

Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3160 is also internally tied to Terminal 4, input Terminal 3 is essentially "guarded" from spurious leakage currents.

Input-Current Variation with Temperature

The input current of the CA3160 Series circuits is typically 5pA at +25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Figure 10 provides data on the typical variation of input bias current as a function of temperature in the CA3160.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3160. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

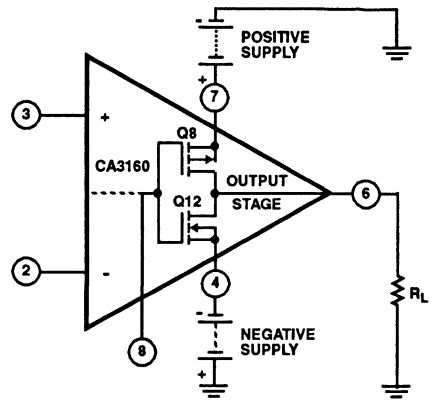
It is well known that the characteristics of a MOSFET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3160 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terminals 2 and 3. Figure 11 shows typical data pertinent to shifts in offset voltage encountered with CA3160 devices in TO-5 packages during life testing. At lower temperatures (TO-5 and plastic) for example at +85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The 2V dc differential voltage example represents conditions when the amplifier output state is "toggled", e.g., as in comparator applications.

Power Supply Considerations

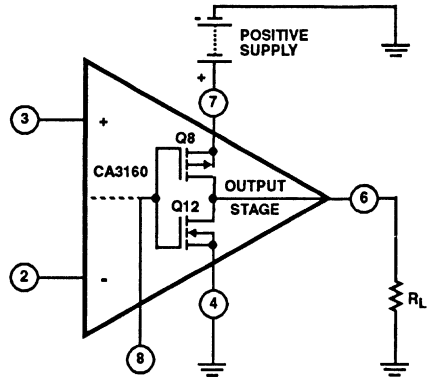
Because the CA3160 is very useful in single supply applications, it is pertinent to review some considerations relating to power supply current consumption under both single and dual supply service. Figures 12(A) and 12(B) show the CA3160 connected for both dual and single supply operation.

Dual-supply operation: When the output voltage at Terminal 6 is 0V, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Figure 4 shows typical quiescent supply-current vs. supply voltage for the CA3160 operated under these conditions.



(A) DUAL POWER SUPPLY OPERATION



(B) SINGLE POWER SUPPLY OPERATION

FIGURE 12. CA3160 OUTPUT STAGE IN DUAL AND SINGLE POWER SUPPLY OPERATION

Since the output stage is operating as a Class A amplifier, the supply current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Figure 3). If either Q8 or Q12 are swung out of their linear regions toward cutoff (a non-linear region), there will be

a corresponding reduction in supply-current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply current to series connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3160, however, continue to draw modest supply-current (see the lower curve in Figure 4) even though the output stage is strobed off. Figure 12(A) shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now-be assumed that a load-resistance of nominal value (e.g., 2kΩ) is connected between Terminal 6 and ground in the circuit of Figure 12(B). Let it further be assumed again that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Figure 6 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply voltages. Figure 3 shows the voltage transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3160 is most advantageous in applications where in the source resistance of the input signal is on the order of 1MΩ or more. In this case, the total input-referred noise voltage is typically only 40μV when the test circuit amplifier of Figure 13 is operated at a total supply voltage of 15V. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1MΩ, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

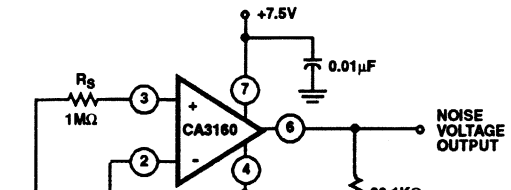
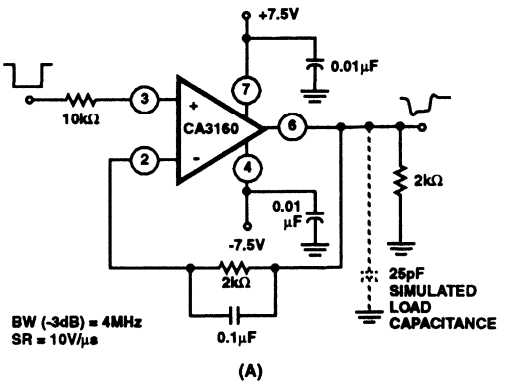
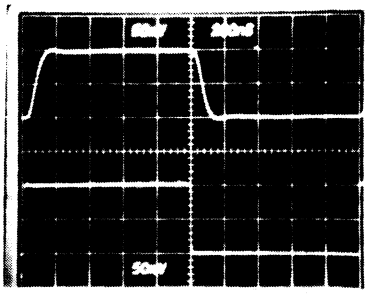


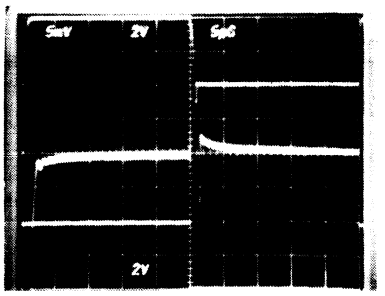
FIGURE 13. TEST CIRCUIT AMPLIFIER (30dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENTS



(A)



(B) SMALL SIGNAL RESPONSE
Top Trace: Output
Bottom Trace: Input



(C) INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME
Top Trace: Output Signal
Center Trace: Difference Signal 5mV/Div.
Bottom Trace: Input Signal

FIGURE 14. SPLIT-SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS

Typical Applications

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3160, are particularly suited to service as voltage followers. Figure 14 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3160 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Figure 15 together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Figure 15B with input-signal ramping. The waveforms in Figure 15C show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5V below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Figure 15C also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3160 in a single supply voltage follower application.

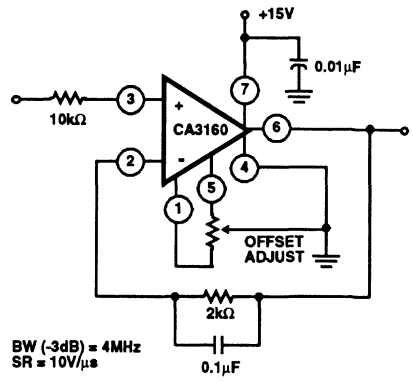
9 Bit CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Figure 16. This system combines the concepts of multiple-switch CMOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3160 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10V logic levels are used in the circuit of Figure 16.

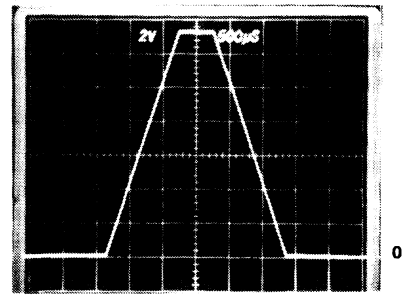
* "Digital-to-Analog Conversion Using the Harris CD4007A COS/MOS IC", Application Note AN6080.

The circuit uses an R/2R voltage-ladder network, with the output-potential obtained directly by terminating the ladder arms at either the positive or the negative power supply terminal. Each CP4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000Ω resistors from the same manufacturing lot.

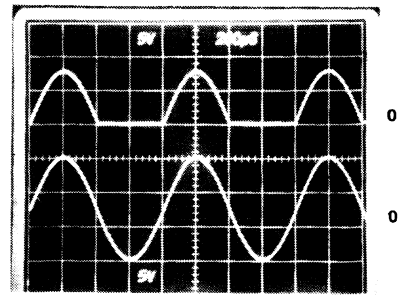
A single 15V supply provides a positive bus for the CA3160 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10V level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.



(A)



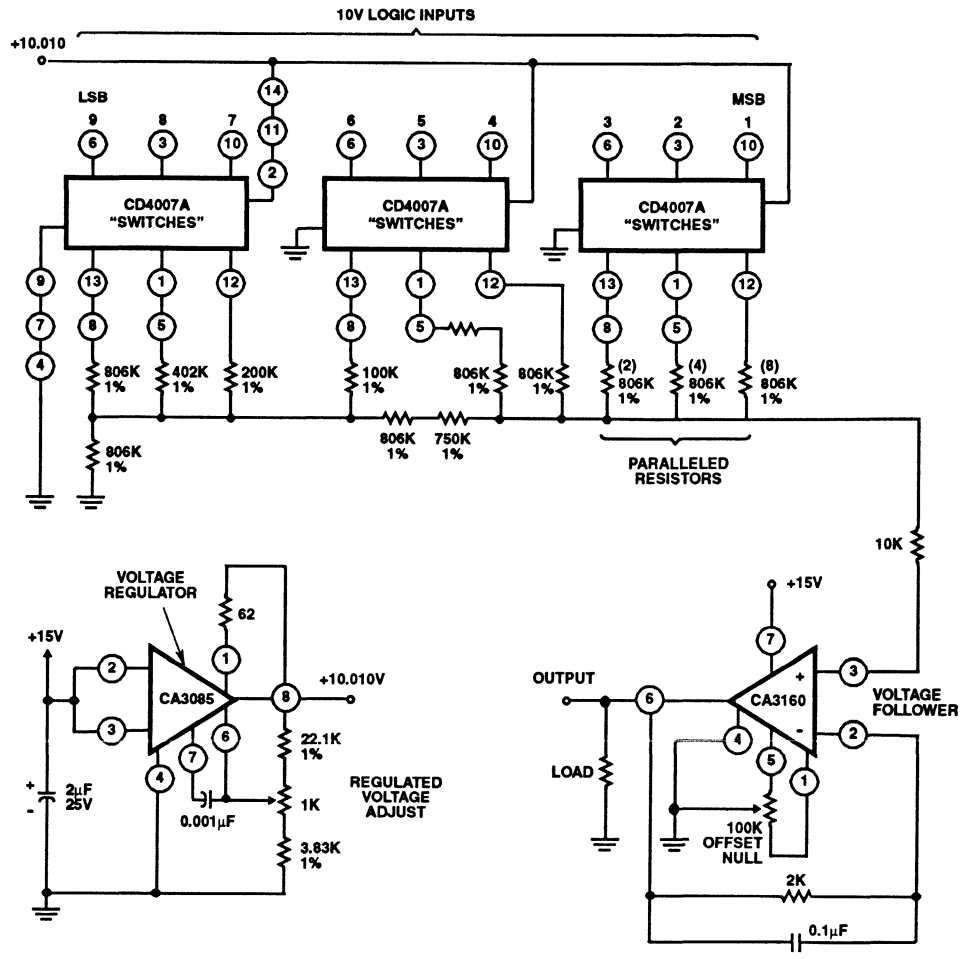
(B) OUTPUT SIGNAL WITH INPUT-SIGNAL RAMPING.



(C) OUTPUT WAVEFORM WITH GROUND REFERENCE SINE WAVE INPUT

Top Trace: Output
Bottom Trace: Input

FIGURE 15. SINGLE SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS. (e.g., FOR USE IN SINGLE SUPPLY D/A CONVERTER; SEE FIGURE 9 IN AN6080)



BIT	REQUIRED RATIO-MATCH
1	Standard
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6 - 9	±1% ABS.

FIGURE 16. 9 BIT DAC USING CMOS DIGITAL SWITCHES AND CA3160

Error-Amplifier in Regulated Power Supplies

The CA3160 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero.

The circuit shown in Figure 17 uses a CA3160 as an error amplifier in a continuously adjustable 1A power supply. One of the key features of this circuit is its ability to regulate down to the vicinity of 0V with only one dc power supply input.

An RC network, connected between the base of the output drive transistor and the input voltage, prevents "turn-on overshoot", a condition typical of many operational amplifier regulator circuits. As the amplifier becomes operational, this RC network ceases to have any influence on the regulator performance.

Precision Voltage-Controlled Oscillator

The circuit diagram of a precision voltage-controlled oscillator is shown in Figure 18. The oscillator operates with a tracking error in the order of 0.02% and a temperature coefficient of 0.01%/°C. A multivibrator (A1) generates pulses of constant amplitude (V) and width (T2). Since the output (Terminal 6) of A1 (a CA3130) can swing within about 10mV of either supply-rail, the output pulse amplitude (V) is essentially equal to V+. The average output voltage (E_{AVG} = V T2/T1) is applied to the non-inverting Input terminal of comparator A2 via an integrating network R3, C2. Comparator A2 operates to establish circuit conditions such that E_{AVG} = V1. This circuit condition is accomplished by feeding an output signal from terminal 6 of A2 through R4, D4 to the inverting terminal (Terminal 2) of A1, thereby adjusting the multivibrator interval, T3.

Voltmeter With High Input Resistance

The voltmeter circuit shown in Figure 19 illustrates an application in which a number of the CA3160 characteristics are exploited. Range-switch SW1 is ganged between input and output circuitry to permit selection of the proper output voltage for feedback to Terminal 2 via 10kΩ current-limiting resistor. The circuit is powered by a single 8.4V mercury battery. With zero input signal, the circuit consumes somewhat less than 500μA plus the meter current required to indicate a given voltage. Thus, at full scale input, the total supply current rises to slightly more than 1500μA.

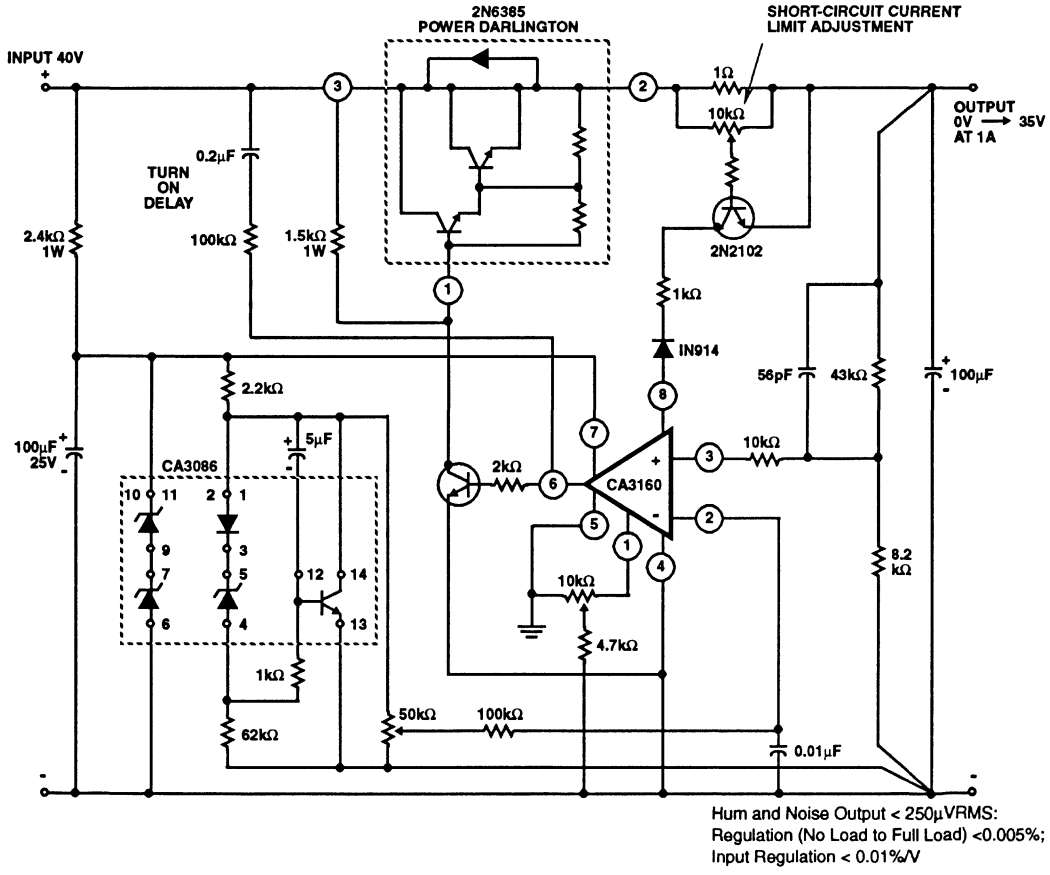


FIGURE 17. VOLTAGE REGULATOR CIRCUIT (0.1V TO 35V AT 1A)

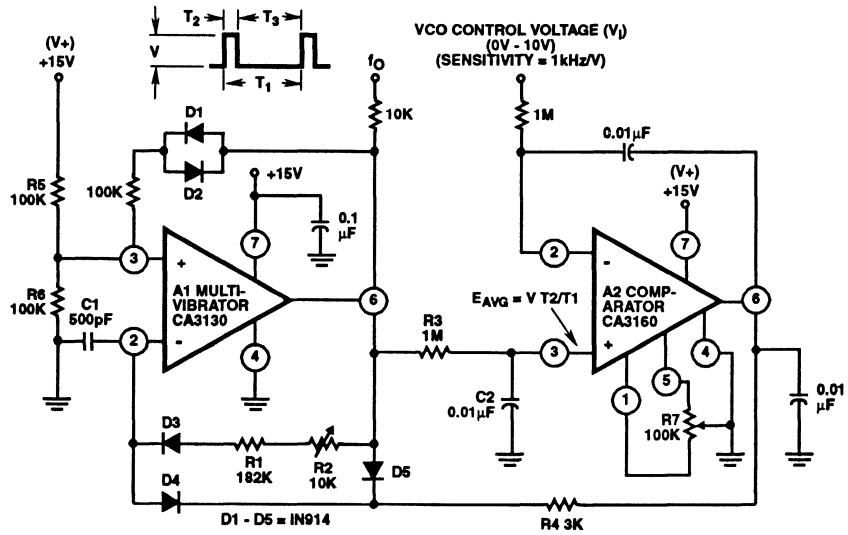


FIGURE 18. VOLTAGE CONTROLLED OSCILLATOR

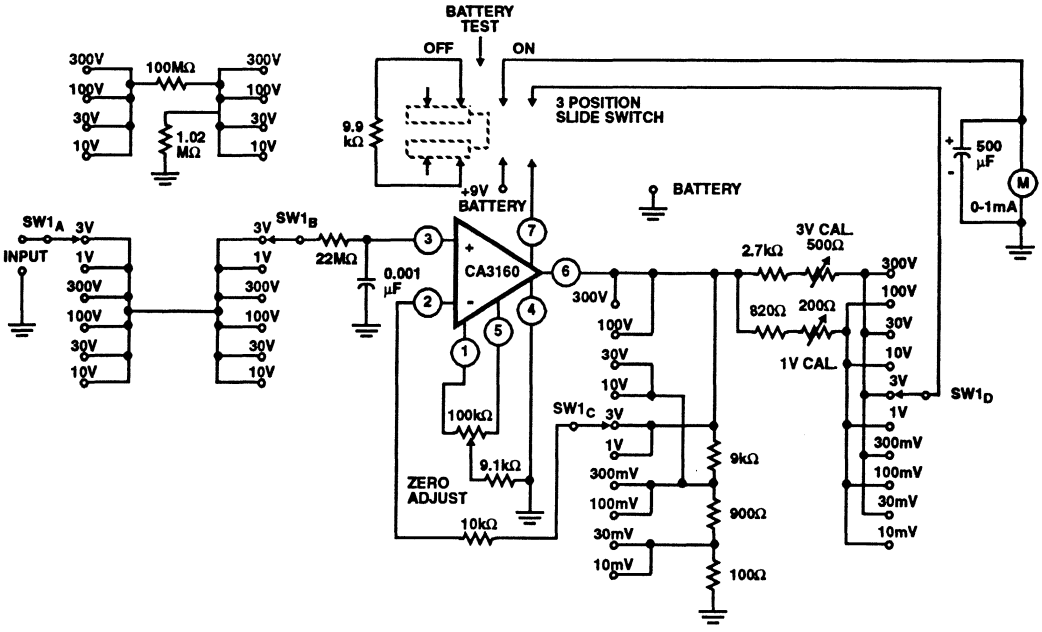
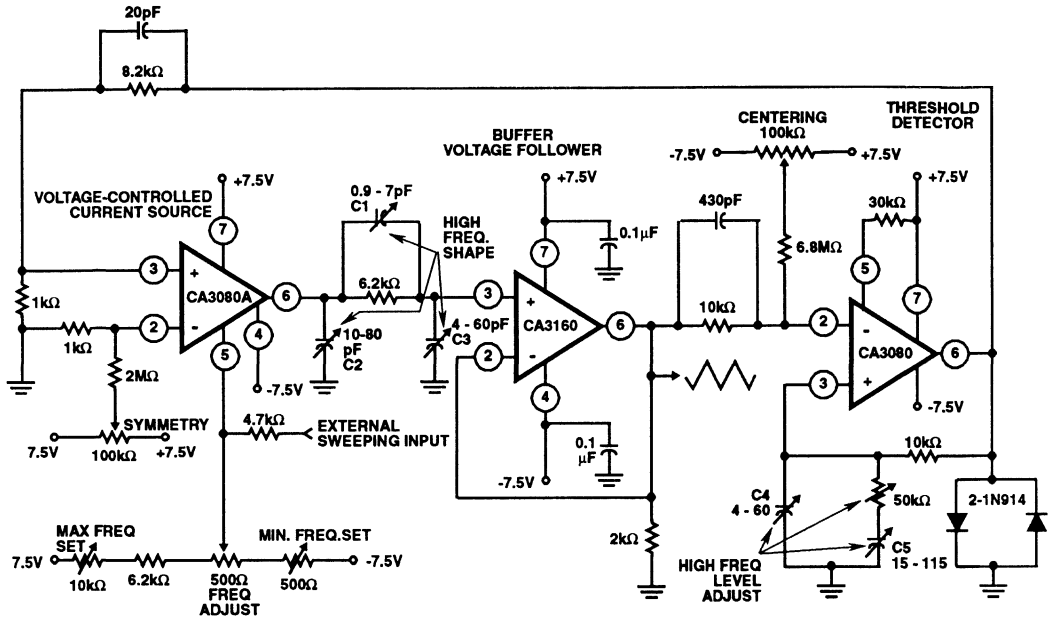


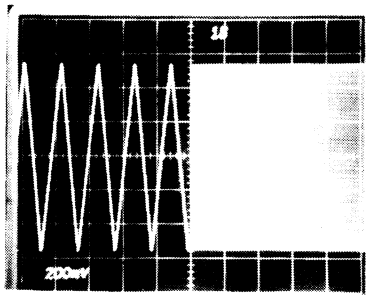
FIGURE 19. HIGH INPUT RESISTANCE DC VOLTMETER

Function Generator

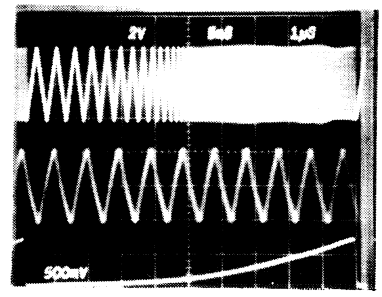
A function generator having a wide tuning range is shown in Figure 20. The adjustment range, in excess of 1,000,000/1, is accomplished by a single potentiometer. Three operational amplifiers are utilized: a CA3160 as a voltage follower, a CA3080 as a high speed comparator, and a second CA3080A as a programmable current source. Three variable capacitors C1, C2, and C3 shape the triangular signal between 500kHz and 1MHz. Capacitors C4, C5, and the trimmer potentiometer in series with C5 maintain essentially constant (+10%) amplitude up to 1MHz.



(A)

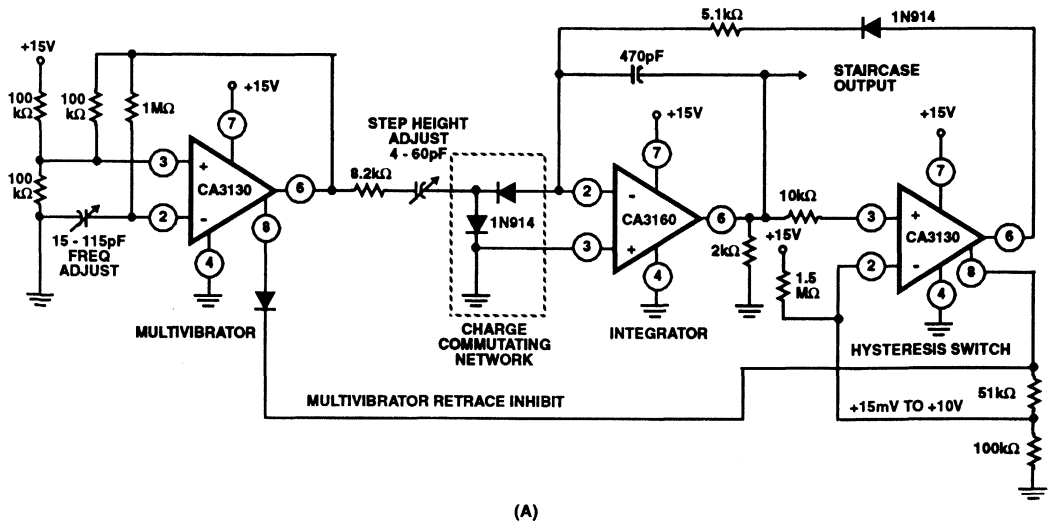


(B) TWO-TONE OUTPUT SIGNAL FROM THE FUNCTION GENERATOR. A SQUARE WAVE SIGNAL MODULATES THE EXTERNAL SWEEPING INPUT TO PRODUCE 1Hz AND 1MHz, SHOWING THE 1,000,000/1 FREQUENCY RANGE OF THE FUNCTION GENERATOR

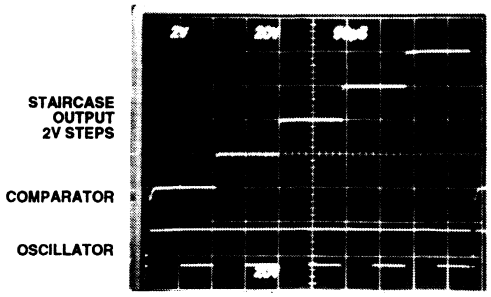


(C) TRIPLE-TRACE OF THE FUNCTION GENERATOR SWEEPING TO 1MHz. THE BOTTOM TRACE IS THE SWEEPING SIGNAL AND THE TOP TRACE IS THE ACTUAL GENERATOR OUTPUT. THE CENTER TRACE DISPLAYS THE 1MHz SIGNAL VIA DELAYED OSCILLOSCOPE TRIGGERING OF THE UPPER SWEPT OUTPUT SIGNAL

FIGURE 20. 1,000,000/1 SINGLE CONTROL FUNCTION GENERATOR: 1MHz to 1Hz



(A)



(B) STAIRCASE GENERATOR WAVEFORM
Top Trace: Staircase Output 2V Steps
Center Trace: Comparator
Bottom Trace: Oscillator

FIGURE 21. STAIRCASE GENERATOR CIRCUIT

Staircase Generator

Figure 21 shows a staircase generator circuit utilizing three CMOS operational amplifiers. Two CA3130's are used; one as a multivibrator, the other as a hysteresis switch. The third amplifier, a CA3160, is used as a linear staircase generator.

Picoammeter Circuit

Figure 22 is a current-to-voltage converter configuration utilizing a CA3160 and CA3140 to provide a picoampere meter for 13pA full scale meter deflection. By placing Terminals 2 and 4 of the CA3160 at ground potential, the CA3160 input is operated in the "guarded mode". Under this operating condition, even slight leakage resistance present between Terminals 3 and 2 or between Terminals 3 and 4 would result in zero voltage across this leakage resistance, thus substantially reducing the leakage current.

If the CA3160 is operated with the same voltage on input Terminals 3 and 2 as on Terminal 4, a further reduction in the input current to the less than one picoampere level can be achieved as shown in Figure 9.

To further enhance the stability of this circuit, the CA3160 can be operated with its output (Terminal 6) near ground, thus markedly reducing the dissipation by reducing the supply current to the device.

The CA3140 stage serves as a X100 gain stage to provide the required plus and minus output swing for the meter and feedback network. A 100-to-1 voltage divider network consisting of a 9.9kΩ resistor in series with a 100Ω resistor sets the voltage at the 10GΩ resistor (in series with Terminal 3) to ±30mV full-scale deflection. This 30mV signal results from ±3V appearing at the top of the voltage divider network which also drives the meter circuitry.

By utilizing a switching technique in the meter circuit and in the 9.9kΩ and 100Ω network similar to that used in voltmeter circuit shown in Figure 19, a current range of 3pA to 1nA full scale can be handled with the single 10GΩ resistor.

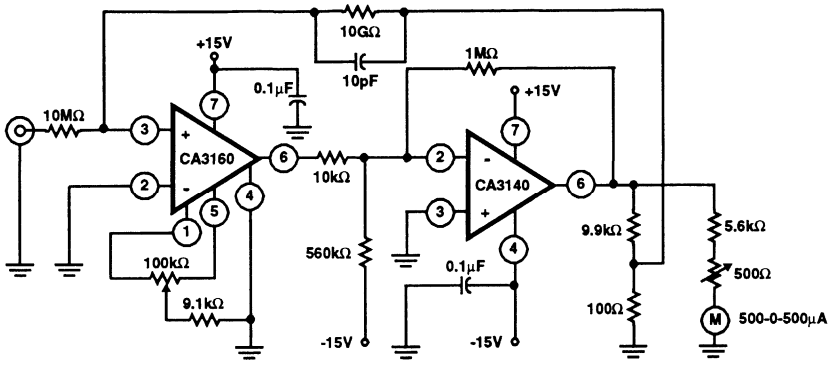
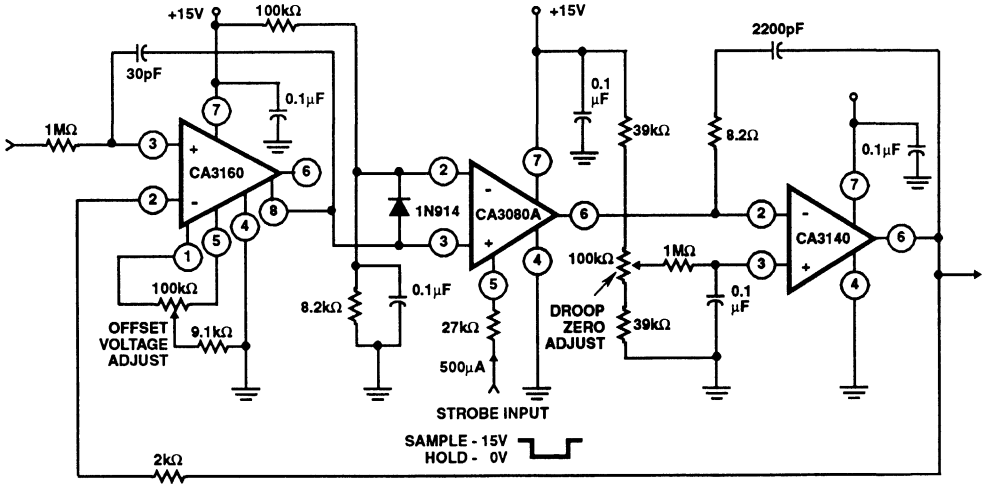
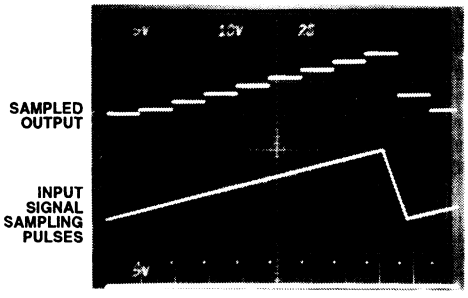


FIGURE 22. CURRENT-TO-VOLTAGE CONVERTER TO PROVIDE A PICOAMMETER WITH ±3pA FULL SCALE DEFLECTION

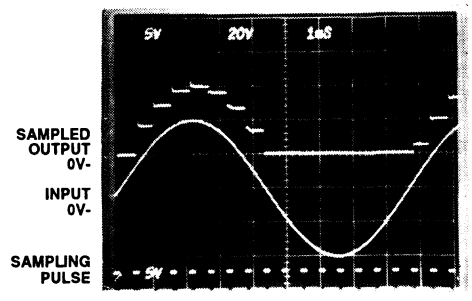


(A)



(B) SAMPLE AND HOLD WAVEFORM

Top Trace: Sampled Output
Center Trace: Input Signal
Bottom Trace: Sampling Pulses



(C) SAMPLE AND HOLD WAVEFORM

Top Trace: Sampled Output
Center Trace: Input
Bottom Trace: Sampling Pulses

FIGURE 23. SINGLE SUPPLY SAMPLE AND HOLD SYSTEM, INPUT 0V TO 10V

Single Supply Sample-and-Hold System

Figure 23 shows a single supply sample-and-hold system using a CA3160 to provide a high input impedance and an input-voltage range of 0V to 10V. The output from the input buffer integrator network is coupled to a CA3080A. The CA3080A functions as a strobeable current source for the CA3140 output integrator and storage capacitor. The CA3140 was chosen because of its low output impedance and constant gain-bandwidth product. Pulse "droop" during the hold interval can be reduced to zero by adjusting the 100kΩ bias-voltage potentiometer on the positive input of the CA3140. This zero adjustment sets the CA3080A output voltage at its zero current position. In this sample-and-hold circuit it is essential that the amplifier bias current be reduced to zero to minimize output signal current during the hold mode. Even with 320mV at the amplifier bias circuit terminal (5) at least 1100pA of output current will be available.

Wien Bridge Oscillator

A simple, single supply Wien Bridge oscillator using a CA3160 is shown in Figure 24. A pair of parallel-connected 1N914 diodes comprise the gain-setting network which standardizes the output voltage at approximately 1.1V. The 500Ω potentiometer is adjusted so that the oscillator will always start and the oscillation will be maintained. Increasing the amplitude of the voltage may lower the threshold level for starting and for sustaining the oscillation, but will introduce more distortion.

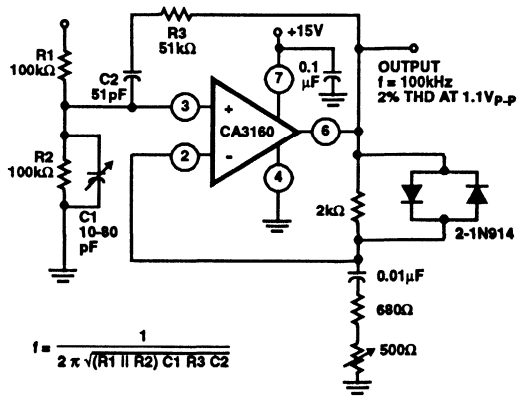


FIGURE 24. SINGLE SUPPLY WEIN BRIDGE OSCILLATOR

Operation with Output Stage Power Booster

The current sourcing and sinking capability of the CA3160 output stage is easily supplemented to provide power-boost capability. In the circuit of Figure 25, three CMOS transistor-pairs in a single CA3600 IC array are shown parallel-connected with the output stage in the CA3160. In the Class A mode of CA3600E shown, a typical device consumes 20mA of supply current at 15V operation. This arrangement boosts the current-handling capability of the CA3160 output stage by about 2.5X.

The amplifier circuit in Figure 25 employs feedback to establish a closed-loop gain of 20dB. The typical large-signal-bandwidth (-3dB) is 190kHz.

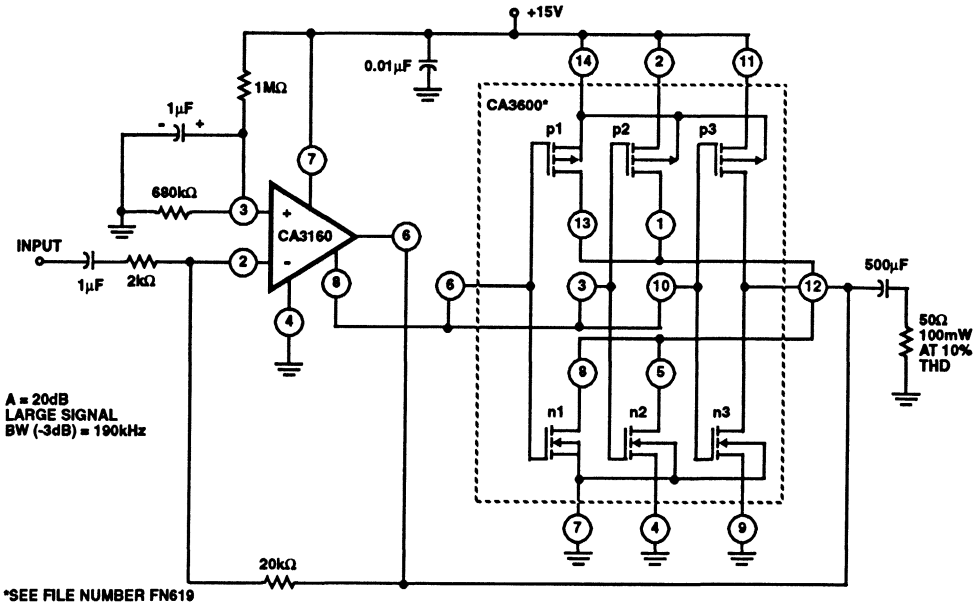


FIGURE 25. CMOS TRANSISTOR ARRAY (CA3600E) CONNECTED AS POWER BOOSTER IN THE OUTPUT STAGE OF THE CA3160

HARRIS SEMICONDUCTOR

CA3193

BiCMOS Precision Operational Amplifiers

March 1993

Features

- Low V_{IO}
  - CA3193A ..... .200μV (Max)
  - CA3193 ..... .500μV (Max)
- Low $\Delta V_{IO}/\Delta T$
  - CA3193A ..... 3μV/°C (Max)
  - CA3193 ..... 5μV/°C (Max)
- Low I_{IO} and I_I
- Low $\Delta I_{IO}/\Delta T$: CA3193 ..... 150pA/°C (Max)
- Low $\Delta I_I/\Delta T$: CA3193 ..... 3.7nA/°C (Max)

Applications

- Thermocouple Preamplifiers
- Strain Gauge Bridge Amplifiers
- Summing Amplifiers
- Differential Amplifiers
- Bilateral Current Sources
- Log Amplifiers
- Differential Voltmeters
- Precision Voltage References
- Active Filters
- Buffers
- Integrators
- Sample-and-Hold Circuits
- Low Frequency Filters

Description

The CA3193A and CA3193 are ultra-stable, precision instrumentation, operational amplifiers that employ both PMOS and bipolar transistors on a single monolithic chip. The CA3193A and CA3193 amplifiers are internally phase compensated and provide a gain bandwidth product of 1.2MHz. They are pin compatible with the industry 741 series and many other IC op amps, and may be used as replacements for 741 series types in most applications.

The CA3193A and CA3193 can also be used as functional replacements for op amp types 725, 108A, OP-5, OP-7, LM11 and LM714 in many applications where nulling is not employed. Because of their low offset voltage and low offset voltage vs temperature coefficient the CA3193A and CA3193 amplifiers have a wider range of applications than most op amps and are particularly well suited for use as thermocouple amplifiers, high gain filters, buffer, strain gauge bridge amplifiers and precision voltage references.

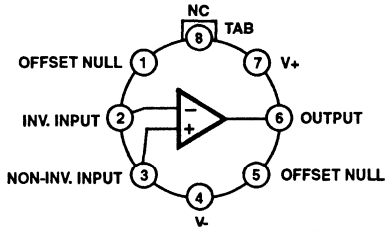
The two types in the CA3193 series are functionally identical. The CA3193A and CA3193 operate from supply voltages of ±3.5V to ±18V.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3193AE	-25°C to +85°C	8 Lead Plastic DIP
CA3193AT	-25°C to +85°C	8 Pin TO-5 Can
CA3193E	0°C to +70°C	8 Lead Plastic DIP
CA3193T	0°C to +70°C	8 Pin TO-5 Can

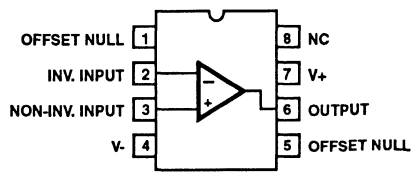
Pinouts

CA3193
(TO-5 CAN)
TOP VIEW



NOTE: Pin 4 is connected to case on S and T suffix.

CA3193
(PDIP)
TOP VIEW



File Number **1249.1**

Specifications CA3193, CA3193A

Absolute Maximum Ratings

DC Supply Voltage ..... ±18V
Differential Input Voltage 5V
DC Input Voltage ..... (V+ -4), V-
Input Current 1mA
Power Dissipation
  Without Heat Sink
    Up to +55°C 630mW
    Above +55°C ..... Derate Linearly 6.67mW/°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Output Short Circuit Duration (Note 1) ..... Indefinite
Lead Temperature (Soldering 10 Sec.) ..... +300 °C

Operating Conditions

Operating Temperature Range
  CA3193A ..... $-25°C \leq T_A \leq +85°C$
  CA3193 ..... $0°C \leq T_A \leq +70°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = 25°C, V+ = 15V and V- = -15V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	LIMITS						UNITS
		CA3193A			CA3193			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage $\lvert V_{IO} \rvert$	V_{IO}	-	140	200	-	300	500	µV
V_{IO} at Max.Temp.		-	-	380	-	-	725	µV
Input Offset Voltage Temperature Coefficient (Over Specified Temperature Range for Each Device)	$\Delta V_{IO}/\Delta T$	-	1	3	-	1	5	µV/°C
Input Offset Current	I_{IO}	-	3	5	-	5	10	nA
$\lvert I_{IO} \rvert$ at Max. Temp.		-	-	11	-	-	17	nA
Input Offset Current Temp. Coefficient (Over Specified Temperature Range for Each Device)	$\Delta I_{IO}/\Delta T$	-	0.03	0.10	-	0.04	0.15	nA/°C
Input Bias Current	I_I	-	10	20	-	20	40	nA
$\lvert I_B \rvert$ at Max. Temp.		-	-	83	-	-	207	nA
Input Bias Current Temp. Coefficient	$\Delta I_I/\Delta T$	-	0.10	1.18	-	0.15	3.70	nA/°C
Input Noise Voltage (0.1 to 10Hz)	$e_{N\ P-P}$	-	0.36	-	-	0.36	-	μV_{P-P}
Input Noise Voltage Density	e_N							
f = 10Hz		-	25	-	-	25	-	$nV/\sqrt{Hz}$
f = 100Hz		-	25	-	-	25	-	$nV/\sqrt{Hz}$
f = 1000Hz		-	24	-	-	24	-	$nV/\sqrt{Hz}$
f = 10kHz		-	24	-	-	24	-	$nV/\sqrt{Hz}$
f = 100kHz		-	22	-	-	22	-	$nV/\sqrt{Hz}$
Input Noise Current (0.1 to 10 Hz)	$I_{N\ P-P}$	-	12	20	-	12	20	pA_{P-P}
Input Noise Current Density	I_N							
f = 10Hz		-	0.83	-	-	0.83	-	$pA/\sqrt{Hz}$
f = 100Hz		-	0.80	-	-	0.80	-	$pA/\sqrt{Hz}$
f = 1000Hz		-	0.75	-	-	0.75	-	$pA/\sqrt{Hz}$
f = 10kHz		-	0.72	-	-	0.72	-	$pA/\sqrt{Hz}$
f = 100kHz		-	0.60	-	-	0.60	-	$pA/\sqrt{Hz}$
Common-Mode Input Voltage Range	V_{ICR}	-12	- 13.5 to 11.5	10	-12	-13.5 to 11.5	10	V

Electrical Specifications T_A = 25°C, V+ = 15V and V- = -15V, Unless Otherwise Specified. **(Continued)**

PARAMETERS	SYMBOL	LIMITS						UNITS
		CA3193A			CA3193			
		MIN	TYP	MAX	MIN	TYP	MAX	
Common-Mode Rejection Ratio	V_{CM} = V_{ICR}	110	115	-	100	110	-	dB
		-	1.78	3.16	-	3.16	10	µV/V
Power Supply Rejection Ratio $\Delta V_{IO}/\Delta V\pm$	PSRR	100	130	-	100	130	-	dB
		-	0.316	10	-	0.316	10	µV/V
Maximum Output Voltage Swing ($R_L \geq 2K\Omega$)	V_{OM}	±13.0	±13.5	-	±13.0	±13.5	-	V
Large-Signal Voltage Gain (V_O = ±10)								
$R_L \geq 2K\Omega$	A_{OL}	110	115	-	100	110	-	dB
$R_L \geq 10K\Omega$		-	125	-	-	115	-	dB
Short-Circuit Output Current to the Opposite Rail	I_{OM} +, I_{OM}-	-25	±7	25	-25	±7	25	mA
Slew Rate, ($R_L \geq 2K\Omega$; Unity Gain Voltage Follower)	SR	-	0.25	-	-	0.25	-	V/µs
Gain-Bandwidth Product, A_{OL} = 0dB, R_L = 2kΩ, C_L = 100pF, V_{IN} = 20, f = 1 kHz	f_T	-	1.20	-	-	1.20	-	MHz
Small-Signal Transient Response (V_{IN} = 20mV_{P-P}, f = 1kHz)	t_R	-	0.29	-	-	0.29	-	µs
Supply Current, R_L = ∞, V+ = 15, V- = -15	I+	-	2.3	3.5	-	2.3	3.5	mA
Temperature Range		- 25	-	85	0	-	70	°C

NOTE:

1. Short circuit may be applied to ground or to either supply.

Functional Block Diagram

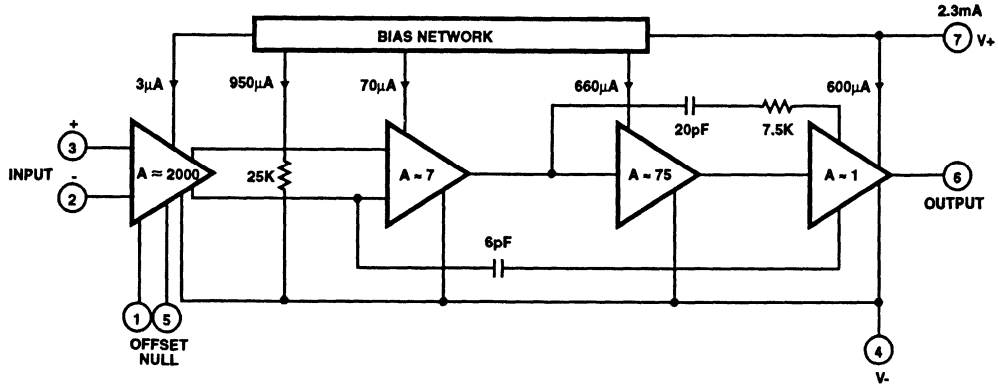


FIGURE 1. BLOCK DIAGRAM OF CA3193A AND CA3193

Schematic Diagrams

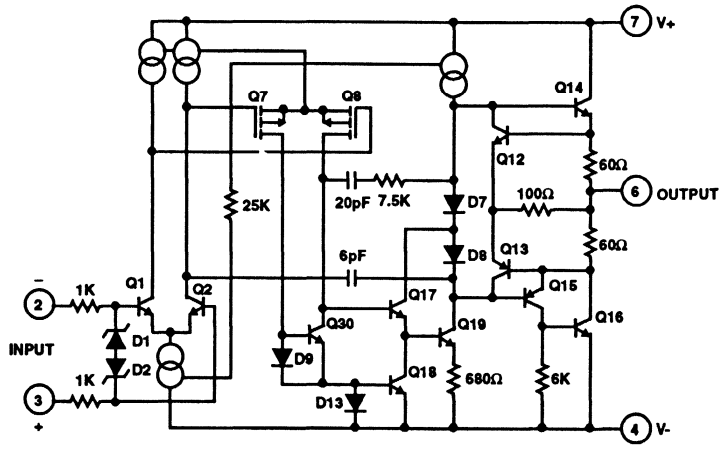


FIGURE 2. CA3193 SIMPLIFIED SCHEMATIC DIAGRAM

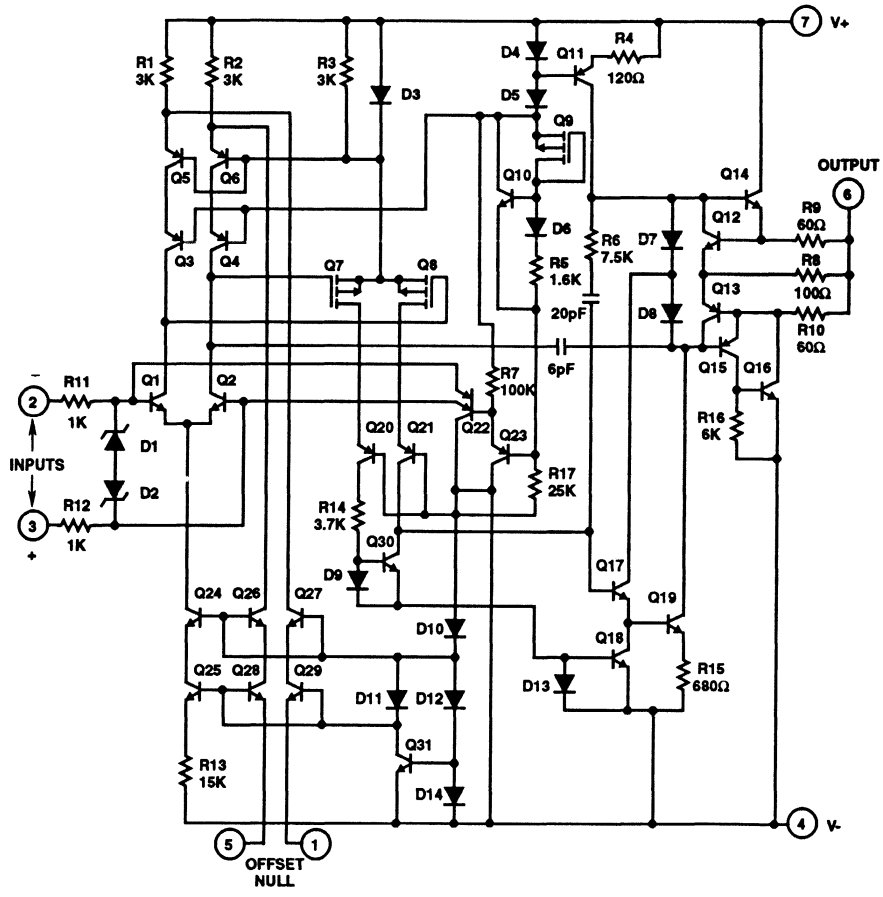


FIGURE 3. SCHEMATIC DIAGRAM OF CA3193A AND CA3193

Circuit Description

The block diagram of the CA3193 amplifier, Figure 1 shows the voltage gain and supply current for each of its four amplifier stages. Simplified and complete schematic diagrams of the CA3193 amplifier are shown in Figures 2 and 3, respectively.

A quad of physically cross-connected n-p-n transistors comprise the input-stage differential pair (Q1, Q2 in Figures 2 and 3); this arrangement contributes to the low input offset-voltage characteristics of the amplifier. The ultra-high gain provided in the first stage ensures that subsequent stages cannot significantly influence the overall offset-voltage characteristics of the amplifier. High load impedances for the input-stage differential pair (Q1, Q2) are provided by the cascode-connected p-n-p transistors Q3, Q5 and Q4, Q6, thereby contributing to the high gain developed in the stage.

The second stage of the amplifier consists of a differential amplifier employing PMOS/FETs (Q7, Q8 in Figures 2 and 3) with appropriate drain loading. Since Q7 and Q8 are MOS/FETs, their loading on the first stage is quite low, thereby making an additional contribution to the high gain developed in the first stage. The second stage is also configured to convert its differential signal to a single-ended output signal by means of current mirror D9, Q30 (Figures 2 and 3) to drive subsequent gain stage.

The third stage of the amplifier consists of Darlington-connected n-p-n transistors (Q17, Q19 in Figures 2 and 3), driving the quasi-complementary Class AB output stage (Q14 and Q15, Q16 in Figures 2 and 3). Output-stage short-circuit protection is activated by voltage drops developed across the 60Ω resistors adjacent to the output terminal (R9 and R10, Figure 3). When the voltage drop developed across either of these resistors reaches a potential equal to 1 V_{BE}, the respective protective transistor (Q12 or Q13) is activated and shunts the base drive from the bases of the output stage transistors (Q14 and Q15, Q16).

Internal frequency compensation for the CA3193 amplifier is provided by two internal networks, a 6pF capacitor connected between the input-stage transistor collectors and the node between the third and output stages and a second network, consisting of a 20pF capacitor in series with a 7.5kΩ resistor connected between the input and output nodes of the third stage.

Typical Performance Curves

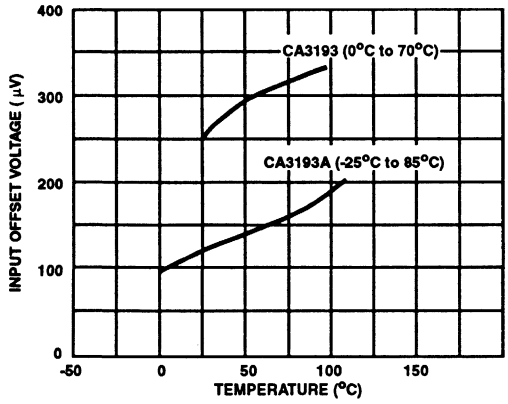


FIGURE 4. TYPICAL INPUT OFFSET-VOLTAGE TEMPERATURE CHARACTERISTIC

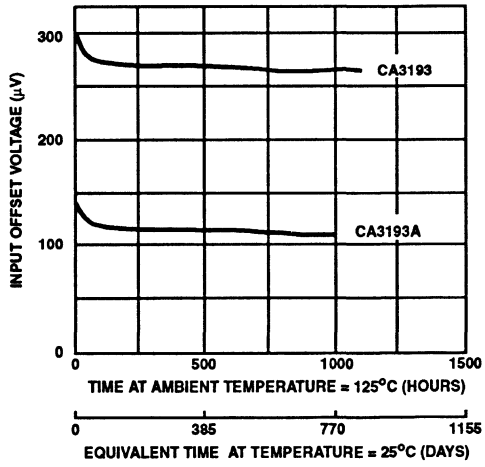


FIGURE 5. INPUT OFFSET VOLTAGE vs TIME

Typical Performance Curves (Continued)

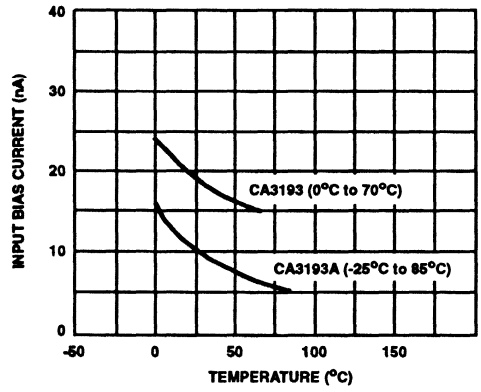


FIGURE 6. TYPICAL INPUT BIAS CURRENT vs TEMPERATURE

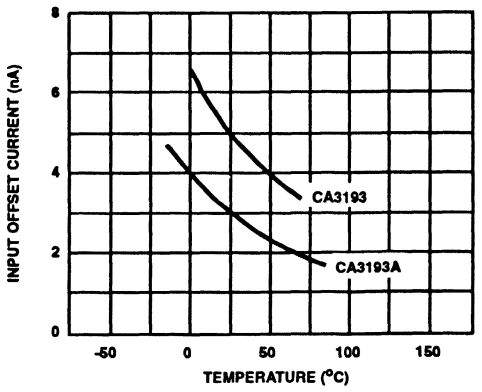


FIGURE 7. TYPICAL INPUT OFFSET CURRENT vs TEMPERATURE

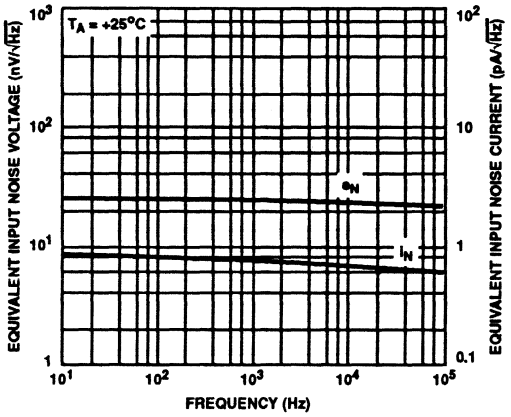


FIGURE 8. INPUT NOISE VOLTAGE AND CURRENT DENSITY vs FREQUENCY

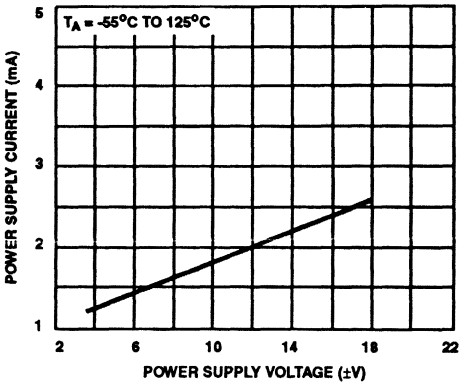


FIGURE 9. POWER SUPPLY VOLTAGE vs SUPPLY CURRENT

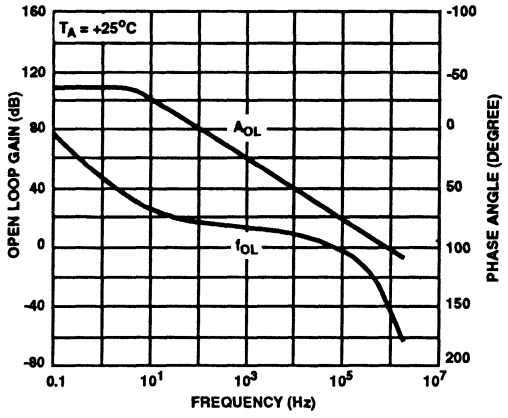


FIGURE 10. OPEN-LOOP GAIN AND PHASE-SHIFT RESPONSE

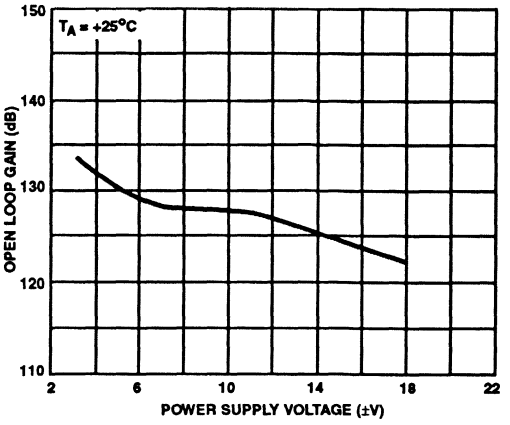


FIGURE 11. OPEN-LOOP GAIN vs POWER-SUPPLY VOLTAGE

Typical Performance Curves (Continued)

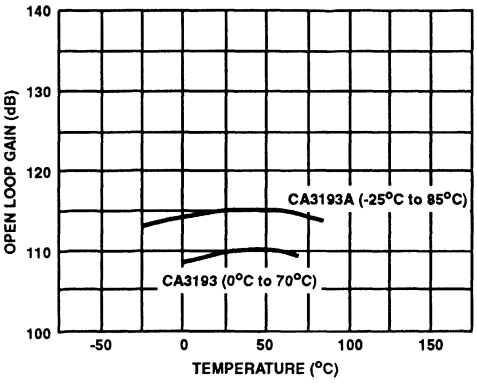


FIGURE 12. OPEN-LOOP GAIN vs TEMPERATURE

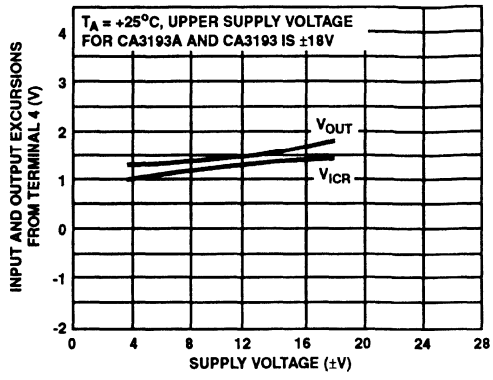


FIGURE 13.

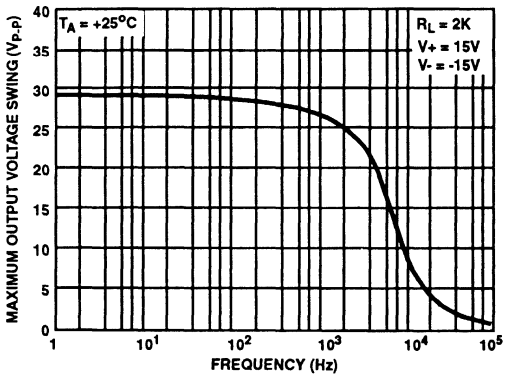


FIGURE 14. MAXIMUM UNDISTORTED OUTPUT VOLTAGE vs FREQUENCY

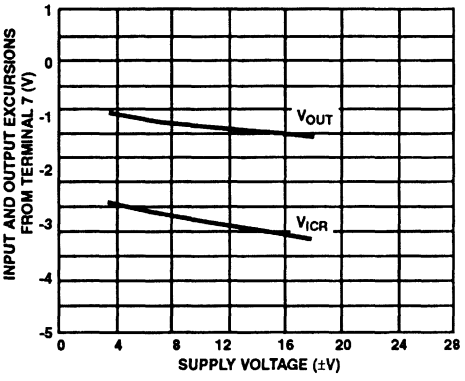


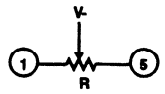
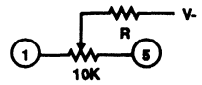
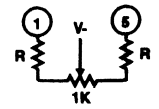
FIGURE 16. OUTPUT-VOLTAGE-SWING CAPABILITY AND COMMON-MODE INPUT-VOLTAGE vs SUPPLY VOLTAGE

Offset Voltage Nulling

The input offset voltage can be nulled to zero by any of the three methods shown in the table below. A 10K potentiometer between terminals 1 and 5, with its wiper returned to V-, will provide a gross nulling for all types. For finer nulling, either of the other two circuits shown below may be used, thus providing simpler improved resolution for all types.

CAUTION: The CA3193 amplifiers will be damaged if they are plugged into op-amp circuits employing nulling with respect to the V+ supply bus.

Offset Voltage Nulling

OFFSET NULLING CIRCUITS			
TYPE	RESISTOR R VALUE	RESISTOR R VALUE	RESISTOR R VALUE
CA3193A	10K	50K	10K
CA3193	10K	20K	5K
	Gross Offset Adjustment	Finer Offset Adjustments	

Test Circuits

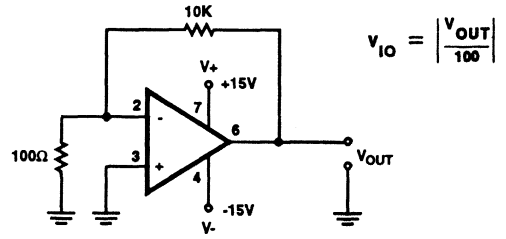
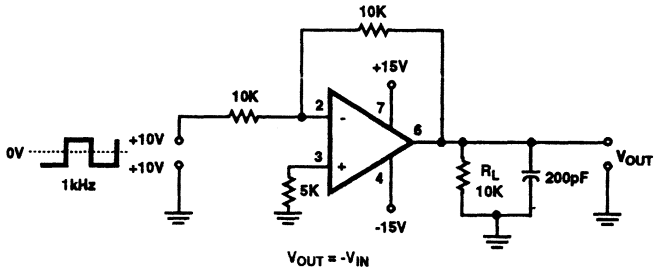
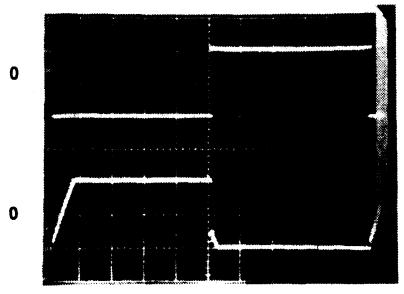


FIGURE 16. INPUT OFFSET VOLTAGE TEST CIRCUIT



(A)



TOP TRACE: INPUT VOLTAGE
BOTTOM TRACE: OUTPUT VOLTAGE

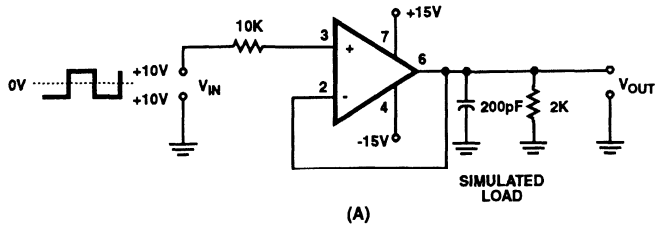
VERT: $\frac{10V}{DIV}$ V+ = 15V, V- = -15V

HORZ: $\frac{0.1ms}{DIV}$ R_L = 10K

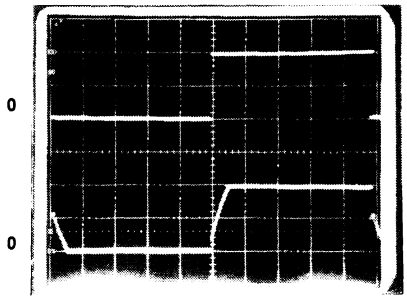
(B)

FIGURE 17. INVERTING AMPLIFIER (A) TEST CIRCUIT (B) RESPONSE TO 1kHz, $20V_{p-p}$ SQUARE WAVE

Test Circuits (Continued)



(A)



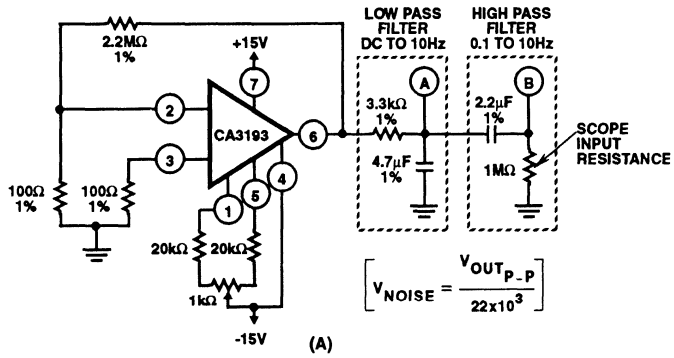
TOP TRACE: INPUT VOLTAGE
BOTTOM TRACE: OUTPUT VOLTAGE

VERT: $\frac{10V}{DIV}$ V+ = 15V, V- = -15V

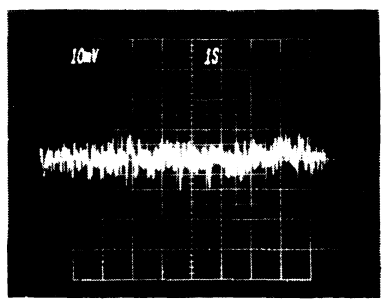
HORZ: $\frac{0.1ms}{DIV}$ R_L = 2K

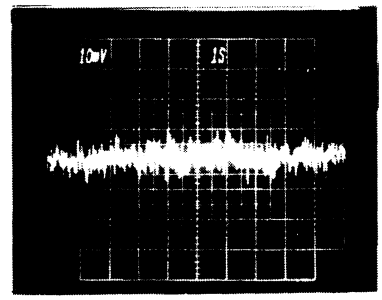
(B)

FIGURE 18. VOLTAGE FOLLOWER (A) TEST CIRCUIT (B) RESPONSE TO $20V_{P-P}$, 1kHz SQUARE WAVE INPUT



(A)

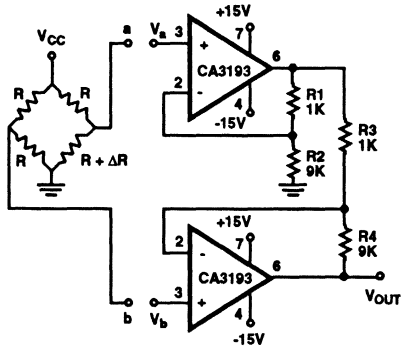




(B) (C)

FIGURE 19. LOW FREQUENCY NOISE (A) TEST CIRCUIT - 0.1 TO 10Hz (B) OUTPUT Ⓐ WAVEFORM - 0 TO 10Hz NOISE (C) OUTPUT Ⓑ WAVEFORM - 0.1 TO 10Hz NOISE

Application Circuits



$$V_{OUT} = -V_a\left(\frac{R2}{R1}+1\right)\frac{R4}{R3} + V_b\left(\frac{R4}{R3}+1\right)$$

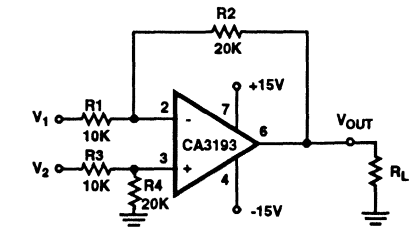
FOR IDEAL RESISTORS WITH $\frac{R1}{R2} = \frac{R3}{R4}$

$$V_{OUT} = V_b - V_a\left(\frac{R4}{R3}+1\right)$$

$$A = \frac{V_{OUT}}{V_b - V_a} = \left(\frac{R4}{R3}+1\right)$$

FOR VALUES ABOVE $V_{OUT} = (V_b - V_a)$ (IO)

FIGURE 20. TYPICAL TWO-OP AMP BRIDGE-TYPE DIFFERENTIAL AMPLIFIER



ALL RESISTANCE VALUES ARE IN OHMS

$$V_{OUT} = V_2\left(\frac{R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right) - V_1\left(\frac{R2}{R1}\right)$$

IF R4=R2, R3=R1 AND $\frac{R2}{R1} = \frac{R4}{R3}$

THEN $V_{OUT} = (V_2 - V_1)\left(\frac{R2}{R1}\right)$

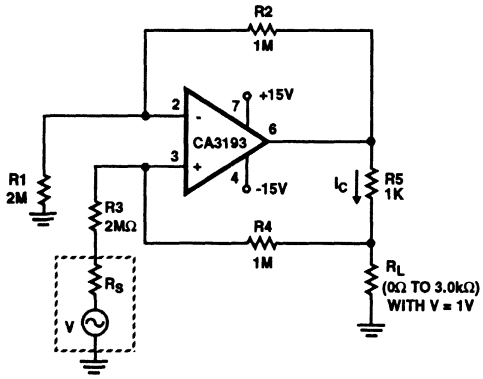
FOR VALUES ABOVE $V_{OUT} = 2(V_2 - V_1)$

IF A_V IS TO BE MADE I AND IF R1 = R3 = R4 = R
WITH R2 = 0.999R (0.1% MISMATCH IN R2)

THEN $V_{OCM} = 0.0005\ V_{IN}$ OR CMRR = 66dB

THUS, THE CMRR OF THIS CIRCUIT IS LIMITED BY THE MATCHING OR MISMATCHING OF THIS NETWORK RATHER THAN THE AMPLIFIER.

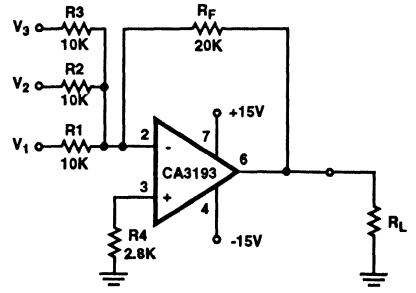
FIGURE 21. DIFFERENTIAL AMPLIFIER (SIMPLE SUBTRACTER) USING CA3193



ALL RESISTORS ARE 1%
IF R1 = R3 AND R2 = R4 + R5 THEN
I_L IS INDEPENDENT OF VARIATIONS IN R_L
FOR R_L VALUES OF 0Ω TO 3kΩ WITH V = 1V

$$I_L = \frac{VR4}{R3R5} = \frac{V\,(1M)}{(2M)\,(1K)} = \frac{V}{2K} = 500\mu A$$

FIGURE 22. USING CA3193 AS A BILATERAL CURRENT SOURCE



$$V_{OUT} = -\left(\frac{R_F}{R1}V_1 + \frac{R_F}{R2}V2 + \frac{R_F}{R3}V3\right)$$

$V_{OUT} = -(2V_1 + 2V_2 + 2V_3)$
ALL RESISTANCE VALUES ARE IN OHMS

FIGURE 23. TYPICAL SUMMING AMPLIFIER APPLICATION

Application Circuits (Continued)

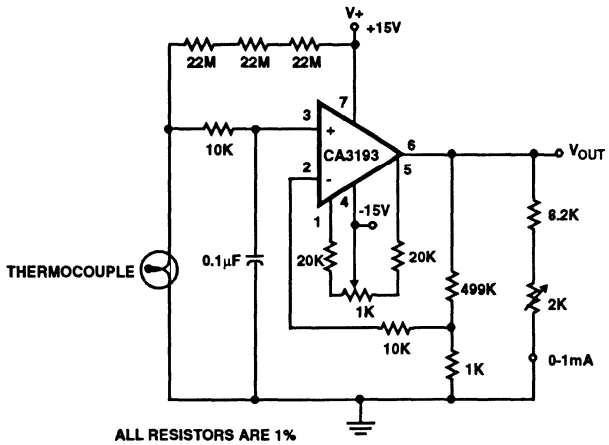


FIGURE 24. THE CA3193 USED IN A THERMOCOUPLE CIRCUIT

The CA3193 is an excellent choice for use with thermocouples. In Figure 24, the CA3193 amplifies the generated signal 500 times. The three 22-megohm resistors will provide full-scale output if the thermocouple opens.

HARRIS SEMICONDUCTOR

CA3240

Dual BiMOS Operational Amplifier with MOSFET Inpu/Bipolar Output

March 1993

Features

- Dual Version of CA3140
- Internally Compensated
- MOSFET Input Stage
  - Very High Input Impedance (Z_{IN}) 1.5TΩ Typ
  - Very Low Input Current (I_I) 10pA Typ. at ±15V
  - Wide Common-Mode Input Voltage Range (V_{ICR}): Can be Swung 0.5V Below Negative Supply Voltage Rail
- Directly Replaces Industry Type 741 in Most Applications

Applications

- Ground Referenced Single Amplifiers in Automobile and Portable Instrumentation
- Sample and Hold Amplifiers
- Long Duration Timers/Multivibrators (Microseconds-Minutes-Hours)
- Photocurrent Instrumentation
- Intrusion Alarm System
- Comparators
- Instrumentation Amplifiers
- Active Filters
- Function Generators
- Power Supplies

Description

The CA3240A and CA3240 are dual versions of the popular CA3140 series integrated circuit operational amplifiers. They combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOSFET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range (typically to 0.5V below the negative supply rail). The bipolar output transistors allow a wide output voltage swing and provide a high output current capability.

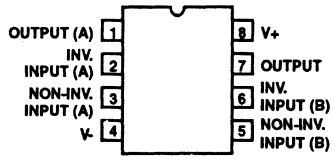
The CA3240A and CA3240 are compatible with the industry standard 1458 operational amplifiers in similar packages.The offset null feature is available only when these types are supplied in the 14 lead dual-in-line plastic package (E1 suffix).

Ordering Information

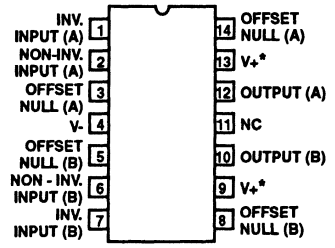
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3240AE	-40°C to +85°C	8 Lead Plastic DIP
CA3240AE1	-40°C to +85°C	14 Lead Plastic DIP
CA3240E	-40°C to +85°C	8 Lead Plastic DIP
CA3240E1	-40°C to +85°C	14 Lead Plastic DIP

Pinouts

CA3240, CA3240A
(PDIP)
TOP VIEW

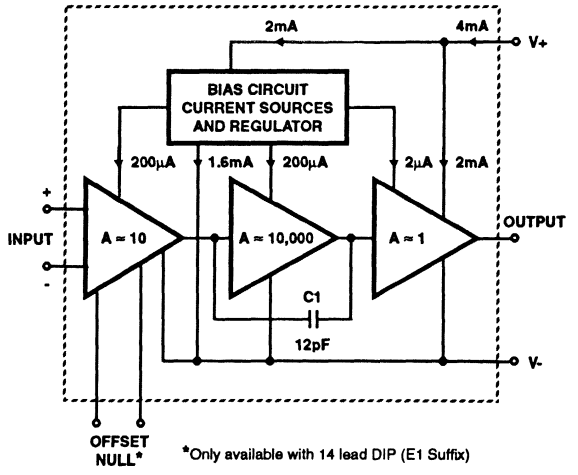


CA3240, CA3240A
(PDIP)
TOP VIEW



* Pins 9 and 13 internally connected through approximately 3Ω

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1050.2**

Absolute Maximum Ratings

Supply Voltage (between V+ and V-) 36V
Differential Input Voltage. 8V
Input Voltage. . . . . (V+ +8V) to (V- -0.5V)
Input Current. 1mA
Output Short Circuit Duration (Note 1) . . . . . Indefinite
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.). . . . . +300°C

Operating Conditions

Operating Temperature Range . . . . . $-40°C \leq T_A \leq +85°C$
Storage Temperature Range. . . . . $-65°C \leq T_A \leq +150°C$
Operating Voltage Range . . . . . 4V to 36V or ±2V to ±18V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

For Equipment Design, V+ = 15V, V- = -15V, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	LIMITS						UNITS
		CA3240A			CA3240			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	-	2	5	-	5	15	mV
Input Offset Current	I_{IO}	-	0.5	20	-	0.5	30	pA
Input Current	I_I	-	10	40	-	10	50	pA
Large-Signal Voltage Gain (See Figures 2, 17)	A_{OL} (Note 2)	20	100	-	20	100	-	kV/V
		86	100	-	86	100	-	dB
Common-Mode Rejection Ratio (See Figure 7)	CMRR	-	32	320	-	32	320	µV/V
		70	90	-	70	90	-	dB
Common-Mode Input Voltage Range (See Figure 14)	V_{ICR}	-15	-15.5 to +12.5	12	-15	-15.5 to +12.5	11	V
Power Supply Rejection Ratio (See Figure 9)	$\Delta V_{IO}/\Delta V\pm$	-	100	150	-	100	150	µV/V
	PSRR	76	80	-	76	80	-	dB
Maximum Output Voltage (Note 3) (See Figures 14, 20)	V_{OM+}	12	13	-	12	13	-	V
	V_{OM-}	-14	-14.4	-	-14	-14.4	-	V
Maximum Output Voltage (Note 4)	V_{OM-}	0.4	0.13	-	0.4	0.13	-	V
Supply Current (See Figure 5) For Both Amps.	I+	-	8	12	-	8	12	mA
Total Device Dissipation	P_D	-	240	360	-	240	360	mW

NOTES:

1. Short circuit may be applied to ground or to either supply. Temperatures and/or supply voltages must be limited to keep dissipation within maximum rating.
2. At V_O = 26Vp-p, +12V, -14V and R_L = 2kΩ.
3. At R_L = 2kΩ.
4. At V+ = 5V, V- = GND, I_{SINK} = 200µA.

Specifications CA3240, CA3240A

Electrical Specifications For Equipment Design, V+ = +15V, V- = -15V, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	TYPICAL VALUES		UNITS
			CA3240A	CA3240	
Input Offset Voltage Adjustment Resistor (E1 Package Only)		Typical Value of Resistor Between Terms. 4 and 3(5) or Between 4 and 14(8) to Adjust Maximum V_{IO}	18	4.7	kΩ
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I		4	4	pF
Output Resistance	R_O		60	60	Ω
Equivalent Wideband Input Noise Voltage (See Figure 19)	e_N	BW = 140kHz, R_S = 1MΩ	48	48	μV
Equivalent Input Noise Voltage (See Figure 8)	e_N	f = 1kHz, R_S = 100Ω	40	40	$nV/\sqrt{Hz}$
		f = 10kHz, R_S = 100Ω	12	12	$nV/\sqrt{Hz}$
Short-Circuit Current to Opposite Supply	$I_{OM}+$	Source	40	40	mA
	$I_{OM}-$	Sink	11	11	mA
Gain Bandwidth Product (See Figures 3 and 17)	f_T		4.5	4.5	MHz
Slew Rate (See Figure 4)	SR		9	9	V/μs
Transient Response:					
Rise Time	t_R	R_L = 2kΩ, C_L = 100pF	0.08	0.08	μs
Overshoot (See Figure 18)	OS	R_L = 2kΩ, C_L = 100pF	10	10	%
Settling Time at 10 Vp-p (See Figure 15)					
1mV	t_S	R_L = 2kΩ, C_L = 100pF, Voltage Follower	4.5	4.5	μs
10mV	t_S	R_L = 2kΩ, C_L = 100pF, Voltage Follower	1.4	1.4	μs
Crosstalk		f = 1kHz	120	120	dB

Electrical Specifications For Equipment Design at V+ = 15V, V- = -15V, T_A = -40 to +85°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage	$\|V_{IO}\|$	3	10	mV
Input Offset Current (Note 3)	$\|I_{IO}\|$	32	32	pA
Input Current (Note 3)	I_I	640	640	pA
Large Signal Voltage Gain (See Figures 2, 17)	A_{OL} (Note 1)	63	63	kV/V
		96	96	dB
Common Mode Rejection Ratio (See Figure 7)	CMRR	32	32	µV/V
		90	90	dB
Common Mode Input Voltage Range (See Figure 14)	V_{ICR}	-15 to +12.3	-15 to +12.3	V
Power Supply Rejection Ratio (See Figure 9)	$\Delta V_{IO}/\Delta V\pm$	150	150	µV/V
	PSRR	76	76	dB
Maximum Output Voltage (Note 2) (See Figures 14 and 20)	$V_{OM}+$	12.4	12.4	V
	$V_{OM}-$	-14.2	-14.2	V
Supply Current (See Figure 5) For Both Amps	I+	8.4	8.4	mA
Total Device Dissipation	P_D	252	252	mW
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	15	15	µV/°C

NOTES:

1. At V_O = 26Vp-p, +12V, -14V and R_L = 2kΩ.
2. At R_L = 2kΩ.
3. At T_A = +85°C.

Specifications CA3240, CA3240A

Electrical Specifications For Design Guidance at V+ = 5V, V- = 0V, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage	$\|V_{IO}\|$	2	5	mV
Input Offset Current	$\|I_{IO}\|$	0.1	0.1	pA
Input Current	I_I	2	2	pA
Input Resistance	R_{IN}	1	1	TΩ
Large Signal Voltage Gain (See Figures 2 and 17)	A_{OL}	100	100	kV/V
		100	100	dB
Common-Mode Rejection Ratio	CMRR	32	32	µV/V
		90	90	dB
Common-Mode Input Voltage Range (See Figure 14)	V_{ICR}	-0.5	-0.5	V
		2.6	2.6	V
Power Supply Rejection Ratio	PSRR	31.6	31.6	µV/V
		90	90	dB
Maximum Output Voltage (See Figures 14 and 20)	$V_{OM}+$	3	3	V
	$V_{OM}-$	0.3	0.3	V
Maximum Output Current				
Source	$I_{OM}+$	20	20	mA
Sink	$I_{OM}-$	1	1	mA
Slew Rate (See Figure 4)	SR	7	7	V/µs
Gain Bandwidth Product (See Figure 3)	f_T	4.5	4.5	MHz
Supply Current (See Figure 5)	I+	4	4	mA
Device Dissipation	P_D	20	20	mW

Schematic Diagram

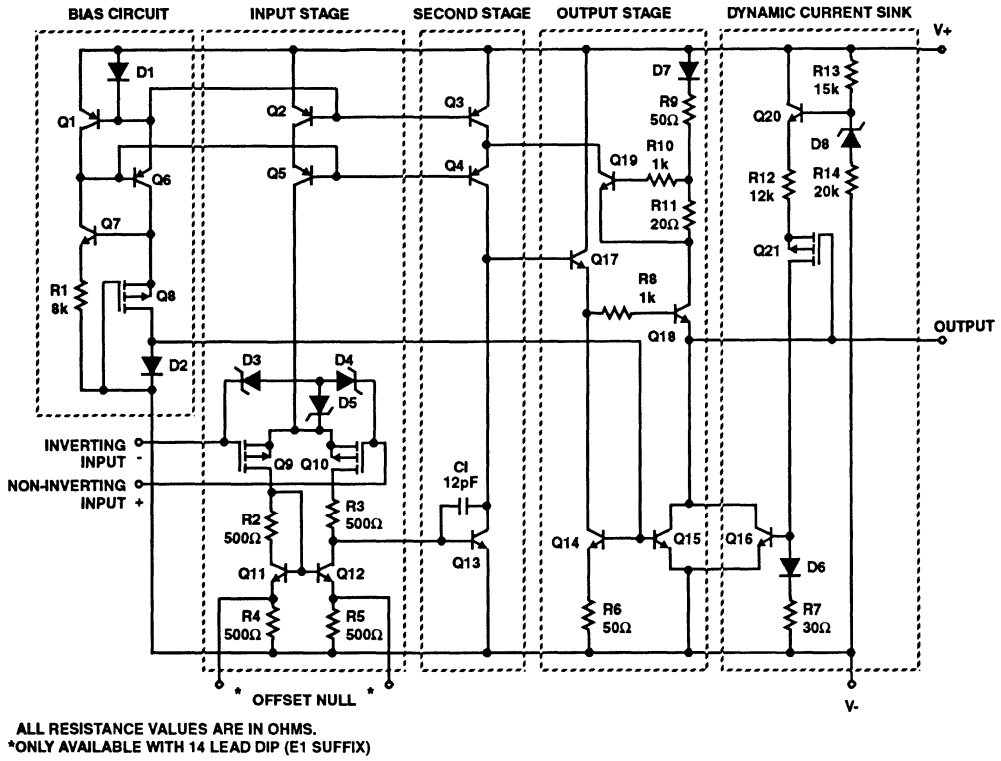


FIGURE 1. SCHEMATIC DIAGRAM OF ONE-HALF CA3240 SERIES.

Circuit Description

The schematic diagram of one amplifier section of the CA3240 is shown in Figure 1. It consists of a differential amplifier stage using PMOS transistors Q9 and Q10 with gate-to-source protection against static discharge damage provided by zener diodes D3, D4, and D5. Constant current bias is applied to the differential amplifier from transistors Q2 and Q5 connected as a constant current source. This assures a high common-mode rejection ratio. The output of the differential amplifier is coupled to the base of gain stage transistor Q13 by means of an n-p-n current mirror that supplies the required differential-to-single-ended conversion. Provision for offset null for types in the 14 lead plastic package (E1 suffix) is provided through the use of this current mirror.

The gain stage transistor Q13 has a high impedance active load (Q3 and Q4) to provide maximum open-loop gain. The collector of Q13 directly drives the base of the compound emitter-follower output stage. Pulldown for the output stage is provided by two independent circuits: (1) constant-current-connected transistors Q14 and Q15 and (2) dynamic current-sink transistor Q16 and its associated circuitry. *The level of pulldown current is constant at about 1mA for Q15 and varies from 0 to 18mA for Q16 depending on the magnitude of the voltage between the output terminal and V+.* The dynamic current sink becomes active whenever the output terminal is more negative than V+ by about 15V. When this condition exists, transistors Q21 and Q16 are turned on causing Q16 to sink current from the output terminal to V-. This current always flows when the output is in the linear region, either from the load resistor or from the emitter of Q18 if no load resistor is present. The purpose of this dynamic sink is to permit the output to go within 0.2V (V_{CE} (sat)) of V- with a 2kΩ load to ground. *When the load is returned to V+, it may be necessary to supplement the 1mA of current from Q15 in order to turn on the dynamic current sink (Q16).* This may be accomplished by placing a resistor (Approx. 2kΩ) between the output and V-.

Typical Performance Curves

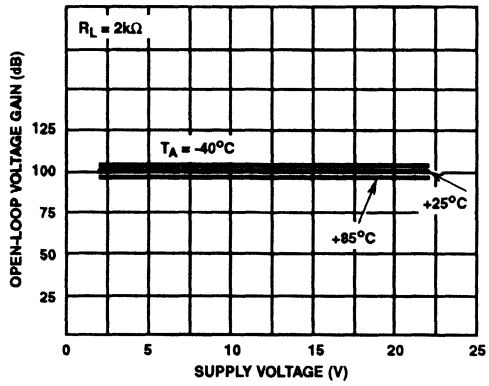


FIGURE 2. OPEN LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE

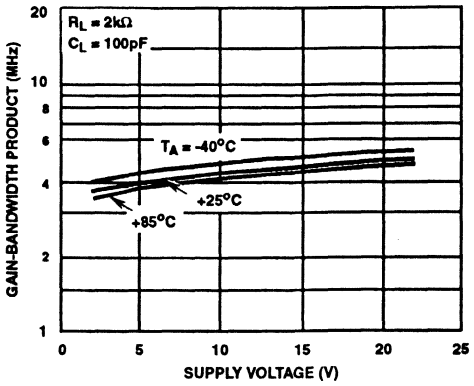


FIGURE 3. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

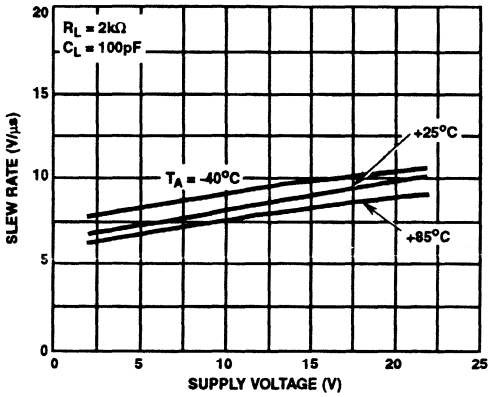


FIGURE 4. SLEW RATE vs SUPPLY VOLTAGE

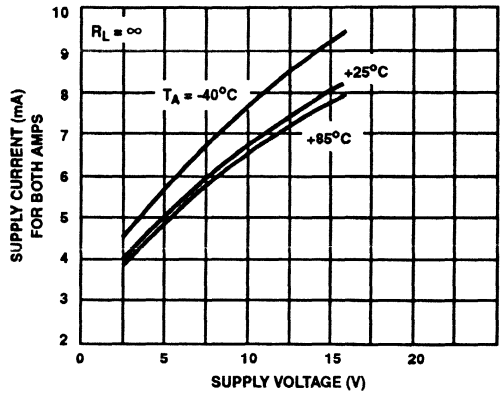


FIGURE 5. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

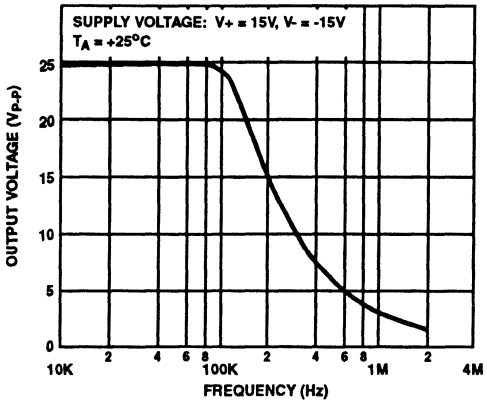


FIGURE 6. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

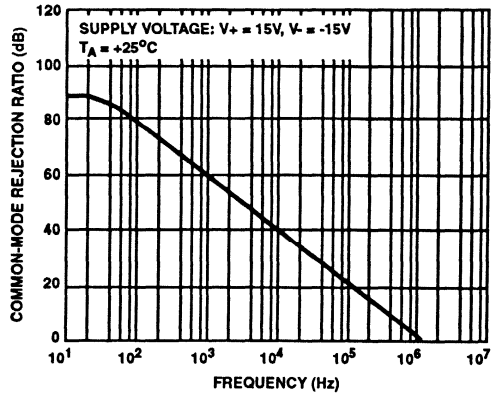


FIGURE 7. COMMON MODE REJECTION RATIO vs FREQUENCY

Typical Performance Curves (Continued)

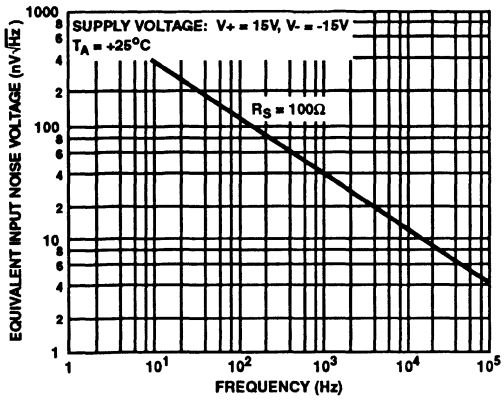


FIGURE 8. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

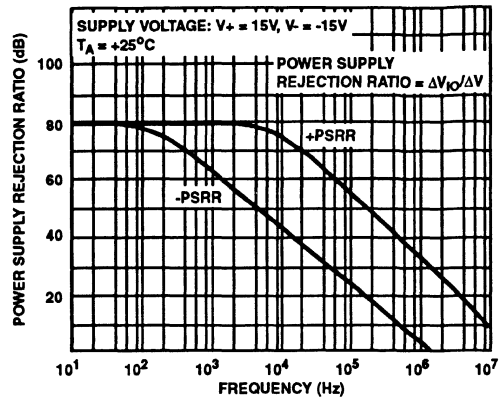


FIGURE 9. POWER SUPPLY REJECTION RATIO vs FREQUENCY

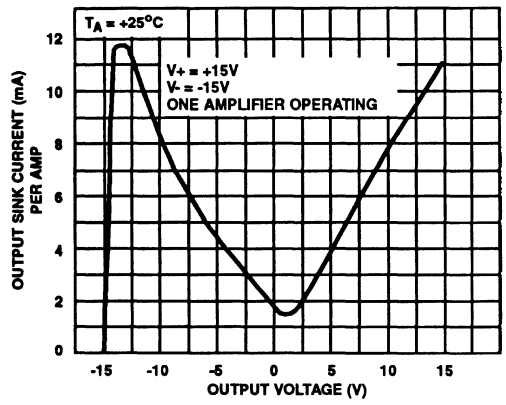


FIGURE 10. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

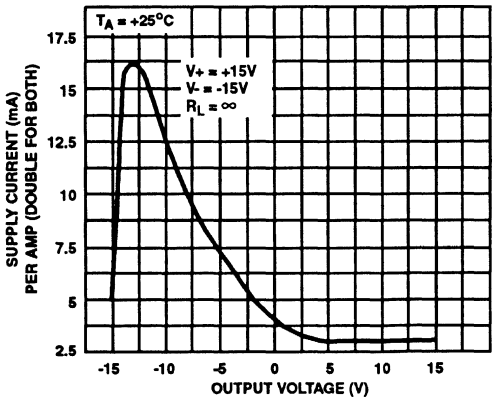


FIGURE 11. SUPPLY CURRENT vs OUTPUT VOLTAGE

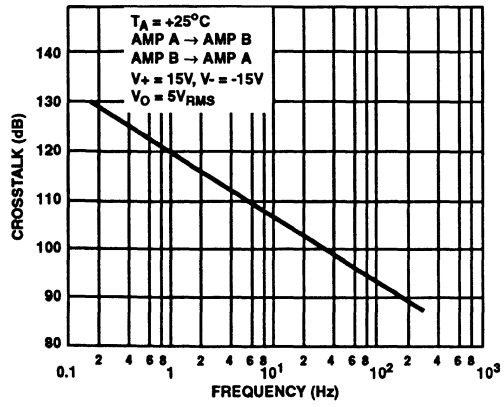


FIGURE 12. CROSSTALK vs FREQUENCY

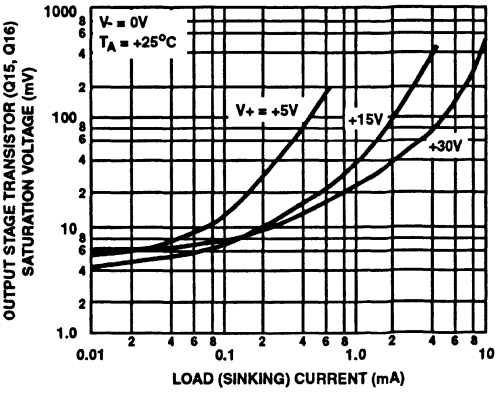


FIGURE 13. VOLTAGE ACROSS OUTPUT TRANSISTORS Q15 AND Q16 vs LOAD CURRENT

Typical Performance Curves (Continued)

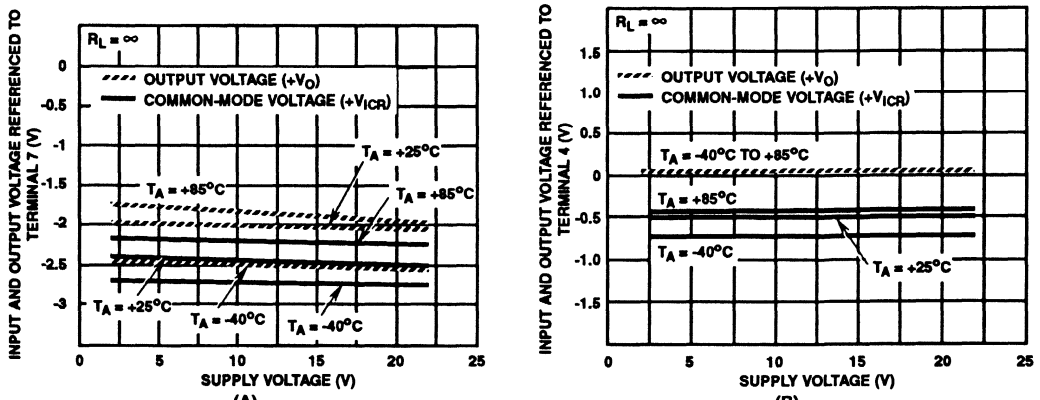
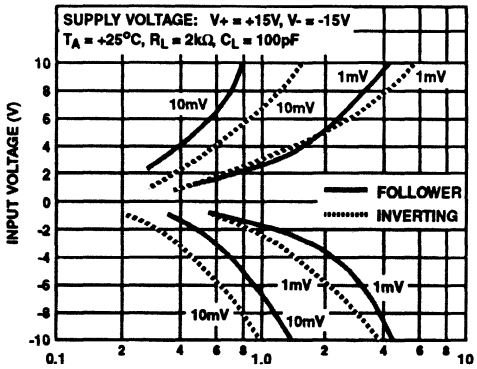
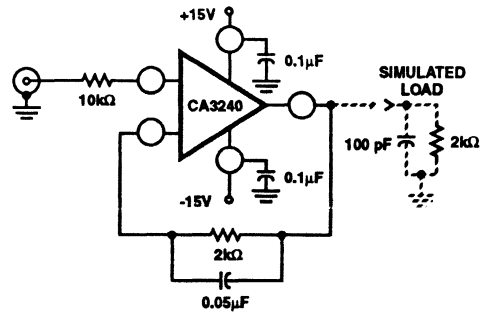


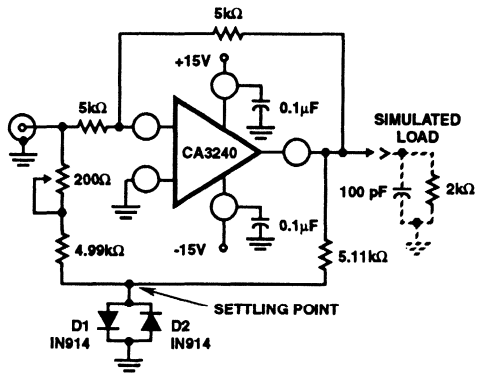
FIGURE 14. OUTPUT-VOLTAGE-SWING CAPABILITY AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE AND TEMPERATURE



(A) SETTLING TIME (μs)



(B) TEST CIRCUIT (FOLLOWER)



(C) TEST CIRCUIT (INVERTING)

FIGURE 15. INPUT VOLTAGE vs SETTLING TIME

Typical Performance Curves (Continued)

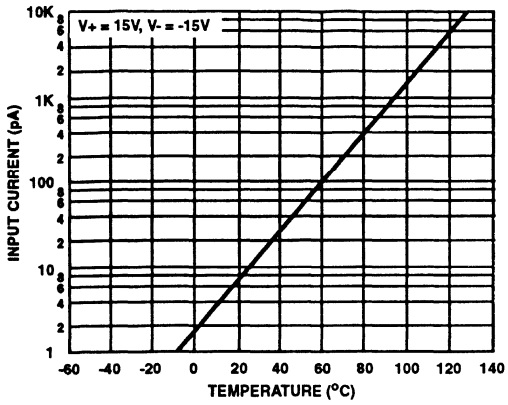


FIGURE 16. INPUT CURRENT vs AMBIENT TEMPERATURE

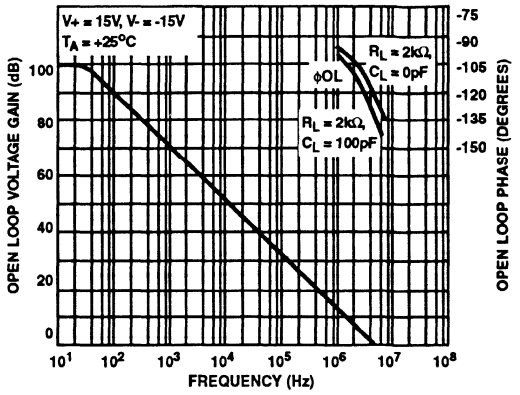
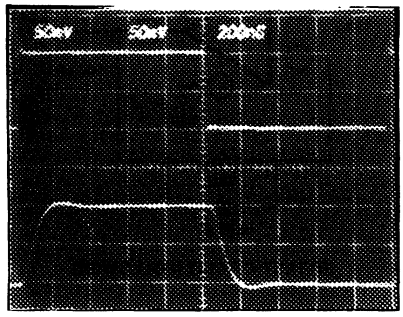


FIGURE 17. OPEN LOOP VOLTAGE GAIN AND PHASE vs FREQUENCY

Top Trace: Input
(50mV/Div.; 200ns/Div.)

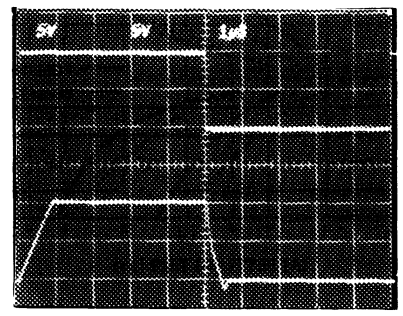
Bottom Trace: Output
(50mV/Div.; 200ns/Div.)



(A) SMALL SIGNAL RESPONSE

Top Trace: Input
(5V/Div.; 1µs/Div.)

Bottom Trace: Output
(5V/Div.; 1µs/Div.)



(B) LARGE SIGNAL RESPONSE

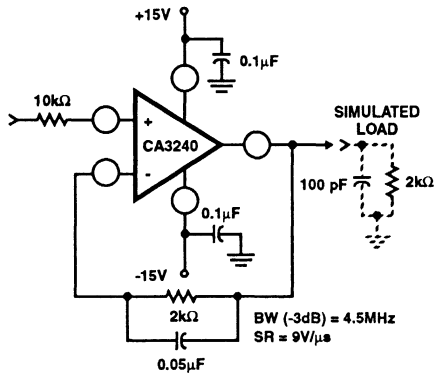


FIGURE 18. SPLIT-SUPPLY VOLTAGE FOLLOWER TEST CIRCUIT AND ASSOCIATED WAVEFORMS

Typical Performance Curves (Continued)

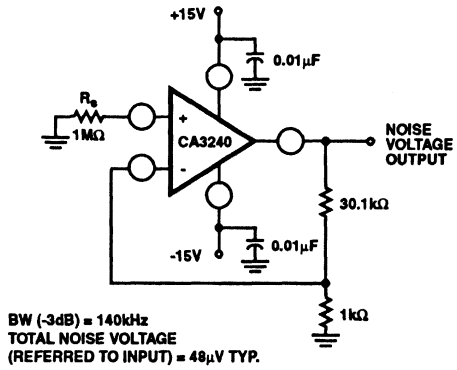


FIGURE 19. TEST CIRCUIT AMPLIFIER (30 dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENT

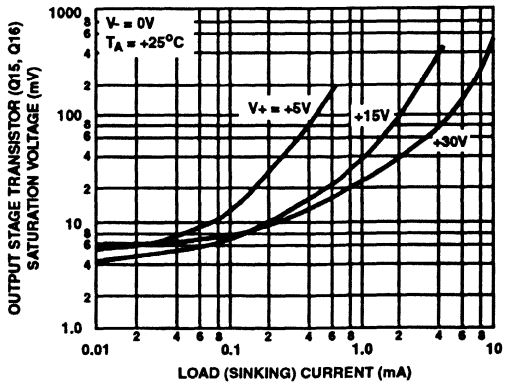


FIGURE 20. VOLTAGE ACROSS OUTPUT TRANSISTORS Q15 AND Q16 AS A FUNCTION OF LOAD CURRENT

Applications Considerations

Output Circuit Considerations

Figure 20 shows output current-sinking capabilities of the CA3240 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

Figure 21 shows some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

Input Circuit Considerations

As indicated by the typical V_{ICR}, this device will accept inputs as low as 0.5V below V-. However, a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3240 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9kΩ resistor is sufficient.

The typical input current is in the order of 10pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, rasing the chip temperature and resulting in increased input current. Figure 22 shows typical input-terminal current versus ambient temperature for the CA3240.

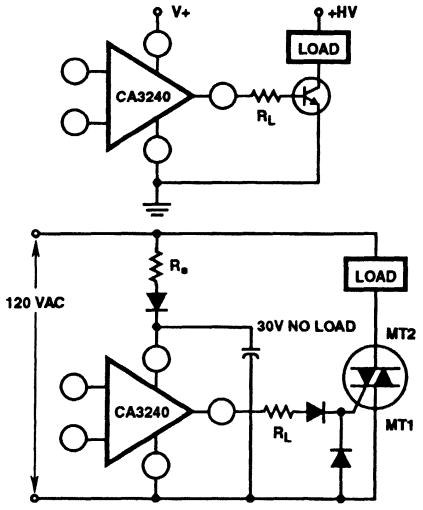


FIGURE 21. METHODS OF UTILIZING THE $V_{CE(SAT)}$ SINKING CURRENT CAPABILITY OF THE CA3240 SERIES

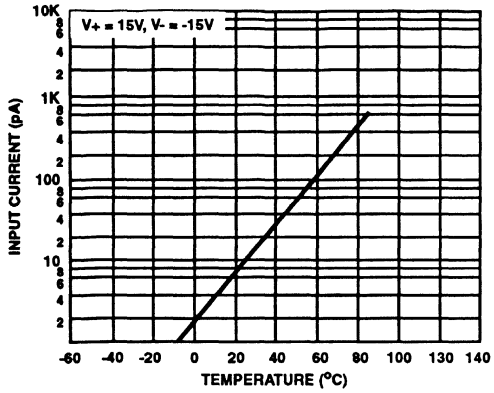


FIGURE 22. INPUT CURRENT vs AMBIENT TEMPERATURE

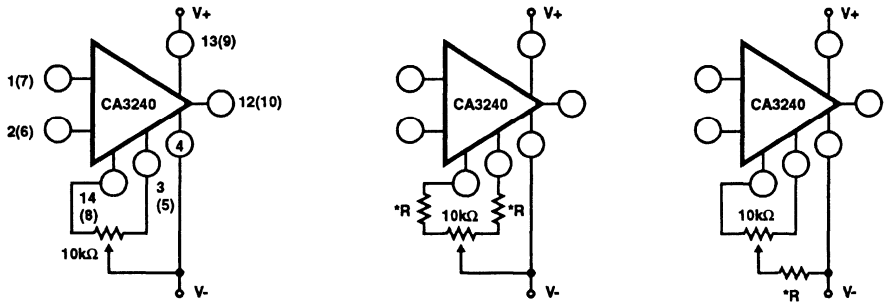
It is well known that MOSFET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

Offset-Voltage Nulling

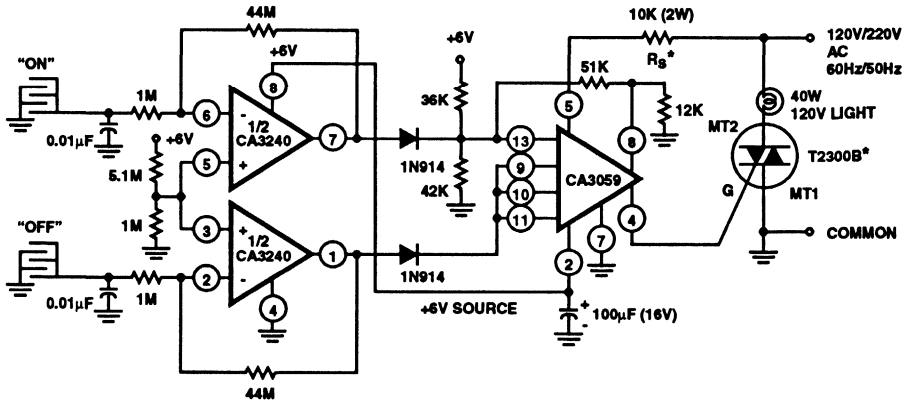
The input-offset voltage of the CA3240AE1 and CA3240E1 can be nulled by connecting a 10kΩ potentiometer between Terminals 3 and 14 or 5 and 8 and returning its wiper arm to Terminal 4, see Figure 23A. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Figure 23B, to optimize its utilization range are given in the table "Electrical Specifications for Equipment Design" shown on third page of this data sheet.

An alternate system is shown in Figure 23C. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.



*See Electrical Specifications Table on third page of this data sheet for value of R.

FIGURE 23. THREE OFFSET-VOLTAGE NULLING METHODS, (CA3240AE1, CA3240E1 ONLY.)



* AT 220V OPERATION, TRIAC SHOULD BE T2300D, R_S = 18K, 5W

FIGURE 24. ON/OFF TOUCH SWITCH

Typical Applications

On/Off Touch Switch

The on/off touch switch shown in Figure 24 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the "on" plate is touched, current flows between the two halves of the grid causing a positive shift in the output voltage (Terminal 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing triac driver. When a positive pulse occurs at Terminal 7 of the CA3240E, the triac is turned on and held on by the CA3059 and its associated positive feedback circuitry (51kΩ resistor and 36kΩ/42kΩ voltage divider). When the positive pulse occurs at Terminal 1 (CA3240E), the triac is turned off and held off in a similar manner. Note that power for the CA3240E is supplied by the CA3059 internal power supply.

The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while allowing sufficiently high circuit impedance to provide protection against electrical shock.

Dual Level Detector (Window Comparator)

Figure 25 illustrates a simple dual liquid level detector using the CA3240E as the sensing amplifier. This circuit operates on the principle that most liquids contain enough ions in solution to sustain a small amount of current flow between two electrodes submersed in the liquid. The current, induced by an 0.5V potential applied between two halves of a PC board grid, is converted to a voltage level by the CA3240E in a circuit similar to that of the on/off touch switch shown in Figure 24. The changes in voltage for both the upper and lower level sensors are processed by the CA3140 to activate an LED whenever the liquid level is above the upper sensor or below the lower sensor.

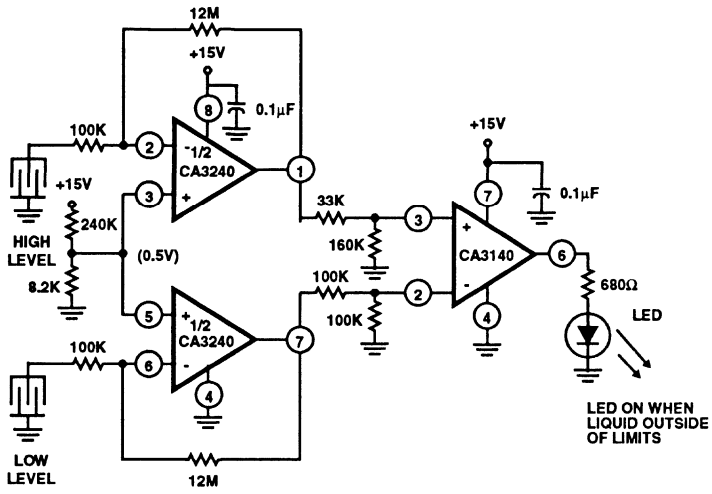


FIGURE 25. DUAL LEVEL DETECTOR

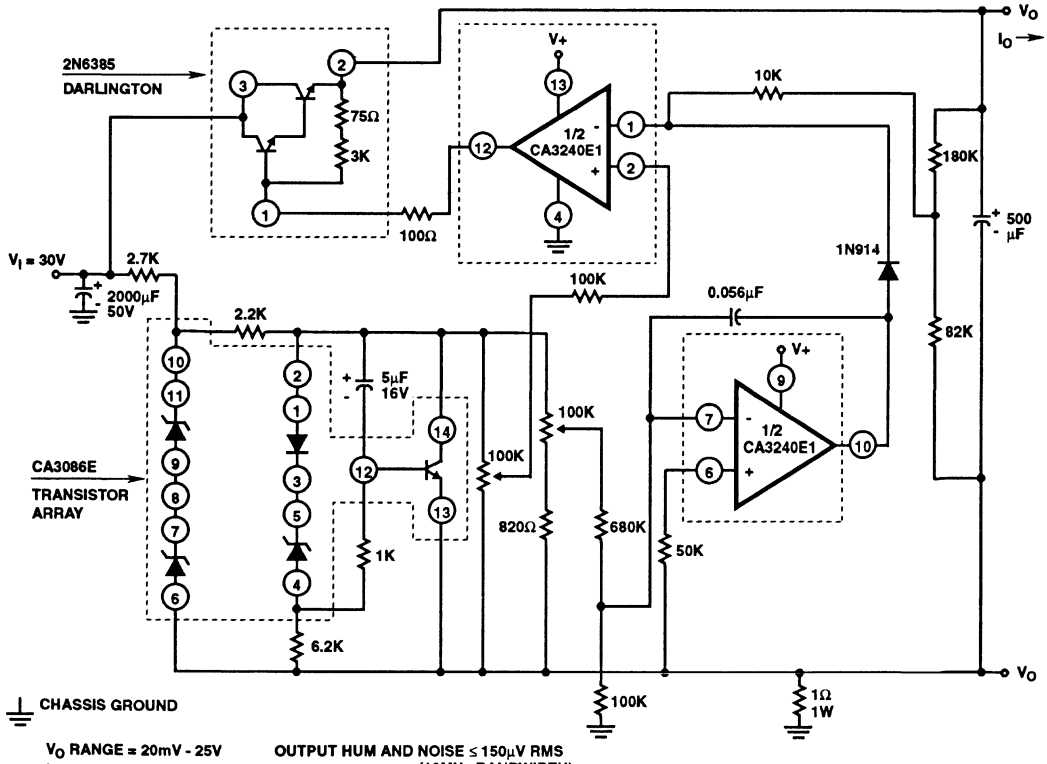


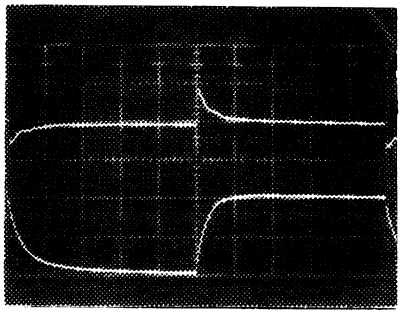
FIGURE 26. CONSTANT-VOLTAGE/CONSTANT-CURRENT POWER SUPPLY

Constant-Voltage/Constant-Current Power Supply

The constant-voltage/constant-current power supply shown in Figure 26 uses the CA3240E1 as a voltage-error and current-sensing amplifier. The CA3240E1 is ideal for this application because its input common-mode voltage range includes ground, allowing the supply to adjust from 20mV to 25V without requiring a negative supply voltage. Also, the ground reference capability of the CA3240E1 allows it to sense the voltage across the 1Ω current-sensing resistor in the negative output lead of the power supply. The CA3086 transistor array functions as a reference for both constant-voltage and constant-current limiting. The 2N6385 power Darlington is used as the pass element and may be required to dissipate as much as 40W. Figure 27 shows the transient response of the supply during a 100mA to 1A load transition.

Precision Differential Amplifier

Figure 28 shows the CA3240E in the classical precision differential amplifier circuit. The CA3240E is ideally suited for biomedical applications because of its extremely high input impedance. To insure patient safety, an extremely high electrode series resistance is required to limit any current that might result in patient discomfort in the event of a fault condition. In this case, 10MΩ resistors have been used to limit the current to less than 2μA without affecting the performance of the circuit. Figure 29 shows a typical electrocardiogram waveform obtained with this circuit.



Top Trace: Output Voltage
(500mV/Div. and 5μs/Div.)

Bottom Trace: Collector Of Load Switching Transistor
Load = 100mA to 1A, (5V/Div. and 5μs/Div.)

FIGURE 27. TRANSIENT RESPONSE

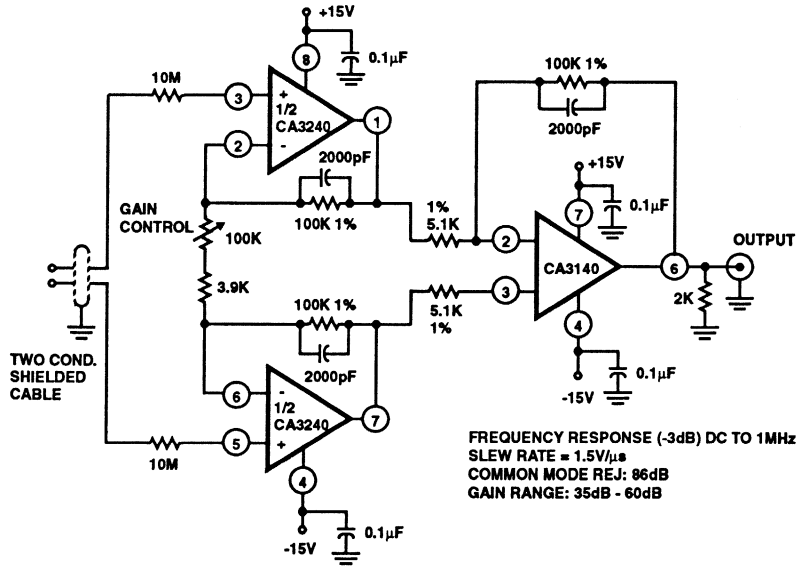
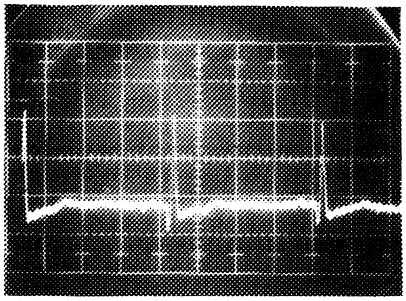


FIGURE 28. PRECISION DIFFERENTIAL AMPLIFIER



Vertical: 1.0mV/Div
(Amplifier Gain = 100X)
(Scope Sensitivity = 0.1V/Div.)

Horizontal: > 0.2 Sec/Div. (Uncal)

FIGURE 29. TYPICAL ELECTROCARDIOGRAM WAVEFORM

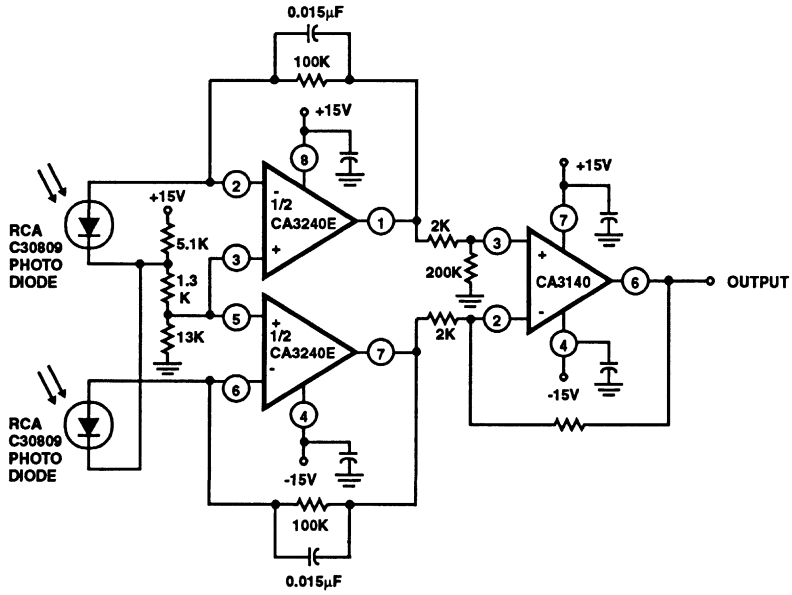


FIGURE 30. DIFFERENTIAL LIGHT DETECTOR

Differential Light Detector

In the circuit shown in Figure 30, the CA3240E converts the current from two photo diodes to voltage, and applies 1V of reverse bias to the diodes. The voltages from the CA3240E outputs are subtracted in the second stage (CA3140) so that only the difference is amplified. In this manner, the circuit can be used over a wide range of ambient light conditions without circuit component adjustment. Also, when used with a light source, the circuit will not be sensitive to changes in light level as the source ages.

HARRIS SEMICONDUCTOR

CA3260

BiMOS Operational Amplifier with MOSFET Input/CMOS Output

March 1993

Features

- MOSFET Input Stage provides
  - Very High Z_I = 1.5TΩ (1.5 x 10^{12}Ω) Typ.
  - Very Low I_I = 5pA Typ. at 15V Operation
    = 2pA Typ. at 5V Operation
- Ideal for Single Supply Applications
- Common Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (Or Both) Supply Rails

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- Ideal Interface with Digital CMOS
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to Zero Volts)
- Wien Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers

Description

CA3260A and CA3260 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA3260 series circuits are dual versions of the popular CA3160 series.

Gate protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute in single supply applications.

A complementary symmetry MOS (CMOS) transistor pair, capable of swinging the output voltage to within 10mV of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

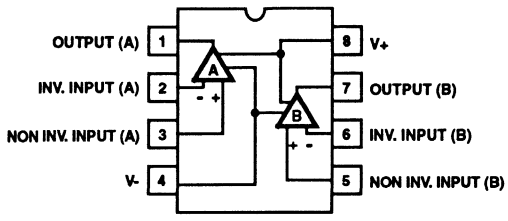
The CA3260 Series circuits operate at supply voltages ranging from 4V to 16V, or ±2V to ±8V when using split supplies. The CA3260A offers superior input characteristics over those of the CA3260.

Ordering Information

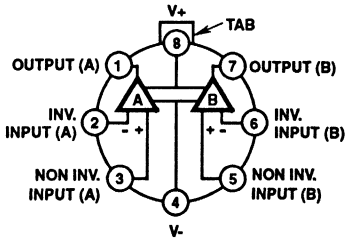
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3260E	-55°C to +125°C	8 Lead Plastic DIP
CA3260T	-55°C to +125°C	8 Pin TO-5 Can
CA3260AE	-55°C to +125°C	8 Lead Plastic DIP
CA3260AT	-55°C to +125°C	8 Pin TO-5 Can

Pinouts

CA3260 (PDIP)
TOP VIEW



CA3260 (TO-5 STYLE CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1266.2**

Absolute Maximum Ratings

DC Supply Voltage
(Between V+ and V Terminals) 16V
Differential Mode
Input Voltage 8V
DC Input Voltage ..... (V+ +8 V) to (V- -0.5 V)
Input Terminal Current 1mA
Output Short Circuit Duration (Note 1) ..... Indefinite
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range (All Types) ..... -55°C to +125°C
Storage Temperature Range (All Types) ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Typical Values Intended Only for Design Guidance

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3260A	CA3260	UNITS
V+ = +7.5V, V- = -7.5V, T_A = +25°C, Unless Otherwise Specified					
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I	f = 1MHz	4.3	4.3	pF
Unity Gain Crossover Frequency	f_T		4	4	MHz
Slew Rate	SR		10	10	V/µs
Transient Response Rise Time	t_R	C_L = 25pF, R_L = 2kΩ (Voltage Follower)	0.09	0.09	µs
Overshoot	OS		10	10	%
Settling Time (to <0.1%, V_{IN} = $4V_{P-P}$)	t_S	C_L = 25pF, R_L = 2kΩ (Voltage Follower)	1.8	1.8	µs
V+ = 5V, V- = 0V, T_A = +25°C, Unless Otherwise Specified					
Input Offset Voltage	V_{IO}		2	6	mV
Input Offset Current	I_{IO}		0.1	0.1	pA
Input Current	I_I		2	2	pA
Common Mode Rejection Ratio	CMRR		70	60	dB
Large Signal Voltage Gain	A_{OL}	V_O = $4V_{P-P}$ R_L = 20kΩ	100	100	kV/V
			100	100	dB
Common Mode Input Voltage Range	V_{ICR}		0 to 2.5	0 to 2.5	V
Supply Current	I+	V_O = 5V, R_L = ∞	1	1	mA
		V_O = 2.5V, R_L = ∞	1.2	1.2	mA
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V+$	200	200	µV/V

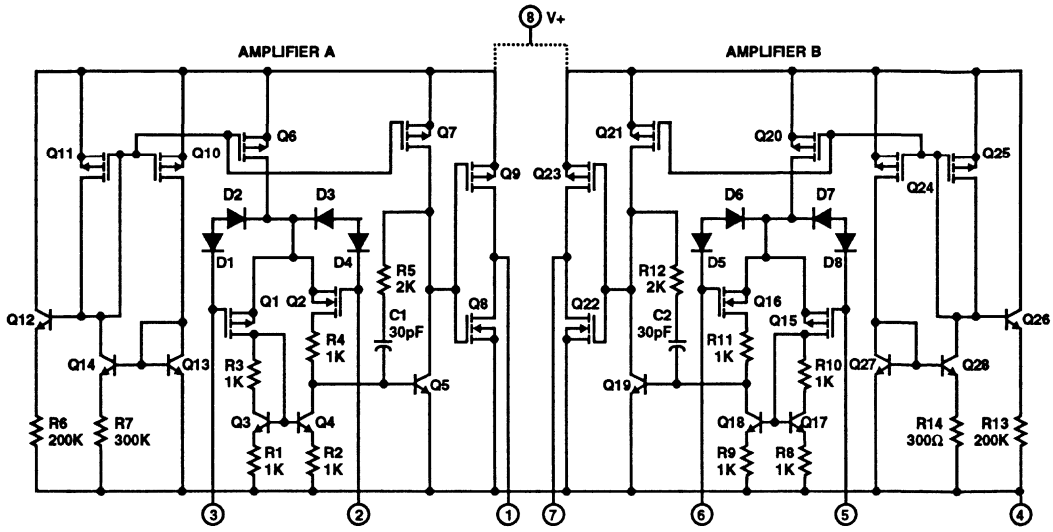
NOTE:

1. Short circuit may be applied to ground or to either supply.

Electrical Specifications For Each Amplifier at T_A = +25°C, V+ = 15V, V- = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA3260A			CA3260			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$\|V_{IO}\|$	V± = ±7.5V	-	2	5	-	6	15	mV
Input Offset Current	$\|I_{IO}\|$	V± = ±7.5V	-	0.5	20	-	0.5	30	pA
Input Current	I_I	V± = ±7.5V	-	5	30	-	5	50	pA
Large Signal Voltage Gain	A_{OL}	V_O = 10V_{P-P}, R_L = 10kΩ	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common Mode Rejection Ratio	CMRR		80	95	-	70	90	-	dB
Common Mode Input Voltage Range	V_{ICR}		0	-0.5 to 12	10	0	-0.5 to 12	10	V
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V\pm$ V± = 17.5V	-	32	150	-	32	320	µV/V
Maximum Output Voltage	V_{OM}+	R_L = 10kΩ	11	13.3	-	11	13.3	-	V
	V_{OM}-		-	0.002	0.01	-	0.002	0.01	V
	V_{OM}+	R_L = ∞	14.99	15	-	14.99	15	-	V
	V_{OM}-		-	0	0.01	-	0	0.01	V
Maximum Output Current	I_{OM}+ Source	V_O = 7.5V	12	22	45	12	22	45	mA
	I_{OM}- Sink		12	20	45	12	20	45	mA
Total Supply Current V_O (Ampli. A) = 7.5V V_O (Ampli. B) = 7.5V	I+	R_L = ∞	-	9	15.5	-	9	15.5	mA
V_O (Ampli. A) = 0V V_O (Ampli. B) = 0V			-	1.2	3	-	1.2	3	mA
V_O (Ampli. A) = 0V V_O (Ampli. B) = 7.5V			-	5	8.5	-	5	8.5	mA
Input Offset Voltage Temp. Drift	$\Delta V_{IO}/\Delta T$		-	6	-	-	8	-	µV/°C
Crosstalk		f = 1kHz	-	120	-	-	120	-	dB

Schematic Diagram



HARRIS SEMICONDUCTOR

CA3280

Dual Variable Operational Amplifier

March 1993

Features

- Low Initial Input Offset Voltage: 500μV Max. (CA3280A)
- Low Offset Voltage Change vs I_{ABC}: <500μV Typical for All Types
- Low Offset Voltage Drift: 5μV/°C Max. (CA3280A)
- Excellent Matching of the Two Amplifiers for All Characteristics
- Internal Current-Driven Linearizing Diodes Reduce the External Input Current to an Offset Component
- Flexible Supply Voltage Range ±2V to ±15V

Applications

- Voltage Controlled Amplifiers
- Voltage Controlled Oscillators
- Multipliers
- Demodulators
- Sample and Hold
- Instrumentation Amplifiers
- Function Generators
- Triangle Wave-to-Sine Wave Converters
- Comparators
- Audio Preamplifiers

Description

The CA3280 and CA3280A types consist of two variable operational amplifiers that are designed to substantially reduce the initial input offset voltage and the offset voltage variation with respect to changes in programming current. This design results in reduced "AGC thump," an objectionable characteristic of many AGC systems. Interdigitation, or crosscoupling, of critical portions of the circuit reduces the amplifier dependence upon thermal and processing variables.

The CA3280 has all the generic characteristics of an operational voltage amplifier except that the forward transfer characteristics is best described by transconductance rather than voltage gain, and the output is current, not voltage. The magnitude of the output current is equal to the product of transconductance and the input voltage. This type of operational transconductance amplifier was first introduced in 1969*, and it has since gained wide acceptance as a gateable, gain controlled building block for instrumentation and audio applications, such as linearization of transducer outputs, standardization of widely changing signals for data processing, multiplexing, instrumentation amplifiers operating from the nanopower range to high current and high speed comparators.

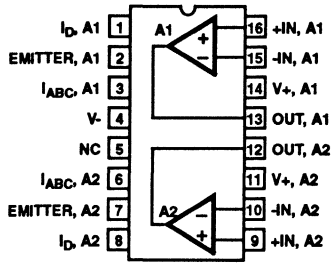
For additional application information on this device and on OTAs in general, please refer to Application Notes: ICAN-6818, ICAN-6668, and ICAN-6077.

Ordering Information

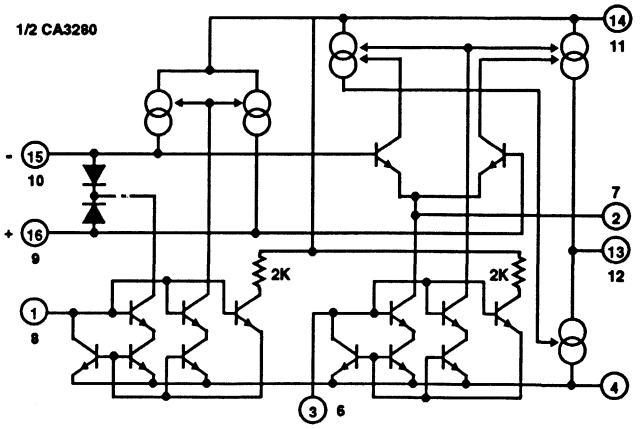
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3280AE	-55°C to +125°C	16 Lead Plastic DIP
CA3280E	0°C to +70°C	16 Lead Plastic DIP
CA3280AF3	-55°C to +125°C	16 Lead Ceramic DIP

Pinout

CA3280
(PDIP, CDIP)
TOP VIEW



Functional Diagram



*"OTA Obsoletes Op Amp", by C. F. Wheatley and H. A. Wittlinger, NEC Proceedings, December 1969.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1174.2**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V-) . . . . . +36V
Differential Input Voltage. 5V
Input Voltage Range . . . . . V+ to V-
Input Current at I_D = 0 . . . . . 100µA
Amplifier Bias Current (I_{ABC}) 10mA
Output Short Circuit Duration* . . . . . Indefinite
Linearizing Diode Bias Current, I_D 5mA
Peak Input Current with Linearizing Diode . . . . . $\pm I_D$
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

*Short circuit may be applied to ground or to either supply

Operating Conditions

Operating Temperature Range
CA3280 . . . . . 0°C to +70°C
CA3280A . . . . . -55°C to +125°C
Storage Temperature Range (All Types) . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

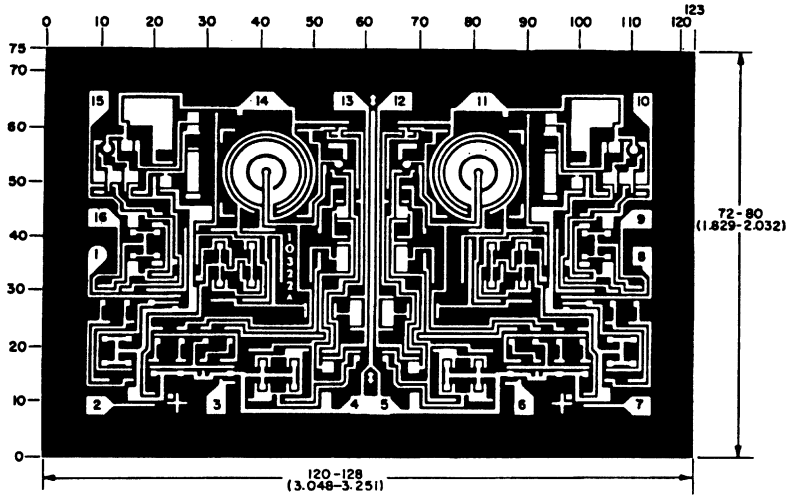
Electrical Specifications at T_A = +25°C, V± = +15V (Unless Otherwise Specified). For Equipment Design

PARAMETER	SYMBOL	TEST CONDITION	LIMITS						UNITS
			CA3280			CA3280A			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	I_{ABC} = 1mA	-	-	3	-	-	0.5	mV
		I_{ABC} = 100µA	-	0.7	3	-	0.25	0.5	mV
		I_{ABC} = 10µA	-	-	3	-	-	0.5	mV
		I_{ABC} = 1mA to 10µA, T_A = Full Temp. Range	-	0.8	4	-	0.8	1.5	mV
Input Offset Voltage Drift	$\lvert\Delta V_{IO}\rvert$	I_{ABC} = 1µA to 1mA	-	0.5	1	-	0.5	1	mV
		I_{ABC} = 100µA, T_A = Full Temp. Range	-	5	-	-	3	5	µV/°C
Amplifier Bias Voltage	V_{ABC}	I_{ABC} = 100µA	-	1.2	-	-	1.2	-	V
Peak Output Voltage		I_{ABC} = 500µA							
Positive	VOM+		12	13.7	-	12.5	13.7	-	V
Negative	VOM-		12	-14.3	-	-13.3	-14.3	-	V
Positive	VOM+	I_{ABC} = 5µA	12	13.9	-	12.5	13.9	-	V
Negative	VOM-		12	-14.5	-	-13.5	-14.5	-	V
Common Mode Input Voltage Range	V_{ICR}	I_{ABC} = 100µA	-13	-	13	-13	-	13	V
Noise Voltage	e_N	I_{ABC} = 500µA							
10Hz			-	20	-	-	20	-	$nV/\sqrt{Hz}$
1kHz			-	8	-	-	8	-	$nV/\sqrt{Hz}$
10kHz			-	7	-	-	7	-	$nV/\sqrt{Hz}$
Input Offset Current	I_{IO}	I_{ABC} = 500µA	-	0.3	0.7	-	0.3	0.7	µA
Input Bias Current	I_{IB}	I_{ABC} = 500µA	-	1.8	5	-	1.8	5	µA
		I_{ABC} = 500µA, T_A = Full Temp. Range	-	3	8	-	3	8	µA
Peak Output Current		I_{ABC} = 500µA							
Source	IOM+		350	410	650	350	410	650	µA
Sink	IOM-		-350	-410	-650	-350	-410	-650	µA

Electrical Specifications at T_A = +25°C, V± = +15V (Unless Otherwise Specified). **For Equipment Design (Continued)**

PARAMETER	SYMBOL	TEST CONDITION	LIMITS						UNITS
			CA3280			CA3280A			
			MIN	TYP	MAX	MIN	TYP	MAX	
Source	IOM+	I_{ABC} = 5µA	3	4.1	7	3	4.1	7	µA
Sink	IOM-		-3	-4.1	-7	-3	-4.1	-7	µA
Sink and Source	IOM-, IOM+	I_{ABC} = 500µA, T_A = Full Temp. Range	350	450	550	350	450	550	µA
Linearization Diodes									
Dynamic Impedance		I_D = 100µA	-	700	-	-	700	-	Ω
Offset Current		I_D = 100µA	-	10	-	-	10	-	µA
		I_D = 10µA	-	0.5	1	-	0.5	1	µA
Diode Network Supply Current		I_{ABC} = 100µA	250	400	800	250	400	800	µA
Amplifier Supply Current (Per Amplifier)	I+	I_{ABC} = 500µA	-	2	2.4	-	2	2.4	mA
Amplifier Output Leakage Current	I_{OL}	I_{ABC} = 0, V_O = 0V	-	0.015	0.1	-	0.015	0.1	nA
		I_{ABC} = 0, V_O = 30V	-	0.15	1	-	0.15	1	nA
Common Mode Rejection Ratio	CMRR	I_{ABC} = 100µA	80	100	-	94	100	-	dB
Power Supply Rejection Ratio	PSRR	I_{ABC} = 100µA	86	105	-	94	105	-	dB
Open Loop Voltage Gain	A_{OL}	I_{ABC} = 100µA, R_L = ∞ V_O = 20V_{P-P}	94	100	-	94	100	-	dB
			50	100	-	50	100	-	kV/V
Forward Transconductance,									
Large Signal	Gm	I_{ABC} = 50µA	-	0.8	1.2	-	0.8	1.2	mmho
Small Signal	gm	I_{ABC} = 1mA	-	16	22	-	16	22	mmho
Input Resistance	R_I	I_{ABC} = 10µA	0.5	-	-	0.5	-	-	MΩ
Channel Separation		f = 1kHz	-	94	-	-	94	-	dB
Open Loop Total Harmonic Distortion	THD	f = 1kHz, I_{ABC} = 1.5mA, R_L = 15kΩ, V_O = 20V_{P-P}	-	0.4	-	-	0.4	-	%
Bandwidth	f_T	I_{ABC} = 1mA, R_L = 100Ω	-	9	-	-	9	-	MHz
Slew Rate, Open Loop	SR	I_{ABC} = 1mA	-	125	-	-	125	-	V/µs
Capacitance		I_{ABC} = 100µA							
Input	C_I		-	4.5	-	-	4.5	-	pF
Output	C_O		-	7.5	-	-	7.5	-	pF
Output Resistance	R_O	I_{ABC} = 100µA	-	63	-	-	63	-	MΩ

Metallization Mask Layout



Dimensions in parentheses are in millimeters and derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

Description

Figures 1 and 2 show the equivalent circuits for the current source and linearization diodes in the CA3280. The current through the linearization network is approximately equal to the programming current. There are several advantages to driving these diodes with a current source. First, only the offset current from the biasing network flows through the input resistor. Second, another input is provided to extend the gain control dynamic range. And third, the input is truly differential and can accept signals within the common mode range of the CA3280.

The structure of the variable operational amplifier eliminates the need for matched resistor networks in differential to single ended converters, as shown in Figure 3. A matched resistor network requires ratio matching of 0.01% or trimming for 80dB of common-mode rejection. The CA3280, with its excellent common mode rejection ratio, is capable of converting a small (±25mV) differential input signal to a single-ended output without the need for a matched resistor network.

Figure 4 shows the CA3280 in a typical gain control application. Gain control can be performed with the amplifier bias current (I_{ABC}). With no diode bias current, the gain is merely gmR_L. For example, with an I_{ABC} of 1mA, the gm is approximately 16mmho. With the CA3280 operating into a 5kΩ resistor, the gain is 80.

The need for external buffers can be eliminated by the use of low value load resistors, but the resulting increase in the required amplifier bias current reduces the input impedance of the CA3280. The linearization diode impedance also decreases as the diode bias current increases, which further loads the input. The diodes, in addition to acting as a linearization network, also operate as an additional attenuation system to accommodate input signals in the volt range when they are applied through appropriate input resistors.

Figure 7 shows a triangle wave-to-sine wave converter using the CA3280. Two 100kΩ resistors are connected between the differential amplifier emitters and V+ to reduce the current flow through the differential amplifier. This allows the amplifier to fully cut off during peak input signal excursions. THD is appropriately 0.37% for this circuit.

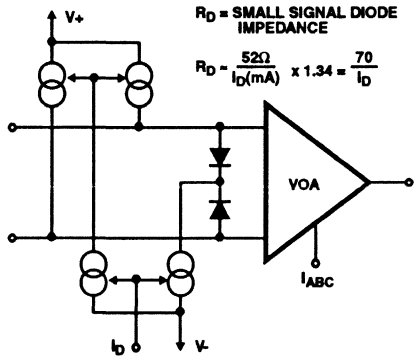


FIGURE 1. VOA SHOWING LINEARIZATION DIODES AND CURRENT DRIVE

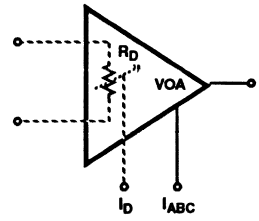


FIGURE 2. BLOCK DIAGRAM OF LINEARIZED VOA

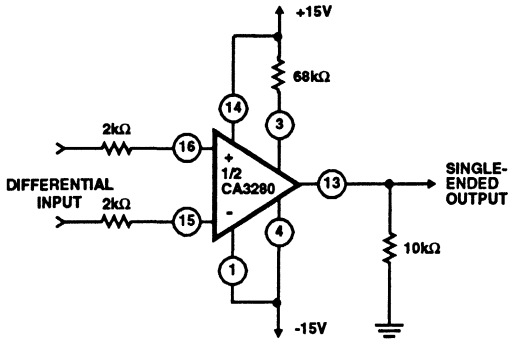


FIGURE 3. DIFFERENTIAL TO SINGLE ENDED CONVERTER

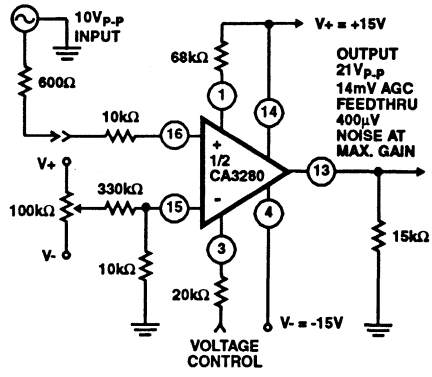


FIGURE 4. TYPICAL GAIN CONTROL CIRCUIT

Test Circuits

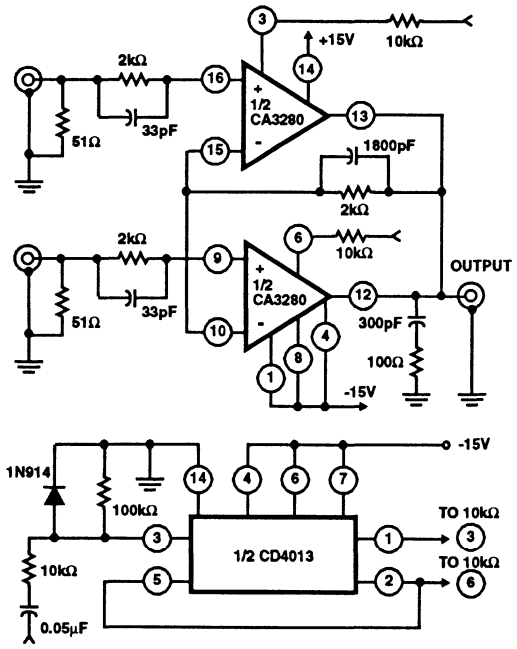


FIGURE 5. TWO CHANNEL LINEAR MULTIPLEXER

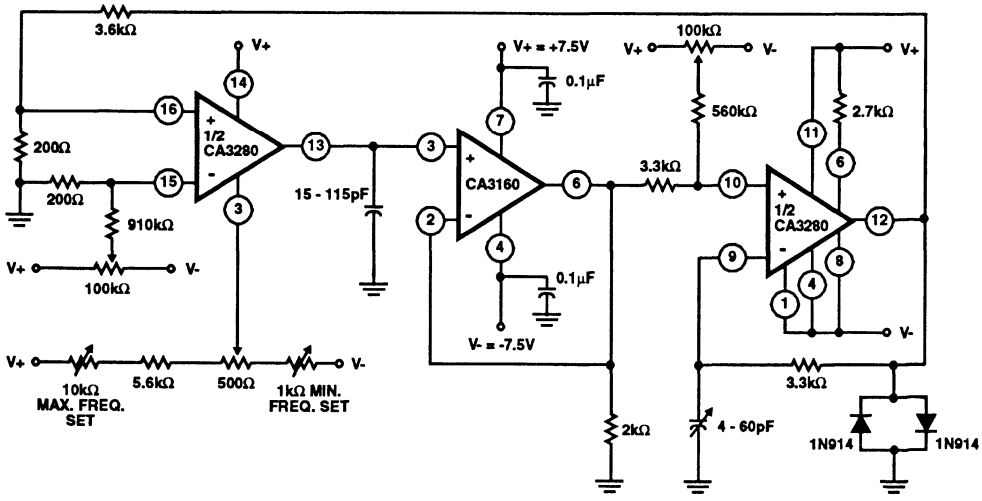


FIGURE 6. CA3280 USED IN CONJUNCTION WITH A CA3160 TO PROVIDE A FUNCTION GENERATOR WITH A TUNABLE RANGE OF 2Hz TO 1MHz

Test Circuits (Continued)

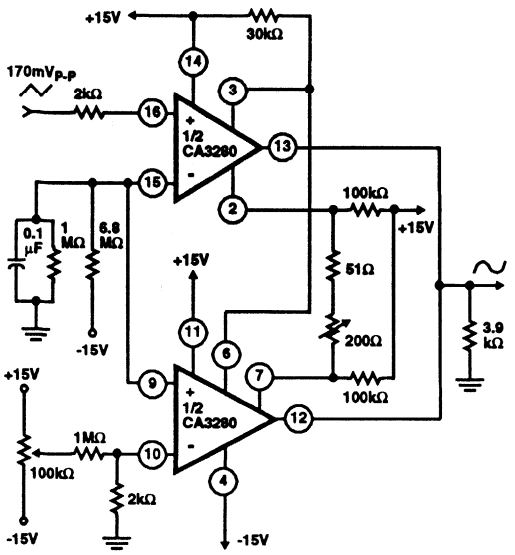


FIGURE 7. TRIANGLE WAVE-TO-SINE WAVE CONVERTER

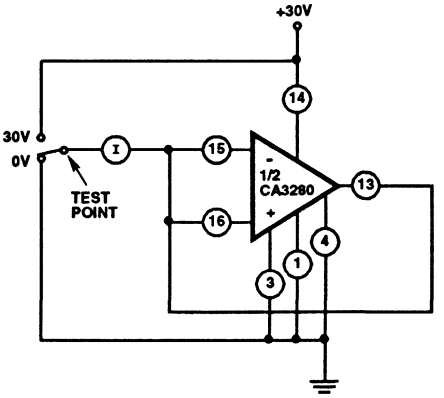


FIGURE 8. LEAKAGE CURRENT TEST CIRCUIT

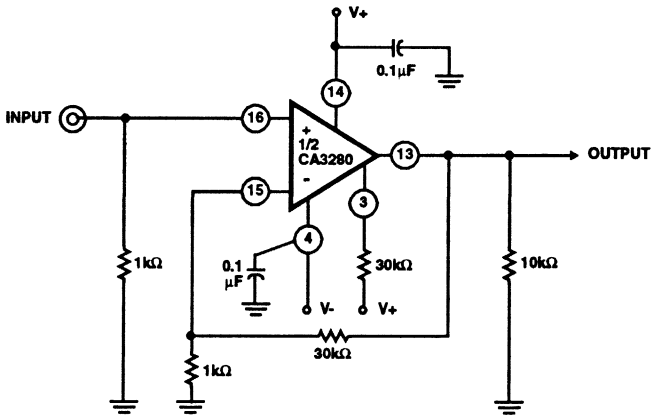
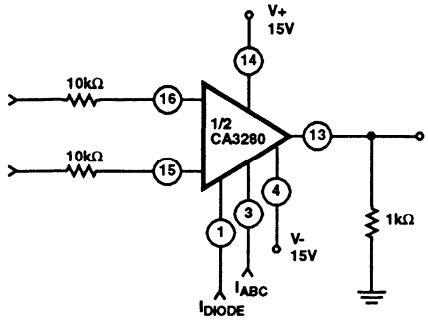
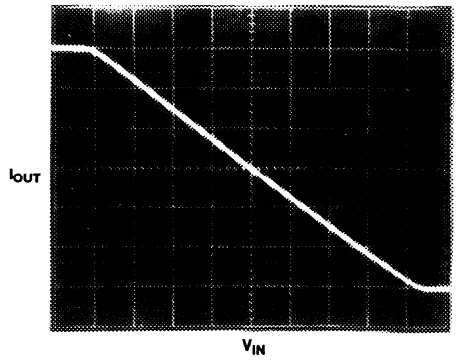


FIGURE 9. CHANNEL SEPARATION TEST CIRCUIT

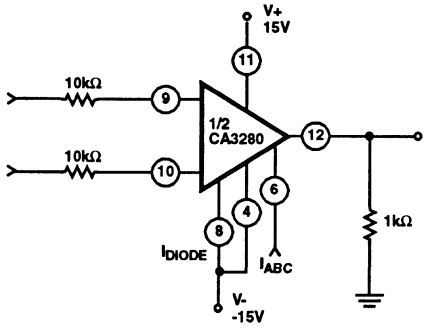
Test Circuits (Continued)

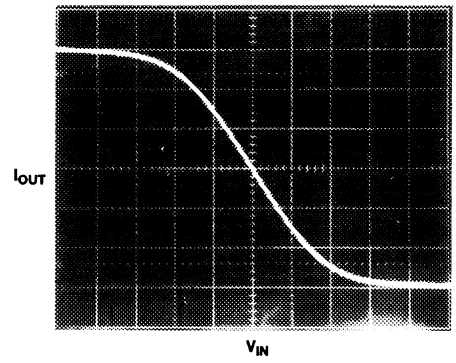




I_{ABC} = 650µA
I_D = 200µA
Vertical = 200µA/Div.
Horizontal = 1V/Div.

(A) EFFECTS OF DIODE LINEARIZATION, WITH DIODE PROGRAMMING TERMINAL ACTIVE





I_{ABC} = 650µA
I_D = 0
Vertical = 200µA/Div.
Horizontal = 25mV/Div.

(B) WITH DIODE PROGRAMMING TERMINAL CUT-OFF

FIGURE 10. CA3280 TRANSFER CHARACTERISTICS

Performance Curves

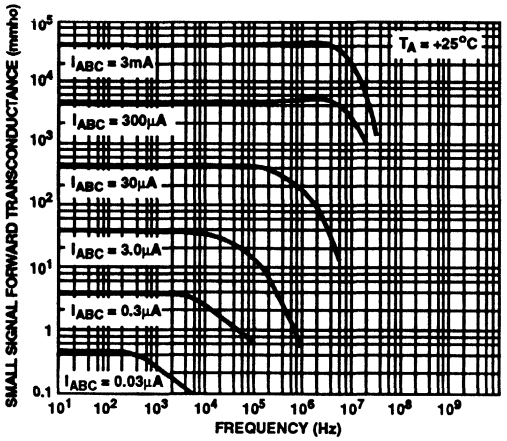


FIGURE 11. AMPLIFIER GAIN vs FREQUENCY

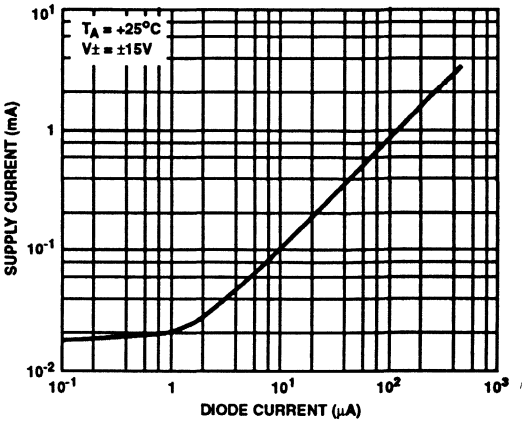


FIGURE 12. SUPPLY CURRENT vs DIODE CURRENT

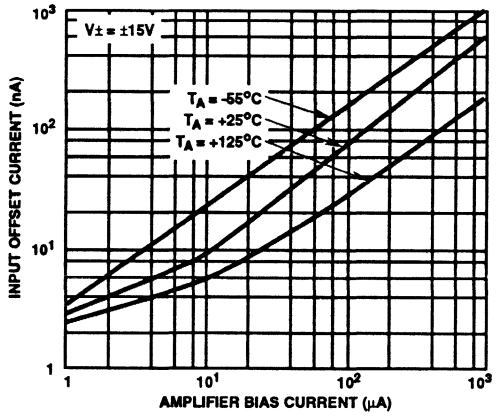


FIGURE 13. INPUT OFFSET CURRENT vs AMPLIFIER BIAS CURRENT

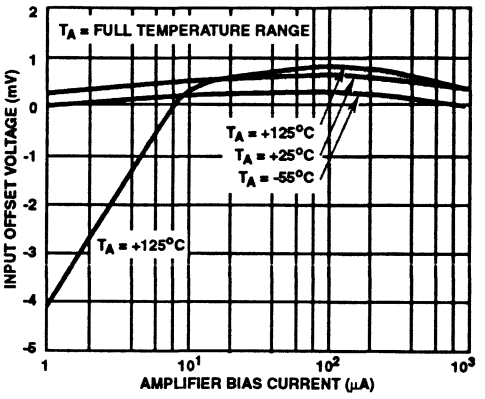


FIGURE 14. INPUT OFFSET VOLTAGE vs AMPLIFIER BIAS CURRENT

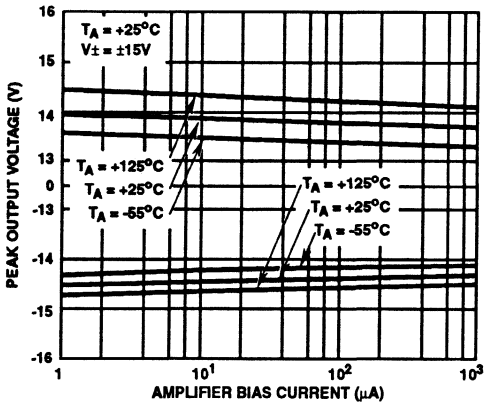


FIGURE 15. PEAK OUTPUT VOLTAGE vs AMPLIFIER BIAS CURRENT

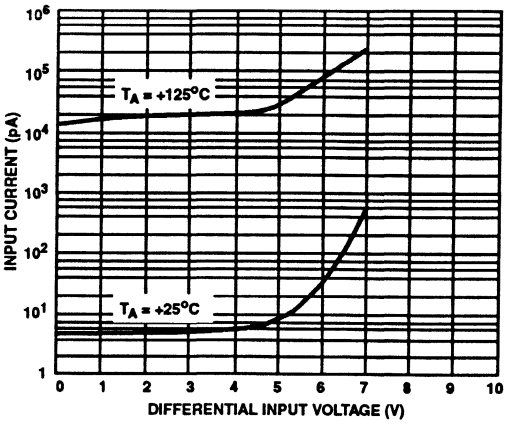


FIGURE 16. INPUT CURRENT vs INPUT DIFFERENTIAL VOLTAGE

Performance Curves (Continued)

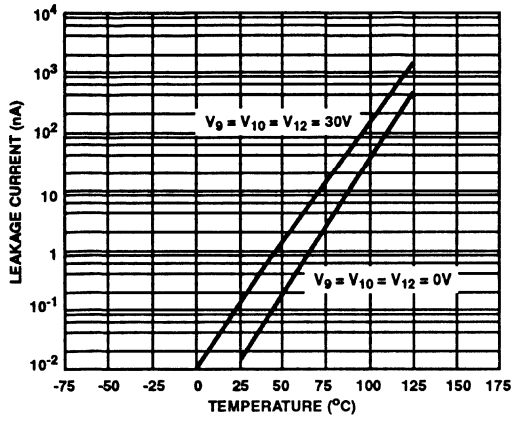


FIGURE 17. LEAKAGE CURRENT vs TEMPERATURE

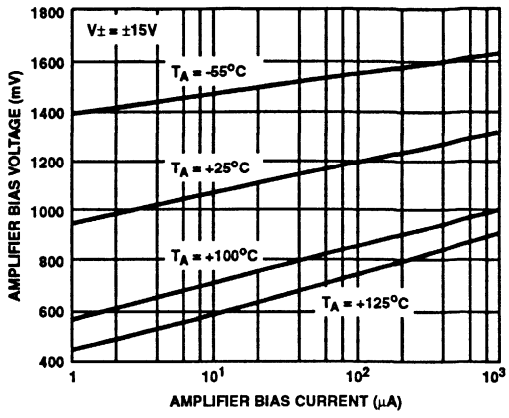


FIGURE 18. AMPLIFIER BIAS VOLTAGE vs AMPLIFIER BIAS CURRENT

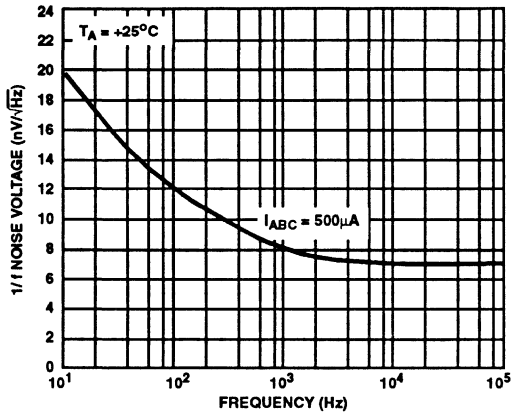


FIGURE 19. 1/F NOISE vs FREQUENCY

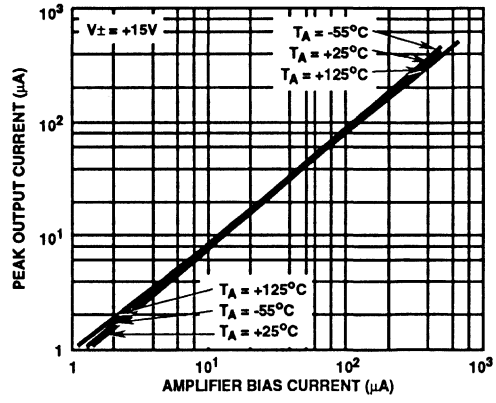


FIGURE 20. PEAK OUTPUT CURRENT vs AMPLIFIER BIAS CURRENT

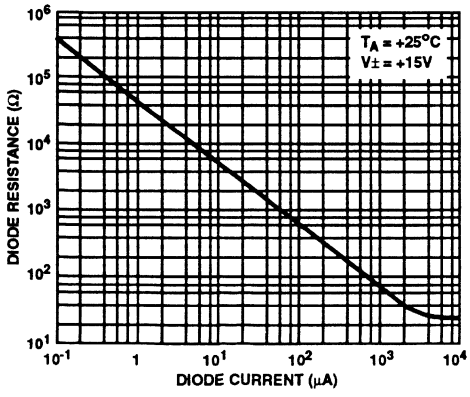


FIGURE 21. DIODE RESISTANCE vs DIODE CURRENT

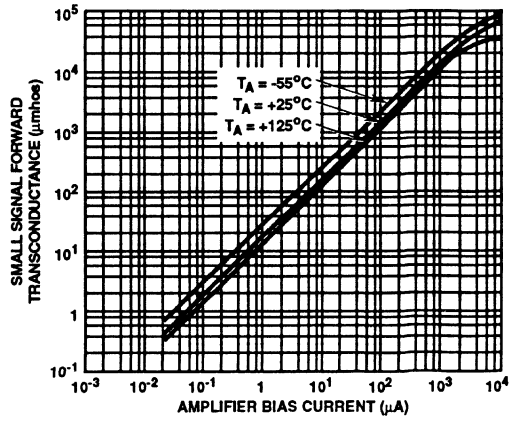


FIGURE 22. AMPLIFIER GAIN vs AMPLIFIER BIAS CURRENT

Performance Curves (Continued)

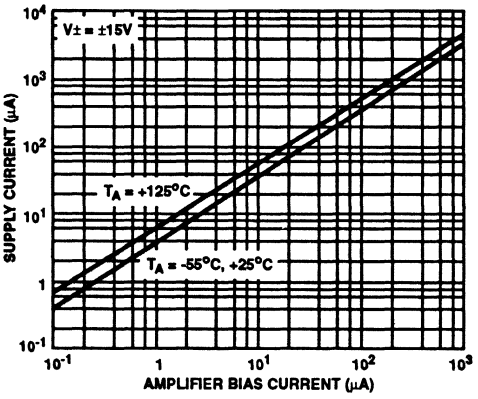


FIGURE 23. SUPPLY CURRENT vs AMPLIFIER BIAS CURRENT

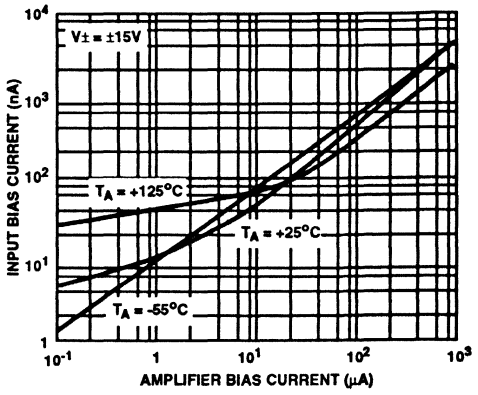


FIGURE 24. INPUT BIAS CURRENT vs AMPLIFIER BIAS CURRENT

HARRIS SEMICONDUCTOR

CA3420

Low Supply Voltage, Low Input Current BiMOS Operational Amplifiers

March 1993

Features

- 2V Supply at 300μA Supply Current
- 1pA (Typ.) Input Current (Essentially Constant to 85°C)
- Rail-to-Rail Output Swing (Drive ±2mA into 1kΩ Load)
- Pin Compatible with 741 Operational Amplifiers

Applications

- pH Probe Amplifiers
- Picoammeters
- Electrometer (High Z) Instruments
- Portable Equipment
- Inaccessible Field Equipment
- Battery-Dependent Equipment (Medical and Military)

Ordering Information

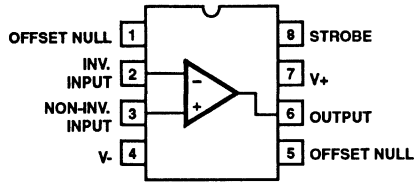
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3420AE	-55°C to +125°C	8 Lead Plastic DIP
CA3420AT	-55°C to +125°C	8 Pin Can
CA3420E	-55°C to +125°C	8 Lead Plastic DIP
CA3420T	-55°C to +125°C	8 Pin Can

Description

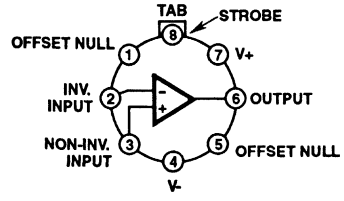
The CA3420A and CA3420 are integrated circuit operational amplifiers that combine PMOS transistors and bipolar transistors on a single monolithic chip. The CA3420A and CA3420 BiMOS operational amplifiers feature gate protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 1pA). The internal bootstrapping network features a unique guardbanding technique for reducing the doubling of leakage current for every 10°C increase in temperature. The CA3420 series operates at total supply voltages from 2V to 20V either single or dual supply. These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Additionally, they have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common mode input voltage capability down to 0.45V below the negative supply terminal, an important attribute for single supply application. The output stage uses a feedback OTA type amplifier that can swing essentially from rail-to-rail. The output driving current of 1.5mA (min) is provided by using nonlinear current mirrors.

Pinouts

CA3420
(PDIP)
TOP VIEW

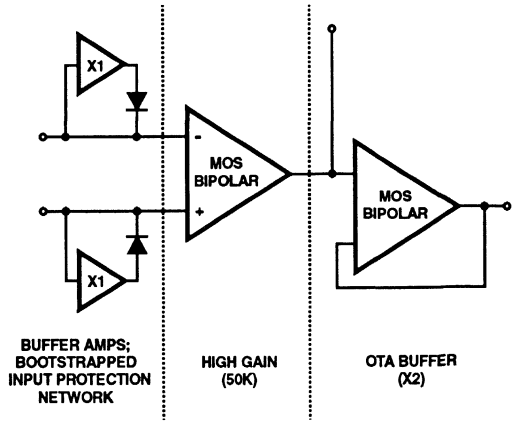


CA3420
(TO-5 CAN)
TOP VIEW



Functional Diagram

CA3420



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1320.2**

Specifications CA3420, CA3420A

Absolute Maximum Ratings

Supply Voltage
(Between V+ and V- Terminals) 22V
Differential Input Voltage..... 15V
DC Input Voltage .....(V+ + 8V) to (V- -0.5V)
Input Current.....1mA
Output Short Circuit Duration (Note 1)..... Indefinite
Junction Temperature..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec)..... +300°C

Operating Conditions

Operating Temperature Range (All Types) .....-55°C to +125°C
Storage Temperature Range (All Types).....-65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Typical Values Intended Only for Design Guidance. V+ = +10V; V- = -10V T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS		CA3420A	CA3420	UNITS
Input Resistance	R_I			150	150	TΩ
Input Capacitance	C_I			4.9	4.9	pF
Output Resistance	R_O			300	300	Ω
Equivalent Input Noise Voltage	e_N	f = 1kHz	R_S = 100Ω	62	62	$nV/\sqrt{Hz}$
		f = 10kHz		38	38	$nV/\sqrt{Hz}$
Short-Circuit Current Source	$I_{OM}+$			2.6	2.6	mA
To Opposite Supply Sink	$I_{OM}-$			2.4	2.4	mA
Gain Bandwidth Product	f_T			0.5	0.5	MHz
Slew Rate	SR			0.5	0.5	V/μs
Transient Response Rise Time	t_R	R_L = 2kΩ, C_L = 100pF		0.7	0.7	μs
Overshoot	OS			15	15	%
Current from Terminal 8 To V-	I_8+			20	20	μA
Current from Terminal 8 To V+	I_8-			2	2	mA

NOTE:

1. Short circuit may be applied to ground or to either supply.

Electrical Specifications For Equipment Design. At V+ = 1V, V- = -1V, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA3420A			CA3420			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$\|V_{IO}\|$		-	2	5	-	5	10	mV
Input Offset Current (Note 1)	$\|I_{IO}\|$		-	0.01	4	-	0.01	4	pA
Input Current (Note 1)	$\|I_I\|$		-	0.02	5	-	1	5	pA
Large Signal Voltage Gain	A_{OL}	R_L = 10kΩ	20	100	-	10	100	-	kV/V
			86	100	-	80	100	-	dB
Common Mode Rejection Ratio	CMRR		-	560	1000	-	560	1800	µV/V
			60	65	-	55	65	-	dB
Common Mode Input Voltage Range	V_{ICR} +		+0.2	+0.5	-	10.2	+0.5	-	V
	V_{ICR} -		-1	-1.3	-	-	-1.3	-	V
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V$	-	32	320	-	100	1000	µV/V
			70	90	-	60	80	-	dB
Max Output Voltage	V_{OM} +	R_L = ∞	+0.90	+0.95	-	+0.90	+0.95	-	V
	V_{OM} -		-0.85	-0.91	-	-0.85	-0.91	-	V
Supply Current	I+		-	350	650	-	350	650	µA
Device Dissipation	P_D		-	0.7	1.1	-	0.7	1.1	mW
Input Offset Voltage Temp. Drift	$\Delta V_{IO}/\Delta T$		-	4	-	-	4	-	µV/°C

NOTE:

1. The maximum limit represents the levels obtainable on high speed automatic test equipment. Typical values are obtained under laboratory conditions.

Electrical Specifications For Equipment Design. At V+ = 10V, V- = -10V, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA3420A			CA3420			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$\|V_{IO}\|$		-	2	5	-	5	10	mV
Input Offset Current (Note 1)	$\|I_{IO}\|$		-	0.03	4	-	0.03	4	pA
Input Current (Note 1)	$\|I_I\|$		-	0.05	5	-	0.05	5	pA
Large Signal Voltage Gain	A_{OL}	R_L = 10kΩ	20	100	-	10	100	-	kV/V
			86	100	-	80	100	-	dB
Common Mode Rejection Ratio	CMRR		-	100	320	-	100	320	µV/V
			70	80	-	70	80	-	dB
Common Mode Input Voltage Range	V_{ICR} +		+9.0	+9.3	-	+8.5	+9.3	-	V
	V_{ICR} -		-10	-10.3	-	-10	-10.3	-	V
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V$	-	32	320	-	32	320	µV/V
			70	90	-	70	90	-	dB
Max Output Voltage	V_{OM} +	R_L = ∞	+9.7	+9.9	-	+9.7	+9.9	-	V
	V_{OM} -		-9.7	-9.85	-	-9.7	-9.85	-	V
Supply Current	I+		-	450	1000	-	450	1000	µA
Device Dissipation	P_D		-	9	14	-	9	14	mW
Input Offset Voltage Temp. Drift	$\Delta V_{IO}/\Delta T$		-	4	-	-	4	-	µV/°C

NOTE:

1. The maximum limit represents the levels obtainable on high speed automatic test equipment. Typical values are obtained under laboratory conditions.

Typical Performance Curves

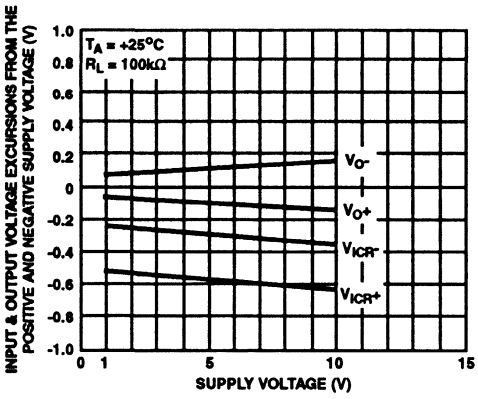


FIGURE 1. OUTPUT VOLTAGE SWING AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

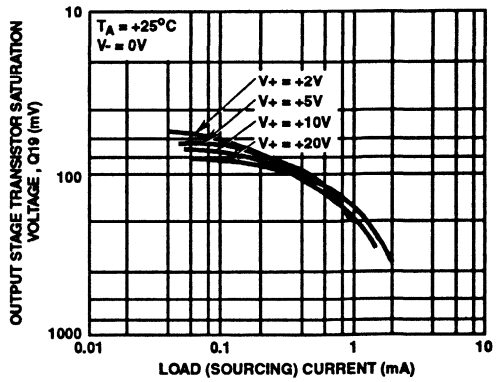


FIGURE 2. OUTPUT VOLTAGE vs LOAD SOURCING CURRENT

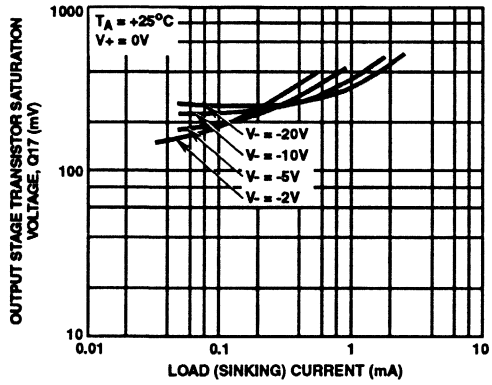


FIGURE 3. OUTPUT VOLTAGE vs LOAD SINKING CURRENT

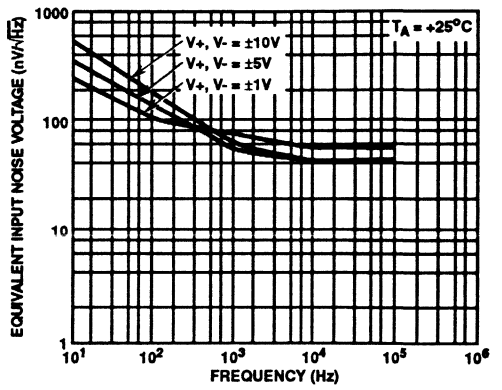


FIGURE 4. INPUT NOISE VOLTAGE vs FREQUENCY

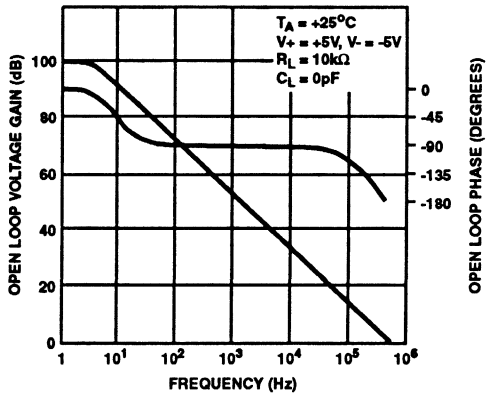


FIGURE 5. OPEN LOOP GAIN AND PHASE SHIFT RESPONSE

Application Circuits

Picoameter Circuit

The exceptionally low input current (typically 0.2pA) makes the CA3420 highly suited for use in a picoameter circuit. With only a single 10GΩ resistor, this circuit covers the range from ±1.5pA. Higher current ranges are possible with suitable switching techniques and current scaling resistors. Input transient protection is provided by the 1MΩ resistor in series with the input. Higher current ranges require that this resistor be reduced. The 10MΩ resistor connected to pin 2 of the CA3420 decouples the potentially high input capacitance often associated with lower current circuits and reduces the tendency for the circuit to oscillate under these conditions.

High Input Resistance Voltmeter

Advantage is taken of the high input impedance of the CA3420 in a high input resistance DC. voltmeter. Only two 1.5V "AA" type penlite batteries power this exceedingly high-input resistance (>1,000,000MΩ) DC voltmeter. Full-scale deflection is ±500mV, ±150mV, and ±15mV. Higher voltage ranges are easily added with external input voltage attenuator networks.

The meter is placed in series with the gain network, thus eliminating the meter temperature coefficient error term.

Supply current in the standby position with the meter undeflected is 300µA. At full-scale deflection this current rises to 800µA. Carbon-zinc battery life should be in excess of 1,000 hours.

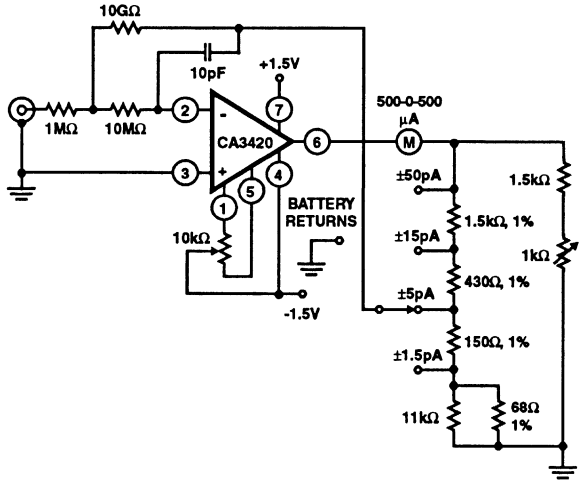


FIGURE 6. PICOAMETER CIRCUIT

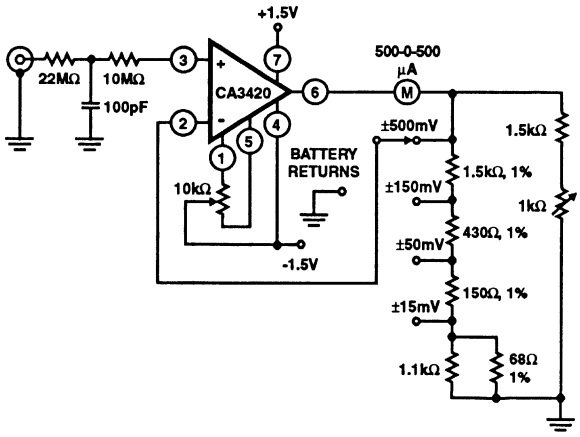


FIGURE 7. HIGH INPUT RESISTANCE VOLTMETER

HARRIS SEMICONDUCTOR

CA3440

March 1993

Nanopower BiMOS Operational Amplifier

Features

- High Input Resistance.....2TΩ (Typ)
- Standby Power at V+ = 5V..... 300nW (Typ)
- Supply Current, BW, Slew Rate Programmable Using External Resistor
- Input Current .....10pA (Typ)
- 5V to 15V Supply
- Output Drives Typical Bipolar Type Loads
- Low Cost 8 Pin Mini-DIP, TO-5 Can, SOIC

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3440AE	-55°C to +125°C	8 Lead Plastic DIP
CA3440AM	-55°C to +125°C	8 Lead SOIC
CA3440AT	-55°C to +125°C	8 Pin Can
CA3440E	-55°C to +125°C	8 Lead Plastic DIP
CA3440M	-55°C to +125°C	8 Lead SOIC
CA3440T	-55°C to +125°C	8 Pin Can

Description

The CA3440A and CA3440* are integrated circuit operational amplifiers that combine the advantages of MOS and bipolar transistors on a single monolithic chip.

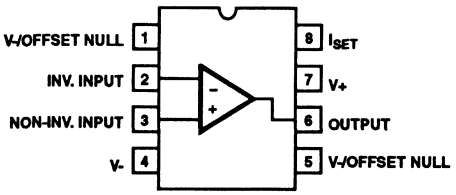
The CA3440A and CA3440 BiMOS op amps feature gate protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 10pA). These devices operate at total supply voltage from 5V to 15V and can be operated over the temperature range from -55°C to +125°C. Their virtues are programmability and very low standby power consumption (300nW). These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminals, an important attribute for single supply applications. The output stage uses MOS complementary source follower form which permits moderate load driving capability (10kΩ) at very low standby currents (50nA).

The CA3440A and CA3440 have the same 8 pin terminal pinout as the "741" and other industry standard op amps with two exceptions: terminals one and five must be connected to the negative supply or to a potentiometer if nulling is required. Terminal 8 must be programmed through an external resistor returned to the negative supply.

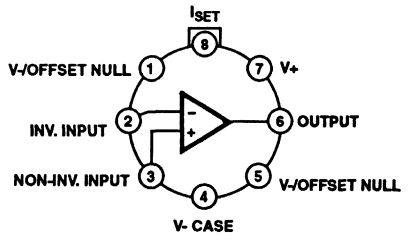
* Formerly Dev. Type No. TA10590.

Pinouts

CA3440
(PDIP, SOIC)
TOP VIEW



CA3440
(TO-5 CAN)
TOP VIEW



File Number 1318.2

Absolute Maximum Ratings

Supply Voltage
(Between V+ and V- Terminals) 25V
Differential Input Voltage..... 9V
DC Input Voltage ..... (V+ +8V) to (V- -0.5V)
Input Current.....1mA
Junction Temperature..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Output Short Circuit Duration (Note 1)..... Indefinite
Lead Temperature (Soldering 10 Sec) ..... +300°C

Operating Conditions

Operating Temperature Range .....-55°C to +125°C
Storage Temperature Range.....-65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Typical Values Intended Only for Design Guidance. V+ = +5V, V- = -5V; R_{SET} = 10MΩ, T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS		CA3440A	CA3440	UNITS
Input Resistance	R_I			2	2	TΩ
Input Capacitance	C_I			3.5	3.5	pF
Output Resistance	R_O			450	450	Ω
Equivalent Input	e_N	f = 1kHz	R_S = 100Ω	110	110	$nV/\sqrt{Hz}$
Noise Voltage		f = 10kHz		110	110	$nV/\sqrt{Hz}$
Short-Circuit Current Source	IOM+			15	15	mA
To Opposite Supply Sink	IOM-			4.5	4.5	mA
Gain Bandwidth Product	f_T			63	63	kHz
Slew Rate	SR			0.03	0.03	V/μs
Transient Response Rise Time	t_R	R_L = 10kΩ, C_L = 100pF		5.6	5.6	μs
Overshoot	OS			10	10	%

NOTE:

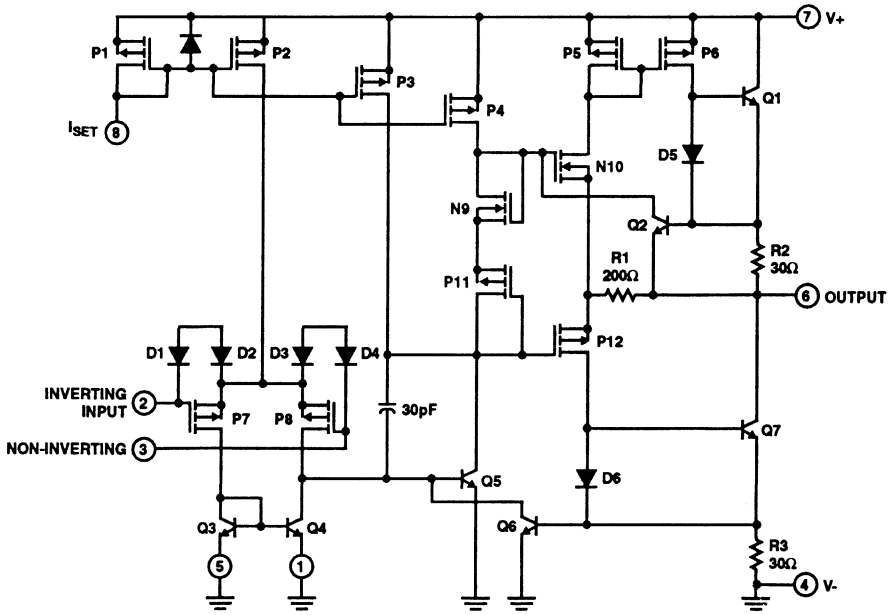
1. Short circuit may be applied to ground or to either supply.

Specifications CA3440, CA3440A

Electrical Specifications For Equipment Design. At V+ = +5V, V- = -5V, R_{SET} = 10MΩ, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA3440A			CA3440			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$\|V_{IO}\|$		-	2	5	-	5	10	mV
Input Offset Current	$\|I_{IO}\|$		-	2.5	20	-	2.5	30	pA
Input Current	$\|I_I\|$		-	10	40	-	10	50	pA
Large Signal Voltage Gain	AOL	R_L = 10kΩ	10	100	-	10	100	-	kV/V
			80	100	-	80	100	-	dB
Common Mode Rejection Ratio	CMRR		-	100	320	-	100	320	µV/V
			70	80	-	70	80	-	dB
Common Mode Input Voltage Range	VICR +		+3.5	+3.7	-	+3.5	+3.7	-	V
	VICR -		-5.0	-5.3	-	-5.0	-5.3	-	V
Power Supply Rejection Ratio	PSRR		-	32	320	-	32	320	µV/V
			70	90	-	70	90	-	dB
Max Output Voltage	VOM +		+3	+3.2	-	+3	+3.2	-	V
	VOM -		-3	-3.2	-	-3	-3.2	-	V
Supply Current	I+		-	10	17	-	10	17	µA
Device Dissipation	P_D		-	100	170	-	100	170	µW
Input Offset Voltage Temp. Drift	$\Delta V_{IO}/\Delta T$		-	4	-	-	4	-	µV/°C

Schematic Diagram



Typical Performance Curves

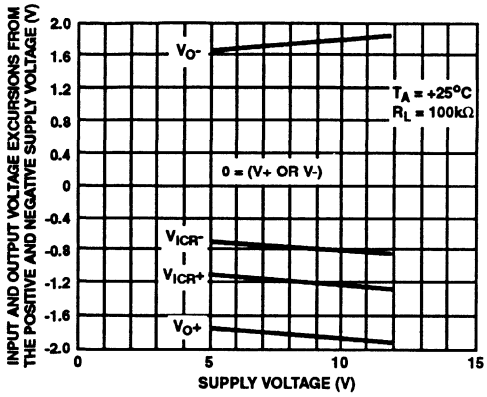


FIGURE 1. OUTPUT VOLTAGE SWING AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

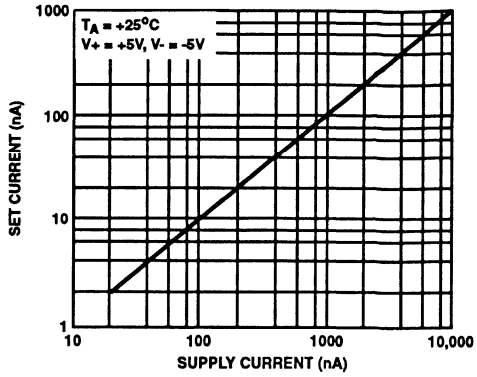


FIGURE 2. SET CURRENT vs SUPPLY CURRENT

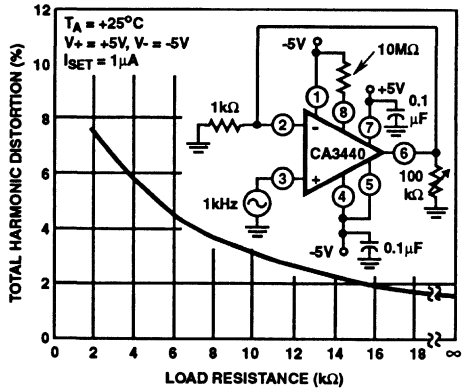


FIGURE 3. TOTAL HARMONIC DISTORTION vs LOAD RESISTANCE

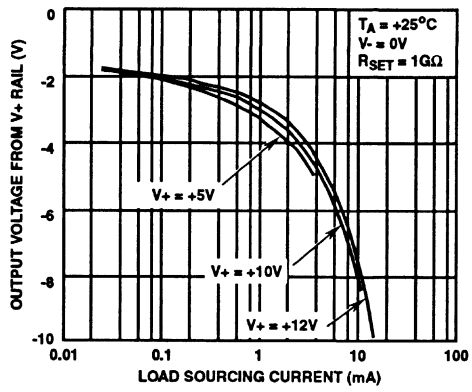


FIGURE 4. OUTPUT VOLTAGE vs SOURCING LOAD CURRENT

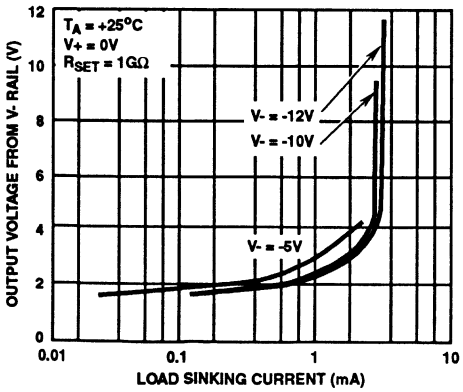


FIGURE 5. OUTPUT VOLTAGE vs SINKING LOAD CURRENT

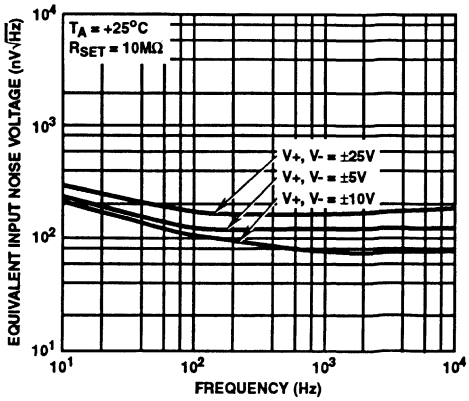


FIGURE 6. INPUT NOISE VOLTAGE vs FREQUENCY

Typical Performance Curves (Continued)

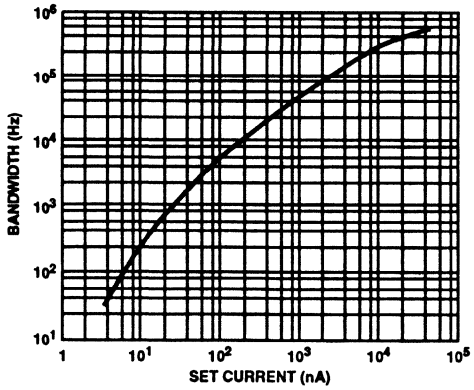


FIGURE 7. BANDWIDTH vs SET CURRENT

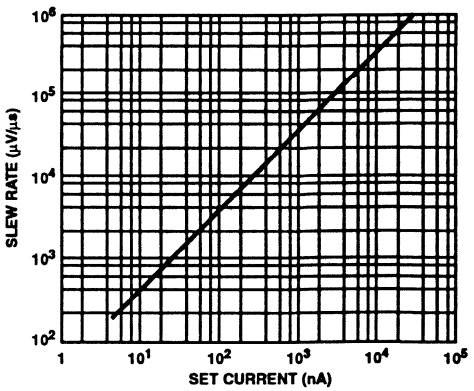


FIGURE 8. SLEW RATE vs SET CURRENT

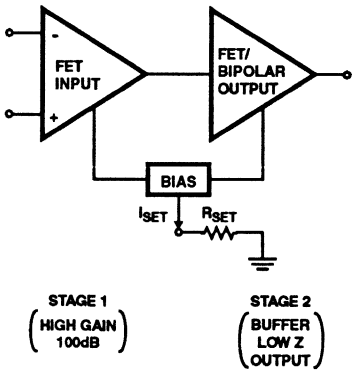


FIGURE 9. NANOPOWER OP AMP (SUPPLY CURRENT PROGRAMMABLE USING R_{SET}), 1pA TYPICAL INPUT BIAS CURRENT, 4.0V TO 15V SUPPLY

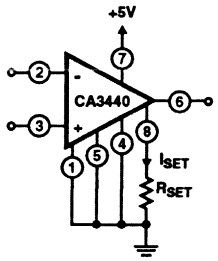


FIGURE 10. NANOPOWER OP AMP (USABLE STANDBY POWER vs PROGRAMMING RESISTOR R_{SET})

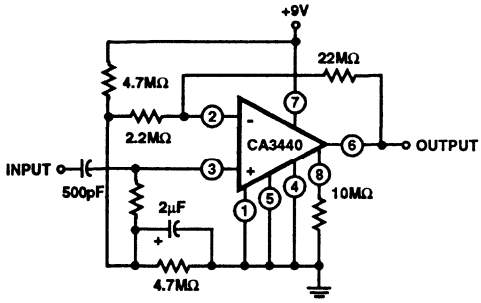
As R_{SET} is increased, I_{SET} and the standby power decrease while the BW/SR also decreases.

Operating at a +5V single supply, the CA3440 exhibits the following characteristics:

R_{SET}	STANDBY POWER	BW	SR
1MΩ	250μW	164kHz	0.17V/μs
10MΩ	25μW	27kHz	0.017V/μs
100MΩ	2.5μW	2.6kHz	0.0017V/μs
1GΩ	250nW	78kHz	0.00017V/μs

The CA3440 is pin compatible with the 741 except that pins 1 and 5 (typical negative nulling pins) must be connected either directly to pin 4 or to a negative nulling potentiometer. In addition, pin 8, the I_{SET} terminal, must be returned to either ground or -V via R_{SET}

Applications Circuits



R_{IN} > 20MΩ
Standby Power = 90μW
Gain = 20dB
BW: 20Hz to 3kHz
SR = 0.016V/μs

FIGURE 11. HIGH INPUT IMPEDANCE AMPLIFIER

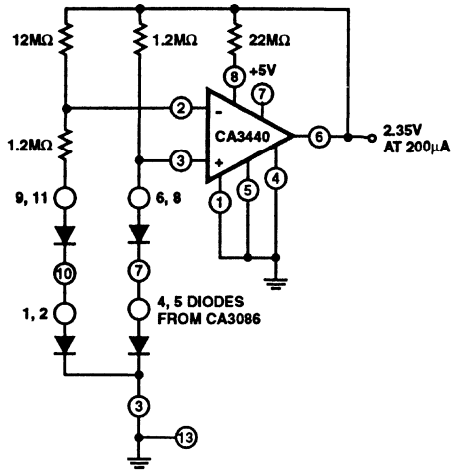


FIGURE 12. MICROPOWER BANDGAP REFERENCE

HARRIS SEMICONDUCTOR

CA3450

Video Line Driver, High Speed Operational Amplifier

March 1993

Features

- High Open Loop Gain at Video Frequencies
  - A_{OL} .....>40dB at f = 5MHz
- Power Bandwidth of 10MHz; A_{CL} = 5; V_O = ±3.5V
- Slew Rate at Full Load..... 330V/µsec ($A_V \geq 10$)
- f_T = 220MHz; C_C = 0pF With a Load of 50Ω II20pFII 1MΩ (Scope Input)
- V_{OUT} = ±4.1V Into 75Ω
- Offset Null Terminals

Applications

- Video Line Driver
- High Frequency Unity Gain Buffer
- Pulse Amplifier
- High Speed Comparator
- High Frequency Oscillator and Video Amplifiers
- Driver for A/D's in Video Applications.....10MHz BW

Description

The CA3450* is a large signal video line driver and high speed operational amplifier capable of driving 50Ω transmission lines and flash A/D's. The uncompensated unity gain crossing occurs at 230MHz without load. It can operate at dual or single supplies of ±7.25V or 14.5V, respectively. The CA3450 can be compensated with a single capacitor network. It has output drive capability of 75mA SINK or SOURCE. The CA3450 is capable of driving Flash A/D's in video or high speed instrumentation (accurate) applications with bandwidth up to 10MHz. Offset voltage nulling terminals are also available.

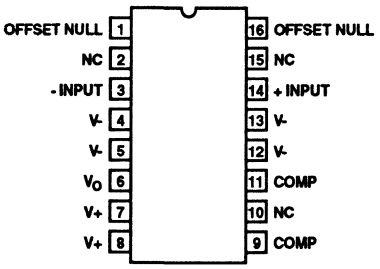
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3450E	-40°C to +85°C	16 Lead Plastic DIP

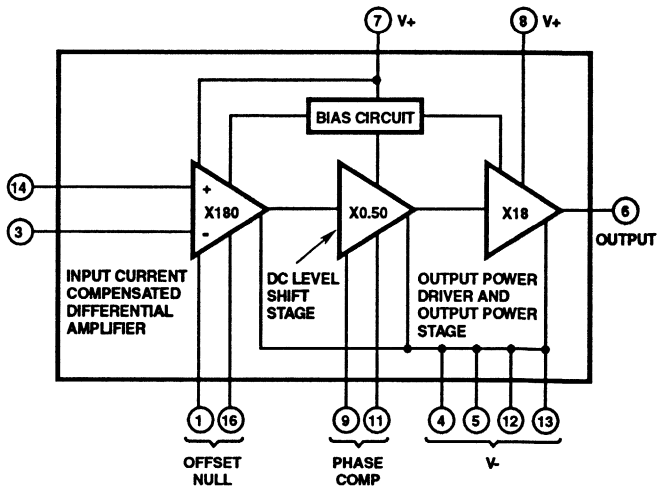
* Formerly Development Type No. TA11371A.

Pinout

CA3450
(PDIP)
TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1732.2**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 14.5V
Differential Input Voltage. 5V
Power Dissipation
  Up to +55°C 1.5W
  Above +55°C. . . . . Derate Linearly 16.6mW/°C
Output Current 100mA
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.). . . . . +300°C

Operating Conditions

Operating Temperature Range . . . . . -40°C to +85°C
Storage Temperature Range. . . . . -65°C to +150°C

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
Plastic DIP Package	60	12

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

At T_A = +25°C, C_C = 5pF, V+, V- = 6V (Note 1)

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
STATIC							
Input Offset Voltage	$\|V_{IO}\|$	T_A = +25°C		-	8	20	mV
		T_A = -40°C to +85°C		-	10	35	mV
Input Bias current	$\|I_{IB}\|$	T_A = +25°C		-	100	400	nA
Input Offset Current	$\|I_{IO}\|$	T_A = +25°C		-	50	200	nA
Open Loop DC Gain	A_{OL}	V_{OUT} = ±25V, R_L = 50Ω	-40°C to +85°C	55	-	-	dB
			+25°C	60	70	-	dB
Power Supply Rejection Ratio	PSRR	ΔV = ±1V		55	65	-	dB
Common Mode Rejection Ratio	CMRR	V_{ICR}± = ±3.5V		50	60	-	dB
Common Mode Input Range	V_{ICR}	T_A = -40°C to +85°C		±3.0	-	-	V
		T_A = +25°C		±3.5	±3.7	-	V
Supply Current	I+	T_A = -40°C to +85°C		-	-	50	mA
		T_A = +25°C		-	30	40	mA
DYNAMIC							
-3dB Bandwidth A_V = 1 (See Figure 8) C_C = 5pF		No Load		-	200	-	MHz
		R_L = 1MΩ||20pF		-	190	-	MHz
		R_L = 50Ω||20pF		-	185	-	MHz
Bandwidth (Unity Gain Crossing) A_V = Open Loop C_C = 0 (See Figure 7)		No Load		210	230	-	MHz
		R_L = 20pF||1MΩ		180	200	-	MHz
		R_L = 50Ω||20pF		180	220	-	MHz
Bandwidth (Unity Gain Crossing) A_V = 10, C_C = 0pF $R_{Feedback}$ = 450Ω $R_{Pin\ 3-G}$ = 50Ω (See Figure 8)		No Load		200	210	-	MHz
		50Ω		175	190	-	MHz
		1M||20pF		180	195	-	MHz
		50Ω||1M||20pF		170	188	-	MHz
Transient Response, Overshoot (See Figure 14)	OS	A_V = 1, C_C = 5pF	R_L = 50Ω||20pF	-	30	-	%
			No Load	-	20	-	%
		A_V ≥10, C_C = 0pF, R_L = 50Ω||20pF		-	10	-	%
Settling Time (See Figure 9)	t_S	2V Step, R_L = 50Ω||20pF	A_V = -1, C_C = 5pF, 0.1%, 10 Bits	-	35	-	ns
			A_V = 1, C_C = 5pF, 0.1%, 10 Bits	-	50	-	ns
			A_V = 10, C_C = 0pF, 0.1%, 10 Bits	-	35	-	ns
			A_V = 10, C_C = 0pF, 1.0%, 7 Bits	-	25	-	ns
Slew Rate (See Figures 8, 15)	SR	A_V = 1, C_C = 5pF	No Load	-	220	-	V/µs
			R_L = 50Ω||20pF	-	160	-	V/µs
		A_V ≥10, C_C = 0pF	No Load	370	440	-	V/µs
			R_L = 50Ω||20pF	300	330	-	V/µs

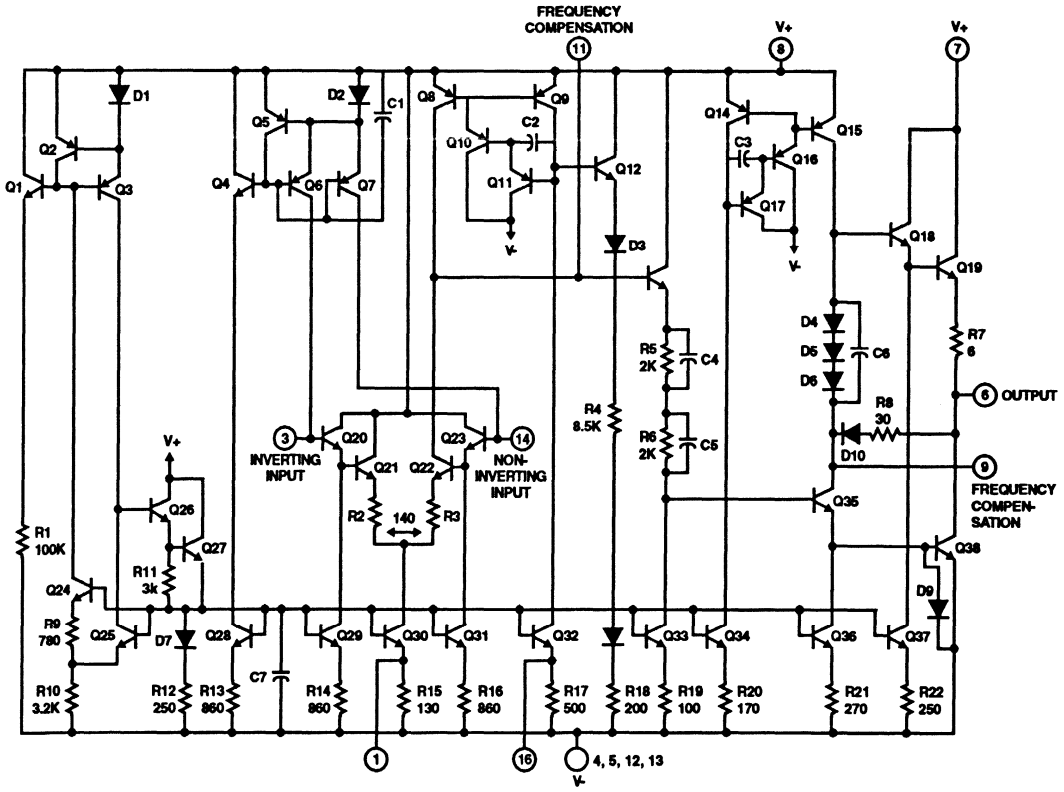
Electrical Specifications At T_A = +25°C, C_C = 5pF, V+, V- = 6V (Note 1) **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Power Bandwidth PBW = SR/π Vpp	PBW	A_V = 5 C_C = 5pF V_{OUT} = ±3.5V	No Load	-	10	-	MHz
			R_L = 50Ω||20pF	-	7.2	-	MHz
		A_V ≥10 C_C = 0pF V_{OUT} = ±2.0V	No Load	29	35	-	MHz
			R_L = 50Ω||20pF	24	26	-	MHz
Input Noise Voltage	e_n	f = 1kHz		-	12	-	nV/√Hz
Differential Gain	DG	See Figure 12		-	0.6	-	%
Differential Phase	DP	See Figure 12		-	0.3	-	Degrees
I_{OUT}		Into +4V or -4V		60	75	-	mA
Output Voltage Swing into 75Ω	VOM+			3.9	4.1	-	V
	VOM-			-3.9	-4.1	-	V
Input Capacitance	C_I	f = 1MHz		-	2.2	-	pF
Input Resistance	R_I			-	1	-	MΩ
Output Resistance	R_{OUT}	See Figure 5, A_V = 1, 30MHz		-	4	-	Ω

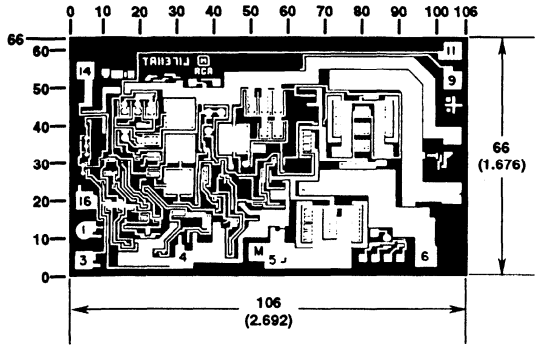
NOTE:

1. All tests are performed with ±6V at the supply terminals.

Schematic Diagram



Metallization Mask Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3mils to +6mils applicable to the nominal dimensions shown.

Typical Performance Curves

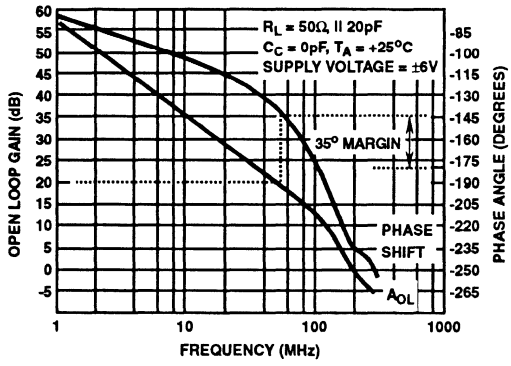


FIGURE 1. BODE PLOT FOR THE CA3450

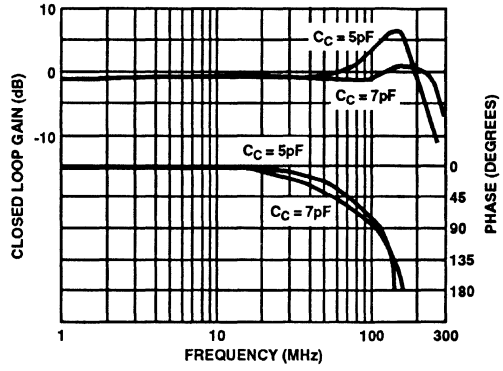


FIGURE 2. CLOSED LOOP GAIN AND PHASE vs FREQUENCY (A_V = 1)

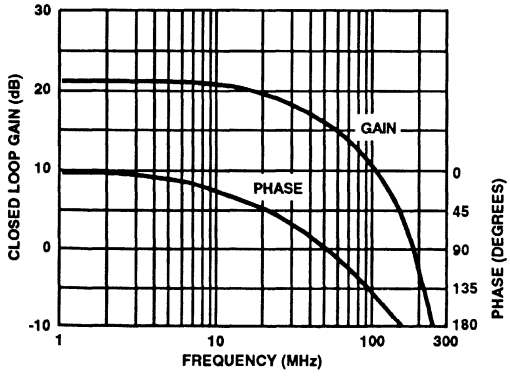


FIGURE 3. CLOSED LOOP GAIN AND PHASE vs FREQUENCY (A_V = 10)

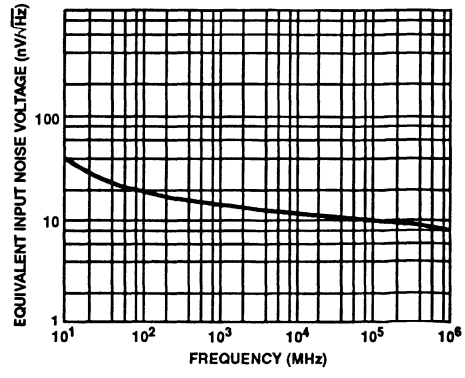


FIGURE 4. EQUIVALENT INPUT NOISE vs FREQUENCY

Typical Performance Curves (Continued)

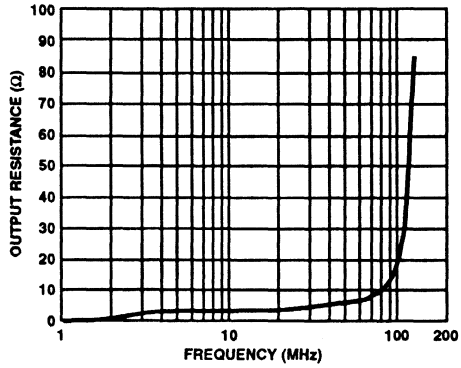


FIGURE 5. OUTPUT RESISTANCE vs FREQUENCY

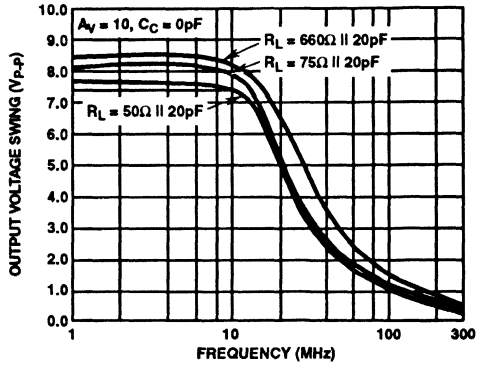
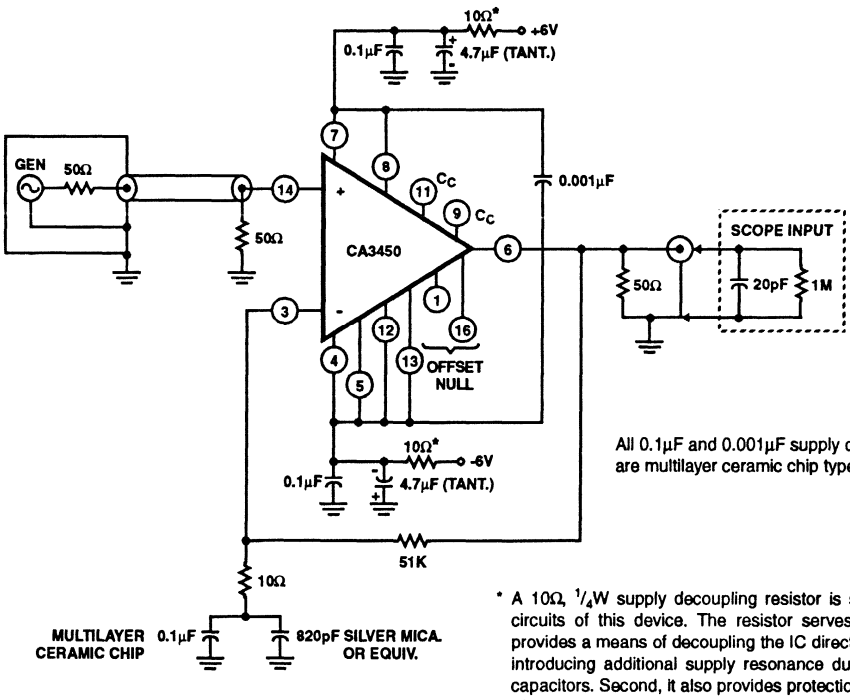


FIGURE 6. OUTPUT VOLTAGE vs FREQUENCY



All 0.1μF and 0.001μF supply decoupling capacitors are multilayer ceramic chip types.

* A 10Ω, 1/4W supply decoupling resistor is shown in all application circuits of this device. The resistor serves two purposes. First it provides a means of decoupling the IC directly at its terminal without introducing additional supply resonance due to parallel connected capacitors. Second, it also provides protection for the device in event of a sustained short circuit applied directly to the output terminals.

FIGURE 7. OPEN LOOP GAIN vs FREQUENCY TEST CIRCUIT

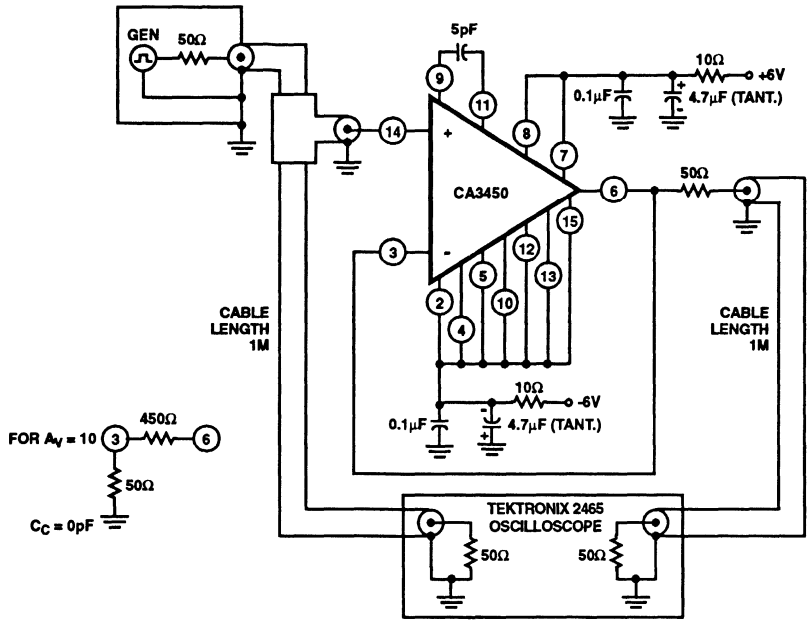


FIGURE 8. UNITY GAIN AND X10 NON-INVERTING AMPLIFIER/AND SLEW RATE TEST CIRCUIT

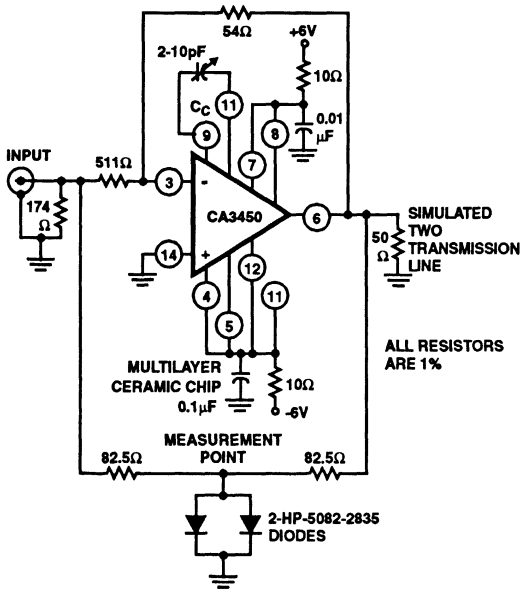


FIGURE 9. CIRCUIT USED TO MEASURE SETTLING TIME

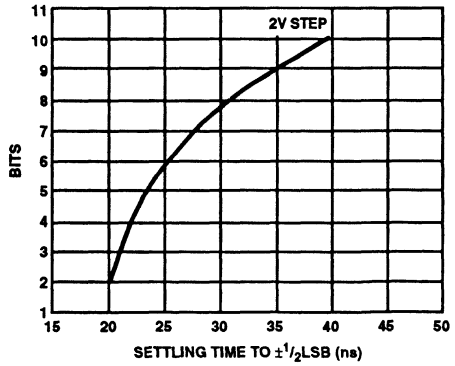


FIGURE 10. ACCURACY IN BITS AS A FUNCTION OF SETTLING TIME

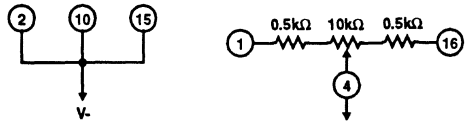


FIGURE 11. NULLING CIRCUIT FOR THE CA3450

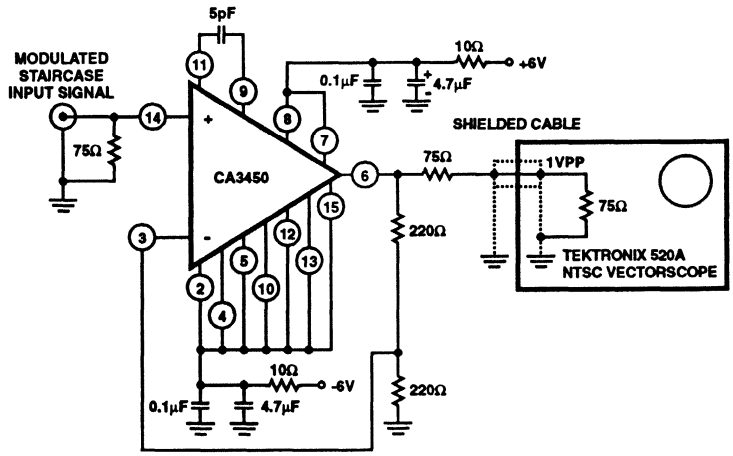


FIGURE 12. CONFIGURATION USED TO MEASURE DIFFERENTIAL GAIN AND PHASE

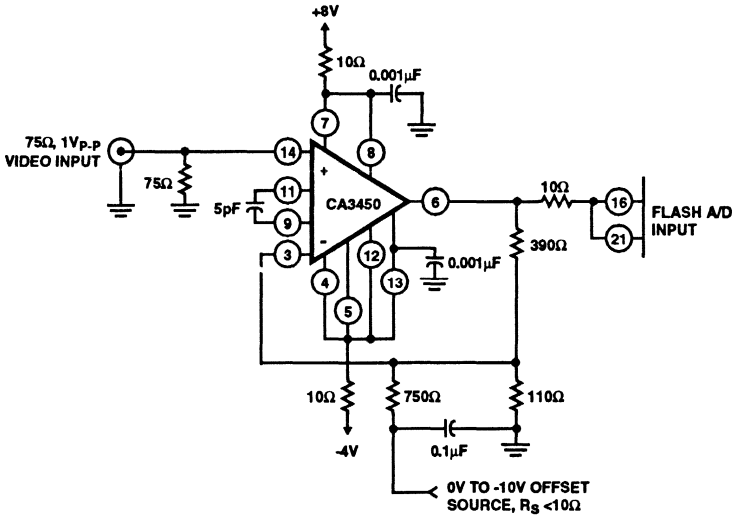


FIGURE 13. TYPICAL HIGH BANDWIDTH X5 AMPLIFIER FOR DRIVING THE CA3318 FLASH A/D

Transient Response Waveforms

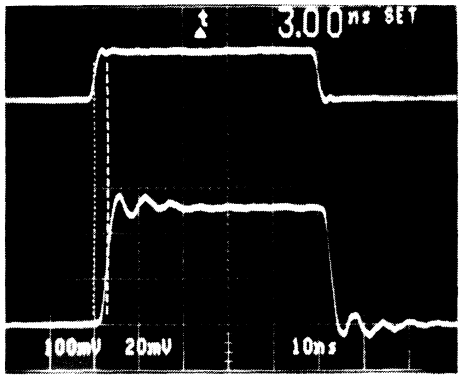


FIGURE 14. TRANSIENT RESPONSE WAVEFORM

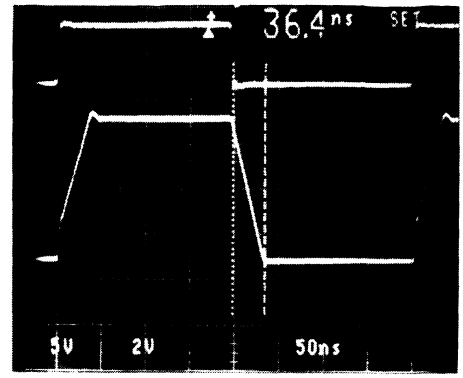


FIGURE 15. SLEW RATE WAVEFORM

HARRIS SEMICONDUCTOR

CA5130

BiMOS Microprocessor Operational Amplifier with MOSFET Input/CMOS Output

March 1993

Features

- MOSFET Input Stage
  - Very High Z_I ..... 1.5TΩ (1.5 x 10^{12}Ω)Typ.
  - Very Low I_I .....5pA Typ. at 15V Operation
    2pA Typ. at 5V Operation
- Ideal for Single Supply Applications
- Common Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can Be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails
- CA5130A, CA5130 Have Full Military Temperature Range Guaranteed Specifications for V+ = 5V
- CA5130A, CA5130 Are Guaranteed to Operate Down to V+ = 4.5V for A_{OL}
- CA5130A, CA5130 Are Guaranteed to Operate at ±7.5V CA3130A, CA3130 Specifications

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- High Input Impedance Comparators (Ideal Interface with Digital CMOS)
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to Zero Volts)
- Peak Detectors
- Single Supply Full Wave Precision Rectifiers
- Photo Diode Sensor Amplifiers
- 5V Logic Systems
- Microprocessor Interface

Description

CA5130A and CA5130 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. They are designed and guaranteed to operate in microprocessors or logic systems that use +5V supplies.

Gate protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute in single supply applications.

A complementary symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10mV of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA5130 Series circuits operate at supply voltages ranging from 4V to 16V, or ±2V to ±8V when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset null capability. Terminal provisions are also made to permit strobing of the output stage.

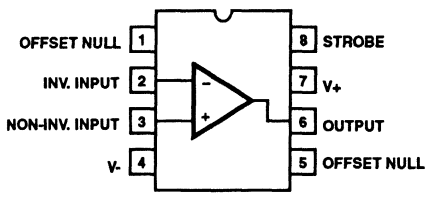
The CA5130A, CA5130 have guaranteed specifications for 5V operation over the full military temperature range of -55°C to +125°C.

Ordering Information

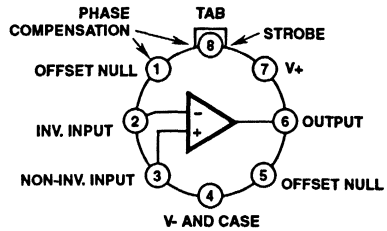
PART #	TEMP. RANGE	PACKAGE
CA5130AE	-55°C to +125°C	8 Lead Plastic DIP
CA5130AM	-55°C to +125°C	8 Lead SOIC
CA5130AT	-55°C to +125°C	8 Pin Can
CA5130E	-55°C to +125°C	8 Lead Plastic DIP
CA5130M	-55°C to +125°C	8 Lead SOIC
CA5130T	-55°C to +125°C	8 Pin Can

Pinouts

CA5130 (PDIP, SOIC)
TOP VIEW



CA5130 (TO-5 CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1923.2**

Absolute Maximum Ratings

DC Supply Voltage (Between V^+ And V^- Terminals) 16V
Differential Input Voltage 8V
DC Input Voltage ..... (V^+ +8 V) to (V^- -0.5V)
Input Terminal Current 1mA
Output Short-Circuit Duration* ..... Indefinite
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range (All Types) ..... -55°C to +125°C
Storage Temperature Range (All Types) ..... -65°C to +150°C

* Short circuit may be applied to ground or to either supply.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, V+ = 5V, V- = 0V (Unless Otherwise Specified)

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA5130A			CA5130			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_O = 2.5V	-	1.5	4	-	2	10	mV
Input Offset Current	I_{IO}	V_O = 2.5V	-	0.1	5	-	0.1	10	pA
Input Current	I_I	V_O = 2.5V	-	2	10	-	2	15	pA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0V to 1V	75	87	-	70	85	-	dB
		V_{CM} = 0V to 2.5V	60	69	-	60	69	-	dB
Input Common Mode Voltage Range	V_{ICR+}		2.5	2.8	-	2.5	2.8	-	V
	V_{ICR-}		-	-0.5	0	-	-0.5	0	V
Power Supply Rejection Ratio	PSRR	Δ+ = 1V; Δ- = 1V	60	75	-	55	73	-	dB
Large Signal Voltage Gain (Note 1)	A_{OL}	V_O = 0.1V to 4.1V, R_L = ∞	100	105	-	95	105	-	dB
		V_O = 0.1V to 3.6V, R_L = 10kΩ	90	97	-	85	95	-	dB
Source Current	I_{SOURCE}	V_O = 0V	1.0	3.1	4.0	1.0	2.6	4.0	mA
Sink Current	I_{SINK}	V_O = 5V	1.0	1.4	4.0	1.0	1.7	4.0	mA
Output Voltage	V_{OUT}								
V_{OM+}		R_L = ∞	4.99	5	-	4.99	5	-	V
V_{OM-}			-	0	0.01	-	0	0.01	V
V_{OM+}		R_L = 10kΩ	4.4	4.7	-	4.4	4.7	-	V
V_{OM-}			-	0	0.01	-	0	0.01	V
V_{OM+}		R_L = 2kΩ	2.5	3.5	-	2.5	3.5	-	V
V_{OM-}			-	0	0.01	-	0	0.01	V
Supply Current	I_{SUPPLY}	V_O = 0V	-	50	100	-	50	100	μA
		V_O = 2.5V	-	260	400	-	260	400	μA

NOTE:

1. For V+ = 4.5V and V- = Gnd; V_{OUT} = 0.5V to 3.2V at R_L = 10kΩ.

Specifications CA5130, CA5130A

Electrical Specifications T_A = -55°C to +125°C, V+ = 5V, V- = 0V (Unless Otherwise Specified)

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA5130A			CA5130			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_O = 2.5V	-	2	10	-	3	15	mV
Input Offset Current	I_{IO}	V_O = 2.5V	-	0.1	5	-	0.1	10	pA
Input Current	I_I	V_O = 2.5V	-	2	10	-	2	15	pA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0V to 1V	60	80	-	60	80	-	dB
		V_{CM} = 0V to 2.5V	55	80	-	50	80	-	dB
Input Common Mode Voltage Range	V_{ICR+}		2.5	2.8	-	2.5	2.8	-	V
	V_{ICR-}		-	-0.5	0	-	-0.5	0	V
Power Supply Rejection Ratio	PSRR	Δ+ = 1V; Δ- = 1V	45	70	-	40	66	-	dB
Large Signal Voltage Gain (Note 1)	A_{OL}	V_O = 0.1V to 4.1V R_L = ∞	94	98	-	90	98	-	dB
		V_O = 0.1V to 3.6V R_L = 10kΩ	80	88	-	75	85	-	dB
Source Current	I_{SOURCE}	V_O = 0V	0.6	2.2	5.0	0.6	-	5.0	mA
Sink Current	I_{SINK}	V_O = 5V	0.6	1.15	5.0	0.6	-	5.0	mA
Output Voltage	V_{OUT}								
V_{OM}+		R_L = ∞	4.99	5	-	4.99	5	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V
V_{OM}+		R_L = 10kΩ	4.0	4.6	-	4.0	4.6	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V
V_{OM}+		R_L = 2kΩ	2.0	3.0	-	2.0	3.0	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V
Supply Current	I_{SUPPLY}	V_O = 0V	-	80	220	-	80	220	μA
		V_O = 2.5V	-	300	500	-	300	500	μA

NOTE:

1. For V+ = 4.5V and V- = Gnd; V_{OUT} = 0.5V to 3.2V at R_L = 10kΩ

Electrical Specifications T_A = +25°C, V+ = 15V, V- = 0V (Unless Otherwise Specified)

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA5130A			CA5130			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V± = ±7.5V	-	2	5	-	8	15	mV
Input Offset Current	I_{IO}	V± = ±7.5V	-	0.5	20	-	0.5	30	pA
Input Current	I_I	V± = ±7.5V	-	5	30	-	5	50	pA
Common Mode Rejection Ratio	CMRR		80	90	-	70	90	-	dB
Input Common Mode Voltage Range	V_{ICR}		10	-0.5 to 12	0	10	-0.5 to 12	0	V
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V\pm$ V± = ±7.5V	-	32	150	-	32	320	μV/V

Electrical Specifications T_A = +25°C, V+ = 15V, V- = 0V (Unless Otherwise Specified) **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA5130A			CA5130			
			MIN	TYP	MAX	MIN	TYP	MAX	
Large Signal Voltage Gain	A_{OL}	V_O = 10V_{P-P}, R_L = 2kΩ	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Maximum Output Current									
Source	I_{OM}+	V_O = 0V	12	22	45	12	22	45	mA
Sink	I_{OM}-	V_O = 15V	12	20	45	12	20	45	mA
Supply Current	I_{SUPPLY}	V_O = 7.5V, R_L = ∞	-	10	15	-	10	15	mA
		V_O = 0V, R_L = ∞	-	2	3	-	2	3	mA
Maximum Output Voltage	V_{OUT}								
V_{OM}+		R_L = ∞	14.99	15	-	14.99	15	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V
V_{OM}+		R_L = 2kΩ	12	13.3	-	12	13.3	-	V
V_{OM}-			-	0.002	0.01	-	0.002	0.01	V
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	10	-	-	10	-	µV/°C

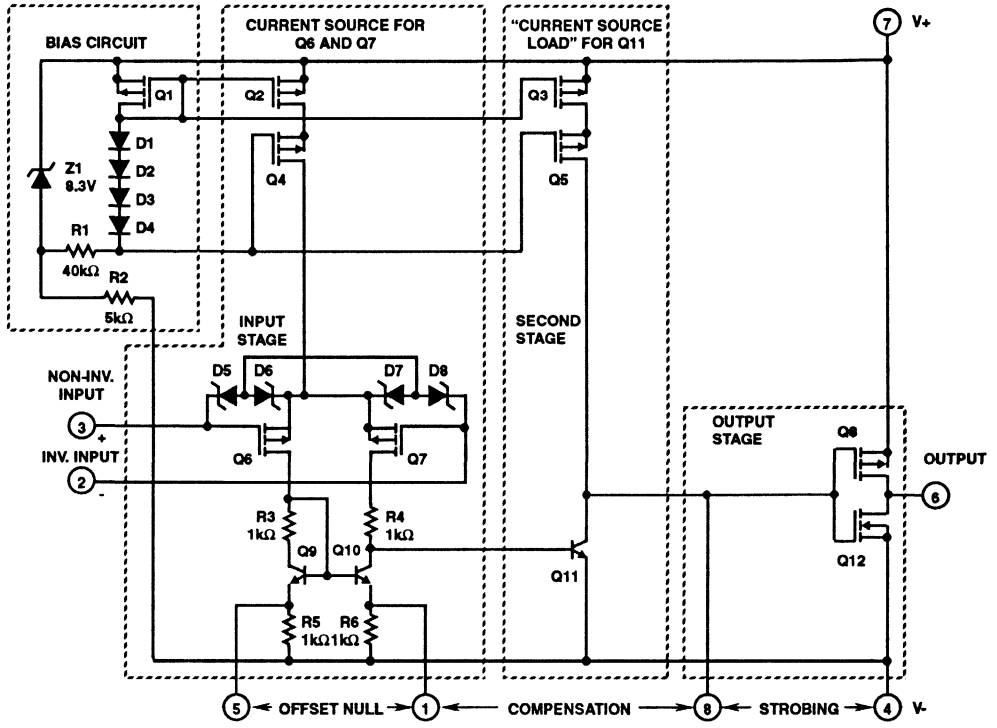
Electrical Specifications Typical Values Intended Only for Design Guidance. T_A = +25°C, V+ = +7.5V, V- = -7.5V (Unless Otherwise Specified)

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			CA5130A	CA5130	
			TYP	TYP	
Input Offset Voltage Adjustment Range		10kΩ Across Terminals 4 and 5 or 4 and 1	±22	±22	mV
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I	f = 1MHz	4.3	4.3	pF
Equivalent Input Noise Voltage	e_N	BW = 0.2MHz, R_S = 1MΩ (Note 1)	23	23	µV
Unity Gain Crossover Frequency	f_T	C_C = 0	15	15	MHz
		C_C = 47pF	4	4	MHz
Slew Rate	SR				
Open Loop		C_C = 0	30	30	V/µs
Closed Loop		C_C = 56pF	10	10	V/µs
Transient Response		C_C = 56pF, C_L = 25pF, R_L = 2kΩ (Voltage Follower)			
Rise Time	t_R		0.09	0.09	µs
Overshoot	OS		10	10	%
Settling Time (To <0.1%, V_{IN} = 4V_{P-P})	t_S	C_C = 56pF, C_L = 25pF, R_L = 2kΩ (Voltage Follower)	1.2	1.2	µs

NOTE:

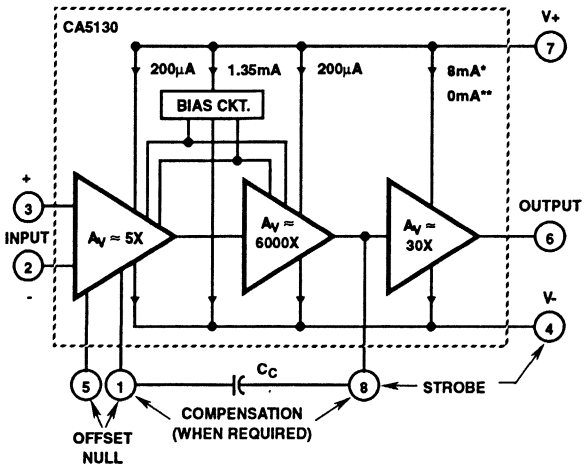
1. Although a 1MΩ source is used for this test, the equivalent input noise remains constant for values of R_S up to 10MΩ.

Schematic Diagram



NOTE: DIODES D5 THROUGH D8 PROVIDE GATE OXIDE PROTECTION FOR MOSFET INPUT STAGE

Block Diagram



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15V

*WITH INPUT TERMINALS BIASED SO THAT TERM. 6 POTENTIAL IS +7.5V ABOVE TERM. 4.

**WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.

Circuit Description

The input terminals shown in the block diagram of the CA5130 Series CMOS Operational Amplifiers may be operated down to 0.5V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA5130 Series circuits are ideal for single supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in the Block Diagram, provide the total gain of the CA5130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).

Input Stages

The circuit of the CA5130 is shown in the Schematic Diagram. It consists of a differential input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror pair transistors also function as a differential-to-single-ended converter to provide base drive to the second stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000Ω potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode connected PMOS transistors Q2, Q4 are the constant current source for the input stage. The biasing circuit for the constant current source is subsequently described. The small diodes D5 through D8 provide gate oxide protection against high voltage transients, e.g., including static electricity during handling for Q6 and Q7.

Second Stage

Most of the voltage gain in the CA5130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47pF capacitor provides sufficient compensation for stable unity gain operation in most applications.

Bias Source Circuit

At total supply voltages, somewhat above 8.3V, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3V across the series connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate bias potential of about 4.5V for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2V is developed across diode connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror connected" to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200μA current in Q1 establishes a similar current in Q2 and Q3 as constant current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3V, zener diode Z1 becomes nonconductive and the potential, developed across series connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply voltage variations. This variation results in deterioration of the power supply rejection ratio (PSRR) at total supply voltages below 8.3V. Operation at total supply voltages below about 4.5V results in seriously degraded performance.

Output Stage

The output stage consists of a drain loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance load, the output can be swung within mV of either supply rail. Because the output stage is a drain loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Figure 3. Typical op amp loads are readily driven by the output stage. Because large signal excursions are nonlinear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 percent accuracy levels, including the negative supply rail.

Typical Performance Curves

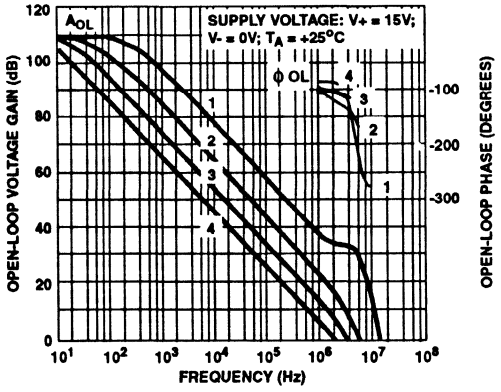


FIGURE 1. OPEN LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY

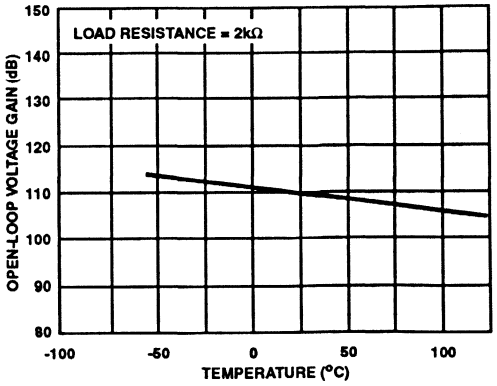


FIGURE 2. OPEN LOOP GAIN vs TEMPERATURE

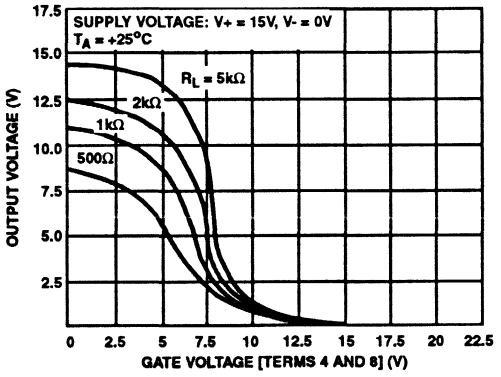


FIGURE 3. VOLTAGE TRANSFER CHARACTERISTICS OF CMOS OUTPUT STAGE

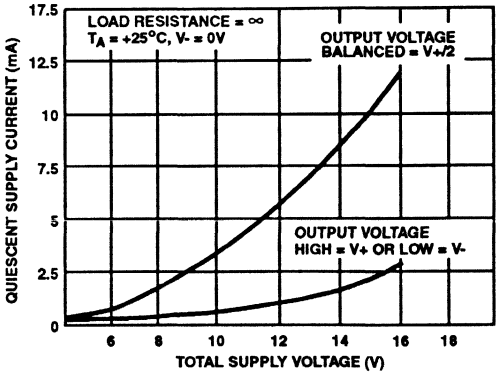


FIGURE 4. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

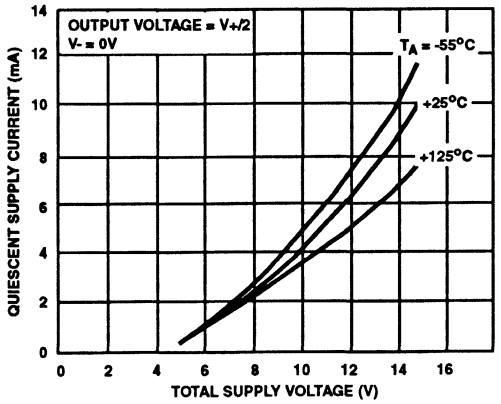


FIGURE 5. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

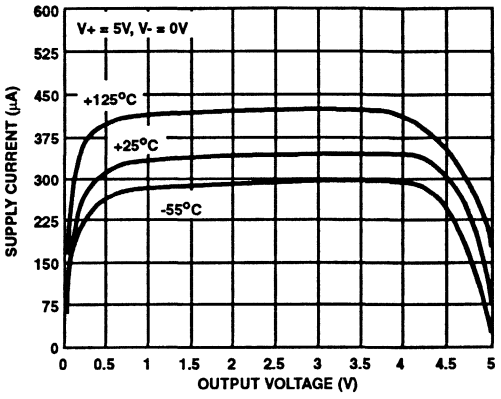


FIGURE 6. SUPPLY CURRENT vs OUTPUT VOLTAGE

Typical Performance Curves (Continued)

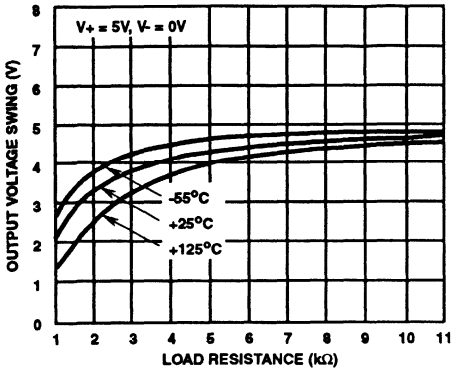


FIGURE 7. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

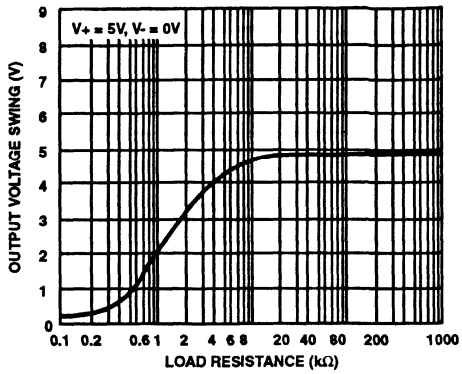


FIGURE 8. OUTPUT SWING vs LOAD RESISTANCE

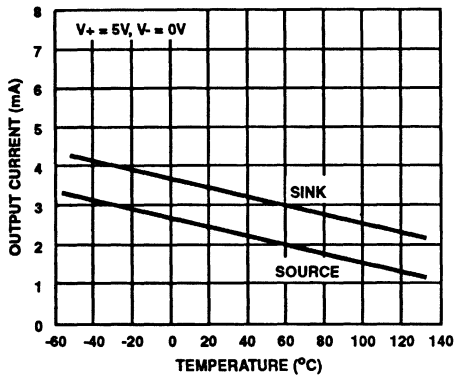


FIGURE 9. OUTPUT CURRENT vs TEMPERATURE

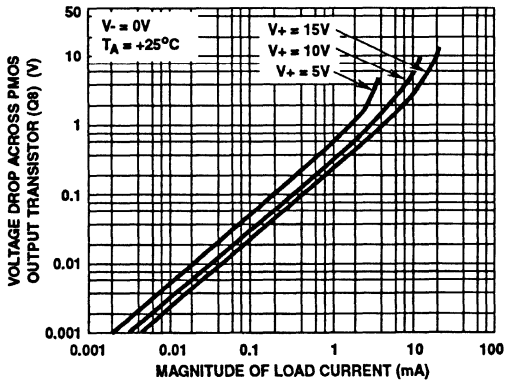


FIGURE 10. VOLTAGE ACROSS PMOS OUTPUT TRANSISTOR (Q8) vs LOAD CURRENT

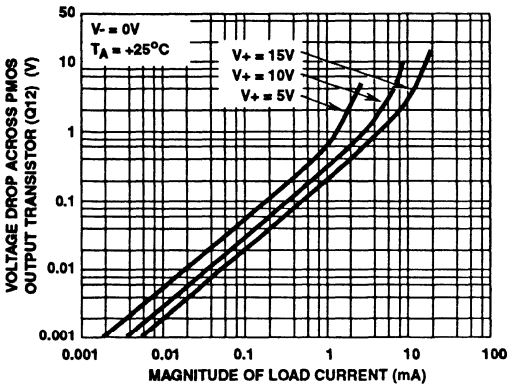


FIGURE 11. VOLTAGE ACROSS NMOS OUTPUT TRANSISTOR (Q12) vs LOAD CURRENT

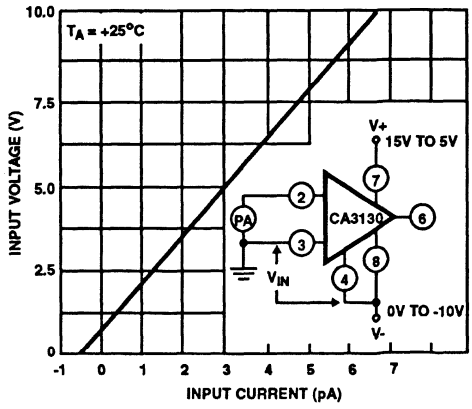


FIGURE 12. INPUT CURRENT vs COMMON MODE VOLTAGE

Typical Performance Curves (Continued)

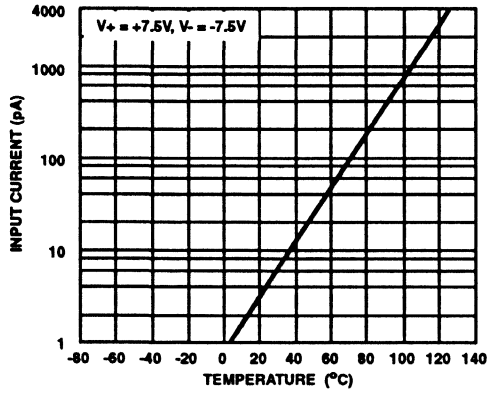


FIGURE 13. INPUT CURRENT vs TEMPERATURE

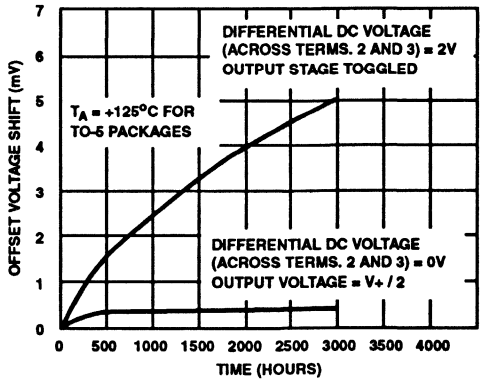


FIGURE 14. TYPICAL INCREMENTAL OFFSET VOLTAGE SHIFT vs OPERATING LIFE

Input Current Variation with Common Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA5130 Series Op Amps is typically 5pA at T_A = +25°C when terminals 2 and 3 are at a common mode potential of +7.5V with respect to negative supply Terminal 4. Figure 12 contains data showing the variation of input current as a function of common mode input voltage at T_A = +25°C. This data shows that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1pA, provided the common mode input voltage does not exceed 2V. As previously noted, the input current is essentially the result of the leakage current through the gate protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA5130 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Offset Nulling

Offset voltage nulling is usually accomplished with a 100,000Ω potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset null adjustment usually can be effected with the slider arm positioned in the midpoint of the potentiometer's total range.

Input Current Variation with Temperature

The input current of the CA5130 Series circuits is typically 5pA at +25°C. The major portion of this input current is due to leakage current through the gate protective diodes in the input circuit. As with any semiconductor junction device, including op amps with a junction FET input stage, the leakage current approximately doubles for every +10°C increase in temperature. Figure 13 provides data on the typical variation of input bias current as a function of temperature in the CA5130.

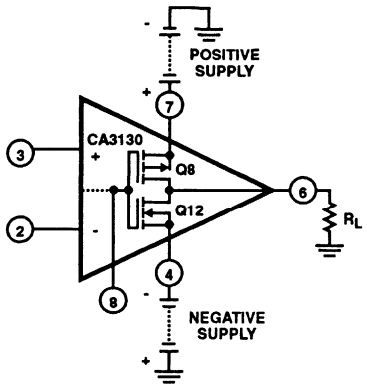
In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA5130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input Offset Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

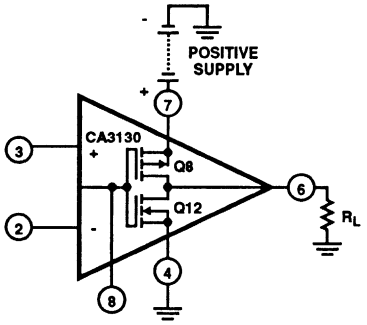
It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA5130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terms. 2 and 3. Figure 14 shows typical data pertinent to shifts in offset voltage encountered with CA5130 devices (TO-5 package) during life testing. At lower temperatures (TO-5 and plastic), for example at +85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The 2V dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

Power-Supply Considerations

Because the CA5130 is very useful in single supply applications, it is pertinent to review some considerations relating to power supply current consumption under both single and dual supply service. Figures 15A and 15B show the CA5130 connected for both dual and single supply operation.



A. DUAL POWER SUPPLY OPERATION



B. SINGLE POWER SUPPLY OPERATION

FIGURE 15. CA5130 OUTPUT STAGE IN DUAL AND SINGLE POWER SUPPLY OPERATION

Dual supply operation: When the output voltage at Term. 6 is 0V, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2, i.e., the voltage drops across Q8 and Q12 are of equal magnitude. Figure 4 shows typical quiescent supply current vs. supply voltage for the CA5130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage transfer characteristics (see Figure 3). If either Q8 or Q12 are swung out of their linear regions toward cutoff (a nonlinear region), there will be a corresponding reduction in supply current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply current to series connected transistors Q8, Q12 goes essentially to zero. The two preceeding stages in the CA5130, however, continue to draw modest supply current (see the lower curve in Figure 4) even though the output stage is strobed off. Figure 15A shows a dual supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load resistance of nominal value (e.g., 2kΩ) is connected between Term. 6 and ground in the circuit of Figure 15B. Let it further be assumed again that the input terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply current must increase as an inverse function of the R_L magnitude. Figure 10 shows the voltage drop across PMOS transistor Q8 as a function of load current at several supply voltages. Figure 3 shows the voltage transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low noise performance considerations, the use of the CA5130 is most advantageous in applications where the source resistance of the input signal is on the order of 1MΩ or more. In this case, the total input referred noise voltage is typically only 23μV when the test circuit amplifier of Figure 16 is operated at a total supply voltage of 15V. This value of total input referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1MΩ, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

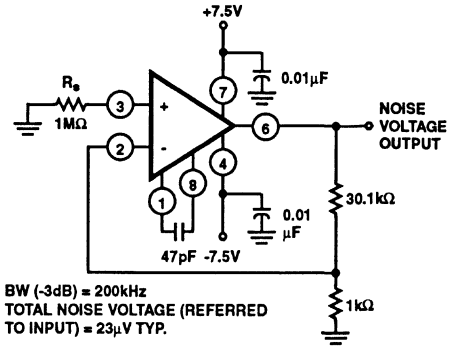


FIGURE 16. TEST-CIRCUIT AMPLIFIER (30dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENTS

Typical Applications

Voltage Followers

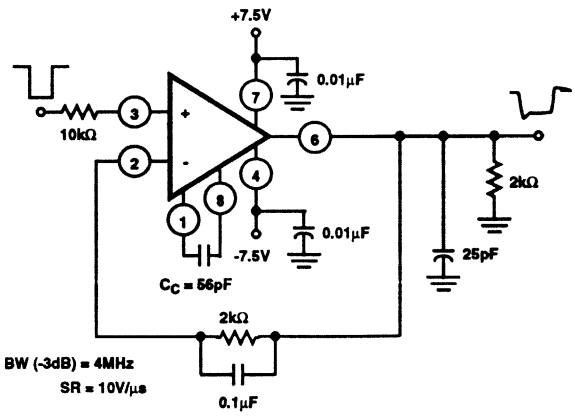
Operational amplifiers with very high input resistances, like the CA5130, are particularly suited to service as voltage followers. Figure 17 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA5130 in a split supply configuration.

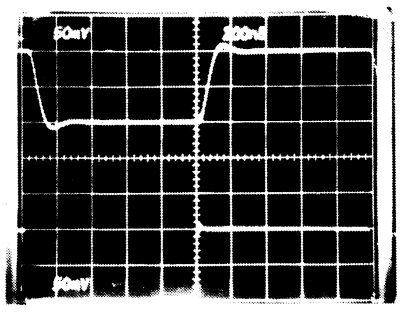
A voltage follower, operated from a single supply, is shown in Figure 18, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Figure 18A with input signal ramping. The waveforms in Figure 18B show that the follower does not lose its input-to-output phase sense, even though the input is being swung 7.5V below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Figure 18B also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA5130 in a single supply voltage follower application.

9 Bit CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Figure 19. This system combines the concepts of multiple switch CMOS IC's a low cost ladder network of discrete metal-oxide film resistors, a CA5130 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10V logic levels are used in the circuit of Figure 19.

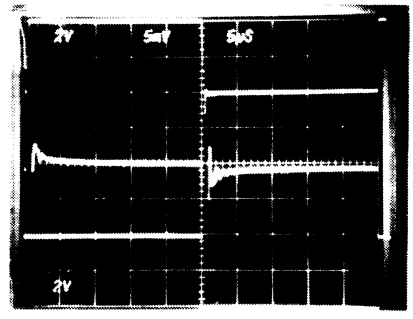
* "Digital-to-Analog Conversion Using the Harris CD4007A CMOS IC", Application Note ICAN-6080.





A. SMALL SIGNAL RESPONSE (50mV/DIV and 200ns/DIV)

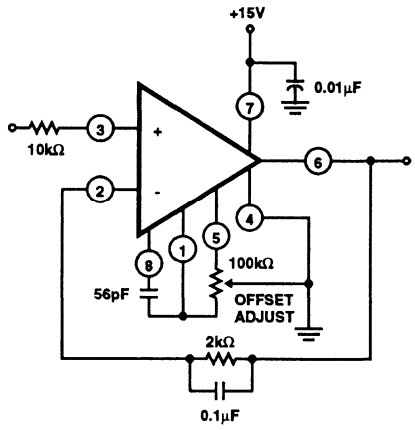
Top Trace: Output
Bottom Trace: Input

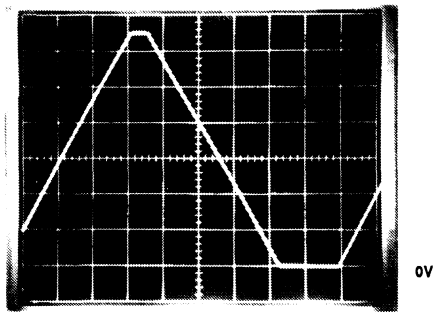


B. INPUT OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME (MEASUREMENT MADE WITH TEKTRONIX 7A13 DIFFERENTIAL AMPLIFIER)

Top Trace: Output Signal (2V/Div and 5μs/Div)
Center Trace: Difference Signal (5mV/Div and 5μs/Div)
Bottom Trace: Input Signal (2V/Div and 5μs/Div)

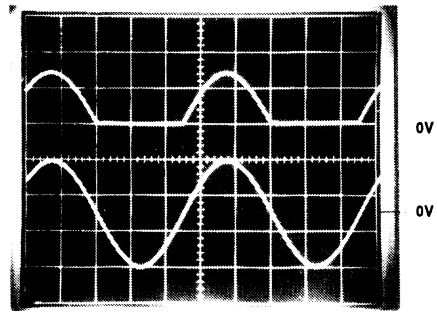
FIGURE 17. CA5130 SPLIT SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS





A. OUTPUT WAVEFORM WITH INPUT SIGNAL RAMPING

(2V/Div and 500ms/Div)



B. OUTPUT WAVEFORM WITH GROUND REFERENCE SINE WAVE INPUT

Top Trace: Output (5V/Div and 200μs/Div)
Bottom Trace: Input (5V/Div and 200μs/Div)

FIGURE 18. SINGLE SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS. (e.g., FOR USE IN SINGLE SUPPLY D/A CONVERTER; SEE FIGURE 9 IN ICAN-6080)

The circuit uses an R/2R voltage ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single pole double throw switch to terminate an arm of the R/2R network at either the positive or negative power supply terminal. The resistor ladder is an assembly of one percent tolerance metal oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000Ω resistors from the same manufacturing lot.

A single 15V supply provides a positive bus for the CA5130 follower amplifier and feeds the CA3085 voltage regulator. A "scale adjust" function is provided by the regulator output control, set to a nominal 10V level in this system. The line voltage regulation (approximately 0.2%) permits a 9 bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the CMOS building blocks simplifies the design of DAC systems tailored to particular needs.

Single Supply, Absolute Value, Ideal Full Wave Rectifier

The absolute value circuit using the CA5130 is shown in Figure 20. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative going excursion of the input signal, the CA5130 functions as a normal inverting amplifier with a gain equal to -R2/R1. When the equality of the two equations shown in Figure 20 is satisfied, the full wave output is symmetrical.

Peak Detectors

Peak detector circuits are easily implemented with the CA5130, as illustrated in Figure 21 for both the peak positive and the peak negative circuit. It should be noted that with large signal inputs, the bandwidth of the peak negative circuit is much less than that of the peak positive circuit. The second stage of the CA5130 limits the bandwidth in this case. Negative going output signal excursion requires a positive going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative going signal excursion at the collector of Q11, the transistor functions in active "pull down" mode so that the intrinsic capacitance can be discharged more expeditiously.

Error Amplifier In Regulated Power Supplies

The CA5130 is an ideal choice for error amplifier service in regulated power supplies since it can function as an error amplifier when the regulated output voltage is required to approach Zero. Figure 22 shows the schematic diagram of a 40mA power supply capable of providing regulated output voltage by continuous adjustment over the range from 0V to 13V. Q3 and Q4 in IC2 (a CA3066 transistor array IC) function as zeners to provide supply voltage for the CA5130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature compensated source of adjustable reference voltage for the error amplifier.

Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor array IC) are connected in parallel as the series pass element. Transistor Q5 in IC3 functions as a current limiting device by diverting base drive from the series pass transistors, in accordance with the adjustment of resistor R2.

Figure 23 contains the schematic diagram of a regulated power supply capable of providing regulated output voltage by continuous adjustment over the range from 0.1V to 50V and currents up to 1A. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington connected series pass transistors Q1, Q2. Transistor Q3 functions in the previously described current limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA5130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Figure 24. Resistors R1 and R2 are used to bias the CA5130 to the midpoint of the supply voltage and R3 is the feedback resistor. The pulse repetition rate is selected by positioning S1 to the desired position and the rate remains essentially constant when the resistors which determine "on period" and "off period" are adjusted.

Function Generator

Figure 25 contains a schematic diagram of a function generator using the CA5130 in the integrator and threshold detector functions. This circuit generates a triangular or square wave output that can be swept over a 1,000,000:1 range (0.1Hz to 100kHz) by means of a single control, R1. A voltage control input is also available for remote sweep control.

The heart of the frequency determining system is an operational transconductance amplifier (OTA)*, IC1, operated as a voltage controlled current source. The output, I_O, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA5130, to provide the triangular wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive going and negative going signal excursions.

Another CA5130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high frequency square wave performance of the circuit.

Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

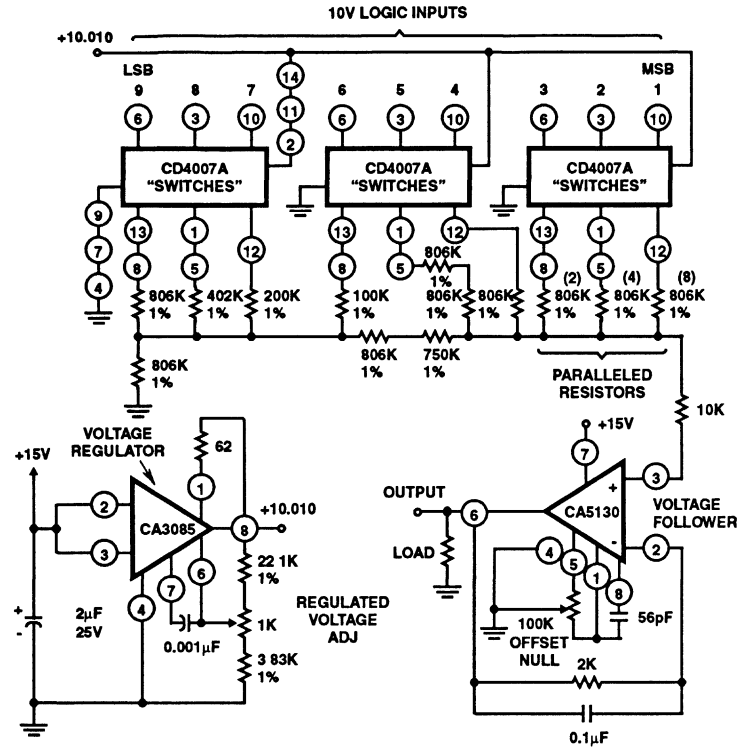
* See File No. 475 and ICAN-6668.

Operation with Output Stage Power-Booster

The current sourcing and sinking capability of the CA5130 output stage is easily supplemented to provide power boost capability. In the circuit of Figure 26, three CMOS transistor pairs in a single CA3600E* IC array are shown parallel connected with the output stage in the CA5130. In the Class A mode of CA3600E shown, a typical device consumes 20mA of supply current at 15V operation. This arrangement boosts the current handling capability of the CA5130 output stage by about 2.5X.

The amplifier circuit in Figure 26 employs feedback to establish a closed-loop gain of 48dB. The typical large signal bandwidth (-3dB) is 50kHz.

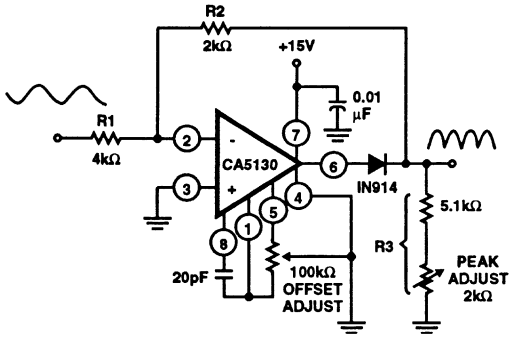
* See File No. 619 for technical information.

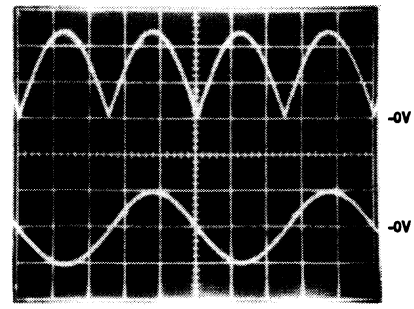


BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6 - 9	±1% ABS

All Resistances In Ohms

FIGURE 19. 9 BIT DAC USING CMOS DIGITAL SWITCHES AND CA5130





$$\text{Gain} = \frac{R_2}{R_1} = X = \frac{R_3}{R_1 + R_2 + R_3}$$

$$R_3 = R_1\left(\frac{X + X^2}{1 - X}\right)$$

$$\text{For } X = 0.5: \frac{2k\Omega}{4k\Omega} = \frac{R_2}{R_1}$$

$$R_3 = 4k\Omega\left(\frac{0.75}{0.5}\right) = 6k\Omega$$

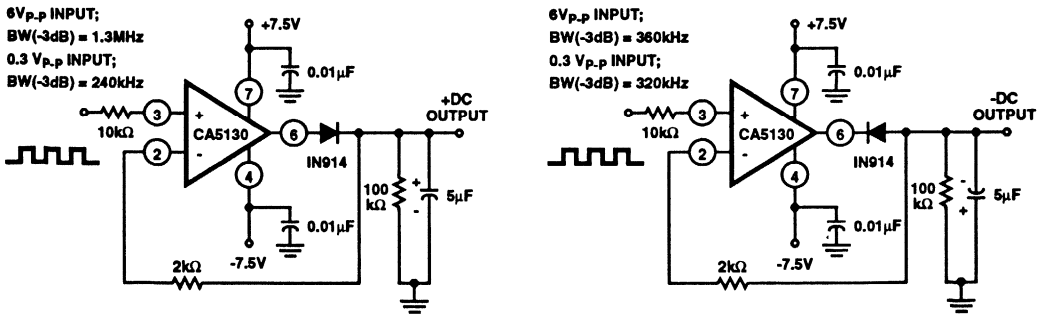
Top Trace: Output Signal (2V/Div)

Bottom Trace: Input Signal (10V/Div)

Time base on both traces: 0.2ms/Div

20Vp-p Input: BW(-3dB) = 230kHz, DC Output (Avg.) = 3.2V
1Vp-p Input: BW(-3dB) = 130kHz, DC Output (Avg.) = 160mV

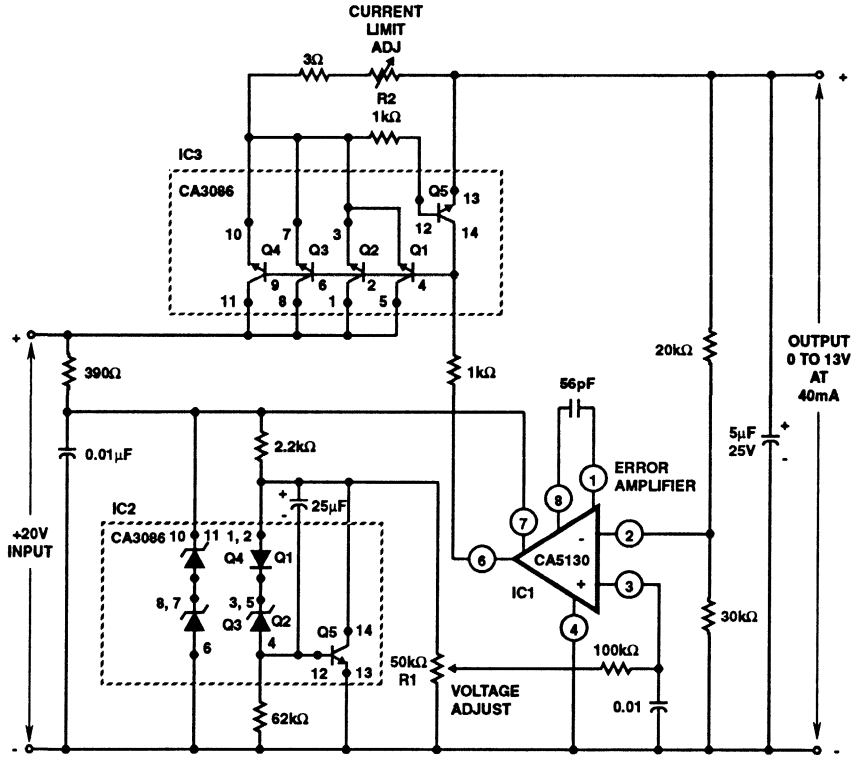
FIGURE 20. SINGLE SUPPLY, ABSOLUTE VALUE, IDEAL FULL WAVE RECTIFIER WITH ASSOCIATED WAVEFORMS



A. PEAK POSITIVE DETECTOR CIRCUIT

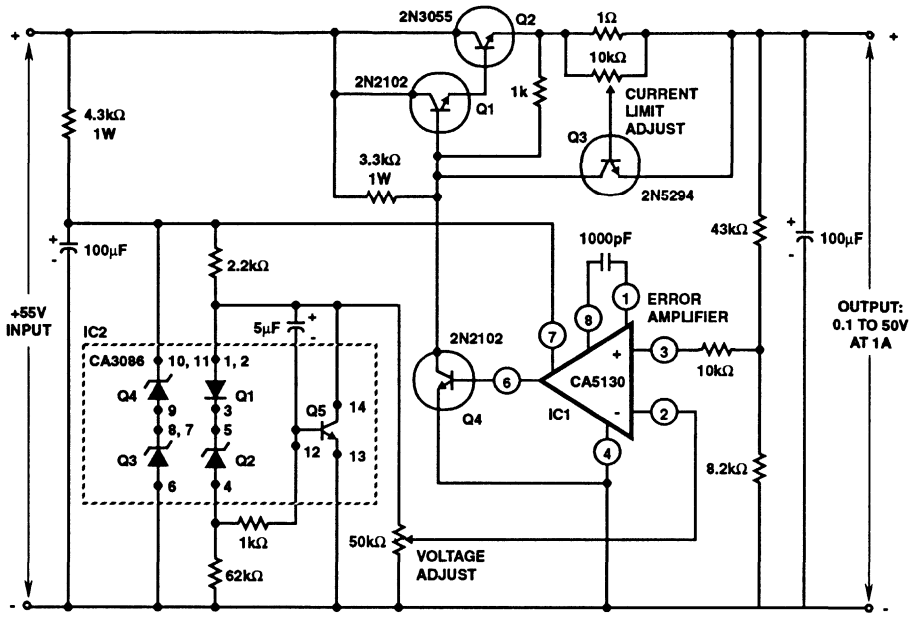
B. PEAK NEGATIVE DETECTOR CIRCUIT

FIGURE 21. PEAK-DETECTOR CIRCUITS



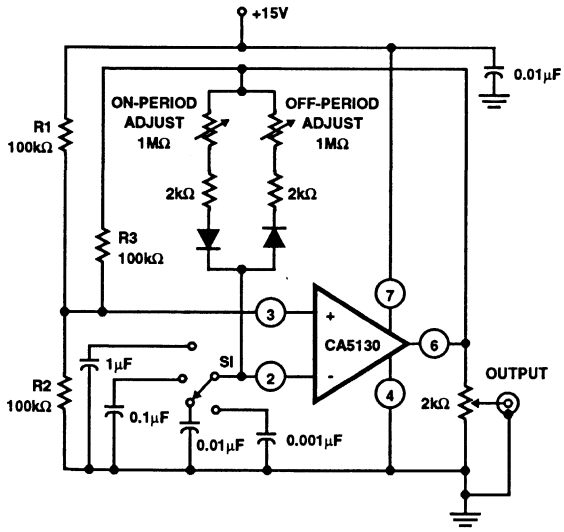
REGULATION (NO LOAD TO FULL LOAD): < 0.01%
INPUT REGULATION: 0.02%/V
HUM AND NOISE OUTPUT: < 25µV UP TO 100kHz

FIGURE 22. VOLTAGE REGULATOR CIRCUIT (0 TO 13V AT 40mA)



REGULATION (NO LOAD TO FULL LOAD): < 0.005%
INPUT REGULATION: 0.01%/V
HUM AND NOISE OUTPUT: < 250μV RMS UP TO 100kHz

FIGURE 23. VOLTAGE REGULATOR CIRCUIT (0.1 TO 50V AT 1A)



FREQUENCY RANGE:

POSITION OF SI	PULSE PERIOD
0.001μF	4μs to 1ms
0.01μF	40μs to 10ms
0.1μF	0.4μs to 100ms
1μF	4μs to 1s

FIGURE 24. PULSE GENERATOR (ASTABLE MULTIVIBRATOR) WITH PROVISIONS FOR INDEPENDENT CONTROL OF "ON" AND "OFF" PERIODS.

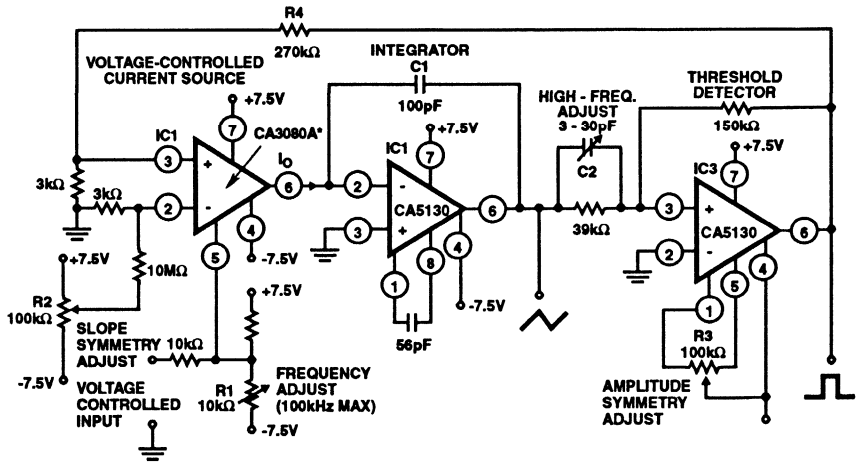


FIGURE 25. FUNCTION GENERATOR (FREQUENCY CAN BE VARIED 1,000,000/1 WITH A SINGLE CONTROL)

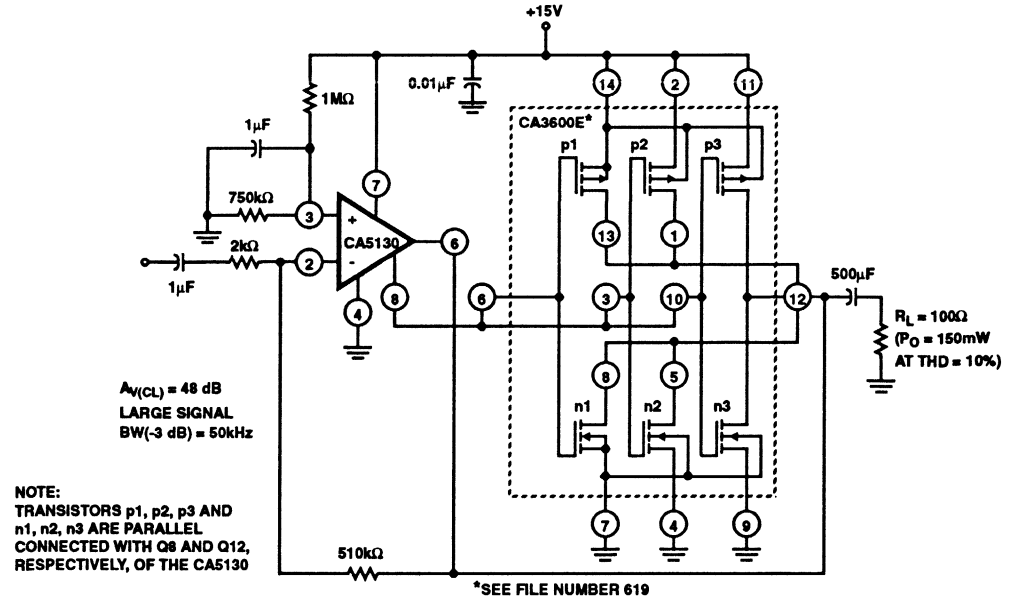


FIGURE 26. CMOS TRANSISTOR ARRAY (CA3600E) CONNECTED AS POWER BOOSTER IN THE OUTPUT STAGE OF THE CA5130

HARRIS SEMICONDUCTOR

CA5160

BiMOS Microprocessor Operational Amplifiers with MOSFET Input/CMOS Output

March 1993

Features

- MOSFET Input Stage
  - Very High Z_I; 1.5TΩ (1.5 x 10^{12}Ω) Typ.
  - Very Low I_I; 5pA Typ. at 15V Operation
    2pA Typ. at 5V Operation
- Common-Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails
- CA5160A, CA5160 Have Full Military Temperature Range Guaranteed Specifications for V+ = 5V
- CA5160A, CA5160 Are Guaranteed to Operate Down to 4.5V for A_{OL}
- CA5160A, CA5160 Are Guaranteed Up to ±7.5V

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- Ideal Interface With Digital CMOS
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single Supply D/A Converter)
- Wien-Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers
- 5V Logic Systems
- Microprocessor Interface

Description

CA5160A and CA5160 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA5160 series circuits are frequency compensated versions of the popular CA5130 series. They are designed and guaranteed to operate in microprocessor or logic systems that use +5V supplies.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common-mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute in single supply applications.

A complementary symmetry MOS (CMOS) transistor pair, capable of swinging the output voltage to within 10mV of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

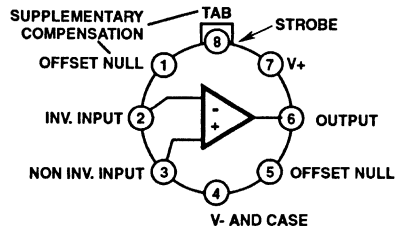
The CA5160 Series circuits operate at supply voltages ranging from +5V to +16V, or ±2.5V to ±8V when using split supplies, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage. They have guaranteed specifications for 5V operation over the full military temperature range of -55°C to +125°C.

Ordering Information

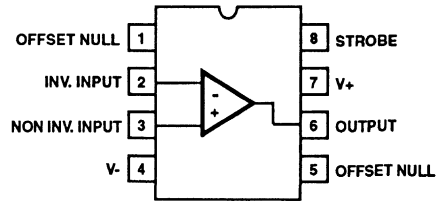
PART NUMBER	TEMP. RANGE	PACKAGE
CA5160AE	-55°C to +125°C	8 Lead Plastic DIP
CA5160AT	-55°C to +125°C	8 Pin Can
CA5160AM	-55°C to +125°C	8 Lead SOIC
CA5160M	-55°C to +125°C	8 Lead SOIC
CA5160E	-55°C to +125°C	8 Lead Plastic DIP
CA5160T	-55°C to +125°C	8 Pin Can

Pinouts

CA5160A, CA5160 (CAN)
TOP VIEW



CA5160A, CA5160 (PDIP, SOIC)
TOP VIEW



CA5160 Series devices have an on-chip frequency compensation network. Supplementary phase-compensation or frequency roll-off (if desired) can be connected externally between terminals 1 and 8.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1924.2**

Absolute Maximum Ratings

Supply Voltage
(Between V+ and V- Terminals) 16V
Differential Input Voltage..... 8V
DC Input Voltage ..... (V+ +8V) to (V- -0.5V)
Input Current.....1mA
Output Short Circuit Duration (Note 2)..... Indefinite
Junction Temperature..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.)..... +300°C

Operating Conditions

Operating Temperature Range .....-55°C to +125°C
Storage Temperature Range.....-65°C to +150°C
Output Short Circuit Duration (Note 1) .....Indefinite

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, V+ = 5V, V- = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA5160A			CA5160			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_O = 2.5V	-	1.5	4	-	2	10	mV
Input Offset Current	I_{IO}	V_O = 2.5 V	-	0.1	5	-	0.1	10	pA
Input Current	I_I	V_O = 2.5V	-	2	10	-	2	15	pA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 1V	75	87	-	70	80	-	dB
		V_{CM} = 0 to 2.5V	60	69	-	60	69	-	dB
Common Mode Input Voltage Range	V_{ICR}+		2.5	2.8	-	2.5	2.8	-	V
	V_{ICR}-		-	-0.5	0	-	-0.5	0	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 1V; ΔV- = 1V	60	75	-	55	67	-	dB
Large Signal Voltage Gain (Note 1)	A_{OL}								
V_O = 0.1 to 4.1V		R_L= ∞	100	117	-	95	117	-	dB
V_O = 0.1 to 3.6V		R_L=10kΩ	90	102	-	85	102	-	dB
Source Current	I_{SOURCE}	V_O = 0V	1.0	3.1	4.0	1.0	2.2	4.0	mA
Sink Current	I_{SINK}	V_O = 5V	1.0	1.6	4.0	1.0	3.4	4.0	mA
Maximum Output Voltage	V_{OUT}								
V_{OM}+		R_L = ∞	4.99	5	-	4.99	5	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V
V_{OM}+		R_L = 10kΩ	4.4	4.7	-	4.4	4.7	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V
V_{OM}+		R_L = 2kΩ	2.5	3.3	-	2.5	3.3	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V

Electrical Specifications T_A = +25°C, V+ = 5V, V- = 0V, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA5160A			CA5160			
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	I_{SUPPLY}	V_O = 0V	-	50	100	-	50	100	µA
	I_{SUPPLY}	V_O = 2.5V	-	320	400	-	320	400	µA

NOTE:

1. For V+ = 4.5V and V- = GND; V_{OUT} = 0.5V to 3.2V at R_L = 10kΩ
2. Short circuit may be applied to ground or to either supply.

Electrical Specifications T_A = -55°C to +125°C, V+ = 5V, V- = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA5160A			CA5160			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_O = 2.5V	-	2	10	-	3	15	mV
Input Offset Current	I_{IO}	V_O = 2.5 V	-	0.1	5	-	0.1	10	nA
Input Current	I_I	V_O = 2.5V	-	2	10	-	2	15	nA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 1V	60	80	-	60	80	-	dB
		V_{CM} = 0 to 2.5V	55	80	-	50	75	-	dB
Common Mode Input Voltage Range	V_{ICR}+		2.5	2.8	-	2.5	2.8	-	V
	V_{ICR}-		-	-0.5	0	-	-0.5	0	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 2V	45	65	-	40	60	-	dB
Large Signal Voltage Gain (Note 1)	A_{OL}								
V_O = 0.1 to 4.1V		R_L= ∞	94	110	-	90	110	-	dB
V_O = 0.1 to 3.6V		R_L=10kΩ	80	100	-	75	100	-	dB
Source Current	I_{SOURCE}	V_O = 0V	0.6	2.2	5.0	0.6	-	5.0	mA
Sink Current	I_{SINK}	V_O = 5V	0.6	1.15	5.0	0.6	-	5.0	mA
Maximum Output Voltage	V_{OUT}								
V_{OM}+		R_L = ∞	4.99	5	-	4.99	5	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V
V_{OM}+		R_L = 10kΩ	4.0	4.3	-	4.0	4.3	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V
V_{OM}+		R_L = 2kΩ	2.0	2.5	-	2.0	2.5	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V

Electrical Specifications T_A = -55°C to +125°C, V+ = 5V, V- = 0V, Unless Otherwise Specified(Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA5160A			CA5160			
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current									
V_O = 0V	I_{SUPPLY}		-	170	220	-	170	220	µA
V_O = 2.5V	I_{SUPPLY}		-	410	500	-	410	500	µA

NOTE:

1. For V+ = 4.5V and V- = GND; V_{OUT} = 0.5V to 3.2V at R_L = 10kΩ

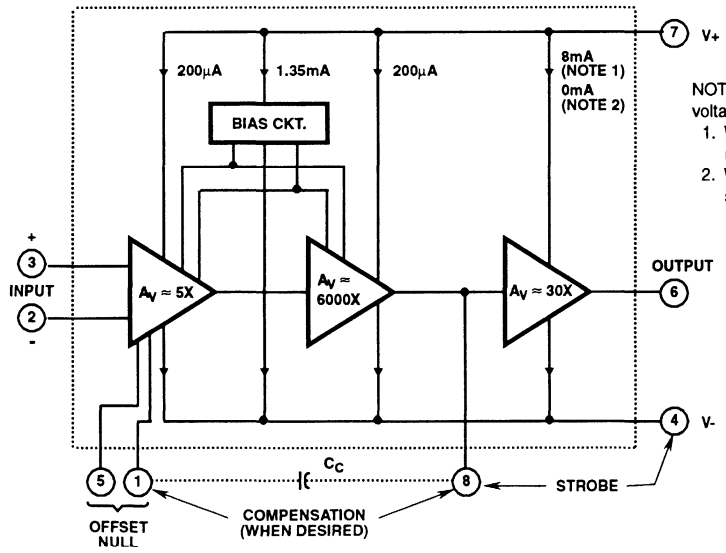
Electrical Specifications T_A = +25°C, V+ = 15V, V- = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA5160A			CA5160			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V± = ±7.5V	-	2	5	-	6	15	mV
Input Offset Current	I_{IO}	V± = ±7.5V	-	0.5	20	-	0.5	30	pA
Input Current	I_I	V± = ±7.5V	-	5	30	-	5	50	pA
Large Signal Voltage Gain	A_{OL}	V_O = 10V_{P-P}, R_L = 2kΩ	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common Mode Rejection Ratio	CMRR		80	95	-	70	90	-	dB
Common Mode Input Voltage Range	V_{ICR}		10	-0.5 to 12	0	10	-0.5 to 12	0	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 1V; ΔV- = 1V, V± = ±7.5V	-	32	150	-	32	320	µV/V
Maximum Output Voltage	V_{OUT}								
V_{OM}+		R_L = 2kΩ	12	13.3	-	12	13.3	-	V
V_{OM}-			-	0.002	0.01	-	0.002	0.01	V
V_{OM}+		R_L = ∞	14.99	15	-	14.99	15	-	V
V_{OM}-			-	0	0.01	-	0	0.1	V
Maximum Output Current	I_O								
I_{OM}+ (Source)		V_O = 0V	12	22	45	12	22	45	mA
I_{OM} (Sink)		V_O = 15V	12	20	45	12	20	45	mA
Supply Current	I+	R_L = ∞, V_O = 7.5V	-	10	15	-	10	15	mA
		R_L = ∞, V_O = 0V	-	2	3	-	2	3	mA
Input Offset Voltage Temp. Drift		$\Delta V_{IO}/\Delta T$	-	6	-	-	8	-	µV/°C

Typical Values Intended Only for Design Guidance T_A = +25°C, V+ = +7.5V, V- = -7.5V (Unless Otherwise Specified)

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS CA5160A TYP	LIMITS CA5160 TYP	UNITS
Input Offset Voltage Adjustment Range		10kΩ Across Terminals 4 and 5 or 4 and 1	±22	±22	mV
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I	f = 1MHz	4.3	4.3	pF
Equivalent Input Noise Voltage	e_N	BW = 0.2MHz, R_S = 1MΩ	40	40	μV
		BW = 0.2MHz, R_S = 10MΩ	50	50	μV
Equivalent Input Noise Voltage	e_N	R_S = 100Ω, 1kHz	72	72	$nV/\sqrt{Hz}$
		R_S = 100Ω, 10kHz	30	30	$nV/\sqrt{Hz}$
Unity Gain Crossover Frequency	f_T		4	4	MHz
Slew Rate	SR		10	10	V/μs
Transient Response Rise Time	t_R	C_C = 25pF, R_L = 2kΩ (Voltage Follower)	0.09	0.09	μs
Overshoot	OS		10	10	%
Settling Time (To <0.1%, V_{IN} = $4V_{P-P}$)	t_S	C_C = 25pF, R_L = 2kΩ (Voltage Follower)	1.8	1.8	μs

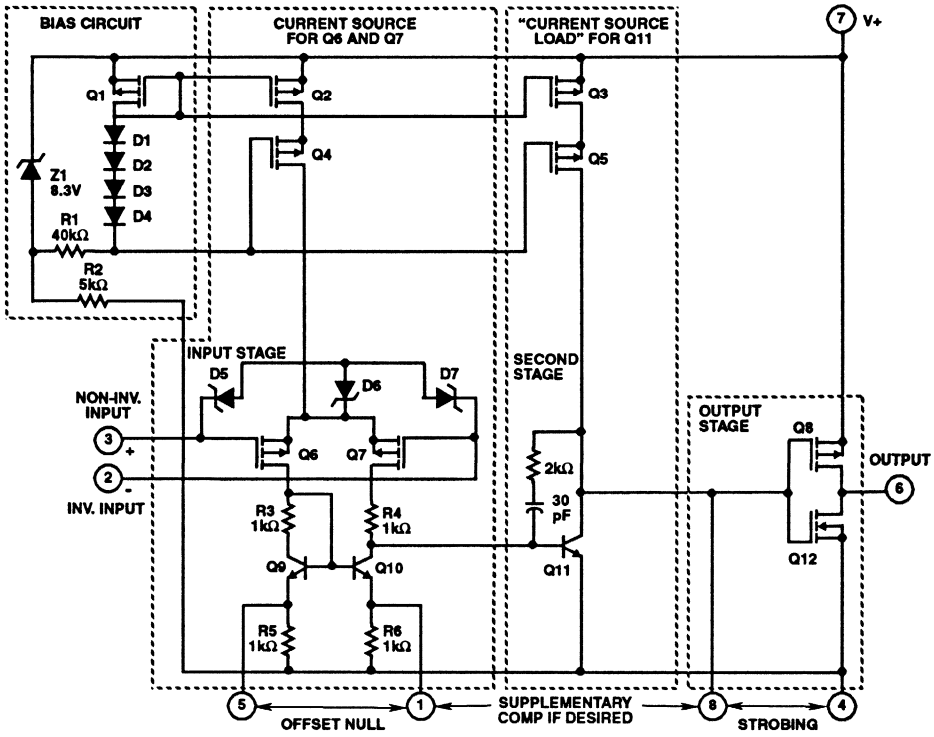
Block Diagram



NOTE: Total supply voltage (for indicated voltage gains) = 15V

1. With input terminals biased so that Terminal 6 potential is +7.5V above terminal 4.
2. With output terminal driven to either supply rail.

Schematic Diagram



NOTE: Diodes D5 Through D7 Provide Gate Oxide Protection For MOSFET Input Stage

Circuit Description

Refer to the block diagram of the CA5160 series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA5160 series circuits are ideal for single supply operation. Three class A amplifier stages, having the individual gain capability and current consumption shown in the block diagram, provide the total gain of the CA5160. A biasing circuit provides two potentials for common use in the first and second stages. Terminals 8 and 1 can be used to supplement the internal phase compensation network if additional phase compensation or frequency roll-off is desired. Terminals 8 and 4 can also be used to strobe the output stage into a low quiescent current state. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).

Input Stages - The circuit of the CA5160 is shown in the schematic diagram. It consists of a differential input stage using PMOS field effect transistors (Q6, Q7) working into a mirror pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000 ohm potentiometer across Terminals 1 and 5 and the potentiometer slider arm to Terminal 4.

Cascode-connected PMOS transistors Q2, Q4, are the constant current source for the input stage. The biasing circuit for the constant current source is subsequently described. The small diodes D5 through D7 provide gate-oxide protection against high voltage transients, including static electricity during handling for Q6 and Q7.

Second Stage

Most of the voltage gain in the CA5160 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is described later. Miller Effect compensation (roll off) is accomplished by means of the 30pf capacitor and 2kΩ resistor connected between the base and collector of transistor Q11. These internal components provide sufficient compensation for unity gain operation in most applications. However, additional compensation, if desired, may be used between Terminals 1 and 8.

Bias-Source Circuit - At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Terminal 7. A potential of about 2.2 volts is developed across diode connected PMOS transistor Q1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror connected" to both Q2 and Q3. Since transistors Q1, Q2 and Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series connected R1, D1-D4, and Q1 varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply voltage variations. This variation results in deterioration of the power supply rejection ration (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage - The output stage consists of a drain loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Figure 3. Typical op-amp loads are readily driven by the output stage. Because large signal excursions are nonlinear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 percent accuracy levels, including the negative supply rail.

Typical Performance Curves

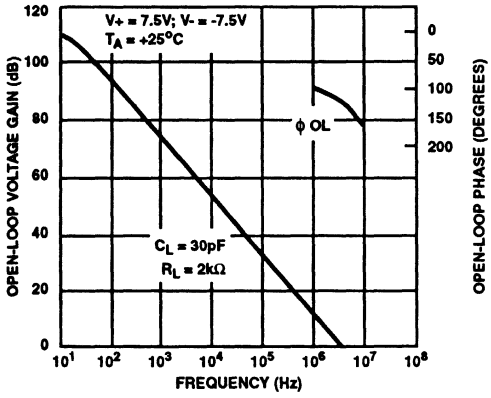


FIGURE 1. OPEN- LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY

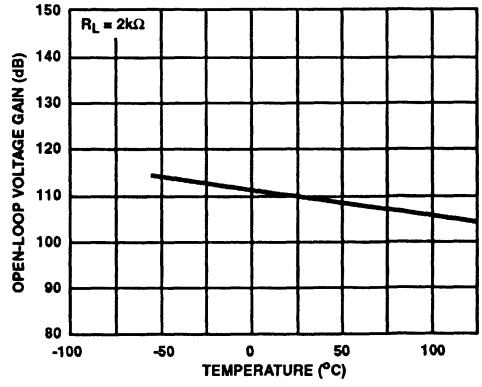


FIGURE 2. OPEN-LOOP GAIN vs TEMPERATURE

Typical Performance Curves

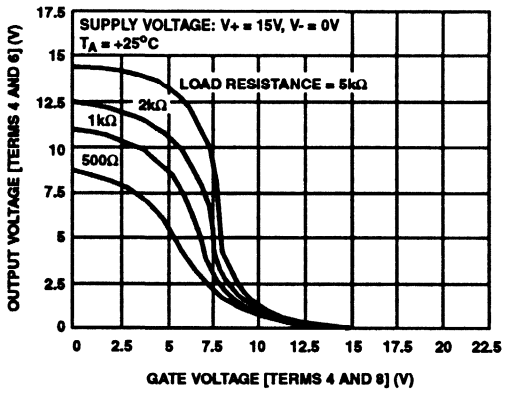


FIGURE 3. VOLTAGE TRANSFER CHARACTERISTICS OF CMOS OUTPUT STAGE

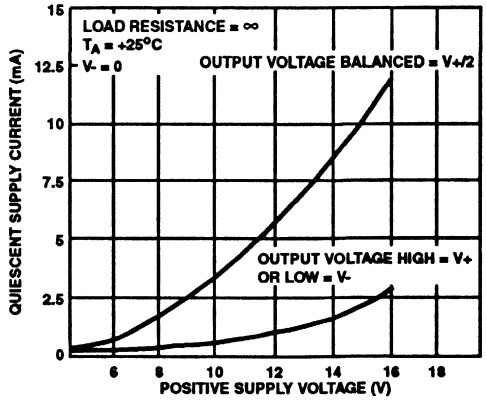


FIGURE 4. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

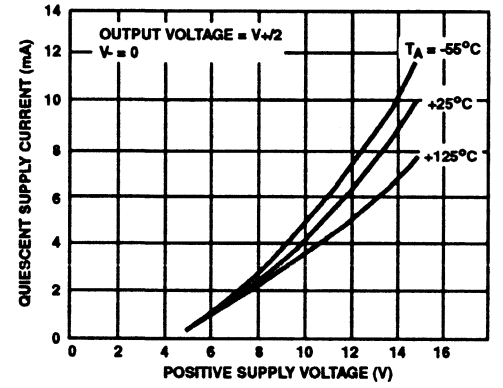


FIGURE 5. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

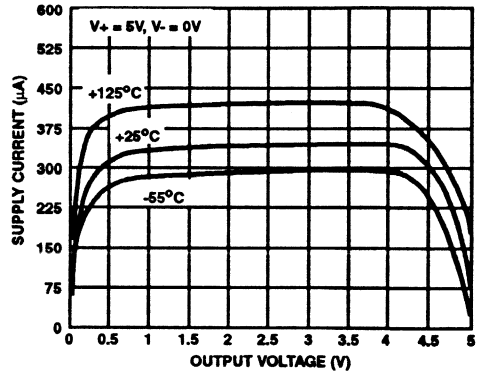


FIGURE 6. SUPPLY CURRENT vs OUTPUT VOLTAGE

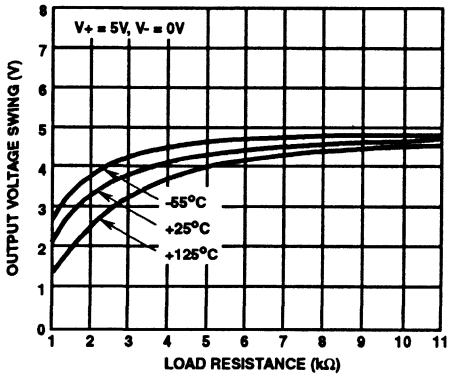


FIGURE 7. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

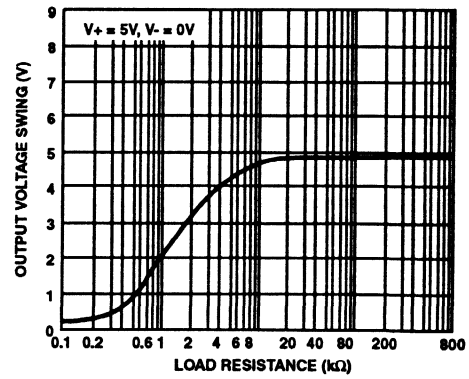


FIGURE 8. OUTPUT SWING vs LOAD RESISTANCE

Typical Performance Curves

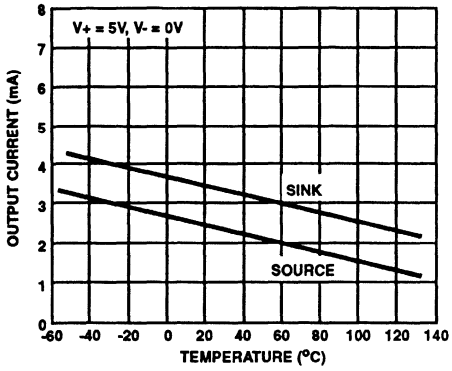


FIGURE 9. OUTPUT CURRENT vs TEMPERATURE

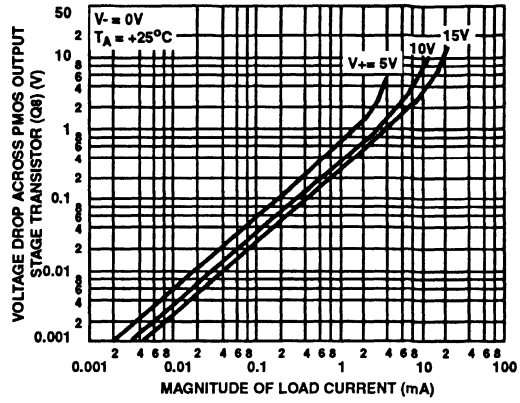


FIGURE 10. VOLTAGE ACROSS PMOS OUTPUT TRANSISTOR (Q8) vs LOAD CURRENT

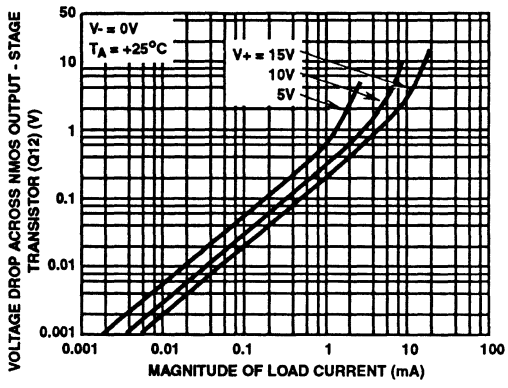


FIGURE 11. VOLTAGE ACROSS NMOS OUTPUT TRANSISTOR (Q12) vs LOAD CURRENT

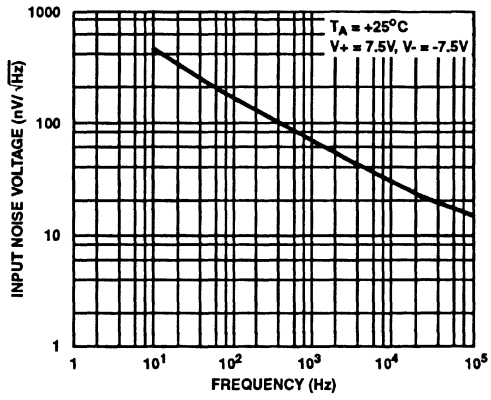


FIGURE 12. EQUIVALENT NOISE VOLTAGE vs FREQUENCY

Offset Nulling

Offset voltage nulling is usually accomplished with a 100,000Ω potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset null adjustment usually can be affected with the slider arm positioned in the mid point of the potentiometer's total range.

Input Current Variation with Common Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA5160 Series Op-Amps is typically 5pA at T_A = +25°C when Terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Figure 13 contains data showing the variation of input current as a function of common-mode input voltage at T_A = +25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA5160 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

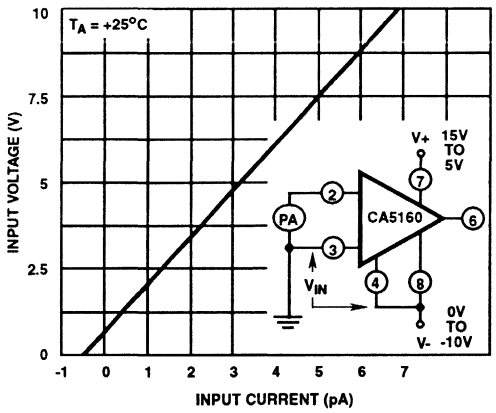


FIGURE 13. CA5160 INPUT CURRENT vs COMMON MODE VOLTAGE

Input Current Variation with Temperature

The input current of the CA5160 series circuits is typically 5 pA at +25°C. The major portion of this input current is due to leakage current through the gate protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Figure 14 provides data on the typical variation of input bias current as a function of temperature in the CA5160.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA5160. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

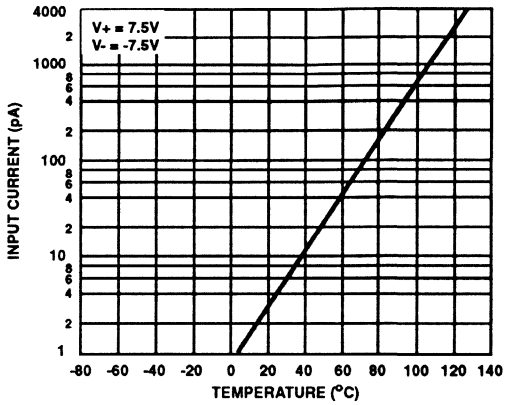


FIGURE 14. INPUT CURRENT vs AMBIENT TEMPERATURE

Input Offset Voltage (V_{IO}) Variation with DC Bias vs Device Operating Life

It is well known that the characteristics of a MOSFET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA5160 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terminals 2 and 3. Figure 15 shows typical data pertinent to shifts in offset voltage encountered with CA5160 devices in TO-5 packages during life testing. At lower temperatures (TO-5 and plastic) for example at +85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output state is "toggled", e.g., as in comparator applications.

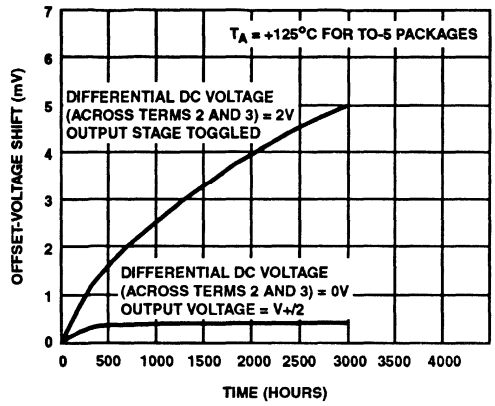


FIGURE 15. TYPICAL INCREMENTAL OFFSET-VOLTAGE SHIFT vs OPERATING LIFE

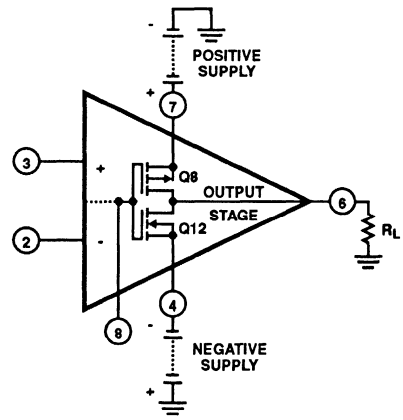
Power Supply Considerations

Because the CA5160 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single-and dual-supply service. Figures 16A and 16B show the CA5160 connected for both dual and single-supply operation.

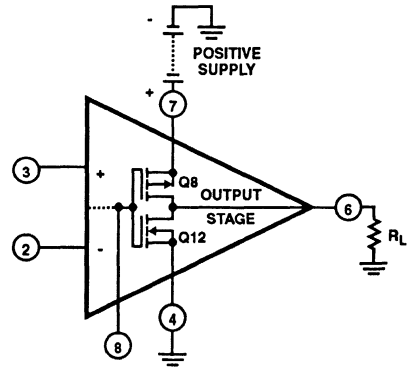
Dual-supply Operation: When the output voltage at Terminal 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single Supply Operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (Number 6) voltage is at V+/2, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Figure 4 shows typical quiescent supply-current vs supply-voltage for the CA5160 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage transfer characteristics (see Figure 3). If either Q8 or Q12 are swung out of their linear regions toward cutoff (a nonlinear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA5160, however, continue to draw modest supply-current (see the lower curve in Figure 4) even through the output stage is strobed off. Figure 16A shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Terminal 6 and ground in the circuit of Figure 16B. Let it further be assumed again that the input terminal bias (Terminals 2 and 3) is such that the output terminal (Number 6) voltage is V+/2. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply current must increase as an inverse function of the R_L magnitude. Figure 10 shows the voltage drop across PMOS transistor Q8 as a function of load current at several supply voltages. Figure 3 shows the voltage transfer characteristics of the output stage for several values of load resistance.



(A) DUAL POWER-SUPPLY OPERATION



(B) SINGLE POWER-SUPPLY OPERATION

FIGURE 16. CA5160 OUTPUT STAGE IN DUAL AND SINGLE POWER-SUPPLY OPERATION

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA5160 is most advantageous in applications where in the source resistance of the input signal is on the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 40μV when the test-circuit amplifier of Figure 17 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

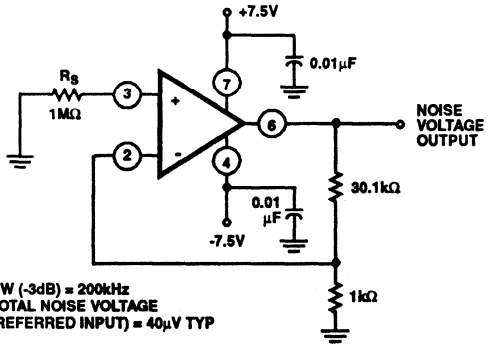


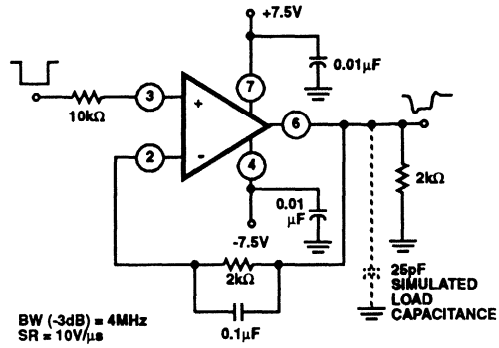
FIGURE 17. TEST-CIRCUIT AMPLIFIER (30dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENTS

Typical Applications

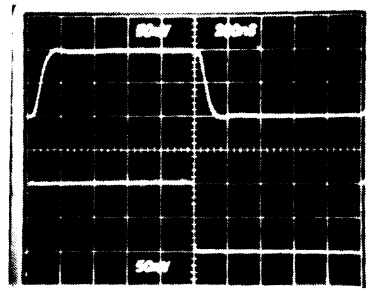
Voltage Followers

Operational amplifiers with very high input resistances, like the CA5160, are particularly suited to service as voltage followers. Figure 18 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA5160 in a split supply-configuration.

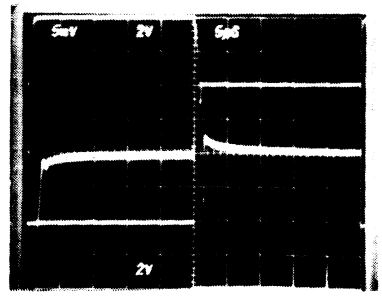
A voltage follower, operated from a single-supply, is shown in Figure 19 together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Figure 19B with input-signal ramping. The waveforms in Figure 19C show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Figure 19C also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA5160 in a single-supply voltage follower application.



(A)



(B) SMALL SIGNAL RESPONSE
Top Trace: Output
Bottom Trace: Input



(C) INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME
Top Trace: Output Signal
Center Trace: Difference Signal 5mV/Div.
Bottom Trace: Input Signal

FIGURE 18. SPLIT-SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS

9-Bit CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Figure 20. This system combines the concepts of multiple-switch CMOS IC's, a low cost ladder network of discrete metal-oxide-film resistors, a CA5160 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10 volt logic levels are used in the circuit of Figure 20.

* "Digital-to-Analog Conversion Using the Harris CD4007A CMOS IC", Application Note AN-6080.

The circuit uses an R/2R voltage-ladder network, with the output-potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one percent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000Ω resistors from the same manufacturing lot.

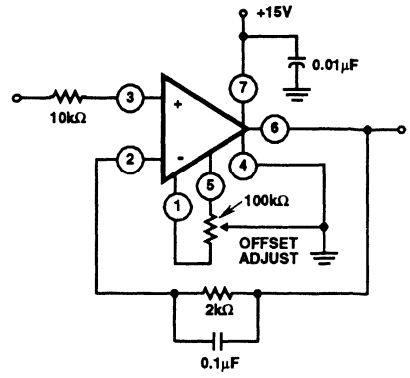
A single 15-volt supply provides a positive bus for the CA5160 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the CMOS building blocks simplifies the design of DAC systems tailored to particular needs.

Error Amplifier In Regulated Power Supplies

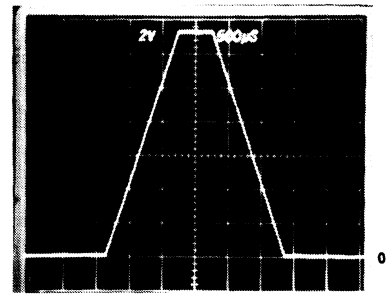
The CA5160 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero.

The circuit shown in Figure 21 uses a CA5160 as an error amplifier in a continuously adjustable 1-ampere power supply. One of the key features of this circuit is its ability to regulate down to the vicinity of zero with only one dc power supply input.

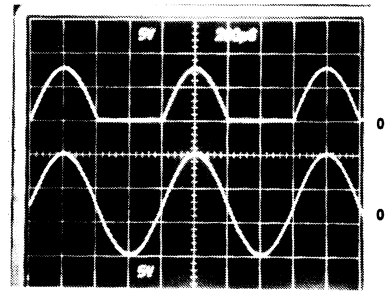
An RC network, connected between the base of the output drive transistor and the input voltage, prevents "turn-on overshoot", a condition typical of many operational-amplifier regulator circuits. As the amplifier becomes operational, this RC network ceases to have influence on the regulator performance.



(A)



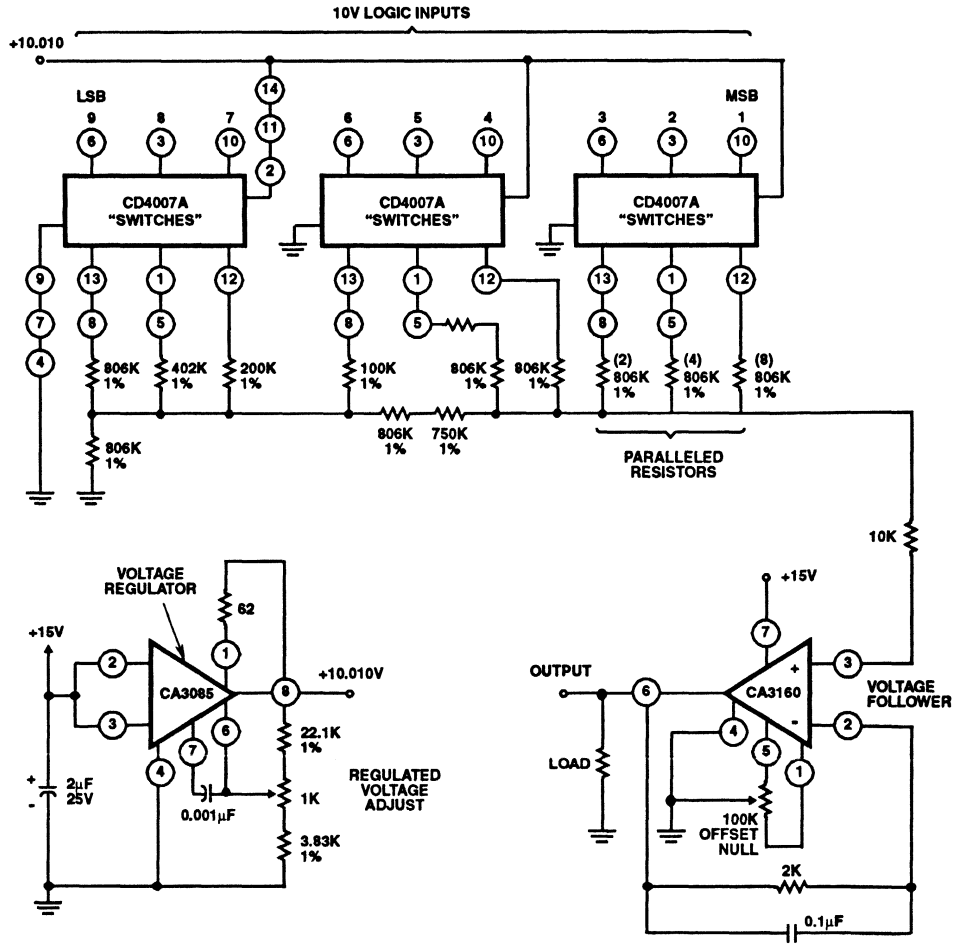
(B) OUTPUT SIGNAL WITH INPUT-SIGNAL RAMPING.



(C) OUTPUT-WAVEFORM WITH GROUND-REFERENCE SINE-WAVE INPUT

Top Trace: Output
Bottom Trace: Input

FIGURE 19. SINGLE-SUPPLY VOLTAGE-FOLLOWER WITH ASSOCIATED WAVEFORMS. (e.g., FOR USE IN SINGLE-SUPPLY D/A CONVERTER; SEE FIGURE 9 IN AN-6080)



BIT	REQUIRED RATIO-MATCH
1	Standard
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6 - 9	±1% ABS.

FIGURE 20. 9-BIT DAC USING CMOS DIGITAL SWITCHES AND CA5160

Precision Voltage-Controlled Oscillator

The circuit diagram of a precision voltage-controlled oscillator is shown in Figure 22. The oscillator operates with a tracking error on the order of 0.02 percent and a temperature coefficient of 0.01%/°C. A multivibrator (A_1) generates pulses of constant amplitude (V) and width (T_2). Since the output (terminal 6) of A_1 (a CA5130) can swing within about 10 millivolts of either supply-rail, the output pulse amplitude (V) is essentially equal to V+. The average output voltage ($E_{avg} = V\ T_2/T_1$) is applied to the non-inverting input terminal of comparator A_2 (a CA5160) via an integrating network R_3, C_2. Comparator A_2 operates to establish circuit conditions such that $E_{avg} = V1$. This circuit condition is accomplished by feeding an output signal from terminal 6 of A_2 through R_4, D_4 to the inverting terminal (terminal 2) of A_1, thereby adjusting the multivibrator interval, T_3.

Voltmeter With High Input Resistance

The voltmeter circuit shown in Figure 23 illustrates an application in which a number of the CA5160 characteristics are exploited. Range-switch SW1 is ganged between input and output circuitry to permit selection of the proper output voltage for feedback to Terminal 2 via 10kΩ current-limiting resistor. The circuit is powered by a single 8.4 volt mercury battery. With zero input signal, the circuit consumes somewhat less than 500 microamperes plus the meter current required to indicate a given voltage. Thus, at full-scale input, the total supply current rises to slightly more than 1500 microamperes.

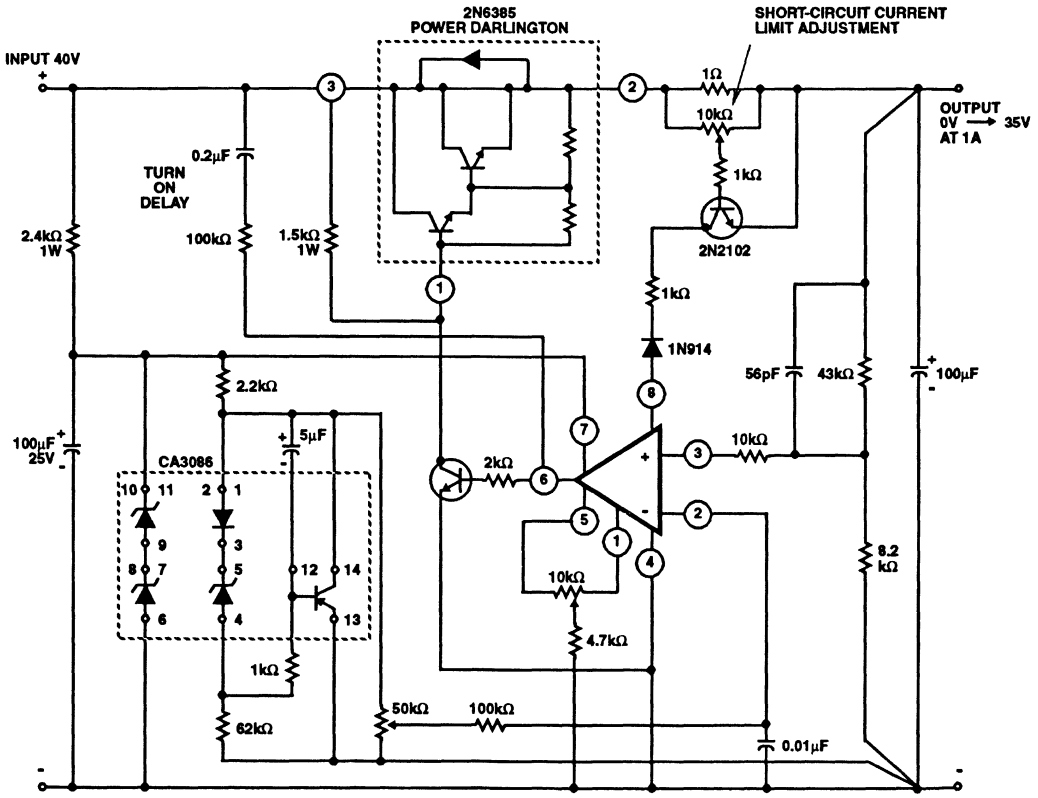


FIGURE 21. CA5160 VOLTAGE REGULATOR CIRCUIT (0.1 TO 35V AT 1A).

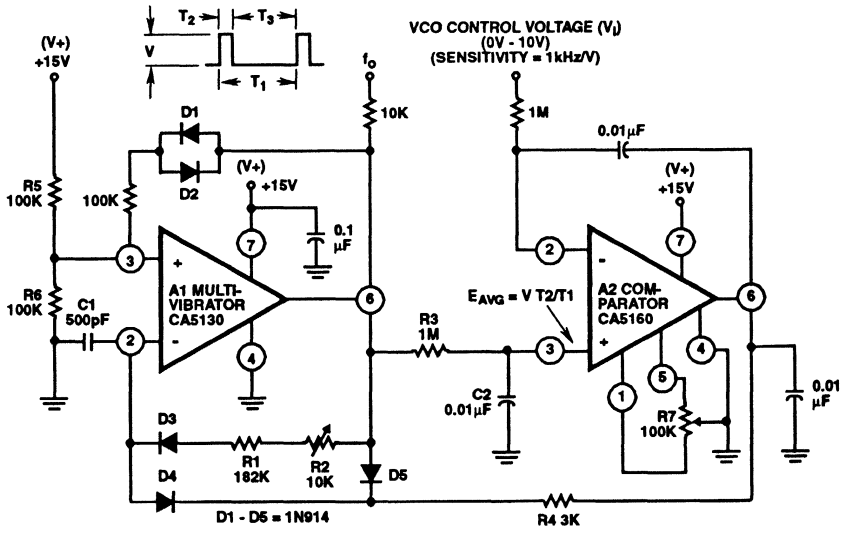


FIGURE 22. VOLTAGE CONTROLLED OSCILLATOR

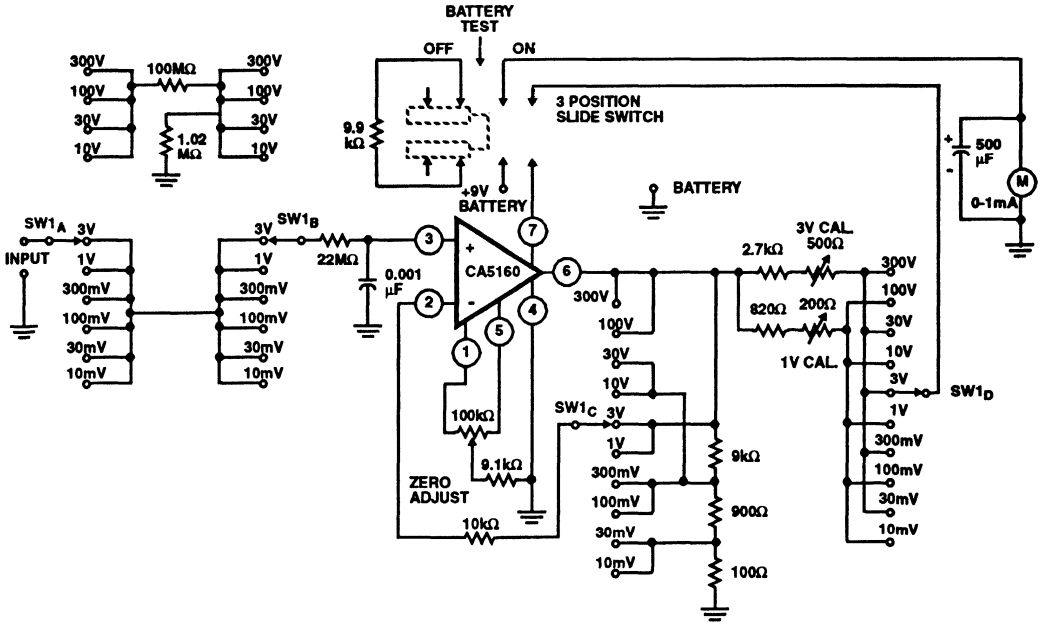
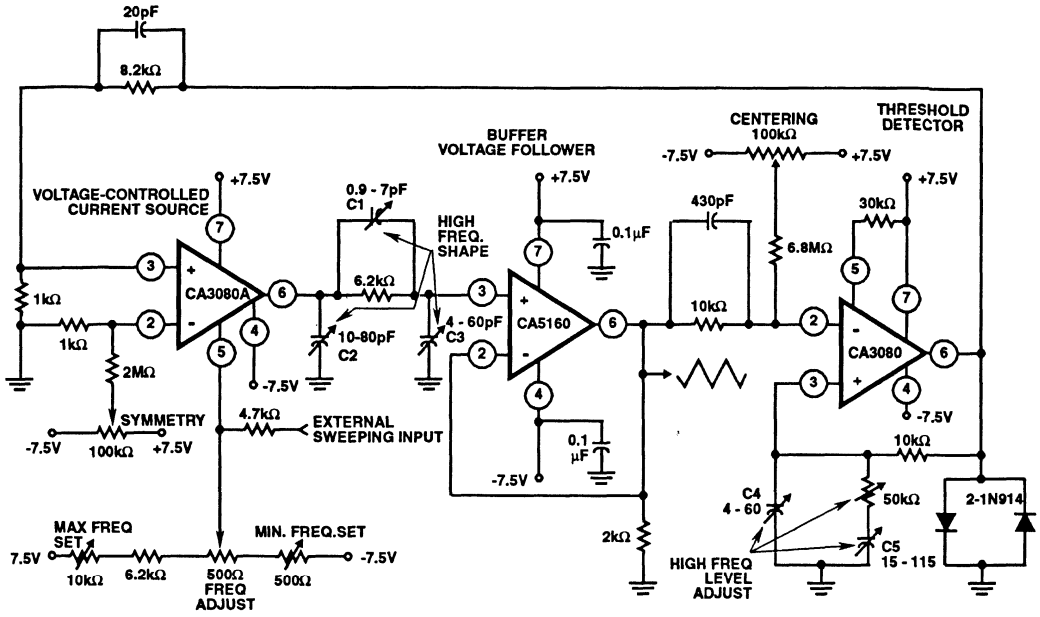
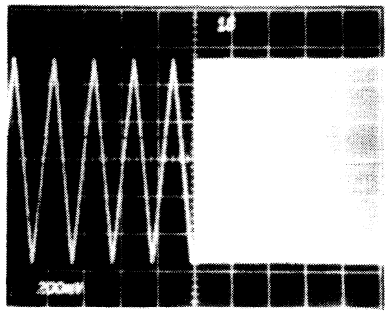


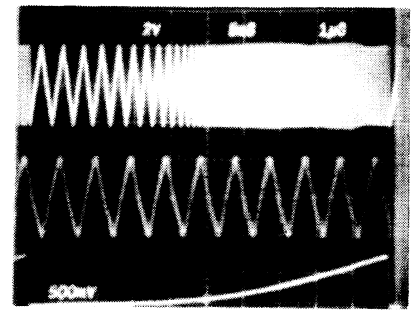
FIGURE 23. CA5160A HIGH INPUT RESISTANCE DC VOLTMETER



(A)

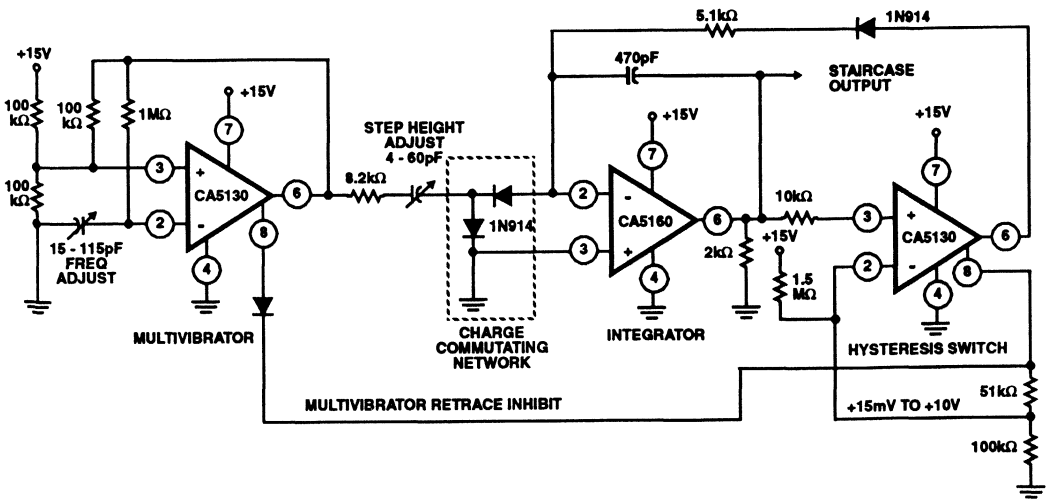


(B) TWO-TONE OUTPUT SIGNAL FROM THE FUNCTION GENERATOR. A SQUARE WAVE SIGNAL MODULATES THE EXTERNAL SWEEPING INPUT TO PRODUCE 1Hz AND 1MHz, SHOWING THE 1,000,000/1 FREQUENCY RANGE OF THE FUNCTION GENERATOR

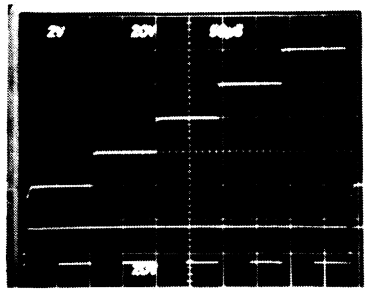


(C) TRIPLE-TRACE OF THE FUNCTION GENERATOR SWEEPING TO 1MHz. THE BOTTOM TRACE IS THE SWEEPING SIGNAL AND THE TOP TRACE IS THE ACTUAL GENERATOR OUTPUT. THE CENTER TRACE DISPLAYS THE 1MHz SIGNAL VIA DELAYED OSCILLOSCOPE TRIGGERING OF THE UPPER SWEPT OUTPUT SIGNAL

FIGURE 24. CA5160 1,000,000/1 SINGLE CONTROL FUNCTION GENERATOR - 1MHz TO 1Hz



(A)



(B) STAIRCASE GENERATOR WAVEFORM
Top Trace: Staircase Output 2V Steps
Center Trace: Comparator
Bottom Trace: Oscillator

FIGURE 25. STAIRCASE GENERATOR CIRCUIT UTILIZING THREE CMOS OPERATIONAL AMPLIFIERS

Function Generator

A function generator having a wide tuning range is shown in Figure 24. The adjustment range, in excess of 1,000,000/1, is accomplished by a single potentiometer. Three operational amplifiers are utilized: a CA5160 as a voltage follower, a CA3080 as a high-speed comparator, and a second CA3080A as a programmable current source. Three variable capacitors C1, C2, and C3 shape the triangular signal between 500kHz and 1MHz. Capacitors C4, C5, and the trimmer potentiometer in series with C5 maintain essentially constant (±10%) amplitude up to 1MHz.

Staircase Generator

Figure 25 shows a staircase generator circuit utilizing three CMOS operational amplifiers. Two CA5130's are used; one as a multivibrator, the other as a hysteresis switch. The third amplifier, a CA5160, is used as a linear staircase generator.

Picoammeter Circuit

Figure 26 is a current-to-voltage converter configuration utilizing a CA5160 and CA3140 to provide a picoampere meter for ±3pA full-scale meter deflection. By placing Terminals 2 and 4 of the CA5160 at ground potential, the CA5160 input is operated in the "guarded mode". Under this operating condition, even slight leakage resistance present between Terminals 3 and 2 or between Terminals 3 and 4 would result in zero voltage across this leakage resistance, thus substantially reducing the leakage current.

If the CA5160 is operated with the same voltage on input Terminals 3 and 2 as on Terminal 4, a further reduction in the input current to the less than one picoampere level can be achieved as shown in Figure 13.

To further enhance the stability of this circuit, the CA5160 can be operated with its output (Terminal 6) near ground, thus markedly reducing the dissipation by reducing the supply current to the device.

The CA3140 stage serves as a X100 gain stage to provide the required plus and minus output swing for the meter and feedback network. A 100-to-1 voltage divider network consisting of a 9.9kΩ resistor in series with a 100Ω resistor sets the voltage at the 10GΩ resistor (in series with Terminal 3) to ±30mV full-scale deflection. This 30mV signal results from ±3V appearing at the top of the voltage divider network which also drives the meter circuitry.

By utilizing a switching technique in the meter circuit and in the 9.9kΩ and 100Ω network similar to that used in voltmeter circuit shown in Figure 23, a current range of 3pA to 1nA full scale can be handled with the single 10GΩ resistor.

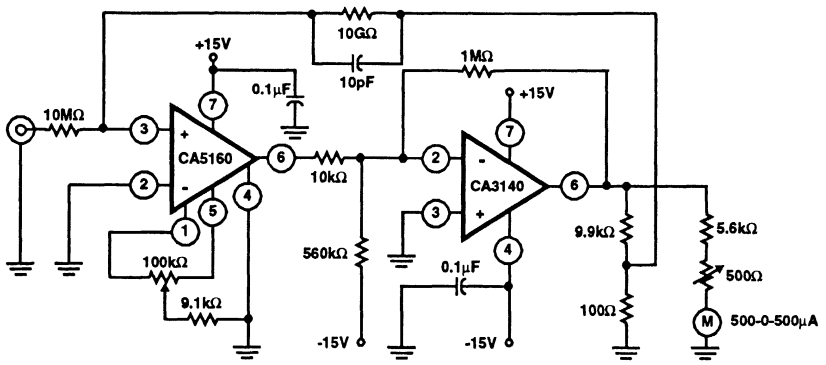
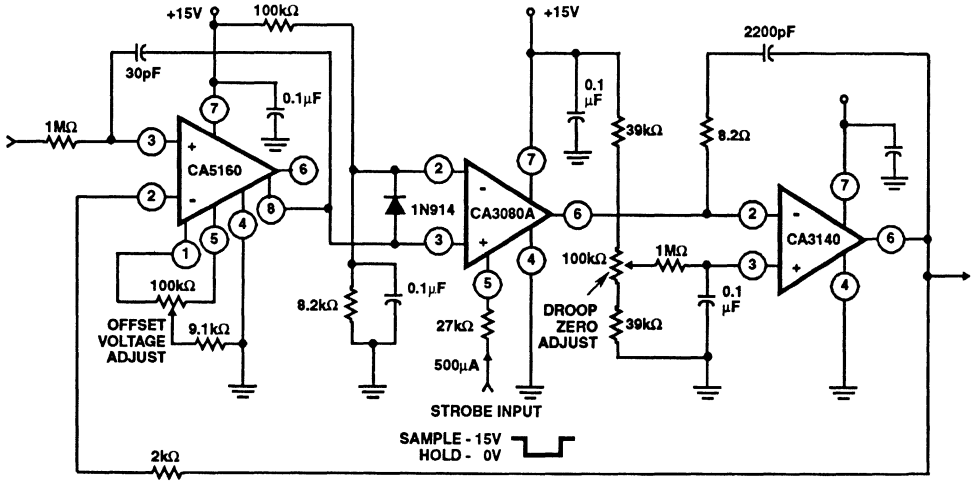
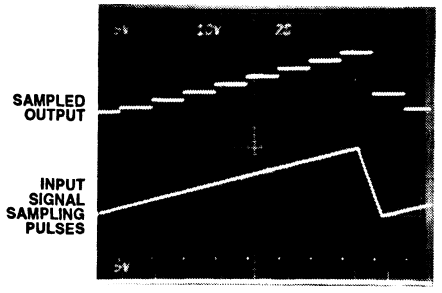


FIGURE 26. CURRENT-TO-VOLTAGE CONVERTER TO PROVIDE A PICOAMMETER WITH ±3pA FULL SCALE DEFLECTION

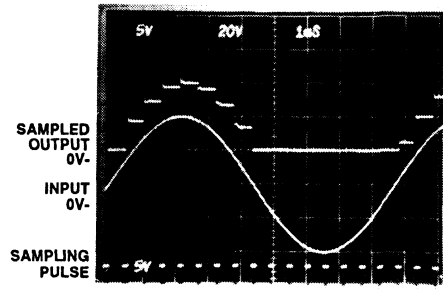


(A)



(B) SAMPLE AND HOLD WAVEFORM

Top Trace: Sampled Output
Center Trace: Input Signal
Bottom Trace: Sampling Pulses



(C) SAMPLE AND HOLD WAVEFORM

Top Trace: Sampled Output
Center Trace: Input
Bottom Trace: Sampling Pulses

FIGURE 27. SINGLE SUPPLY SAMPLE AND HOLD SYSTEM, INPUT 0V TO 10V

Single Supply Sample-and-Hold System

Figure 27 shows a single-supply sample-and-hold system using a CA5160 to provide a high input impedance and an input-voltage range of 0V to 10V. The output from the input buffer integrator network is coupled to a CA3080A. The CA3080A functions as a strobeable current source for the CA3140 output integrator and storage capacitor. The CA3140 was chosen because of its low output impedance and constant gain-bandwidth product. Pulse "droop" during the hold interval can be reduced to zero by adjusting the 100kΩ bias-voltage potentiometer on the positive input of the CA3140. This zero adjustment sets the CA3080A output voltage at its zero current position. In this sample-and-hold circuit it is essential that the amplifier bias current be reduced to zero to minimize output signal current during the hold mode. Even with 320mV at the amplifier bias circuit terminal (5) at least ±100pA of output current will be available.

Wien Bridge Oscillator

A simple, single-supply Wien Bridge oscillator using a CA5160 is shown in Figure 28. A pair of parallel-connected 1N914 diodes comprise the gain-setting network which standardizes the output voltage at approximately 1.1V. The 500Ω potentiometer is adjusted so that the oscillator will always start and the oscillation will be maintained. Increasing the amplitude of the voltage may lower the threshold level for starting and for sustaining the oscillation, but will introduce more distortion.

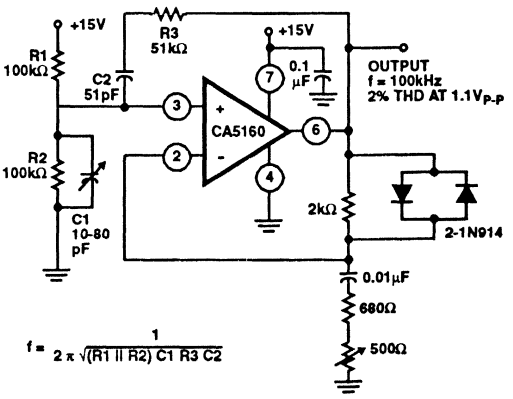


FIGURE 28. SINGLE-SUPPLY WEIN BRIDGE OSCILLATOR

Operation with Output-Stage Power-Booster

The current sourcing and sinking capability of the CA5160 output stage is easily supplemented to provide power-boost capability. In the circuit of Figure 29, three CMOS transistor-pairs in a single CA3600 IC array are shown parallel-connected with the output stage in the CA5160. In the Class A mode of CA3600E shown, a typical device consumes 20mA of supply current at 15V operation. This arrangement boosts the current-handling capability of the CA5160 output stage by about 2.5X.

The amplifier circuit in Figure 29 employs feedback to establish a closed-loop gain of 20dB. The typical large-signal-bandwidth (-3dB) is 190kHz.

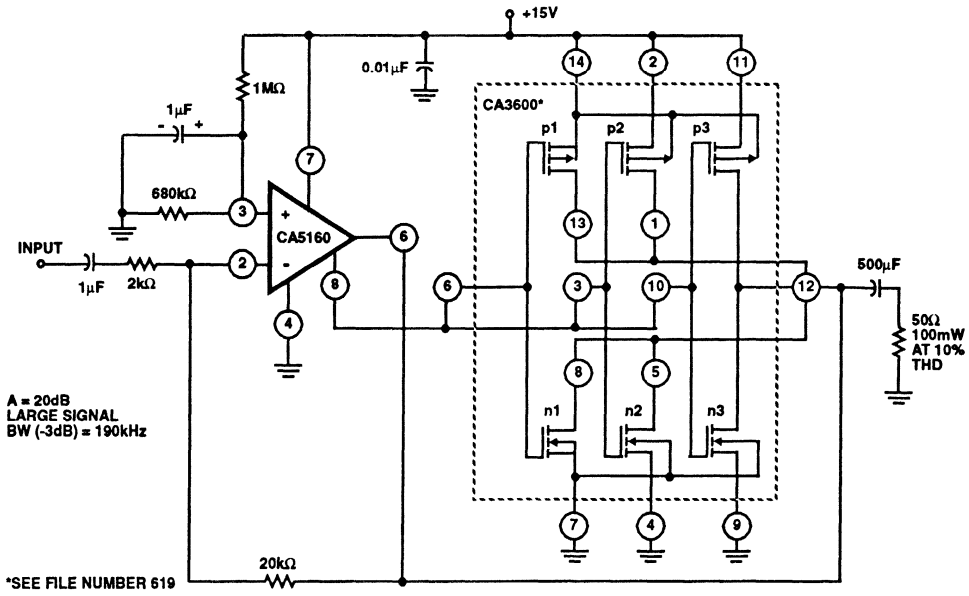


FIGURE 29. CMOS TRANSISTOR ARRAY (CA3600E) CONNECTED AS POWER BOOSTER IN THE OUTPUT STAGE OF THE CA5160.

HARRIS SEMICONDUCTOR

CA5260

BiMOS Microprocessor Operational Amplifiers with MOSFET Input/CMOS Output

March 1993

Features

- MOSFET Input Stage provides
  - Very High Z_I = 1.5TΩ (1.5 x 10^{12}Ω) Typ.
  - Very Low I_I = 5pA Typ. at 15V Operation
    = 2pA Typ. at 5V Operation
- Ideal for Single Supply Applications
- Common Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails
- CA5260A, CA5260 Have Full Military Temperature Range Guaranteed Specifications for V+ = 5V
- CA5260A, CA5260 are Guaranteed to Operate Down to 4.5V for A_{OL}
- Fully guaranteed to operate from -55°C to +125°C at V+ = 5V, V- = Gnd

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- Ideal Interface with Digital CMOS
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to Zero Volts)
- Wien Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers
- 5V Logic Systems
- Microprocessor Interface

Description

The CA5260A and CA5260 are integrated-circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA5260 series circuits are dual versions of the popular CA5160 series. They are designed and guaranteed to operate in microprocessor or logic systems that use +5V supplies.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5V below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10mV of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA5260 Series circuits operate at supply voltages ranging from 4.5V to 16V, or ±2.25V to ±8V when using split supplies.

The CA526OA, CA5260 have guaranteed specifications for 5V operation over the full military temperature range of -55°C to +125°C.

Ordering Information

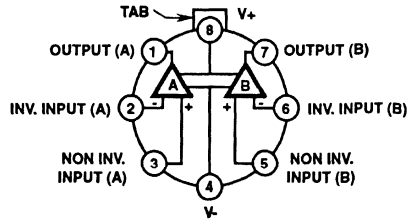
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA5260AE	-55°C to +125°C	8 Lead Plastic DIP
CA5260AM	-55°C to +125°C	8 Lead SOIC
CA5260AM96	-55°C to +125°C	8 Lead SOIC*
CA5260AT	-55°C to +125°C	8 Pin TO-5 Can
CA5260E	-55°C to +125°C	8 Lead Plastic DIP
CA5260M	-55°C to +125°C	8 Lead SOIC
CA5260M96	-55°C to +125°C	8 Lead SOIC*
CA5260T	-55°C to +125°C	8 Pin TO-5 Can

* Denotes Tape and Reel

Pinouts

CA5260 (PDIP, SOIC)
TOP VIEW

CA5260 (TO-5 STYLE CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1929.2**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V Terminals) 16V
Differential Input Voltage. 8V
Input Voltage. . . . . (V+ +8 V) to (V- -0.5 V)
Input Current. 1mA
Output Short Circuit Duration (Note 1) . . . . . Indefinite
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.). . . . . +300°C

Operating Conditions

Operating Temperature Range (All Types) . . . . . -55°C to +125°C
Storage Temperature Range (All Types) . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Typical Values Intended Only for Design Guidance, V+ = 5V, V- = 0V, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	TYPICAL VALUES		UNITS
			CA5260A	CA5260	
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I	f = 1MHz	4.3	4.3	pF
Unity Gain Crossover Frequency	f_T		3	3	MHz
Slew Rate	SR	V_{OUT} = 2.5V_{P-P}	5	5	V/µs
Transient Response		C_L = 25pF, R_L = 2kΩ (Voltage Follower)			
Rise Time	t_R		0.09	0.09	µs
Overshoot	OS		10	10	%
Settling Time (To <0.1%, V_{IN} = 4V_{P-P})	t_S	C_L = 25pF, R_L = 2kΩ (Voltage Follower)	1.8	1.8	µs

Electrical Specifications

T_A = +25°C, V+ = 5V, V- = 0V

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA3260A			CA5260			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_O = 2.5V	-	1.5	4	-	2	15	mV
Input Offset Current	I_{IO}	V_O = 2.5V	-	1	10	-	1	10	pA
Input Current	I_I	V_O = 2.5V	-	2	15	-	2	15	pA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 1V	80	85	-	70	85	-	dB
		V_{CM} = 0 to 2.5V	50	55	-	50	55	-	dB
Common Mode Input Voltage Range	V_{ICR}+		2.5	3	-	2.5	3	-	V
	V_{ICR}-		-	-0.5	0	-	-0.5	0	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 1V; ΔV- = 1V	75	84	-	70	84	-	dB
Large Signal Voltage Gain (Note 2)	A_{OL}	R_L = ∞, V_O = 0.5 to 4V	107	113	-	105	111	-	dB
		R_L = 10kΩ, V_O = 0.5 to 3.6V	83	86	-	80	86	-	dB
Source Current	I_{SOURCE}	V_O = 0V	1.75	2.2	-	1.75	2.2	-	mA
Sink Current	I_{SINK}	V_O = 5V	1.70	2	-	1.70	2	-	mA

Electrical Specifications T_A = +25°C, V+ = 5V, V- = 0V (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA3260A			CA5260			
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_{OM}+	R_L = ∞	4.99	5	-	4.99	5	-	V
	V_{OM}-		-	0	0.01	-	0	0.01	V
	V_{OM}+	R_L = 10kΩ	4.4	4.7	-	4.4	4.7	-	V
	V_{OM}-		-	0	0.01	-	0	0.01	V
	V_{OM}+	R_L = 2kΩ	3	3.4	-	3	3.4	-	V
	V_{OM}-		-	0	0.01	-	0	0.01	V
Supply Current	I_{SUPPLY}	V_O = 0V	-	1.60	2.0	-	1.60	2.0	mA
		V_O = 2.5V	-	1.80	2.25	-	1.80	2.25	mA

NOTES:
1. Short circuit may be applied to ground or to either supply.
2. For V+ = 4.5V and V- = GND; V_{OUT} = 0.5V to 3.2V at R_L = 10kΩ.

Electrical Specifications T_A = -55°C to +125°C, V+ = 5V, V- = 0V

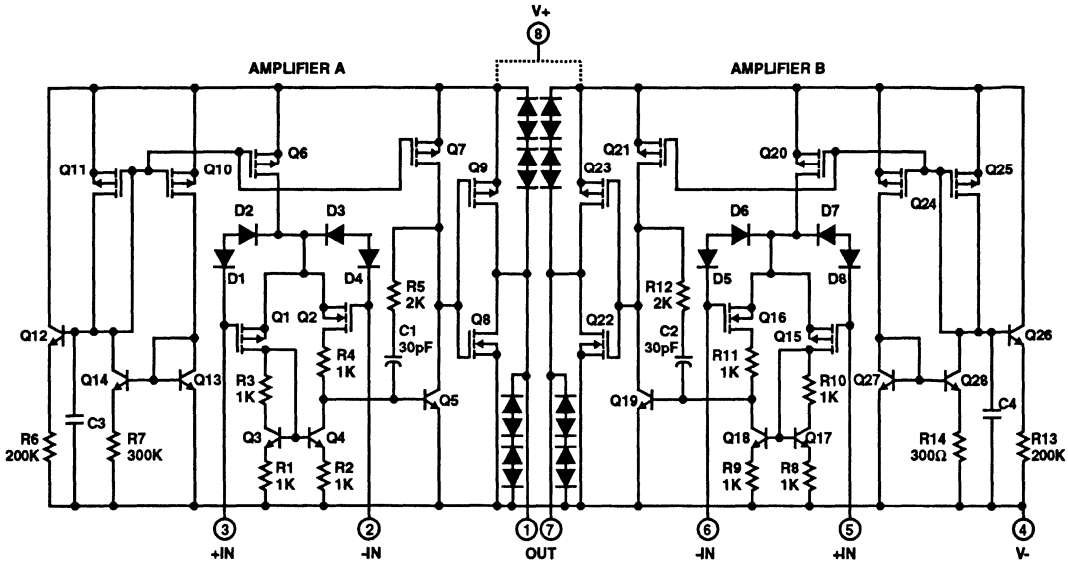
PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA3260A			CA5260			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_O = 2.5V	-	2	15	-	3	20	mV
Input Offset Current	I_{IO}	V_O = 2.5V	-	1	10	-	1	10	nA
Input Current	I_I	V_O = 2.5V	-	2	15	-	2	15	nA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 1V	65	78	-	60	78	-	dB
		V_{CM} = 0 to 2.5V	50	60	-	50	60	-	dB
Common Mode Input Voltage Range	V_{ICR}+		2.5	3	-	2.5	3	-	V
	V_{ICR}-		-	-0.5	0	-	-0.5	0	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 1V; ΔV- = 1V	62	65	-	60	65	-	dB
Large Signal Voltage Gain (Note 2)	A_{OL}	R_L = ∞, V_O = 0.5 to 4V	70	78	-	70	78	-	dB
		R_L = 10kΩ, V_O = 0.5 to 3.6V	60	65	-	60	65	-	dB
Source Current	I_{SOURCE}	V_O = 0V	1.3	1.6	-	1.3	1.6	-	mA
Sink Current	I_{SINK}	V_O = 5V	1.2	1.4	-	1.2	1.4	-	mA
Output Voltage	V_{OM}+	R_L = ∞	4.99	5	-	4.99	5	-	V
	V_{OM}-		-	0	0.01	-	0	0.01	V
	V_{OM}+	R_L = 10kΩ	4.2	4.4	-	4.2	4.4	-	V
	V_{OM}-		-	0	0.01	-	0	0.01	V
	V_{OM}+	R_L = 2kΩ	2.5	2.7	-	2.5	2.7	-	V
	V_{OM}-		-	0	0.01	-	0	0.01	V
Supply Current	I_{SUPPLY}	V_O = 0V	-	1.65	2.2	-	1.65	2.2	mA
		V_O = 2.5V	-	1.95	2.35	-	1.95	2.35	mA

NOTES:
1. Short circuit may be applied to ground or to either supply.
2. For V+ = 4.5V and V- = GND; V_{OUT} = 0.5V to 3.2V at R_L = 10kΩ.

Electrical Specifications Each Amplifier at T_A = 25°C, V+ = 15V, V- = 0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA3260A			CA5260			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V± = ±7.5	-	2	5	-	6	15	mV
Input Offset Current	I_{IO}	V± = ±7.5	-	0.5	20	-	0.5	30	pA
Input Current	I_I	V± = ±7.5	-	5	30	-	5	50	pA
Large Signal Voltage Gain	A_{OL}	V_O = $10V_{P-P}$, R_L = 10kΩ	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common Mode Rejection Ratio	CMRR		80	95	-	70	90	-	dB
Common Mode Input Voltage Range	V_{ICR}		10	-0.5 to 12	0	10	-0.5 to 12	0	V
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V\pm$	PSRR	V± = ±7.5	-	32	150	-	32	320	µV/V
Maximum Output Voltage	V_{OM}+	R_L = 10kΩ	11	13.3	-	11	13.3	-	V
	V_{OM}-		-	0.002	0.01	-	0.002	0.01	V
	V_{OM}+	R_L = ∞	14.99	15	-	14.99	15	-	V
	V_{OM}-		-	0	0.01	-	0	0.01	V
Maximum Output Current	I_{OM}+ (Source)	V_O = 7.5V	12	22	45	12	22	45	mA
	I_{OM}- (Sink)		12	20	45	12	20	45	mA
Total Supply Current, R_L = ∞	I+	V_O (Amp A) = 7.5V V_O (Amp B) = 7.5V	-	9	16.5	-	9	16.5	mA
		V_O (Amp A) = 0V V_O (Amp B) = 0V	-	1.2	4	-	1.2	4	mA
		V_O (Amp A) = 0V V_O (Amp B) = 7.5V	-	5	9.5	-	5	9.5	mA
Input Offset Voltage Temp. Drift	$\Delta V_{IO}/\Delta T$		-	6	-	-	8	-	µV/°C
Crosstalk		f = 1kHz	-	120	-	-	120	-	dB

Schematic Diagram



HARRIS SEMICONDUCTOR

CA5420

Low Supply Voltage, Low Input Current BiMOS Operational Amplifier

March 1993

Features

- CA5420A, CA5420 at 5V Supply Voltage with Full Military Temperature Range Guaranteed Specifications
- CA5420A, CA5420 Guaranteed to Operate from ±1V to ±10V Supplies
- 2V Supply at 300μA Supply Current
- 1pA (Typ.) Input Current (Essentially Constant to 85 °C)
- Rail-to-Rail Output Swing (Drive ±2mA into 1kΩ Load)
- Pin Compatible with 741 Op Amp

Applications

- pH Probe Amplifiers
- Picoammeters
- Electrometer (High Z) Instruments
- Portable Equipment
- Inaccessible Field Equipment
- Battery Dependent Equipment (Medical and Military)
- 5V Logic Systems
- Microprocessor Interface

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA5420AE	-55°C to +125°C	8 Lead Plastic DIP
CA5420AM	-55°C to +125°C	8 Lead SOIC
CA5420AT	-55°C to +125°C	8 Pin Can
CA5420E	-55°C to +125°C	8 Lead Plastic DIP
CA5420M	-55°C to +125°C	8 Lead SOIC
CA5420T	-55°C to +125°C	8 Pin Can

Description

The CA5420A and CA5420* are integrated circuit operational amplifiers that combine PMOS transistors and bipolar transistors on a single monolithic chip. They are designed and guaranteed to operate in microprocessor logic systems that use V+ = 5V, V- = Gnd, since they can operate down to ±1V supplies. They will also be suitable for 3.3V logic systems.

The CA5420A and CA5420 BiMOS operational amplifiers feature gate-protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 1pA). The internal bootstrapping network features a unique guardbanding technique for reducing the doubling of leakage current for every 10°C increase in temperature. The CA5420 series operates at total supply voltages from 2V to 20V either single or dual supply. These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Additionally, they have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.45V below the negative supply terminal, an important attribute for single supply application. The output stage uses a feedback OTA type amplifier that can swing essentially from rail-to-rail. The output driving current of 1.0mA (min) is provided by using nonlinear current mirrors.

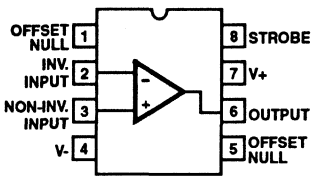
These devices have guaranteed specifications for 5V operation over the full military temperature range of -55°C to +125°C.

The CA5420 series has the same 8 lead pinout used for the industry standard 741.

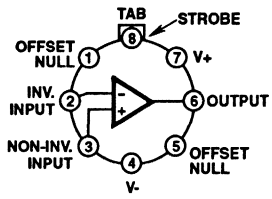
* Formerly Dev. Type No. TA1 0841

Pinouts

CA5420
(PDIP, SOIC)
TOP VIEW



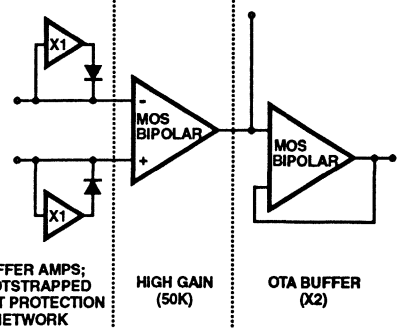
CA5420
(TO-5 CAN)
TOP VIEW



NOTE: Pin 4 is connected to Case.

Functional Diagram

CA5420



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1925.2

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 22V
Differential Input Voltage 15V
Input Voltage . . . . . (V+ + 8V) to (V- -0.5V)
Input Current 1mA
Output Short Circuit Duration (Note 1) . . . . . Indefinite
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Operating Temperature Range (All Types) . . . . . -55°C to +125°C
Storage Temperature Range (All Types) . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Typical Values Intended Only for Design Guidance. V+ = +5V; V- = Gnd, T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS		CA5420A	CA5420	UNITS
Input Resistance	R_I			150	150	TΩ
Input Capacitance	C_I			4.9	4.9	pF
Output Resistance	R_O			300	300	Ω
Equivalent Input Noise Voltage	e_N	f = 1kHz	R_S = 100Ω	62	62	$nV/\sqrt{Hz}$
		f = 10kHz		38	38	$nV/\sqrt{Hz}$
Short-Circuit Current Source	$I_{OM}+$			2.6	2.6	mA
To Opposite Supply Sink	$I_{OM}-$			2.4	2.4	mA
Gain Bandwidth Product	f_T			0.5	0.5	MHz
Slew Rate	SR			0.5	0.5	V/μs
Transient Response Rise Time	t_R	R_L = 2kΩ, C_L = 100pF		0.7	0.7	μs
Overshoot	OS			15	15	%
Current from Terminal 8 To V-	I_8+			20	20	μA
Current from Terminal 8 To V+	I_8-			2	2	mA
Settling Time	0.01%	A_V = 1	$2V_{P-P}$ Input	8	8	μs
	0.10%	A_V = 1	$2V_{P-P}$ Input	4.5	4.5	μs

NOTE:

1. Short circuit may be applied to ground or to either supply.

Electrical Specifications T_A = +25°C, V+ = 5V, V- = 0, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA5420A			CA5420			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_O = 2.5V	-	1	5	-	1.5	10	mV
Input Offset Current	I_{IO}	V_O = 2.5V	-	0.02	0.5	-	0.02	1	pA
Input Current	I_I	V_O = 2.5V	-	0.02	1	-	0.02	2	pA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 3.7V, V_O = 2.5V	75	83	-	70	80	-	dB
Common Mode Input Voltage Range	V_{ICR} +	V_O = 2.5V	3.7	4	-	3.7	4	-	V
	V_{ICR} -		-	-0.3	0	-	-0.3	0	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 1V; ΔV- = 1V	75	83	-	70	80	-	dB
Large Signal Voltage Gain	A_{OL}								
V_O = 0.5 to 4V		R_L = ∞	85	87	-	85	87	-	dB
V_O = 0.5 to 4V		R_L = 10kΩ	85	87	-	85	87	-	dB
V_O = 0.7 to 3V		R_L = 2kΩ	80	85	-	80	85	-	dB
Source Current	I_{SOURCE}	V_O = 0V	1.2	2.7	-	1.2	2.7	-	mA
Sink Current	I_{SINK}	V_O = 5V	1.2	2.1	-	1.2	2.1	-	mA
Output Voltage	V_{OM} +	R_L = ∞	4.9	4.94	-	4.9	4.94	-	V
	V_{OM} -		-	0.13	0.15	-	0.13	0.15	V
	V_{OM} +	R_L = 10kΩ	4.7	4.9	-	4.7	4.9	-	V
	V_{OM} -		-	0.12	0.15	-	0.12	0.15	V
	V_{OM} +	R_L = 2kΩ	3.5	4.6	-	3.5	4.6	-	V
	V_{OM} -		-	0.1	0.15	-	0.1	0.15	V
Supply Current	I_{SUPPLY}	V_O = 0V	-	400	500	-	400	500	μA
		V_O = 2.5V		430	550	-	430	550	μA

Electrical Specifications T_A = -55°C to +125°C, V+ = 5V, V- = 0, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA5420A			CA5420			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_O = 2.5V	-	2	10	-	3	15	mV
Input Offset Current	I_{IO}	V_O = 2.5V	-	1.5	3	-	1.5	3	nA
Up to T_A = 85°C	I_{IO}		-	2	10	-	2	10	pA
Input Current	$\|I_I\|$	V_O = 2.5V	-	2	5	-	2	5	nA
Up to T_A = 85°C	$\|I_I\|$		-	10	15	-	15	25	pA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 3.7V, V_O = 2.5V	70	80	-	65	75	-	dB
Common Mode Input Voltage Range	V_{ICR} +	V_O = 2.5V	3.7	4	-	3.7	4	-	V
	V_{ICR} -		-	-0.3	0	-	-0.3	0	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 1V; ΔV- = 1V	70	83	-	65	80	-	dB
Large Signal Voltage Gain	A_{OL}								
V_O = 0.5 to 4V		R_L = ∞	85	87	-	80	85	-	dB
V_O = 0.7 to 4V		R_L = 10kΩ	80	87	-	80	85	-	dB
V_O = 0.7 to 2.5V		R_L = 2kΩ	75	80	-	75	80	-	dB
Source Current	I_{SOURCE}	V_O = 0V	1	2.7	-	1	2.7	-	mA
Sink Current	I_{SINK}	V_O = 5V	1	2.1	-	1	2.1	-	mA
Output Voltage	V_{OM} +	R_L = ∞	4.8	4.9	-	4.8	4.9	-	V
	V_{OM} -		-	0.16	0.2	-	0.16	0.2	V
	V_{OM} +	R_L = 10kΩ	4.7	4.9	-	4.7	4.9	-	V
	V_{OM} -		-	0.15	0.2	-	0.15	0.20	V
	V_{OM} +	R_L = 2kΩ	3	4	-	3	4	-	V
	V_{OM} -		-	0.14	0.2	-	0.14	0.2	V
Supply Current	I_{SUPPLY}	V_O = 0V	-	430	550	-	430	550	µA
		V_O = 2.5V		480	600	-	480	600	µA

Specifications CA5420, CA5420A

Electrical Specifications For Equipment Design at V+ = 1V, V- = -1V, T_A = 25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA5420A			CA5420			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}		-	2	5	-	5	10	mV
Input Offset Current	$\|I_{IO}\|$		-	0.01	4 (Note 1)	-	0.01	4 (Note 1)	pA
Input Current	$\|I_I\|$		-	0.02	5 (Note 1)	-	0.02	5 (Note 1)	pA
Large Signal Voltage Gain	A_{OL}	R_L = 10kΩ	20	100	-	10	100	-	kV/V
			86	100	-	80	100	-	dB
Common Mode Rejection Ratio	CMRR		-	560	1000	-	560	1800	µV/V
			60	65	-	55	65	-	dB
Common Mode Input Voltage Range	V_{ICR} +		0.2	0.5	-	0.2	0.5	-	V
	V_{ICR} -		-1	-1.3	-	-	-1.3	-	V
Power Supply Rejection Ratio	PSRR		-	32	320	-	100	1000	µV/V
			70	90	-	60	80	-	dB
Maximum Output Voltage	V_{OM} +	R_L = ∞	0.9	0.95	-	0.9	0.95	-	V
	V_{OM} -		-0.85	-0.91	-	-0.85	-0.91	-	V
Supply Current	I_{SUPPLY}		-	350	650	-	350	650	µA
Device Dissipation	P_D		-	0.7	1.1	-	0.7	1.1	mW
Input Offset Voltage Temp. Drift	$\Delta V_{IO}/\Delta T$		-	4	-	-	4	-	µV/°C

Electrical Specifications For Equipment Design at V+ = 10V, V- = -10V, T_A = 25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA5420A			CA5420			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}		-	2	5	-	5	10	mV
Input Offset Current	$\|I_{IO}\|$		-	0.03	4 (Note 1)	-	0.03	4 (Note 1)	pA
Input Current	$\|I_I\|$		-	0.05	5 (Note 1)	-	0.05	5 (Note 1)	pA
Large Signal Voltage Gain	A_{OL}	R_L = 10kΩ	20	100	-	10	100	-	kV/V
			86	100	-	80	100	-	dB
Common Mode Rejection Ratio	CMRR		-	100	320	-	100	320	µV/V
			70	80	-	70	80	-	dB
Common Mode Input Voltage Range	V_{ICR} +		9	9.3	-	8.5	9.3	-	V
	V_{ICR} -		-10	-10.3	-	-10	-10.3	-	V
Power Supply Rejection Ratio	PSRR		-	32	320	-	32	320	µV/V
			70	90	-	70	90	-	dB
Maximum Output Voltage	V_{OM} +	R_L = ∞	9.7	9.9	-	9.7	9.9	-	V
	V_{OM} -		-9.7	-9.85	-	-9.7	-9.85	-	V
Supply Current	I_{SUPPLY}		-	450	1000	-	450	1000	µA
Device Dissipation	P_D		-	9	14	-	9	14	mW
Input Offset Voltage Temp. Drift	$\Delta V_{IO}/\Delta T$		-	4	-	-	4	-	µV/°C

NOTE:

1. The maximum limit represents the levels obtainable on high-speed automatic test equipment. Typical values are obtained under laboratory conditions.

Typical Performance Curves

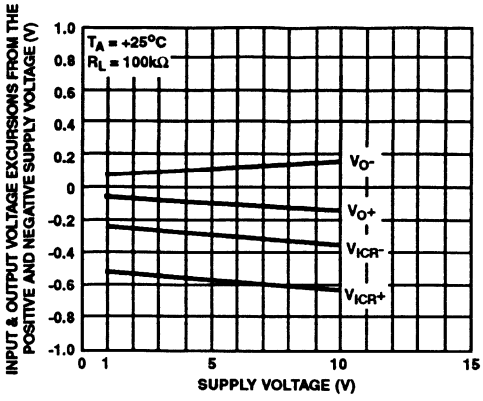


FIGURE 1. OUTPUT VOLTAGE SWING AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

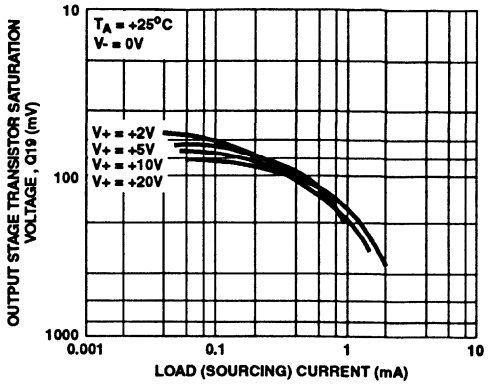


FIGURE 2. OUTPUT VOLTAGE vs LOAD SOURCING CURRENT

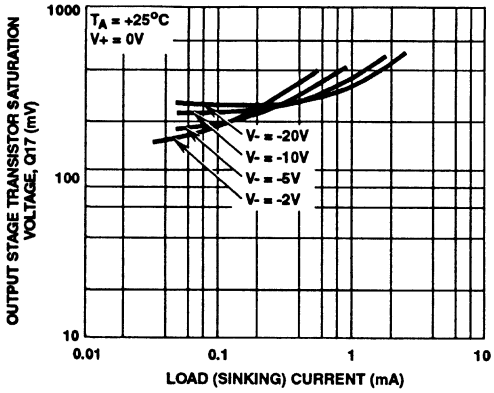


FIGURE 3. OUTPUT VOLTAGE vs LOAD SINKING CURRENT

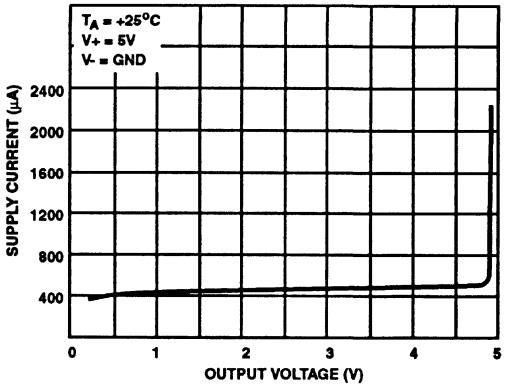


FIGURE 4. SUPPLY CURRENT vs OUTPUT VOLTAGE

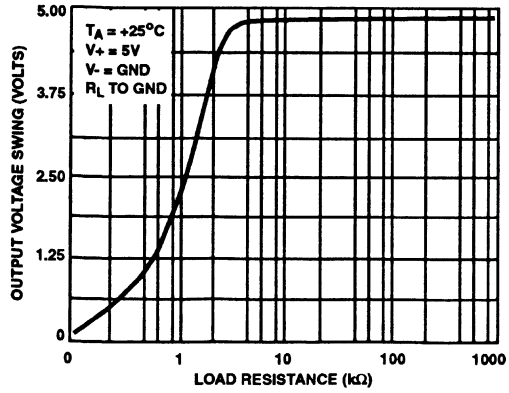


FIGURE 5. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

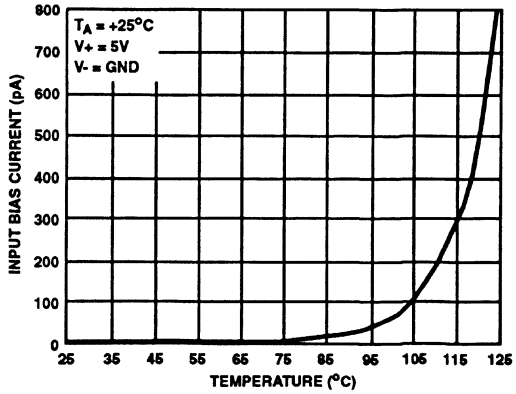


FIGURE 6. INPUT BIAS CURRENT DRIFT ($\Delta I_B/\Delta T$)

Typical Performance Curves (Continued)

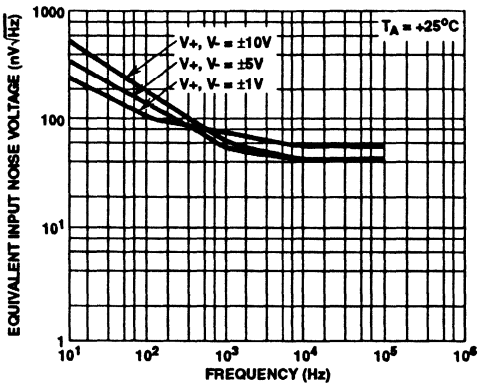


FIGURE 7. INPUT NOISE VOLTAGE vs FREQUENCY

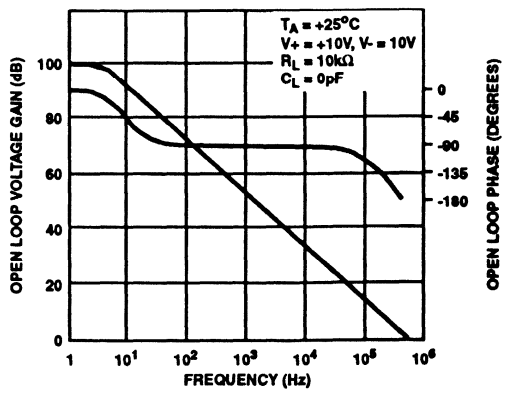


FIGURE 8. OPEN LOOP GAIN AND PHASE SHIFT RESPONSE

Application Circuits

Picoammeter Circuit

The exceptionally low input current (typically 0.2pA) makes the CA5420 highly suited for use in a picoammeter circuit. With only a single 10GΩ resistor, this circuit covers the range from ±1.5pA. Higher current ranges are possible with suitable switching techniques and current scaling resistors. Input transient protection is provided by the 1MΩ resistor in series with the input. Higher current ranges require that this resistor be reduced. The 10MΩ resistor connected to pin 2 of the CA5420 decouples the potentially high input capacitance often associated with lower current circuits and reduces the tendency for the circuit to oscillate under these conditions.

High Input Resistance Voltmeter

Advantage is taken of the high input impedance of the CA5420 in a high input resistance DC voltmeter. Only two 1.5V "AA" type penlite batteries power this exceedingly high-input resistance (>1,000,000MΩ) DC voltmeter. Full-scale deflection is ±500mV, ±150mV, and ±15mV. Higher voltage ranges are easily added with external input voltage attenuator networks.

The meter is placed in series with the gain network, thus eliminating the meter temperature coefficient error term.

Supply current in the standby position with the meter undeflected is 300μA. At full-scale deflection this current rises to 800μA. Carbon-zinc battery life should be in excess of 1,000 hours.

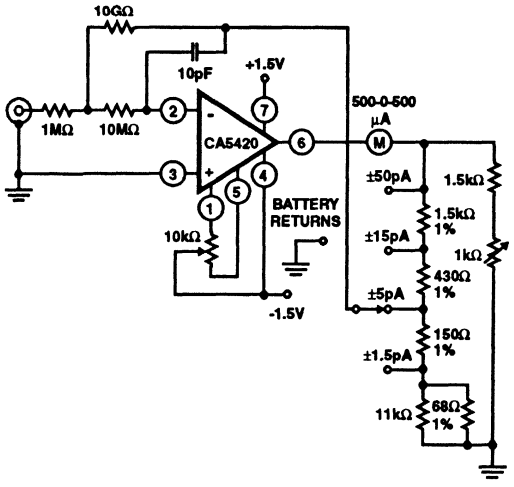


FIGURE 6. PICOAMMETER CIRCUIT

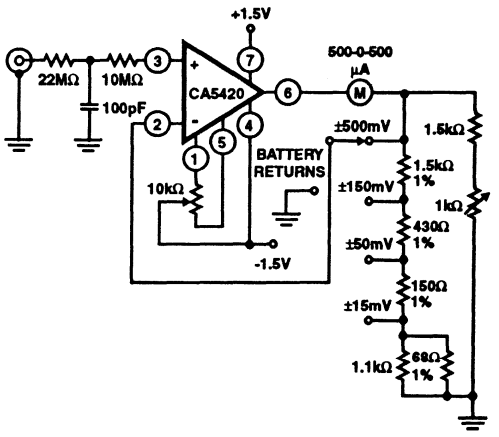


FIGURE 7. HIGH INPUT RESISTANCE VOLTMETER

HARRIS SEMICONDUCTOR

CA5470

Quad Microprocessor BiMOS-E Operational Amplifiers with MOSFET Input/Bipolar Output

March 1993

Features

- High Speed CMOS Input Stage Provides
  - Very High ZI .....5TΩ (5 x 10^{12}Ω) Typ.
  - Very Low I_I..... 0.5pA (Typ) at 5V Operation
  - Very Low I_{IO}..... 0.5pA (Typ) at 5V Operation
- ESD Protection to 2000V
- 3V to 16V Power Supply Operation
- Fully Guaranteed Specifications Over Full Military Range
- Wide BW (14MHz); High SR (5V/μs) at 5V Supply
- Wide V_{ICR} Range From -0.5V to 3.7V (Typ) at 5V Supply
- Ideally Suited for CMOS and HCMOS Applications

Applications

- Bar Code Readers
- Photodiode Amplifiers (IR)
- Microprocessor Buffering
- Ground Reference Single Supply Amplifiers
- Fast Sample and Hold
- Timers
- Voltage Controlled Oscillators
- Voltage Followers
- V to I Converters
- Peak Detectors
- Precision Rectifiers
- 5V Logic Systems
- 3V Logic Systems

Description

The CA5470 series are integrated circuit operational amplifiers that combine the advantages of both high speed CMOS and bipolar transistors on a single monolithic chip. They are constructed in the BiMOS-E process which adds drain-extension implants to 3μm polygate CMOS, enhancing both the voltage capability and providing vertical bipolar transistors for broadband analog/digital functions. This process lends itself easily to high speed operational amplifiers, comparators, analog switches and interface peripherals, resulting in twice the speed of the conventional CMOS transistors having similar feature size.

BiMOS-E are broadbased bipolar transistors that have high transconductance, gains more constant with current level, stable "precision" base-emitter offset voltages and superior drive capability. Excellent interface with environmental potentials enable use in 5V logic systems and future 3.3V logic systems.

ESD capability exceeds the standard 2000V level. The CA5470 series can operate with single supply voltages from 3V to 16V or ±1.5V to ±8V. They have guaranteed specifications at both 5V and ±7.5V at room temperature as well as over the full -55°C to +125°C military range.

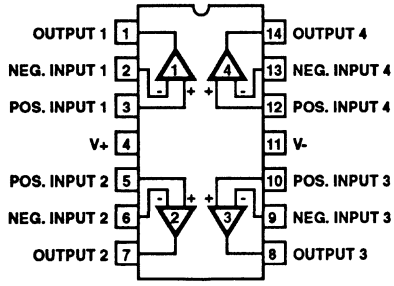
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA5470E	-55°C to +125°C	14 Lead Plastic DIP
CA5470M	-55°C to +125°C	14 Lead SOIC
CA5470M96	-55°C to +125°C	14 Lead SOIC*

* Denotes Tape and Reel

Pinout

CA5470 (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1946.2**

Absolute Maximum Ratings

DC Supply Voltage (Between V^+ And V^- Terminals) 16V
Differential Input Voltage 8V
Input Voltage ..... (V^+ +8 V) to (V^- -0.5V)
Input Current 1mA
Power Dissipation:
  Without Heat Sink
    Up To +55°C 630mW
    Above +55°C ..... Derate Linearly 6.67 mW/°C
  With Heat Sink
    Up To +90°C 1W
    Above +90°C ..... Derate Linearly 16.7 mW/°C
  Small Outline Package
    Up To +65°C 500mW
    Above +65°C ..... Derate Linearly 5.9 mW/°C
Output Short Circuit Duration (Note 1) ..... Indefinite
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec) ..... +300°C

Operating Conditions

Operating Temperature Range (All Types) ..... -55°C to +125°C
Storage Temperature Range (All Types) ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications Typical Values Intended Only for Design Guidance. V+ = 5V, V- = 0V, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
Input Resistance	R_I		5	TΩ
Input Capacitance	C_I	f = 1MHz	3.1	pF
Unity Gain Crossover Frequency	f_T		14	MHz
Slew Rate	SR	V_{OUT} = 3.65V_{P-P}	5	V/µs
Transient Response:		C_L = 25pF, R_L= 2kΩ (Voltage Follower)		
Rise Time/Fall Time	t_R		27/25	ns
Overshoot	OS		20	%
Settling Time (To <0.1%, V_{IN} = 4V_{P-P})	t_S	C_L = 25pF, R_L= 2kΩ (Voltage Follower)	1	µs
Full Power BW (V_{OUT} = 3.65V_{P-P}) SR = 5V/µs	FPBW	A_V = 1	436	kHz

Electrical Specifications T_A = +25°C, V+ = 5V, V- = GND

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Offset Voltage	$\|V_{IO}\|$		-	6	22	mV
Input Offset Current	$\|I_{IO}\|$		-	0.5	50 (Note 2)	pA
Input Current	I_I		-	0.5	50 (Note 2)	pA
Common Mode Input Range	V_{ICR}		3.5	-0.5 to 3.7	0	V
Common Mode Rejection Ratio	CMRR	V_{ICR} = 0 to 3.5V	55	70	-	dB
Power Supply Rejection Ratio	PSRR	ΔV = 2V	60	75	-	dB
Positive Output Voltage Swing	V_{OM}+	R_L = 2kΩ to GND	4	4.4	-	V
Negative Output Voltage Swing	V_{OM}-	R_L = 2kΩ to GND	-	0.06	0.10	V
Total Supply Current	I_{SUPPLY}	V_{OUT} = 2.5V, R_L = ∞	-	6	7	mA
Unity Gain Bandwidth Product	f_T		10	14	-	MHz
Slew Rate	SR		4	5	-	V/µs
Output Current						
Source to opposite supply	I_{SOURCE}		4	5.5	-	mA
Sink to opposite supply	I_{SINK}		1.0	1.2	-	mA
Open Loop Gain	A_{OL}	0.5V to 3.5V, R_L = 10kΩ	80	90	-	dB

NOTE:
1. Short circuit may be applied to ground or to either supply.
2. This is the lowest value that can be tested reliably. Almost all devices will be <10pA.

Electrical Specifications T_A = -55°C to +125°C, V+ = 5V, V- = GND

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Offset Voltage	$\|V_{IO}\|$		-	6	25	mV
Input Offset Current	$\|I_{IO}\|$		-	550	5500	pA
Input Current	I_I		-	550	11000	pA
Common Mode Input Range	V_{ICR}		3.5	-0.5 to 3.7	0	V
Common Mode Rejection Ratio	CMRR	V_{ICR} = 0 to 3.5V	50	65	-	dB
Power Supply Rejection Ratio	PSRR	ΔV = 2V	58	75	-	dB
Positive Output Voltage Swing	V_{OM}+	R_L = 2kΩ to GND	3.8	4.2	-	V
Negative Output Voltage Swing	V_{OM}-	R_L = 2kΩ to GND	-	0.08	0.11	V
Total Supply Current	I_{SUPPLY}	V_{OUT} = 2.5V	-	9	11	mA
Unity Gain Bandwidth Product	f_T		8	12	-	MHz
Slew Rate	SR		3	5	-	V/μs
Output Current						
Source to opposite supply	I_{SOURCE}		4	5.5	-	mA
Sink to opposite supply	I_{SINK}		0.8	1.2	-	mA
Open Loop Gain	A_{OL}	0.5V to 3.5V, R_L = 10kΩ	80	90	-	dB

Electrical Specifications T_A = +25°C, V+ = 7.5V, V- = -7.5

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Offset Voltage	$\|V_{IO}\|$		-	5	25	mV
Input Offset Current	$\|I_{IO}\|$		-	0.5	50 (Note 1)	pA
Input Current	I_I		-	1	50 (Note 1)	pA
Common Mode Input Range	V_{ICR}		5.8	-7.8 to 6.0	-7.5	V
Common Mode Rejection Ratio	CMRR	V_{ICR} = 0 to 13.3V	60	70	-	dB
Power Supply Rejection Ratio	PSRR	ΔV = 1V	60	76	-	dB
Positive Output Voltage Swing	V_{OM}+					
		R_L = 2kΩ to GND	6.3	6.5	-	V
		R_L = 10kΩ to GND	6.4	6.6	-	V
Negative Output Voltage Swing	V_{OM}-					
		R_L = 2kΩ to GND	-	-2.6	-2	V
		R_L = 10kΩ to GND	-	-7.3	-7.1	V
Total Supply Current	I_{SUPPLY}	V_{OUT} = GND, R_L = ∞	-	10	12	mA
Unity Gain Bandwidth Product	f_T		12	16	-	MHz
Slew Rate	SR		4	7	-	V/μs
Output Current						
Source to opposite supply	I_{SOURCE}		6.2	6.8	-	mA
Sink to opposite supply	I_{SINK}		1	1.4	-	mA
Open Loop Gain	A_{OL}	-5V to +5V, R_L = 10kΩ	80	90	-	dB

NOTE:

1. This is the lowest value that can be tested reliably. Almost all devices will be <10pA.

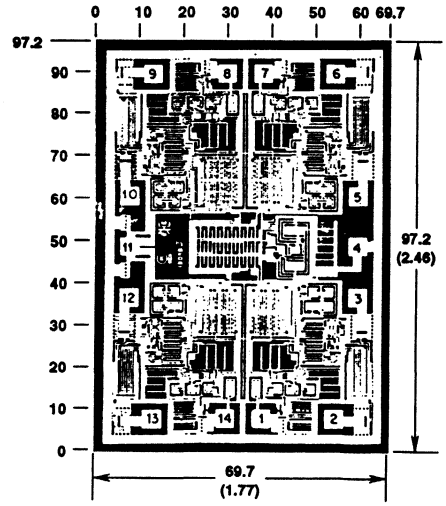
Electrical Specifications T_A = -55°C to +125°C, V+ = 7.5V, V- = -7.5

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Offset Voltage	$\|V_{IO}\|$		-	5	30	mV
Input Offset Current	$\|I_{IO}\|$		-	550	5500	pA
Input Current	I_I		-	1100	11000	pA
Common Mode Input Range	V_{ICR}		5.8	-7.8 to 6.0	-7.5	V
Common Mode Rejection Ratio	CMRR	V_{ICR} = 0 to 3.5V	58	70	-	dB
Power Supply Rejection Ratio	PSRR	ΔV = 1V	60	76	-	dB
Positive Output Voltage Swing	V_{OM}+					
		R_L = 2kΩ to GND	4.75	5.5	-	V
		R_L = 10kΩ to GND	6.1	6.4	-	V
Negative Output Voltage Swing	V_{OM}-					
		R_L = 2kΩ to GND	-	-2.6	-2	V
		R_L = 10kΩ to GND	-	-7.3	-7.1	V
Total Supply Current	I_{SUPPLY}	V_{OUT} = GND, R_L = ∞	-	12	18	mA
Unity Gain Bandwidth Product	f_T		10	15	-	MHz
Slew Rate	SR		3	7	-	V/μs
Output Current						
Source to opposite supply	I_{SOURCE}		6.2	6.8	-	mA
Sink to opposite supply	I_{SINK}		1	1.4	-	mA
Open Loop Gain	A_{OL}	-5V to +5V, R_L = 10kΩ	80	90	-	dB

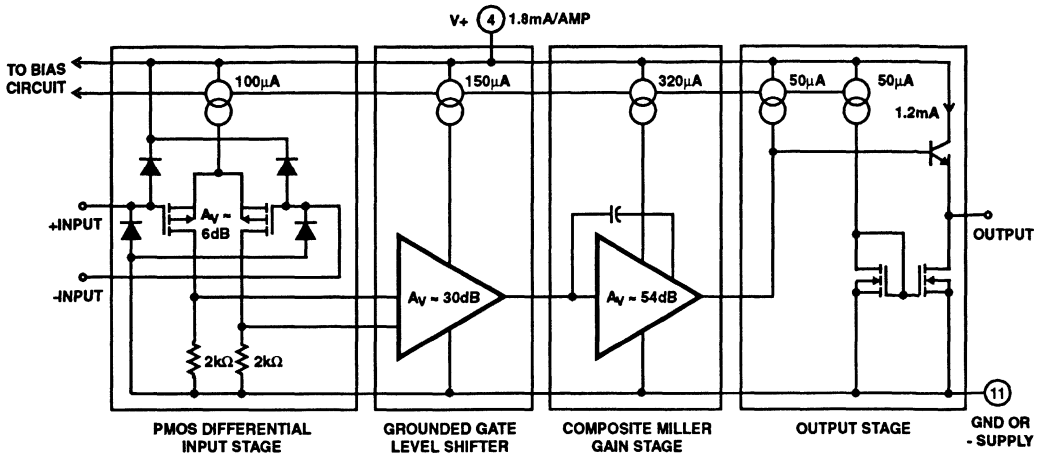
Metallization Mask Layout

Dimensions in parentheses are in millimeters and derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.



Block Diagram ($^1/_4$ of CA5470)



Typical Performance Curve

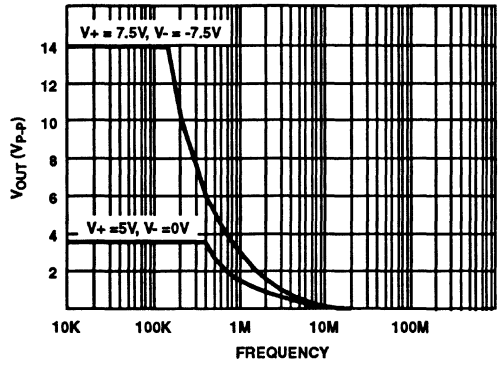


FIGURE 1. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

HA-2400, HA-2404 HA-2405

PRAM Four Channel Programmable Amplifiers

March 1993

Features

- Programmability
- High Rate Slew 30V/µs
- Wide Gain Bandwidth 40MHz
- High Gain 150kV/V
- Low Offset Current 5nA
- High Input Impedance 30MΩ
- Single Capacitor Compensation
- DTL/TTL Compatible Inputs

Applications

- Thousands of Applications; Program
  - Signal Selection/Multiplexing
  - Operational Amplifier Gain
  - Oscillator Frequency
  - Filter Characteristics
  - Add-Subtract Functions
  - Integrator Characteristics
  - Comparator Levels
- For Further Design Ideas, See App. Note 514.

Description

HA-2400/04/05 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

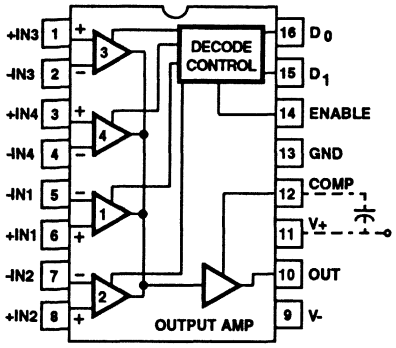
Each channel of the HA-2400/04/05 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing signal selection and mathematical function designs. With 30V/µs slew rate, 40MHz gain bandwidth and 30MΩ input impedance these devices are ideal building blocks for signal generators, active filters and data acquisition designs. Programmability, coupled with 4mV typical offset voltage and 5nA offset current, makes these amplifiers outstanding components for signal conditioning circuits.

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HA1-2400-2	-55°C to +125°C	16 Lead Ceramic DIP
HA1-2404-4	-25°C to +85°C	16 Lead Ceramic DIP
HA1-2405-5	0°C to +75°C	16 Lead Ceramic DIP
HA3-2405-5	0°C to +75°C	16 Lead Plastic DIP
HA4P2405-5	0°C to +75°C	20 Lead PLCC

Pinouts

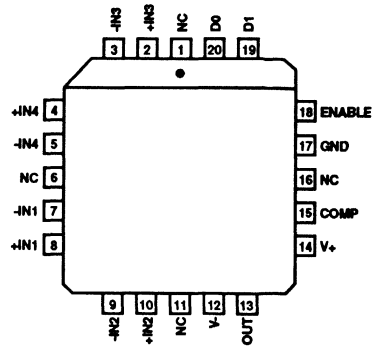
HA-2400/04 (CDIP)
HA-2405 (CDIP, PDIP)
TOP VIEW



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	None

HA-2405 (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2891.1**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 45.0V
Differential Input Voltage. . . . . V_{SUPPLY}
Digital Input Voltage . . . . . -0.76V to +10.0V
Output Current . . . . . Short Circuit Protected, I_{SC} <±33mA)
Internal Power Dissipation (Note 13)
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Operating Temperature Range
HA-2400-2 . . . . . -55°C ≤ T_A ≤ +125°C
HA-2404-4 . . . . . -25°C ≤ T_A ≤ +85°C
HA-2405-5 . . . . . 0°C ≤ T_A ≤ +75°C
Storage Temperature Range . . . . . -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions: V_{SUPPLY} = ±15V, Unless Otherwise Specified. Digital Inputs: V_{IL} = +0.5V, V_{IH} = +2.4. Limits apply to each of the four channels, when addressed.

PARAMETER	TEMP	HA-2400/04 LIMITS			HA-2405 LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	4	9	-	4	9	mV
	Full	-	-	11	-	-	11	mV
Bias Current (Note 12)	+25°C	-	50	200	-	50	250	nA
	Full	-	-	400	-	-	500	nA
Offset Current (Note12)	+25°C	-	5	50	-	5	50	nA
	Full	-	-	100	-	-	100	nA
Input Resistance (Note 12)	+25°C	-	30	-	-	30	-	MΩ
Common Mode Range	Full	±9.0	-	-	±9.0	-	-	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 1, 5)	+25°C	50	150	-	50	150	-	kV/V
	Full	25	-	-	25	-	-	kV/V
Common Mode Rejection Ratio (Note 2)	Full	80	100	-	74	100	-	dB
Gain Bandwidth (Notes 3, 14)	+25°C	20	40	-	20	40	-	MHz
Gain Bandwidth (Notes 4, 14)	+25°C	4	8	-	4	8	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0	-	±10.0	±12.0	-	V
Output Current	+25°C	10	20	-	10	20	-	mA
Full Power Bandwidth (Notes 3, 5, 15)	+25°C	640	950	-	640	950	-	kHz
Full Power Bandwidth (Notes 4, 5, 15)	+25°C	200	250	-	200	250	-	kHz
TRANSIENT RESPONSE (Note 16)								
Rise Time (Notes 4, 6)	+25°C	-	20	45	-	20	50	ns
Overshoot (Notes 4, 6)	+25°C	-	25	40	-	25	40	%
Slew Rate (Notes 3, 7)	+25°C	20	30	-	20	30	-	V/µs
Slew Rate (Notes 4, 7,14)	+25°C	6	8	-	6	8	-	V/µs
Settling Time (Notes 4, 7, 8, 14)	+25°C	-	1.5	2.5	-	1.5	2.5	µs
CHANNEL SELECT CHARACTERISTICS								
Digital Input Current (V_{IN} = 0V)	Full	-	1	1.5	-	1	1.5	mA
Digital Input Current (V_{IN} = +5.0V)	Full	-	5	-	-	5	-	nA
Output Delay (Notes 9, 14)	+25°C	-	100	250	-	100	250	ns
Crosstalk (Note 10)	+25°C	-80	-110	-	-74	-110	-	dB

Electrical Specifications Test Conditions: V_{SUPPLY} = ±15V, Unless Otherwise Specified. Digital Inputs: V_{IL} = +0.5V, V_{IH} = +2.4. Limits apply to each of the four channels, when addressed. **(Continued)**

PARAMETER	TEMP	HA-2400/04 LIMITS			HA-2405 LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	4.8	6.0	-	4.8	6.0	mA
Power Supply Rejection Ratio (Note 11)	Full	74	90	-	74	90	-	dB

NOTES:

1. R_L = 2kΩ
2. V_{CM} = ±5VDC
3. A_V = +10, C_{COMP} = 0, R_L = 2kΩ, C_L = 50pF.
4. A_V = +1, C_{COMP} = 15pF, R_L = 2kΩ, C_L = 50pF.
5. V_{OUT} = 20V peak to peak.
6. V_{OUT} = 200mV peak.
7. V_{OUT} = 10.0V peak to peak.
8. To 0.1% of final value.
9. To 10% of final value; output then slews at normal rate to final value
10. Unselected input to output; V_{IN} = ±10VDC
11. V_{SUPPLY} = ±10VDC to ±20VDC
12. Unselected channels have approximately the same input parameters.
13. Maximum power dissipation including output load, must be designed to maintain the junction temperature below +175°C for the ceramic package, and below +150°C for the plastic packages.
14. Guaranteed by design.
15. Full Power Bandwidth based on slew rate measurement using: $FPBW = \frac{SR}{2\pi V_{PEAK}}$; V_{PEAK} = 5V
16. See Figure 11 for test circuit.

Schematic Diagram

HA-2400

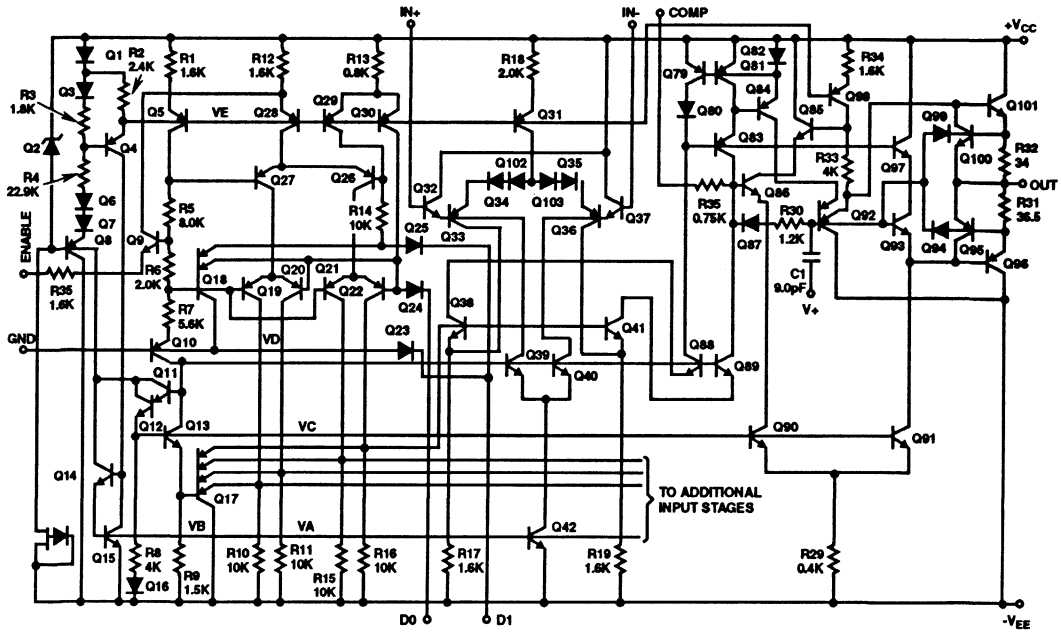


Diagram Includes: One Input Stage, Decode Control, Bias Network, and Output Stage

Typical Performance Curves

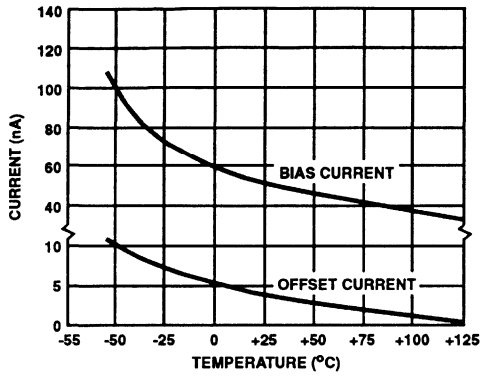


FIGURE 1. INPUT BIAS CURRENT AND OFFSET CURRENT vs TEMPERATURE

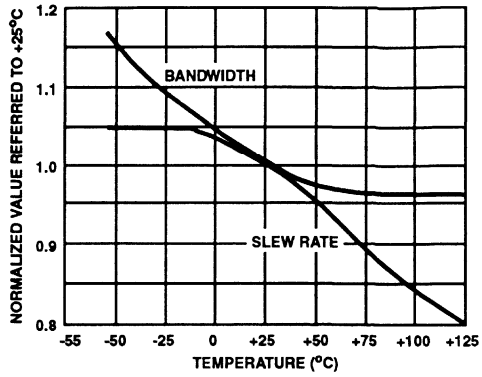


FIGURE 2. NORMALIZED AC PARAMETERS vs TEMPERATURE

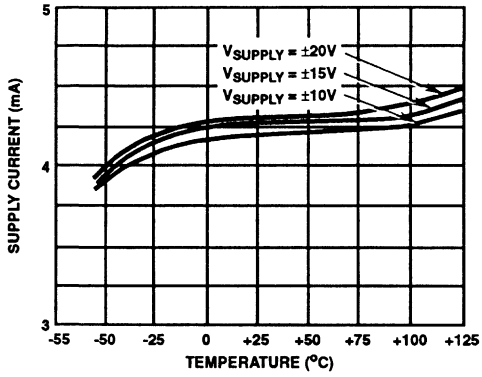


FIGURE 3. POWER SUPPLY CURRENT vs TEMPERATURE

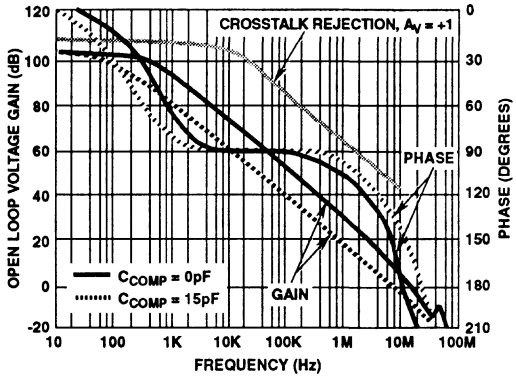


FIGURE 4. OPEN LOOP FREQUENCY AND PHASE RESPONSE

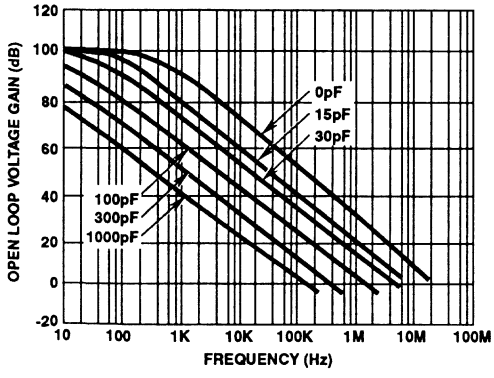


FIGURE 5. FREQUENCY RESPONSE vs C_{COMP}

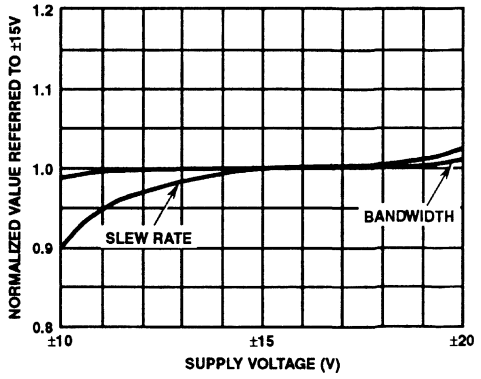


FIGURE 6. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

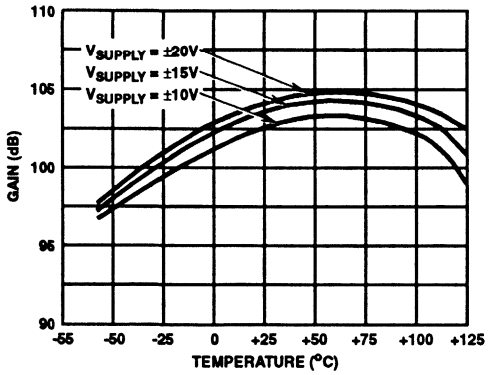


FIGURE 7. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

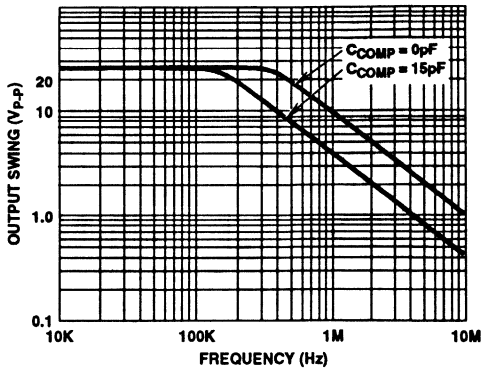


FIGURE 8. OUTPUT VOLTAGE SWING vs FREQUENCY

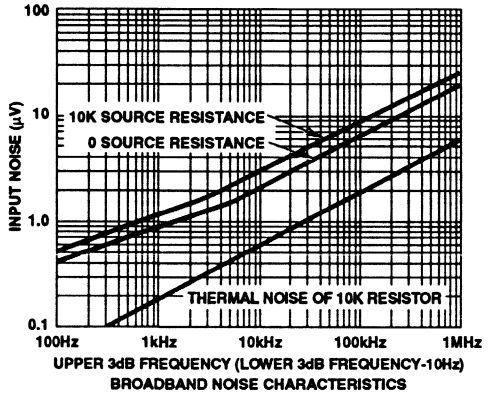


FIGURE 9. EQUIVALENT INPUT NOISE vs BANDWIDTH

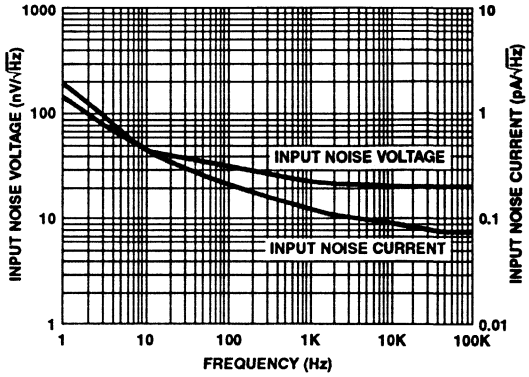


FIGURE 10. INPUT NOISE vs FREQUENCY

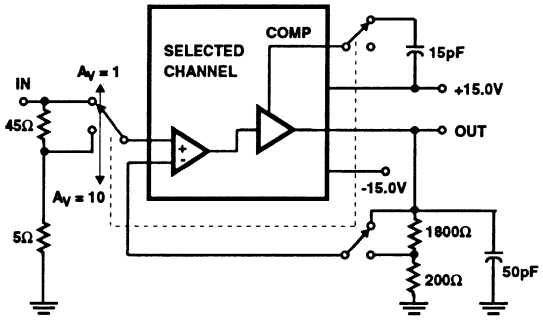


FIGURE 11. SLEW RATE AND TRANSIENT RESPONSE

Typical Applications

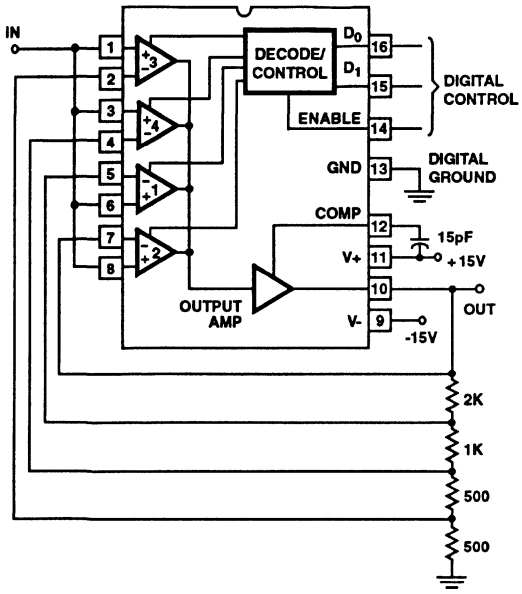
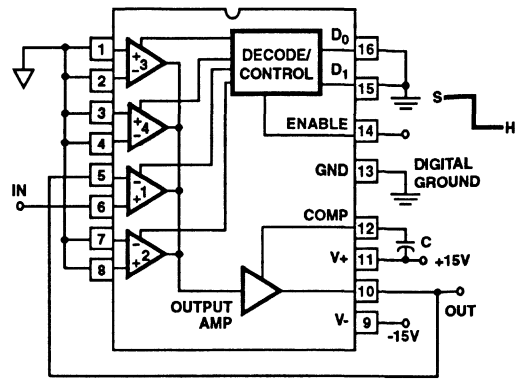


FIGURE 12. HA-2400 AMPLIFIER, NONINVERTING PROGRAMMABLE GAIN



Sample Charging Rate $= \frac{I_1}{C} V/Sec$

Hold Drift Rate $= \frac{I_2}{C} V/Sec$

Switch Pedestal Error $= \frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$A

$I_2 \approx 200 \times 10^{-9}$A at +25°C

$\approx 600 \times 10^{-9}$A at -55°C

$\approx 100 \times 10^{-9}$A at +125°C

$Q \approx 2 \times 10^{-12}$ Coulomb

FIGURE 13. HA-2400 SAMPLE AND HOLD

For more examples, see Harris Application Note 514

HARRIS SEMICONDUCTOR

HA-2406

Digitally Selectable Four Channel Operational Amplifier

March 1993

Features

- TTL Compatible Inputs
- Single Capacitor Compensation
- Low Crosstalk ..... -110dB
- High Slew Rate 20V/μs
- Low Offset Current 5nA
- Offset Voltage 7mV
- High Gain-Bandwidth 30MHz
- High Input Impedance 30MΩ

Applications

- Digital Control Of:
  - Analog Signal Multiplexing
  - Op Amp Gains
  - Oscillator Frequencies
  - Filter Characteristics
  - Comparator Levels
- For Further Design Ideas See Application Note 514

Description

The HA-2406 is a monolithic device consisting of four op amp input stages that can be individually connected to one output stage by decoding two TTL lines into four channel select signals. In addition to allowing each channel to be addressed, an enable control disconnects all input stages from the output stage when asserted low.

Each input-output combination of the HA-2406 is designed to be a 20V/μs, 30MHz gain-bandwidth amplifier that is stable at a gain of ten. By connecting one external 15pF capacitor all amplifiers are compensated for unity gain operation. The compensation lead may also be used to limit the output swing to TTL levels through suitable clamping diodes and divider networks (see Application Note 514).

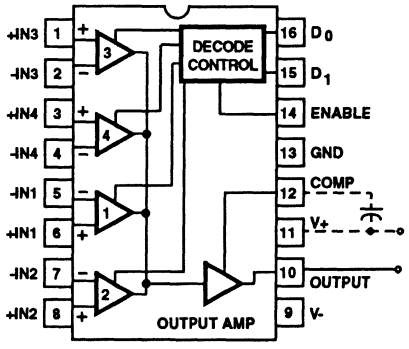
Dielectric isolation and short-circuit protected output stages contribute to the quality and durability of the HA-2406. When used as a simple amplifier, its dynamic performance is very good and when its added versatility is considered, the HA-2406 is unmatched in the analog world. It can replace a number of individual components in analog signal conditioning circuits for digital signal processing systems. Its advantages include saving board space and reducing power supply requirements.

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HA1-2406-5	0°C to +75°C	16 Lead Ceramic DIP
HA3-2406-5	0°C to +75°C	16 Lead Plastic DIP
HA9P2406-5	0°C to +75°C	16 Lead Wide Body SOIC
HA9P2406-9	-40°C to +85°C	16 Lead Wide Body SOIC

Pinout

HA-2406
(PDIP, CDIP, 300 mil SOIC)
TOP VIEW



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	None

Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals 45.0V
Differential Input Voltage. . . . . V_{SUPPLY}
Output Current . . . . . Short Circuit Protected (I_{SC} < ±33mA)
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Operating Temperature Range:
HA-2406-5 . . . . . 0°C ≤ T_A ≤ +75°C
HA-2406-9 . . . . . -40°C ≤ T_A ≤ +85°C
Storage Temperature Range . . . . . -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications Test Conditions: V_{SUPPLY} = 15.0V, Unless Otherwise Specified. Digital Inputs: V_{IL} = +0.5V, V_{IH} = +2.4V. Limits apply to each of the four channels, when addressed.

PARAMETER	TEMPERATURE	HA-2406-5, -9 LIMITS			UNITS
		MIN	TYP	MAX	
INPUT CHARACTERISTICS					
Offset Voltage	+25°C	-	7	10	mV
	Full	-	-	12	mV
Bias Current (Note 12)	+25°C	-	50	250	nA
	Full	-	-	500	nA
Offset Current (Note 12)	+25°C	-	5	50	nA
	Full	-	-	100	nA
Input Resistance (Note 12)	+25°C	-	30	-	MΩ
Common Mode Range	Full	±9.0	-	-	V
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Notes 1, 5)	+25°C	40	150	-	kV/V
	Full	20	-	-	kV/V
Common Mode Rejection Ratio (Note 2)	Full	74	80	-	dB
Gain Bandwidth (Note 3, 15)	+25°C	15	30	-	MHz
Gain Bandwidth (Note 4, 15)	+25°C	3	6	-	MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 1)	Full	±10.0	±12.0	-	V
Output Current (Note 13)	+25°C	10	15	-	mA
Full Power Bandwidth (Notes 3, 5, 14, 15)	+25°C	240	320	-	kHz
Full Power Bandwidth (Notes 4, 5, 14)	+25°C	64	95	-	kHz
TRANSIENT RESPONSE (Note 16)					
Rise Time (Notes 4, 6)	+25°C	-	30	100	ns
Overshoot (Notes 4, 6)	+25°C	-	25	40	%
Slew Rate (Notes 3, 7, 15)	+25°C	15	20	-	V/µs
Slew Rate (Notes 4, 7)	+25°C	4	6	-	Vµs
Settling Time (Notes 4, 7, 8, 15)	+25°C	-	2.0	3.5	µs
CHANNEL SELECT CHARACTERISTICS					
Digital Input Current (V_{IN} = 0V)	Full	-	1	1.5	mA
Digital Input Current (V_{IN} = +5.0V)	Full	-	15	-	nA
Output Delay (Note 9, 15)	+25°C	-	150	300	ns
Crosstalk (Note 10)	+25°C	-74	-110	-	dB

Electrical Specifications Test Conditions: V_{SUPPLY} = 15.0V, Unless Otherwise Specified. Digital Inputs: V_{IL} = +0.5V, V_{IH} = +2.4V. Limits apply to each of the four channels, when addressed. **(Continued)**

PARAMETER	TEMPERATURE	HA-2406-5, -9 LIMITS			UNITS
		MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS					
Supply Current	+25°C	-	4.8	7.0	mA
Power Supply Rejection Ratio (Note 11)	Full	74	90	-	dB

NOTES:

1. R_L = 2kΩ.
2. V_{CM} = ±5VDC.
3. A_V = +10, C_{COMP} = 0, R_L = 2kΩ, C_L = 50pF.
4. A_V = +1, C_{COMP} = 15pF, R_L = 2kΩ, C_L = 50pF.
5. V_{OUT} = 20V peak to peak.
6. V_{OUT} = 200mV peak to peak.
7. V_{OUT} = 10.0V peak to peak.
8. To 0.1% of final value.
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; V_{IN} = ±10VDC.
11. V_{SUPPLY} = ±10VDC to ±20VDC.
12. Unselected channels have approximately the same input parameters.
13. V_{OUT} = ±10V.
14. Full power Bandwidth based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
15. Sample tested.
16. See Figure 11 for test circuit.

Schematic Diagram

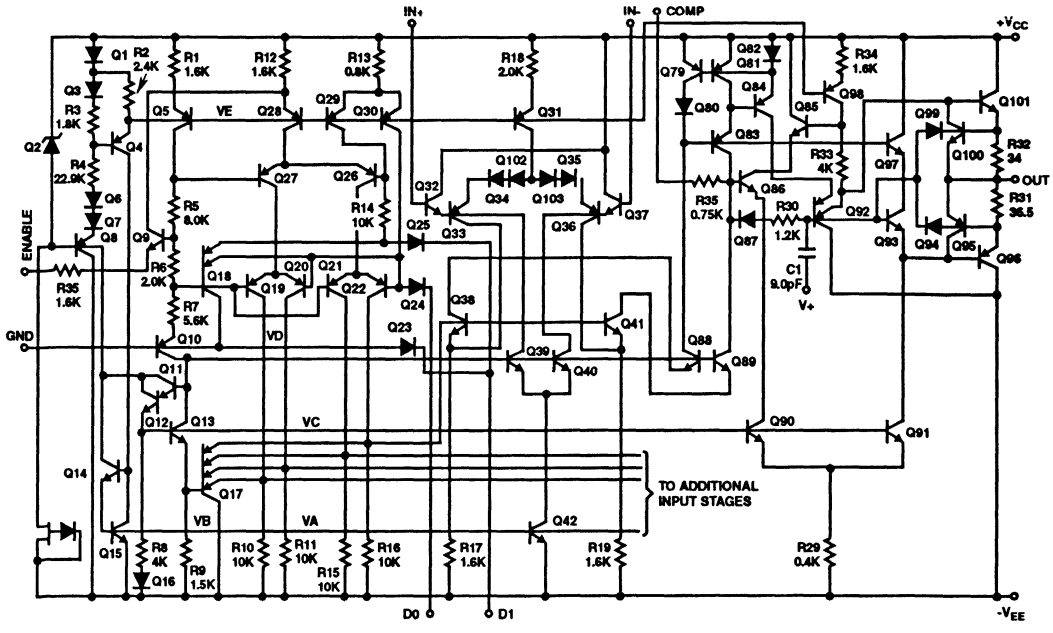


Diagram Includes: One Input Stage, Decode Control, Bias Network, and Output Stage

Typical Performance Curves

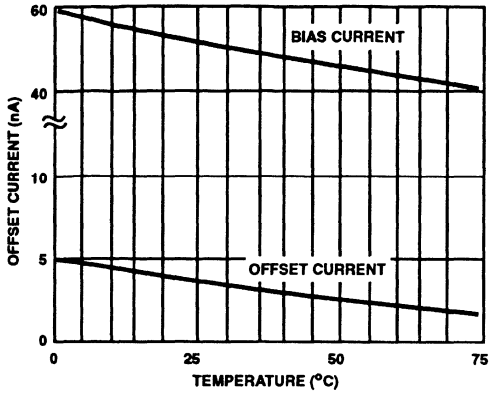


FIGURE 1. INPUT BIAS CURRENT AND OFFSET CURRENT vs TEMPERATURE

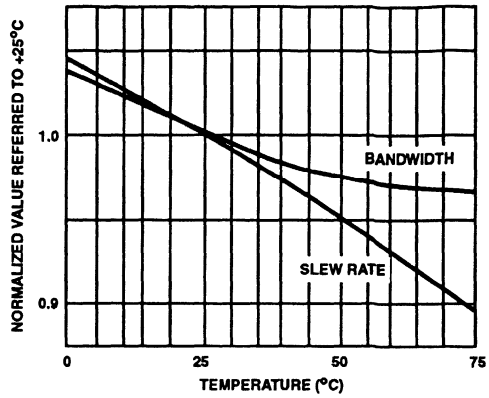


FIGURE 2. NORMALIZED A.C. PARAMETERS vs TEMPERATURE

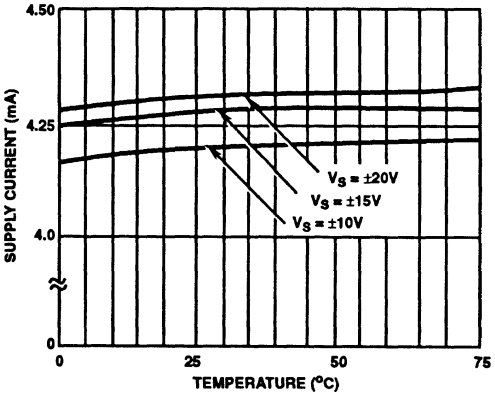


FIGURE 3. POWER SUPPLY CURRENT vs TEMPERATURE

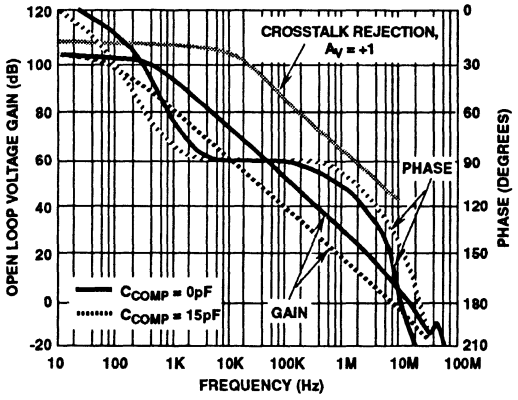


FIGURE 4. OPEN LOOP FREQUENCY AND PHASE RESPONSE

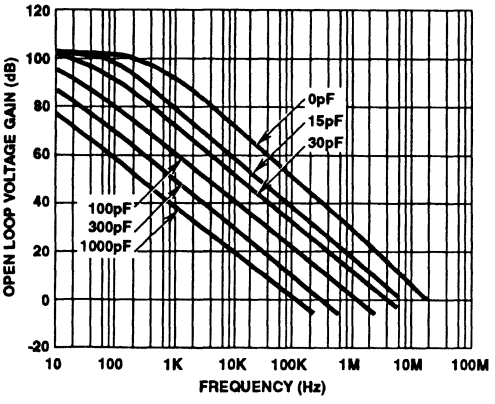


FIGURE 5. FREQUENCY RESPONSE vs C_{COMP}

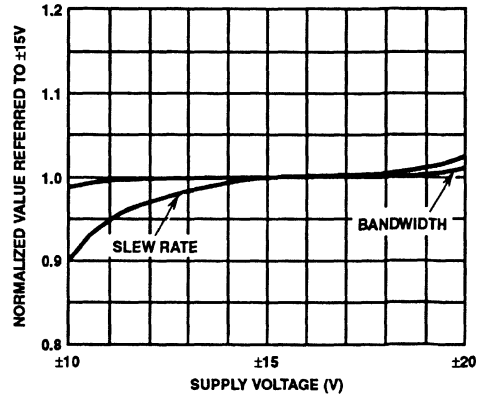


FIGURE 6. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

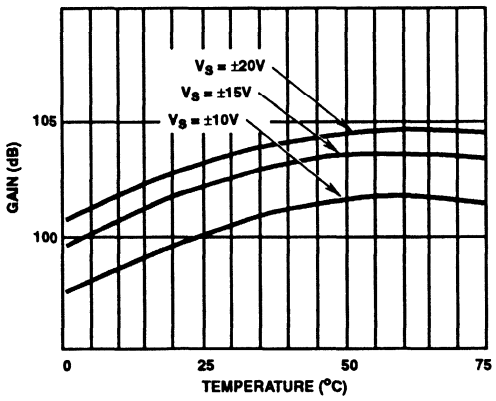


FIGURE 7. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

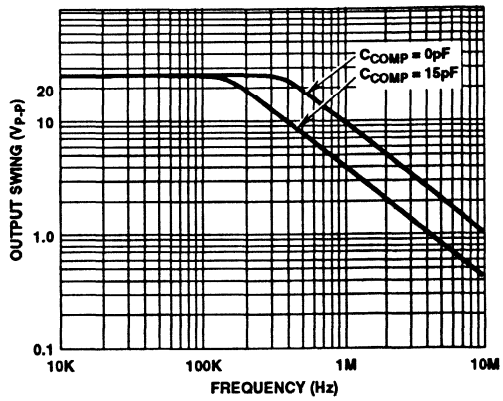


FIGURE 8. OUTPUT VOLTAGE SWING vs FREQUENCY

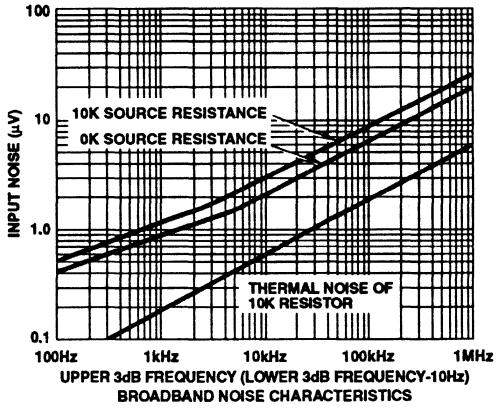


FIGURE 9. EQUIVALENT INPUT NOISE vs BANDWIDTH

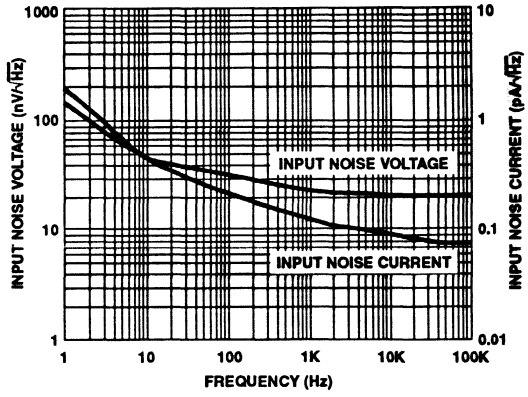


FIGURE 10. INPUT NOISE vs FREQUENCY

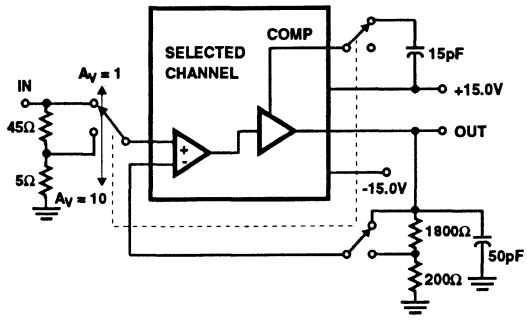


FIGURE 11. SLEW RATE AND TRANSIENT RESPONSE

Typical Applications

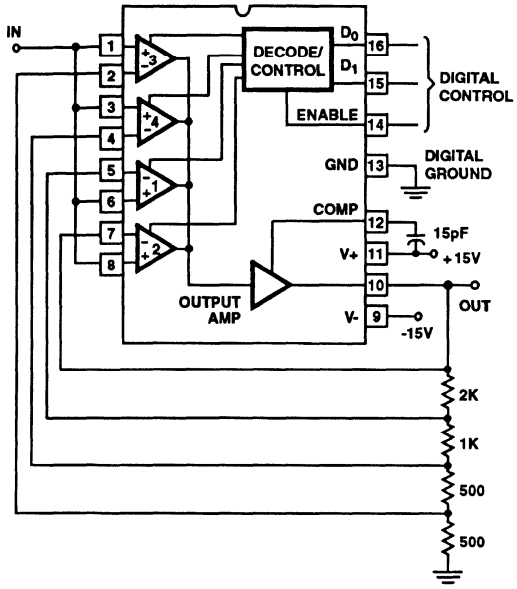
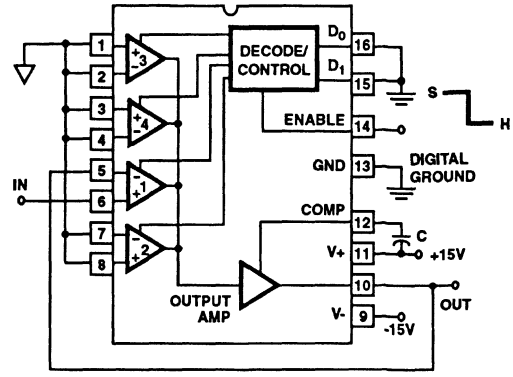


FIGURE 12. HA-2406 AMPLIFIER, NONINVERTING PROGRAMMABLE GAIN



Sample Charging Rate $= \frac{I_1}{C} V/Sec$

Hold Drift Rate $= \frac{I_2}{C} V/Sec$

Switch Pedestal Error $= \frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$A

$I_2 \approx 200 \times 10^{-9}$A at +25°C

$\approx 600 \times 10^{-9}$A at -55°C

$\approx 100 \times 10^{-9}$A at +125°C

$Q \approx 2 \times 10^{-12}$ Coulomb

FIGURE 13. HA-2406 SAMPLE AND HOLD

For more examples, see Harris Application Note 514

HARRIS SEMICONDUCTOR

HA-2444

Selectable, Four Channel Video Operational Amplifier

March 1993

Features

- Digital Selection of Input Channel
- Unity Gain Stability
- Gain Flatness to 10MHz. 0.1dB
- Differential Gain 0.03%
- Differential Phase. . . . . 0.03°
- Fast Channel Selection 60ns
- Crosstalk Rejection 60dB

Applications

- Video Multiplexer
- Programmable Gain Amplifier
- Special Effects Processors
- Video Distribution Systems
- Heads-up/Night Vision Displays
- Medical Imaging Systems
- Radar Video

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA3-2444-5	0°C to +75°C	16 Lead Plastic DIP
HA3-2444-9	-40°C to +85°C	16 Lead Plastic DIP
HA9P2444-5	0°C to +75°C	16 Lead Wide Body SOIC
HA9P2444-9	-40°C to +85°C	16 Lead Wide Body SOIC

Description

The HA-2444 is a channel-selectable video op amp consisting of four differential inputs, a single-ended output, and digital control circuitry allowing two digital inputs to activate one of the four differential inputs. The HA-2444 also includes a high impedance output state allowing the outputs of multiple HA-2444s to be wire-OR'd. Functionally, the HA-2444 is equivalent to four wideband video op amps and a wideband multiplexer.

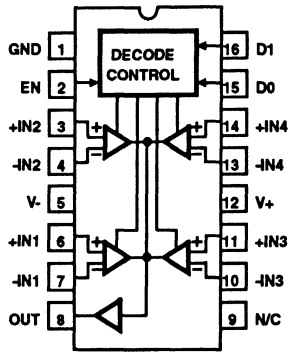
Unlike similar competitor devices, the HA-2444 is not restricted to multiplexing. Any op amp configuration can be used with any of the inputs. Signal amplification, addition, integration, and more can be put under digital control with broadcast quality performance.

The key video parameters of the HA-2444 have been optimized without compromising dc performance. Gain Flatness to 10MHz is only 0.1dB. Differential gain and phase are typically 0.03% and 0.03 degrees, respectively. Laser trimming allows offset voltages in the 4.0mV range and a unique common current source design assures minimal channel-to-channel mismatch, while maintaining 60dB of crosstalk rejection at 5MHz. Open loop gain of 76dB and low input offset and bias currents enhance the performance of this versatile device.

For information about military grade devices, please refer to the HA-2444/883 data sheet. The HA-2444/883 devices are offered in Ceramic DIP and Ceramic Flatpack packages.

Pinout

HA-2444
(PDIP, 300mil SOIC)
TOP VIEW



Logic Operation

TRUTH TABLE

EN	D1	D0	SELECTED CHANNEL
H	L	L	1
H	L	H	2
H	H	L	3
H	H	H	4
L	X	X	NONE-OUT is set to a high impedance state.

L = Low State (0.8V Max.)
H = High State (2.4V Min.)
X = Don't Care

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2490.5**

Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals ..... 35V (±17.5V)
Differential Input Voltage 6V
Peak (Short Duration) Output Current ..... ±40mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-2444-5 ..... $0°C \le T_A \le +75°C$
HA-2444-9 ..... $-40°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
Plastic DIP Package	88	27
SOIC Package	96	26

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +15V, V- = -15V, R_L = 1kΩ, $C_L \le$ 10pF, V_{IL} = 0.8V, V_{IH} = 2.4V. Unless Otherwise Specified. Specifications Apply to All Channels.

PARAMETER	TEMP	HA-2444-5, -9 MIN	HA-2444-5, -9 TYP	HA-2444-5, -9 MAX	UNITS
INPUT CHARACTERISTICS					
Input Offset Voltage	+25°C	-	4	7	mV
	Full	-	-	15	mV
Average Input Offset Voltage Drift	Full	-	10	-	µV/°C
Channel to Channel Offset Voltage Mismatch	+25°C	-	-	5	mV
	Full	-	-	8	mV
Input Bias Current	+25°C	-	9	15	µA
	Full	-	-	20	µA
Average Input Bias Current Drift	Full	-	0.04	-	µA/°C
Input Offset Current	+25°C	-	2	4	µA
	Full	-	-	6	µA
Average Input Offset Current Drift	Full	-	10	-	nA/°C
Common Mode Range	Full	-	±11.5	-	V
Differential Input Resistance (Note 16)	+25°C	50	90	-	kΩ
Differential Input Capacitance	+25°C	-	3	-	pF
Input Noise Voltage Density f = 1000Hz	+25°C	-	26	-	$nV/\sqrt{Hz}$
Input Noise Current Density f = 1000Hz	+25°C	-	4	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Note 3)	+25°C	71	76	-	dB
	Full	68	-	-	dB
Common Mode Rejection Ratio (Note 4)	Full	70	80	-	dB
Minimum Stable Gain	+25°C	+1	-	-	V/V
Unity Gain Bandwidth (Notes 2, 5)	+25°C	-	45	-	MHz
Gain Bandwidth Product (Note 5)	+25°C	-	50	-	MHz
Phase Margin (Note 2)	+25°C	-	65	-	Degrees
Gain Margin (Note 2)	+25°C	-	8.0	-	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing (R_L = 1kΩ)	Full	±10	±11	-	V
Output Voltage Swing (R_L = 75Ω) (Note 16)	+25°C	±2	-	-	V
Full Power Bandwidth (Note 6)	Full	3.8	5.1	-	MHz
Output Current (Note 17)	Full	±25	-	-	mA
Disabled Output Current (Note 18)	Full	-	-	860	µA
Output Resistance	+25°C	-	20	-	Ω
TRANSIENT RESPONSE					
Rise Time (Notes 2, 7)	+25°C	-	7	-	ns
Overshoot (Notes 2, 7)	+25°C	-	10	-	%

Electrical Specifications V+ = +15V, V- = -15V, R_L = 1kΩ, $C_L \leq$ 10pF, V_{IL} = 0.8V, V_{IH} = 2.4V. Unless Otherwise Specified. Specifications Apply to All Channels. **(Continued)**

PARAMETER		TEMP	HA-2444-5, -9 MIN	TYP	MAX	UNITS
Slew Rate (Notes 2, 9)		Full	120	160	-	V/µs
Settling Time to 0.1% of ±10V Output (Note 8)		+25°C	-	120	-	ns
SWITCHING CHARACTERISTICS						
Channel Select Time (Note 10)		0 to +85°C	-	60	100	ns
		-40 to 0°C	-	80	125	ns
Output Enable Time (Note 11)		Full	-	40	100	ns
Digital Input Voltages	V_{IH}	Full	2.4	-	-	V
	V_{IL}	Full	-	-	0.8	V
D0/D1 Input Current	(V_{IL} = 0.0V	Full	-	0.7	1	mA
	(V_{IH} = 5.0V)	Full	-	-	1.2	µA
EN Input Current	(V_{IL} = 0.0V)	Full	-	-	50	µA
	(V_{IH} = 5.0V)	Full	-	-	1.2	µA
Crosstalk Rejection (Note 12)		+25°C	-	60	-	dB
VIDEO PARAMETERS						
Differential Phase (Note 14)		+25°C	-	0.03	-	Degrees
Differential Gain (Note 14)		+25°C	-	0.03	-	%
Gain Flatness (Notes 2, 13) (10MHz)		+25°C	-	0.1	-	dB
Chrominance to Luminance Gain (Note 14)		+25°C	-	0.1	-	dB
Chrominance to Luminance Delay (Note 14)		+25°C	-	7	-	ns
POWER SUPPLY						
I_{CC}		Full	-	20	25	mA
I_{EE}		Full	-	20	25	mA
Supply Current (Output Disabled) (Note 19)		Full	-	-	10	mA
PSRR (Note 15)		Full	65	80	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. A_V = +1.
3. V_{OUT} = ±5V.
4. V_{CM} = ±5V.
5. V_{OUT} = ±100mV.
6. Full Power Bandwidth is calculated by: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; V_{PEAK} = 5V.
7. V_{OUT} = 0 to ±200mV.
8. Settling time to 0.1% with a 10V step. Specified with the channel pre-selected and the output stage enabled. A_V = -1.
9. V_{OUT}= -5V to +5V or +5V to -5V.
10. The time required for an enabled HA-2444 to switch from one input channel to another. Measured from the 50% point of the digital input to 50% of the output. A_V = +1 for all channels. V_{OUT} switches from 0V to 5V.
11. The time required to enable the output with a channel preselected. Measured from the 50% point of the Enable input to 4V on the output. A_V = +1 for all channels. V_{IN} = 5V for the selected channel.
12. V_{IN} = 5Vp-p, fo = 5MHz, for one of the 3 unselected channels. V_{IN} = 0 for the selected channel. A_V = +1 for all channels.
13. V_{IN} = 200mV_{RMS}.
14. Tested with a VM700A video tester using a NTC-7 Composite input signal.
15. V_S = ±15V to ±20V.
16. These parameters are not tested. The limits are guaranteed based on lab characterization and reflect lot to lot variation.
17. V_{OUT} = ±10V, V_{EN} = 2.4V, 50% Duty Cycle max.
18. V_{OUT} = ±5V, V_{EN} = 0.8V.
19. Applies to I_{CC} and I_{EE}. V_{OUT} = 0V, V_{EN} = 0.8V.

HARRIS SEMICONDUCTOR

HA-2500, HA-2502 HA-2505

Precision High Slew Rate Operational Amplifiers

March 1993

Features

- High Slew Rate 30V/μs
- Fast Settling 330ns
- Wide Power Bandwidth 500kHz
- High Gain Bandwidth 12MHz
- High Input Impedance 50MΩ
- Low Offset Current 10nA
- Internally Compensated For Unity Gain Stability

Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HA2-2500-2	-55°C to +125°C	8 Pin TO-99 Can
HA2-2502-2	-55°C to +125°C	8 Pin TO-99 Can
HA2-2505-5	0°C to +75°C	8 Pin TO-99 Can
HA3-2505-5	0°C to +75°C	8 Lead Plastic DIP
HA4P2505-5	0°C to +75°C	20 Lead Plastic LCC
HA7-2500-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-2502-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-2505-5	0°C to +75°C	8 Lead Ceramic DIP

Description

HA-2500, HA-2502, HA-2505 comprises a series of monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

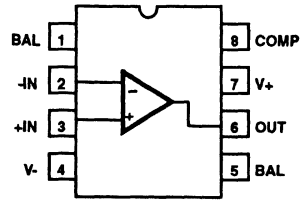
These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits. Slew rates of ±30V/μs and 330ns (0.1%) settling time make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. 12MHz small signal bandwidth and 500kHz power bandwidth make these devices well suited to R.F. and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current, HA-2500, HA-2502, HA-2505 are particularly useful components in signal conditioning designs.

The gain and offset voltage figures of the HA-2500 series are optimized by internal component value changes while the similar design of the HA-2510 series is maximized for slew rate.

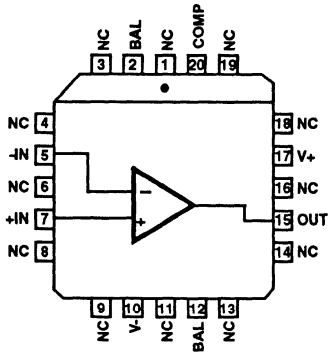
Mil-Std-883 product and data sheets are available upon request.

Pinouts

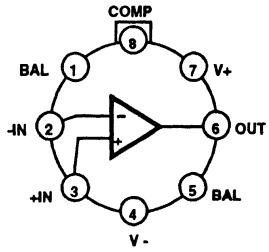
HA-2500/02 (CDIP)
HA-2505 (PDIP, CDIP)
TOP VIEW



HA-2505
(PLCC)
TOP VIEW



HA-2500/02/05
(TO-99 CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2890.1**

Absolute Maximum Ratings (Note 6)

Supply Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 15V
Peak Output Current 50mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-2500/2502-2 ..... $-55°C \le T_A \le +125°C$
HA-2505-5 ..... $0°C \le T_A \le +75°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

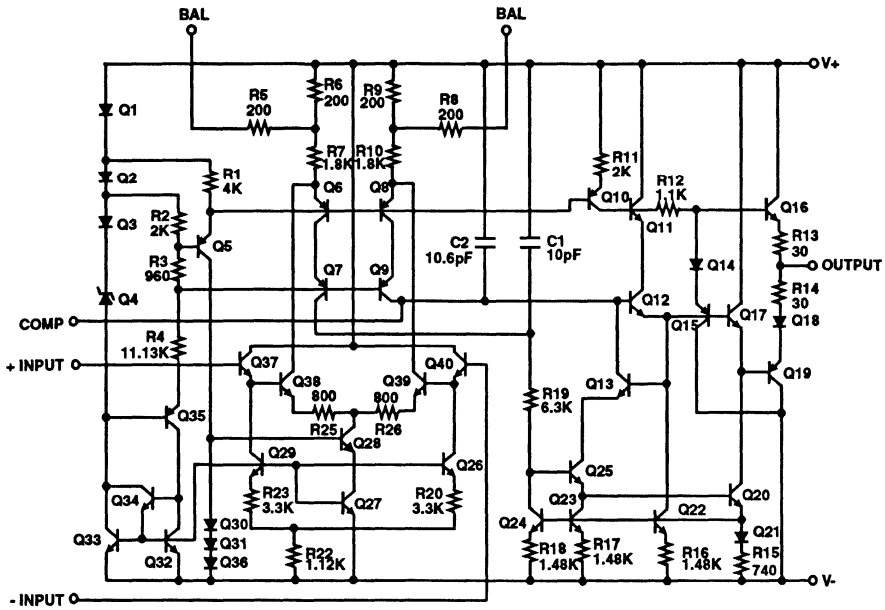
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = +15V, V- = -15V DC

PARAMETER	TEMP	HA-2500-2			HA-2502-2			HA-2505-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	-	2	5	-	4	8	-	4	8	mV
	Full	-	-	8	-	-	10	-	-	10	mV
Offset Voltage Average Drift	Full	-	20	-	-	20	-	-	20	-	µV/°C
Bias Current	+25°C	-	100	200	-	125	250	-	125	250	nA
	Full	-	-	400	-	-	500	-	-	500	nA
Offset Current	+25°C	-	10	25	-	20	50	-	20	50	nA
	Full	-	-	50	-	-	100	-	-	100	nA
Input Resistance (Note 10)	+25°C	25	50	-	20	50	-	20	50	-	MΩ
Common Mode Range	Full	±10	-	-	±10	-	-	±10	-	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	20	30	-	15	25	-	15	25	-	kV/V
	Full	15	-	-	10	-	-	10	-	-	kV/V
Common Mode Rejection Ratio (Note 2)	Full	80	90	-	74	90	-	74	90	-	dB
Gain Bandwidth Product (Note 3)	+25°C	-	12	-	-	12	-	-	12	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10	±12	-	±10	±12	-	±10	±12	-	V
Output Current (Note 4)	+25°C	±10	±20	-	±10	±20	-	±10	±20	-	mA
Full Power Bandwidth (Note 4, 11)	+25°C	350	500	-	300	500	-	300	500	-	kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 7 and 8)	+25°C	-	25	50	-	25	50	-	25	50	ns
Overshoot (Notes 1, 5, 7 and 8)	+25°C	-	25	40	-	25	50	-	25	50	%
Slew Rate (Notes 1, 5, 8 and 12)	+25°C	±25	±30	-	±20	±30	-	±20	±30	-	V/µs
Settling Time to 0.1% (Note 1, 5, 8 and 12)	+25°C	-	0.33	-	-	0.33	-	-	0.33	-	µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C	-	4	6	-	4	6	-	4	6	mA
PSRR (Note 9)	Full	80	90	-	74	90	-	74	90	-	dB

NOTES:
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10V$
5. $C_L = 50pF$
6. Absolute Maximum Ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired.
7. $V_O = \pm 200mV$
8. See Transient Response Test Circuits and Waveforms.
9. $\Delta V = \pm 5V$
10. This parameter value is based on design calculations.
11. Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = Slew Rate/$2\pi V_{PEAK}$
12. $V_{OUT} = \pm 5V$.

Schematic

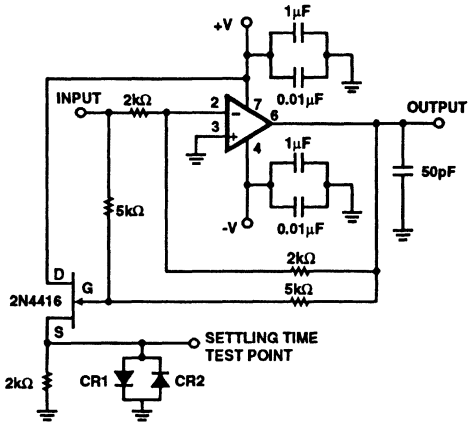


Die Characteristics

Transistor Count 40
Die Dimensions ..... 57 x 65 x 19 mils
Substrate Potential ..... Unbiased
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Metal Can	117	36
Plastic Mini-DIP	96	34
Ceramic Mini-DIP	115	36
Plastic LCC	74	33

Settling Time Circuit



- $A_V = -1$
- Feedback and Summing Resistor Ratios should be 0.1% matched.
- Clipping Diodes CR1 and CR2 are optional. HP5082-2810 recommended.

Test Circuits

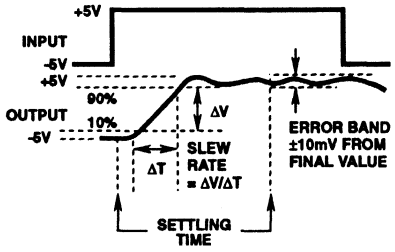


FIGURE 1. SLEW RATE AND SETTLING TIME

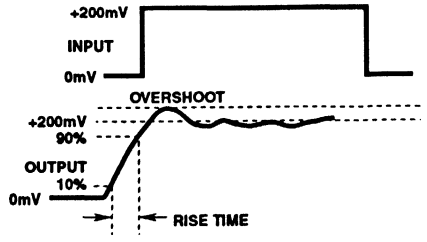


FIGURE 2. TRANSIENT RESPONSE

NOTE: Measured on both positive and negative transitions from 0V to +200mv and 0V to -200mV at the output.

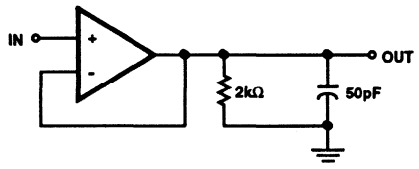


FIGURE 3. SLEW RATE AND TRANSIENT RESPONSE

NOTE: Measured on both positive and negative transitions from 0V to +200mv and 0V to -200mV at the output.

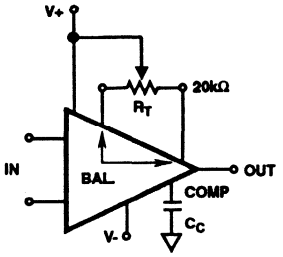


FIGURE 4. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK UP

Tested offset adjustment range is $|V_{OS}|$ + 1mV| minimum referred to output. Typical ranges are ±6mV with R_T = 20kΩ

Typical Performance Curves

V+ = +15VDC, V- = -15VDC, T_A = +25°C, Unless Otherwise Specified

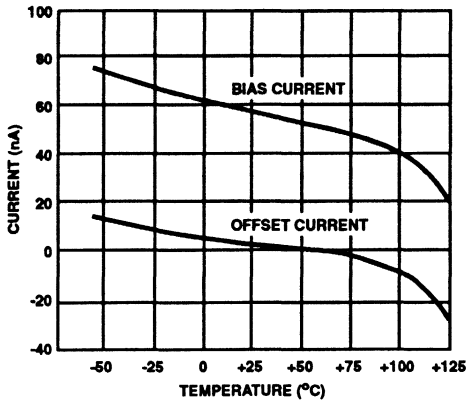


FIGURE 5. INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE

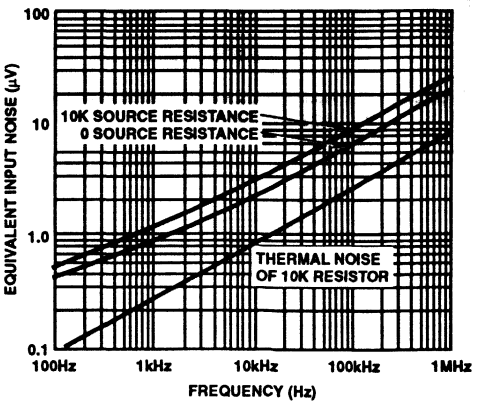


FIGURE 6. EQUIVALENT INPUT NOISE vs. BANDWIDTH (With 10Hz High Pass Filter)

Typical Performance Curves

V+ = +15VDC, V- = -15VDC, T_A = +25°C, Unless Otherwise Specified **(Continued)**

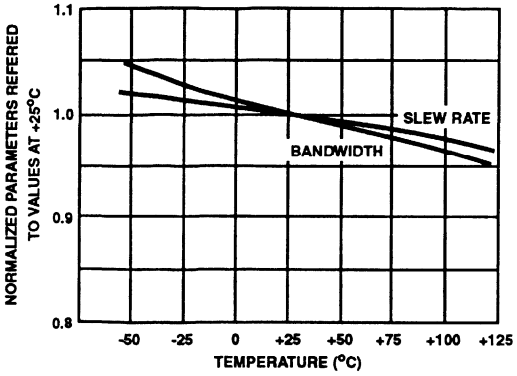


FIGURE 7. NORMALIZED AC PARAMETERS vs TEMPERATURE

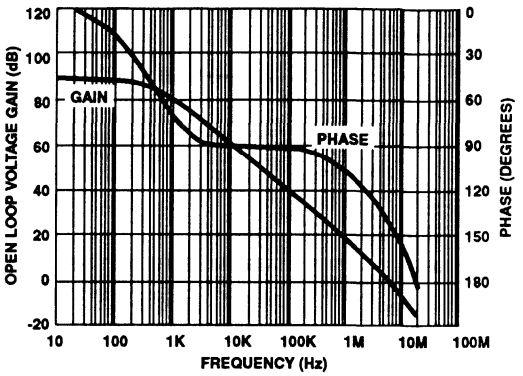


FIGURE 8. OPEN LOOP FREQUENCY AND PHASE RESPONSE

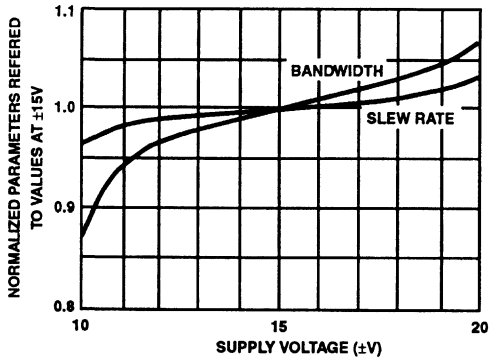


FIGURE 9. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C

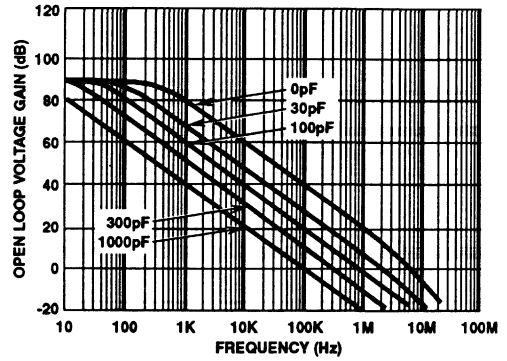


FIGURE 10. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

Typical Performance Curves

V+ = +15VDC, V- = -15VDC, T_A = +25°C, Unless Otherwise Specified **(Continued)**

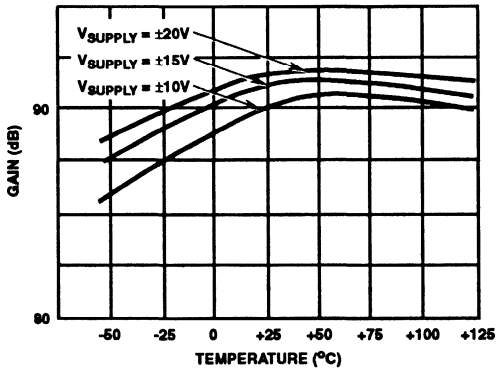


FIGURE 11. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

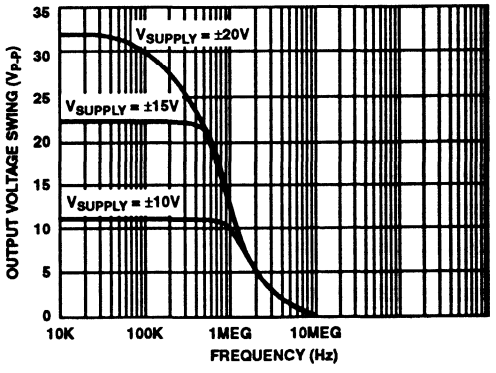


FIGURE 12. OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C

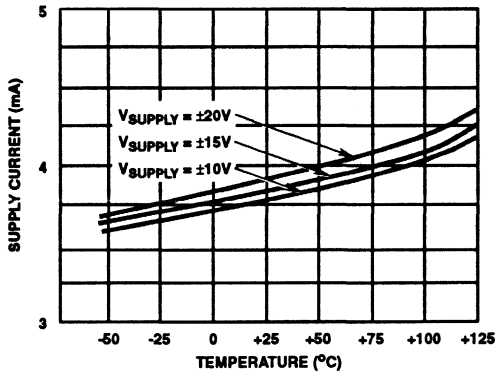


FIGURE 13. POWER SUPPLY CURRENT vs TEMPERATURE

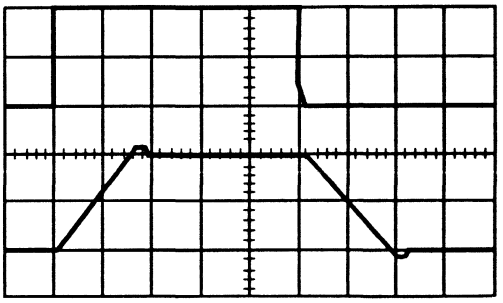


FIGURE 14. VOLTAGE FOLLOWER PULSE RESPONSE

R_L = 2kΩ, C_L = 50pF — Vertical = 5V/Div.
Upper Trace: Input — Horizontal = 200ns/Div.
Lower Trace: Output — T_A = +25°C, V_S = ±15V

HARRIS SEMICONDUCTOR

HA-2510, HA-2512 HA-2515

March 1993

High Slew Rate Operational Amplifiers

Features

- High Rate Slew 60V/μs
- Fast Settling 250ns
- Wide Power Bandwidth 1,000kHz
- High Gain Bandwidth 12MHz
- High Input Impedance 100MΩ
- Low Offset Current 10nA
- Internally Compensated for Unity Gain Stability

Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

HA-2510/12/15 are a series of high performance operational amplifiers which set the standards for maximum slew rate, highest accuracy and widest bandwidths for internally compensated monolithic devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

The ±60V/μs slew rate and 250ns (0.1%) settling time of these amplifiers is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2510/12/15's superior 12MHz gain bandwidth and 1000kHz power bandwidth is extremely useful in R.F. and video applications. For accurate signal conditioning these amplifiers also provide 10nA offset current, coupled with 100MΩ input impedance, and offset trim capability.

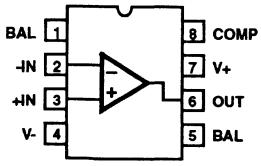
Mil-Std-883 product and data sheets are available upon request.

Ordering Information

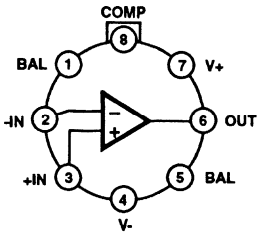
PART NUMBER	TEMP. RANGE	PACKAGE
HA2-2510-2	-55°C to +125°C	8 Pin Can
HA2-2512-2	-55°C to +125°C	8 Pin Can
HA2-2515-5	0°C to +75°C	8 Pin Can
HA3-2515-5	0°C to +75°C	8 Lead Plastic DIP
HA7-2510-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-2512-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-2515-5	0°C to +75°C	8 Lead Ceramic DIP

Pinouts

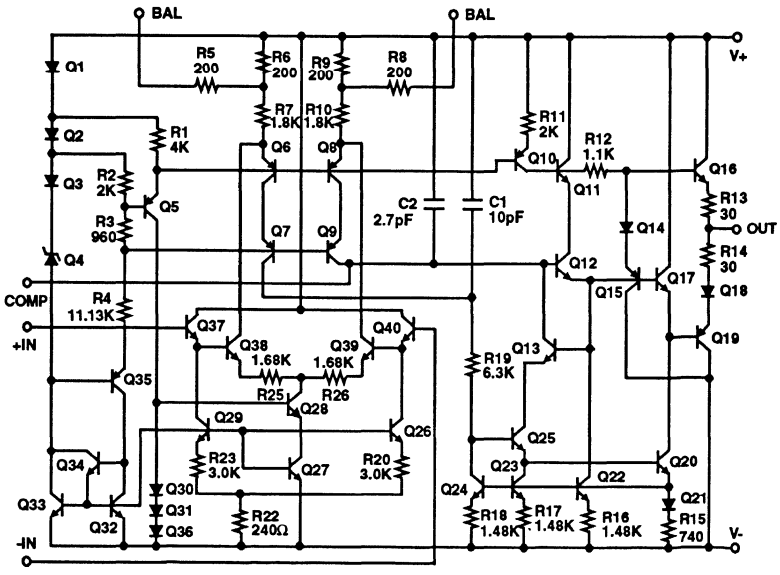
HA-2510/12 (CDIP)
HA-2515 (PDIP, CDIP)
TOP VIEW



HA-2510/12/15 (TO-99 CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2893.1**

Absolute Maximum Ratings (Note 6)

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage. 15V
Peak Output Current. 50mA
Junction Temperature. . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.). . . . . +300°C

Operating Conditions

Operating Temperature Range
HA-2510/12-2 . . . . . $-55°C \le T_A \le +125°C$
HA-2515-5 . . . . . $0°C \le T_A \le +75°C$
Storage Temperature Range . . . . . $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = +15VDC, V- = -15VDC

PARAMETER	TEMP	HA-2510-2			HA-2512-2			HA-2515-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	-	4	8	-	5	10	-	5	10	mV
	Full	-	-	11	-	-	14	-	-	14	mV
Offset Voltage Average Drift	Full	-	20	-	-	25	-	-	30	-	µV/°C
Bias Current	+25°C	-	100	200	-	125	250	-	125	250	nA
	Full	-	-	400	-	-	500	-	-	500	nA
Offset Current	+25°C	-	10	25	-	20	50	-	20	50	nA
	Full	-	-	50	-	-	100	-	-	100	nA
Input Resistance (Note 10)	+25°C	50	100	-	40	100	-	40	100	-	MΩ
Common Mode Range	Full	±10.0	-	-	±10.0	-	-	±10.0	-	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 1, 4)	+25°C	10	15	-	7.5	15	-	7.5	15	-	kV/V
	Full	7.5	-	-	5	-	-	5	-	-	kV/V
Common Mode Rejection Ratio (Note 2)	Full	80	90	-	74	90	-	74	90	-	dB
Gain Bandwidth Product (Notes 3)	+25°C	-	12	-	-	12	-	-	12	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0	-	±10.0	±12.0	-	±10.0	±12.0	-	V
Output Current (Note 4)	+25°C	±10	±20	-	±10	±20	-	±10	±20	-	mA
Full Power Bandwidth (Notes 4, 11)	+25°C	750	1000	-	600	1000	-	600	1000	-	kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 7, 8)	+25°C	-	25	50	-	25	50	-	25	50	ns
Overshoot (Notes 1, 5, 7, 8)	+25°C	-	25	40	-	25	50	-	25	50	%
Slew Rate (Notes 1, 5, 8, 12)	+25°C	±50	±65	-	±40	±60	-	±40	±60	-	V/µs
Settling Time to 0.1% (Notes 1, 5, 8, 12)	+25°C	-	0.25	-	-	0.25	-	-	0.25	-	µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C	-	4	6	-	4	6	-	4	6	mA
Power Supply Rejection Ratio (Note 19)	Full	80	90	-	74	90	-	74	90	-	dB

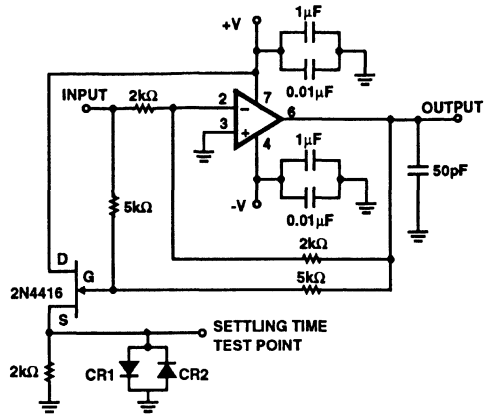
NOTES:

1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 10VDC$
3. $A_V > 10$.
4. $V_O = \pm 10V$.
5. $C_L = 50pF$.
6. Absolute Maximum Ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired.
7. $V_O = \pm 200mV$.
8. See Transient Response Test Circuits and Waveforms.
9. $\Delta V = \pm 5V$.
10. This parameter value is based on design calculations.
11. Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = Slew Rate/$2\pi V_{PEAK}$.
12. $V_{OUT} = \pm 5V$.

Die Characteristics

Transistor Count		40
Die Dimensions		57 x 65 x 19 mils
Substrate Potential		Unbiased
Process		Bipolar-DI
Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Metal Can	117	36
Plastic Mini-DIP	96	34
Ceramic Mini-DIP	115	36

Settling Time Circuit



- $A_V = -1$
- Feedback and summing resistor ratios should be 0.1% matched.
- Clipping diodes CR1 and CR2 are optional. HP5082-2810 recommended.

Test Circuits

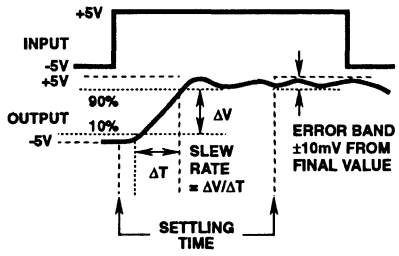


FIGURE 1. SLEW RATE AND SETTLING TIME

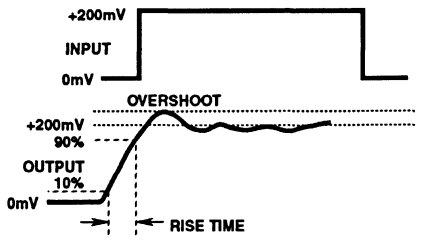


FIGURE 2. TRANSIENT RESPONSE

NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

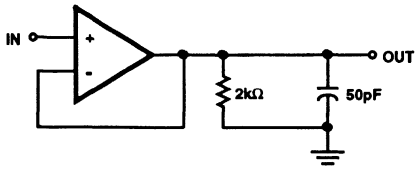


FIGURE 3. SLEW RATE AND TRANSIENT RESPONSE

NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

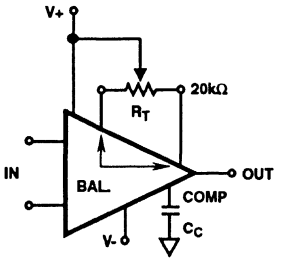


FIGURE 4. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK UP

Tested offset adjustment range is $|V_{OS}|$ + 1mV| minimum referred to output. Typical ranges are ±6mV with R_T = 20kΩ

Typical Performance Curves

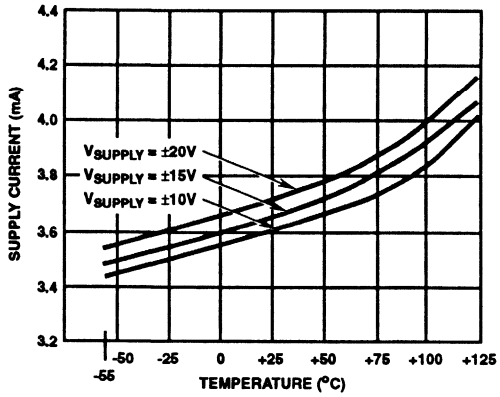


FIGURE 5. POWER SUPPLY CURRENT vs TEMPERATURE

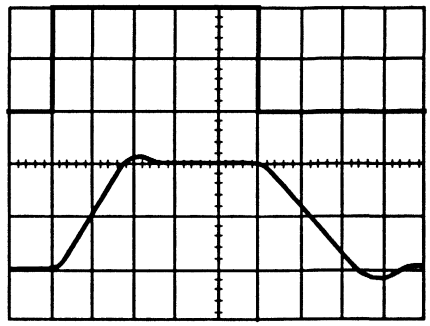


FIGURE 6. VOLTAGE FOLLOWER PULSE RESPONSE

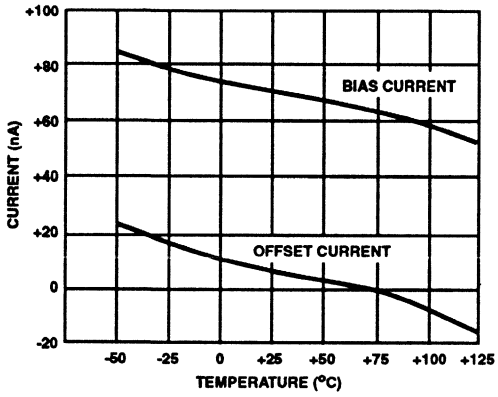


FIGURE 7. INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

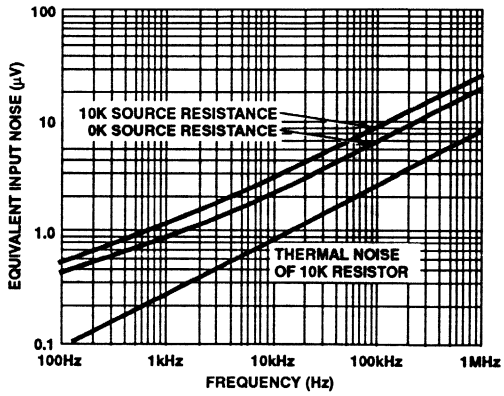


FIGURE 8. EQUIVALENT INPUT NOISE vs BANDWIDTH (WITH 10Hz HIGH PASS FILTER)

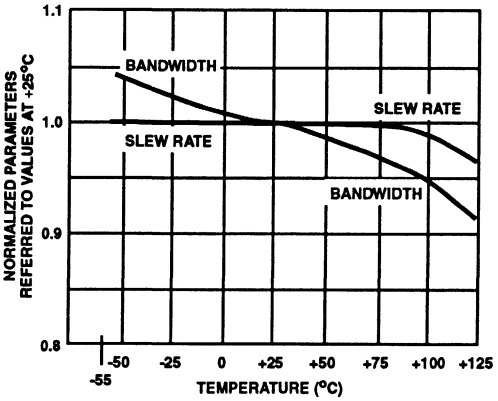


FIGURE 9. NORMALIZED AC PARAMETERS vs TEMPERATURE

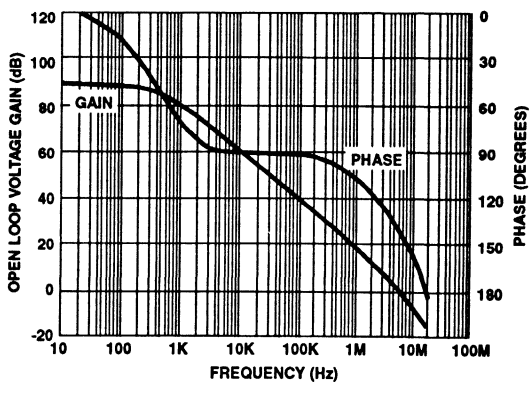


FIGURE 10. OPEN LOOP GAIN AND PHASE RESPONSE

Typical Performance Curves (Continued)

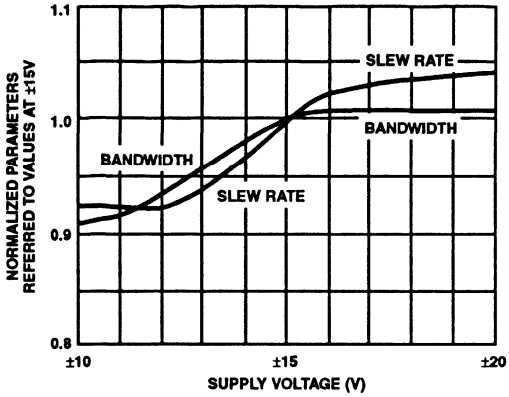


FIGURE 11. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C

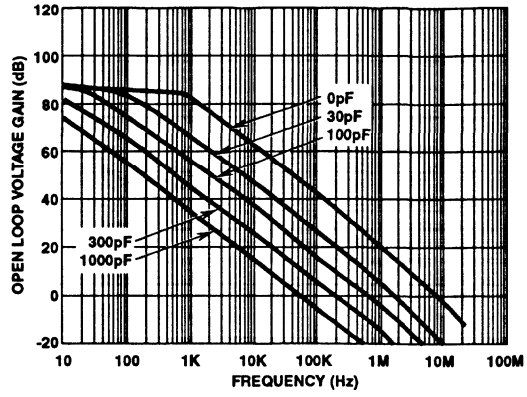


FIGURE 12. OPEN LOOP GAIN RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

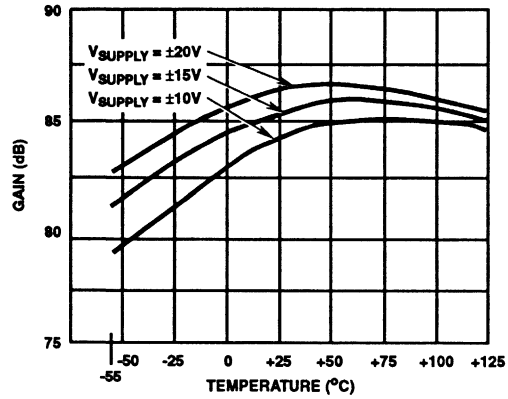


FIGURE 13. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

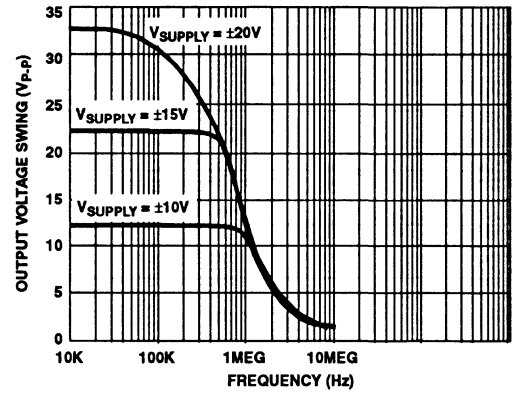


FIGURE 14. OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C

HARRIS SEMICONDUCTOR

HA-2520, HA-2522 HA-2525

Uncompensated High Slew Rate Operational Amplifiers

March 1993

Features

- High Slew Rate 120V/μs
- Fast Settling 200ns
- Wide Power Bandwidth 2MHz
- High Gain Bandwidth ($A_V \geq 3$) 20MHz
- High Input Impedance 100MΩ
- Low Offset Current 10nA

Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

HA-2520/2522/2525 comprise a series of monolithic operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at close loop gains greater than 3 without external compensation. In addition, these high performance components also provide low offset current and high input impedance.

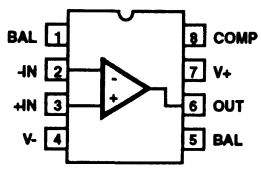
120V/μs slew rate and 200ns (0.2%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for R.F. and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complemented by 10nA offset current, 100MΩ input impedance and offset trim capability. MIL-STD-883 product and data sheets are available upon request.

Ordering Information

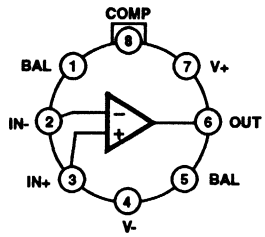
PART NUMBER	TEMP. RANGE	PACKAGE
HA2-2520-2	-55°C to +125°C	8 Pin Can
HA2-2522-2	-55°C to +125°C	8 Pin Can
HA2-2525-5	0°C to +75°C	8 Pin Can
HA3-2525-5	0°C to +75°C	8 Lead Plastic DIP
HA4P2525-5	0°C to +75°C	20 Lead PLCC
HA7-2520-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-2522-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-2525-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P2525-5	0°C to +75°C	8 Lead SOIC

Pinouts

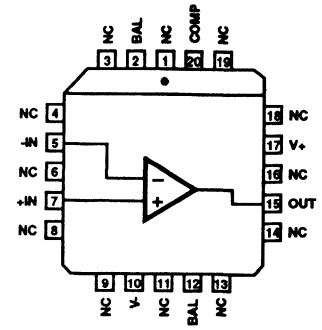
HA-2520/22 (CDIP)
HA-2525 (PDIP, CDIP, SOIC)
TOP VIEW



HA-2520/22/25
(TO-99 METAL CAN)
TOP VIEW



HA-2525
(PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2894.1**

Absolute Maximum Ratings (Note 13)

Supply Voltage (Between V+ and V- Terminals) 40.0V
Differential Input Voltage 15.0V
Output Current 50mA
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Operating Temperature Range
HA-2520/2522-2 . . . . . $-55°C \leq T_A \leq +125°C$
HA-2525-5 . . . . . $0°C \leq T_A \leq +75°C$
Storage Temperature Range . . . . . $-65°C \leq T_A \leq +150°C$

Electrical Specifications

V+ = +15VDC, V- = -15VDC

PARAMETER	TEMP	HA-2520-2 LIMITS			HA-2522-2 LIMITS			HA-2525-5 LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	-	4	8	-	5	10	-	5	10	mV
	Full	-	-	11	-	-	14	-	-	14	mV
Offset Voltage Drift	Full	-	20	-	-	25	-	-	30	-	µV/°C
Bias Current	+25°C	-	100	200	-	125	250	-	125	250	nA
	Full	-	-	400	-	-	500	-	-	500	nA
Offset Current	+25°C	-	10	25	-	20	50	-	20	50	nA
	Full	-	-	50	-	-	100	-	-	100	nA
Input Resistance (Note 9)	+25°C	50	100	-	40	100	-	40	100	-	MΩ
Common Mode Range	Full	±10.0	-	-	±10.0	-	-	±10.0	-	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 1, 4)	+25°C	10	15	-	7.5	15	-	7.5	15	-	kV/V
	Full	7.5	-	-	5	-	--	5	-	-	kV/V
Common Mode Rejection Ratio (Note 2)	Full	80	90	-	74	90	-	74	90	-	dB
Gain Bandwidth (Notes 3, 12)	+25°C	10	20	-	10	20	-	10	20	-	MHz
Minimum Stable Gain	+25°C	3	-	-	3	-	-	3	-	-	V/V
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0	-	±10.0	±12.0	-	±10.0	±12.0	-	V
Output Current (Note 4)	+25°C	±10	±20	-	±10	±20	-	±10	±20	-	mA
Full Power Bandwidth (Notes 4, and 10)	+25°C	1.5	2.0	-	1.2	2.0	-	1.2	2.0	-	MHz
TRANSIENT RESPONSE (A_V = +3)											
Rise Time (Notes 1, 5, 6, and 8)	+25°C	-	25	50	-	25	50	-	25	50	ns
Overshoot (Notes 1, 5, 6, and 8)	+25°C	-	25	40	-	25	50	-	25	50	%
Slew Rate (Notes 1, 5, 8, and 11)	+25°C	±100	±120	-	±80	±120	-	±80	±120	-	V/µs
Settling Time (Notes 1, 5, 8, 11)	+25°C	-	0.20	-	-	0.20	-	-	0.20	-	µs

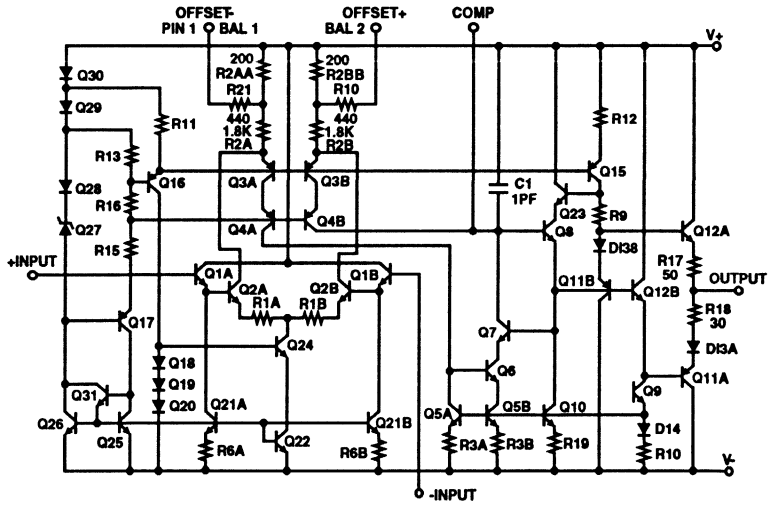
Electrical Specifications V+ = +15VDC, V- = -15VDC **(Continued)**

PARAMETER	TEMP	HA-2520-2 LIMITS			HA-2522-2 LIMITS			HA-2525-5 LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C	-	4	6	-	4	6	-	4	6	mA
Power Supply Rejection Ratio (Note 7)	Full	80	90	-	74	90	-	74	90	-	dB

NOTES:

1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. See Transient Response Test Circuits and Waveforms.
9. This parameter value is based on design calculations.
10. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
11. $V_{OUT} = \pm 5V$
12. Guaranteed by design.
13. Absolute Maximum Ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

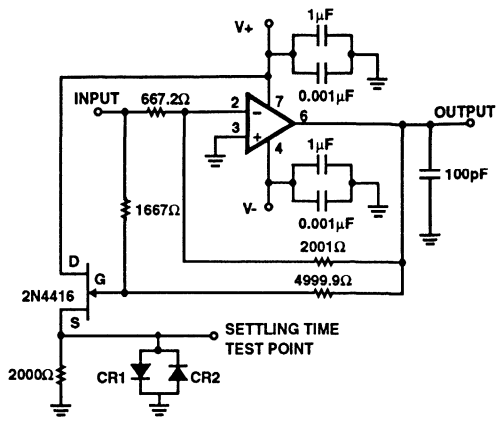
Schematic Diagram



Die Characteristics

Transistor Count		40
Die Dimensions		57 x 67 x 19 mils
Substrate Potential		Unbiased
Process		Bipolar-DI
Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Metal Can	117	36
Plastic Mini-DIP	96	34
Ceramic Mini-DIP	115	36
PLCC	74	33
SOIC	157	43

Settling Time Circuit



- $A_V = -3$
- Feedback and Summing Resistor Ratios should be 0.1% matched.
- Clipping Diodes CR1 and CR2 are optional. HP5082-2810 recommended.

Test Circuits

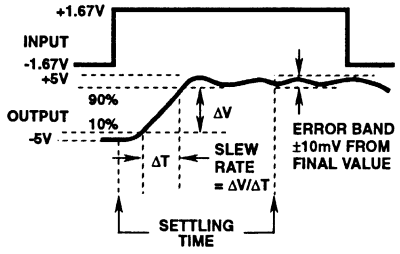


FIGURE 1. SLEW RATE AND SETTLING TIME

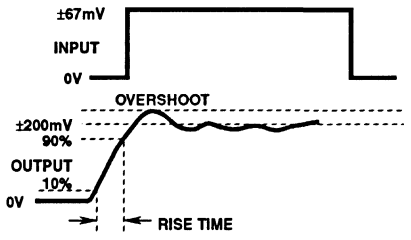


FIGURE 2. TRANSIENT RESPONSE

NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

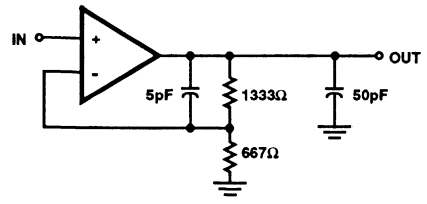


FIGURE 3. SLEW RATE AND TRANSIENT RESPONSE

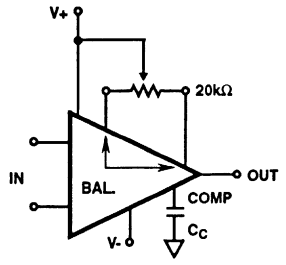


FIGURE 4. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK-UP

Tested offset adjustment range is $|V_{OS}| + 1mV|$ minimum referred to output. Typical ranges are ±20mV with $R_T = 20k\Omega$

Typical Performance Curves V+ = 15VDC, V- = -15VDC, T_A = +25°C, Unless Otherwise Specified

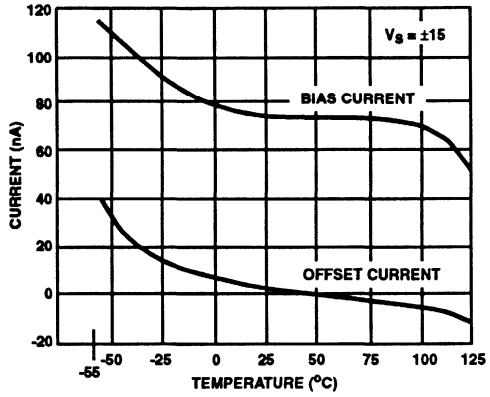


FIGURE 5. INPUT BIAS AND OFFSET CURRENTS vs TEMPERATURE

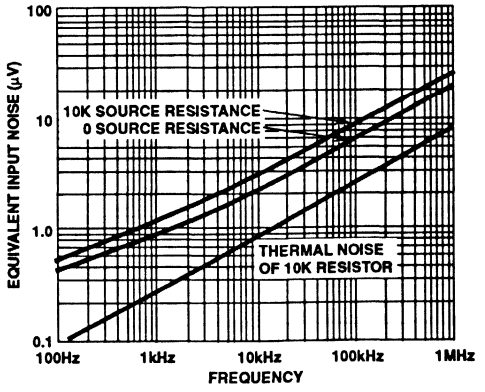


FIGURE 6. EQUIVALENT INPUT NOISE vs BANDWIDTH (WITH 10Hz HIGH PASS FILTER)

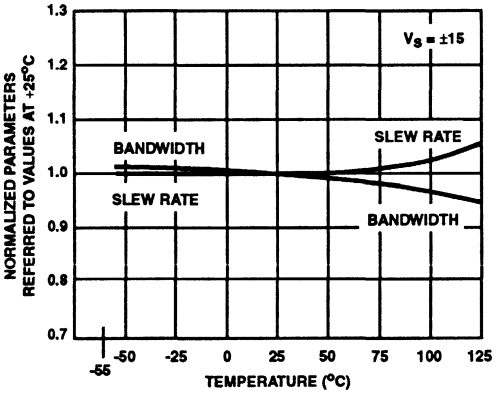


FIGURE 7. NORMALIZED AC PARAMETERS vs TEMPERATURE

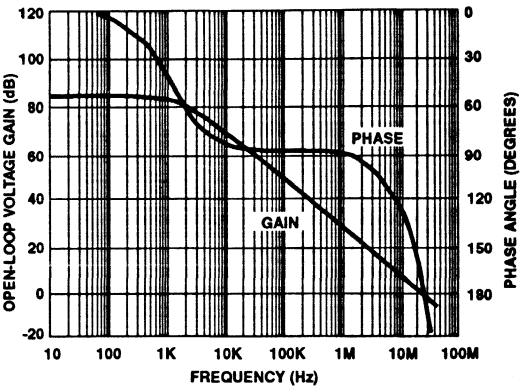


FIGURE 8. OPEN LOOP FREQUENCY AND PHASE RESPONSE

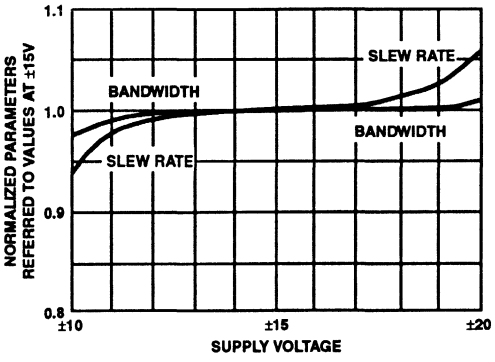


FIGURE 9. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C

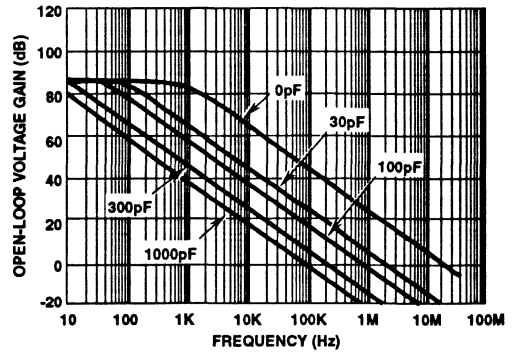


FIGURE 10. OPEN LOOP GAIN RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GND

NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

Typical Performance Curves $V+ = 15VDC, V- = -15VDC, T_A = +25°C$, Unless Otherwise Specified(Continued)

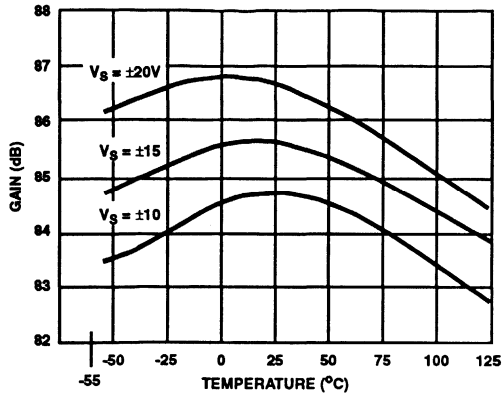


FIGURE 11. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

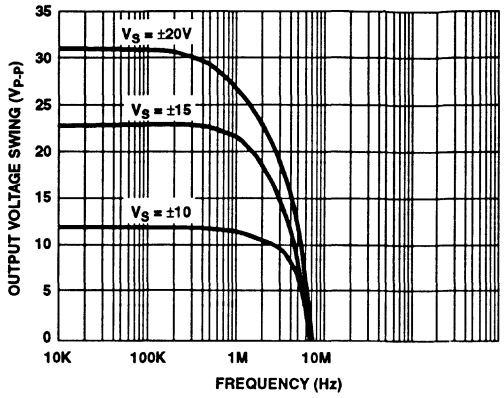


FIGURE 12. OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C

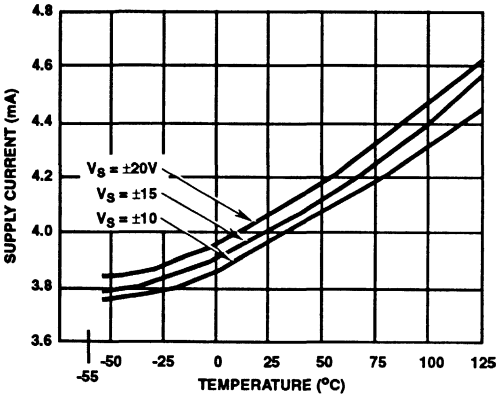


FIGURE 13. POWER SUPPLY CURRENT vs TEMPERATURE

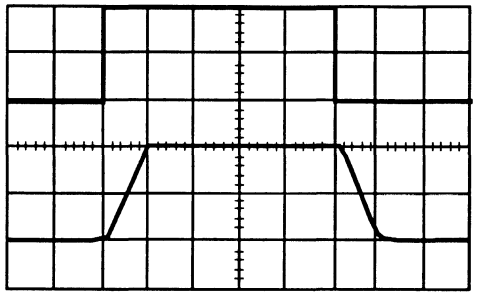


FIGURE 14. PULSE RESPONSE ($A_V = +3$)

$R_L = 2k\Omega$, $C_L = 50pF$, Horizontal = 100ns/Div.
Upper Trace: Input; 1.67V/Div., Lower Trace: Output; 5V/Div.
$T_A = +25°C$, $V_S = \pm 15V$

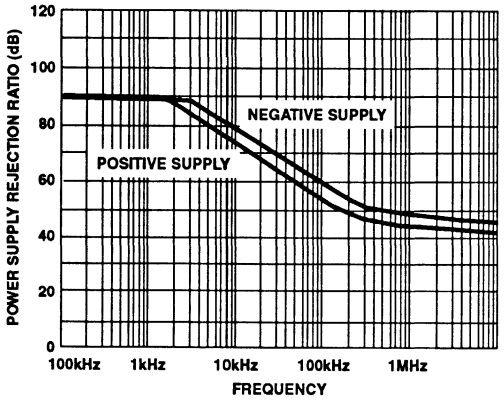
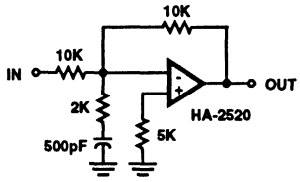


FIGURE 15. POWER SUPPLY REJECTION RATIO vs FREQUENCY

Typical Application



NOTE: Compensation Circuit for $A_V = -1$
Slew Rate ≈ 120V/µs
Bandwidth ≈ 10MHz
Settling Time (0.1%) ≈ 500ns
Capacitance at pin 8 must be minimized for maximum bandwidth.
Tested and functional with supply voltages from ±4V to ±15V.

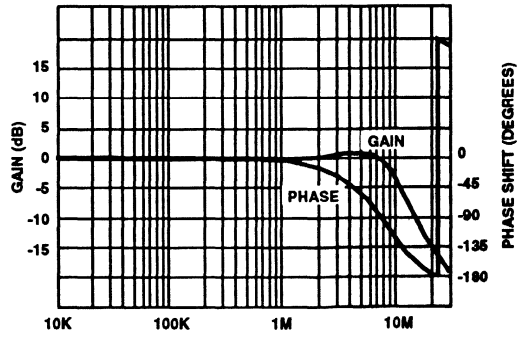


FIGURE 16. FREQUENCY RESPONSE FOR INVERTING UNITY GAIN CIRCUIT

HARRIS SEMICONDUCTOR

HA-2529

Uncompensated, High Slew Rate High Output Current, Operational Amplifier

March 1993

Features

- High Slew Rate 150V/µs
- Fast Settling 200ns
- Wide Power Bandwidth 2MHz
- Wide Gain Bandwidth ($A_V \geq 3$) 20MHz
- High Input Impedance 130MΩ
- Low Offset Current 5nA
- High Output Current ..... ±30mA

Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HA2-2529-2	-55°C to +125°C	8 Pin Can
HA2-2529-5	0°C to +75°C	8 Pin Can
HA3-2529-5	0°C to +75°C	8 Lead Plastic DIP
HA7-2529-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-2529-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P2529-5	0°C to +75°C	8 Lead SOIC

Description

The HA-2529 is a monolithic operational amplifier which typifies excellence of design. With a design based on years of experience coupled with the reliable dielectric isolation process, this amplifier provides an outstanding combination of DC and AC parameters at closed loop gains greater than 3.

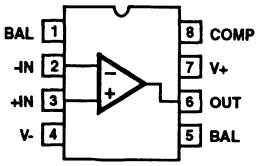
The HA-2529 offers 150V/µs slew rate and fast settling time (200ns), while consuming a mere 6mA of quiescent current, making this amplifier ideal for video circuitry and data acquisition designs. With 20MHz gain bandwidth combined with 7.5kV/V open loop gain, the HA-2529 is an ideal component for demanding signal conditioning designs. This device provides ±30mA output current drive with an output voltage swing of ±10V making it suited for pulse amplifier and R.F. amplifier components.

The HA-2529 will upgrade output current, slew rate, offset voltage drift and offset current drift in systems presently using the HA-2520/22/25 or EHA-2520/22/25.

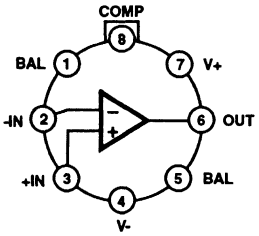
Mil-Std-883 product and data sheets are available upon request.

Pinouts

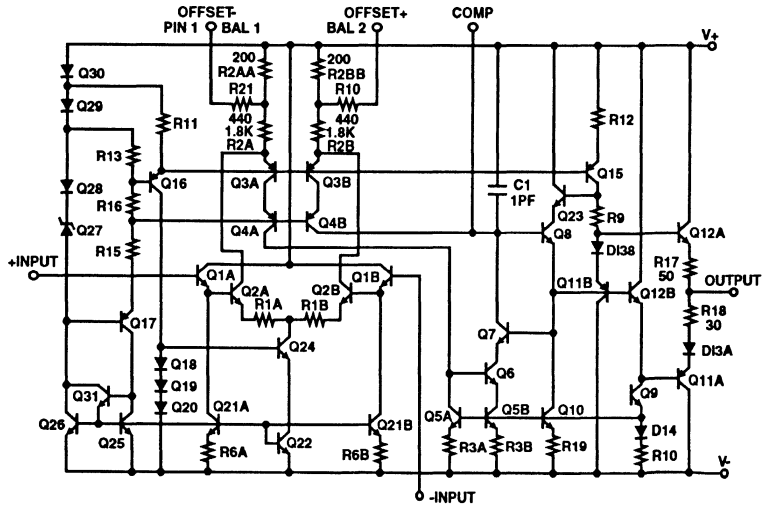
HA-2529
(PDIP, CDIP, SOIC)
TOP VIEW



HA-2529
(TO-99 CAN)
TOP VIEW



Schematic Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2895.1**

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage. 15V
Peak Output Current. 90mA
Internal Power Dissipation (Note 10) 300mW
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.). . . . . +300°C

Operating Conditions

Operating Temperature Range
HA-2529-2 . . . . . $-55°C \le T_A \le +125°C$
HA-2529-5 . . . . . $0°C \le T_A \le +75°C$
Storage Temperature Range . . . . . $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V_S = \pm15V$, $C_L = 50pF$, $R_L = 2k\Omega$, Unless Otherwise Specified

PARAMETER	TEMPERATURE	HA-2529-2 -55°C to +125°C			HA-2529-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage (Note 8)	+25°C	-	2	5	-	2	10	mV
	Full	-	-	8	-	-	14	mV
Average Offset Voltage Drift (Note 8)	Full	-	10	-	-	10	-	µV/°C
Bias Current (Note 8)	+25°C	-	50	200	-	50	250	nA
	Full	-	80	400	-	80	400	nA
Average Bias Current Drift (Note 8)	Full	-	0.2	-	-	0.2	-	nA/°C
Offset Current (Note 8)	+25°C	-	5	25	-	5	50	nA
	Full	-	10	50	-	10	100	nA
Average Offset Current Drift	Full	-	0.02	-	-	0.02	-	nA/°C
Common Mode Range	Full	±10	±13	-	±10	±13	-	V
Differential Input Resistance (Note 11)	+25°C	50	130	-	50	130	-	MΩ
Differential Input Capacitance	+25°C	-	3	-	-	3	-	pF
Input Noise Voltage (f = 1kHz)	+25°C	-	20	-	-	20	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C	-	1.8	-	-	1.8	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	10	18	-	7.5	18	-	kV/V
	Full	7.5	15	-	5	15	-	kV/V
Common Mode Rejection Ratio (Note 5)	Full	80	100	-	74	100	-	dB
Gain Bandwidth Product (Note 2, 11)	+25°C	15	20	-	15	20	-	MHz
Minimum Stable Gain	+25°C	3	-	-	3	-	-	V/V
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10	±12	-	±10	±12	-	V
Full Power Bandwidth (Notes 3 & 6)	+25°C	2.1	2.6	-	2.1	2.6	-	MHz
Output Current (Note 8)	+25°C	30	35	-	30	35	-	mA
	Full	25	30	-	25	30	-	mA
Output Resistance (Open Loop)	+25°C	-	30	-	-	30	-	Ω
TRANSIENT RESPONSE (A_V = +3)								
Rise Time (Note 2, 7)	+25°C	-	20	45	-	20	50	ns
Overshoot (Note 2, 7)	+25°C	-	10	30	-	10	30	%
Slew Rate (Note 3, 7)	+25°C	135	150	-	135	150	-	V/µs
Settling Time (Note 4, 7)	+25°C	-	200	-	-	200	-	ns

Electrical Specifications $V_S = \pm15V$, $C_L = 50pF$, $R_L = 2k\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMPERATURE	HA-2529-2 -55°C to +125°C			HA-2529-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	4.5	6	-	4.5	6	mA
Power Supply Rejection Ratio (Note 12)	Full	80	90	-	74	90	-	dB

NOTES:

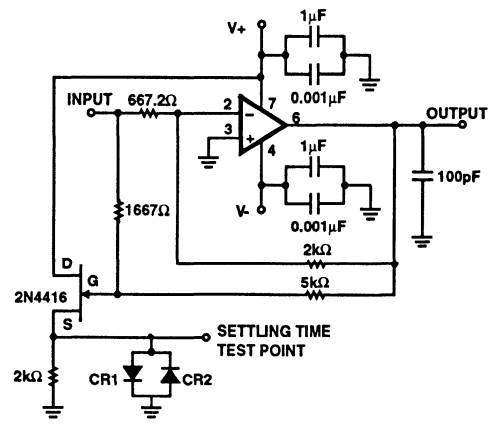
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $V_{OUT} = \pm200mV$, $A_V \geq 3$.
3. $V_{OUT} = \pm10V$.
4. Settling Time is specified to 0.1% of final value for a 10V output step and $A_V = -3$.
5. $\Delta V_{CM} = \pm10V$.
6. Full Power Bandwidth is guaranteed by equation: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
7. See Transient Response and Settling Time Test Circuits.
8. Refer to typical performance curve in data sheet.
9. $V_{OUT} = \pm5V$.
10. Refer to package thermal constants in Die Characteristics section.
11. Parameter is guaranteed by design and characterization data.
12. $\Delta V_S = \pm10V$ to $\pm20V$.

Die Characteristics

Transistor Count 40
Die Dimensions ..... 57 x 67 x 19 mils
Substrate Potential ..... V-
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Metal Can	117	36
Plastic Mini-DIP	96	34
Ceramic Mini-DIP	115	36
SOIC	157	43

Settling Time Circuit



- $A_V = -3$
- Feedback and summing resistor ratios should be 0.1% matched.
- Clipping diodes CR1 and CR2 are optional. HP5082-2810 recommended.

Test Circuits

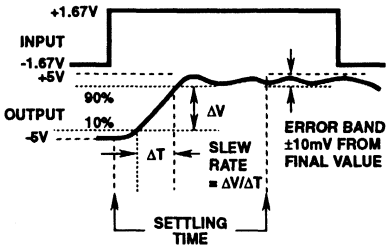


FIGURE 1. SLEW RATE AND SETTLING TIME

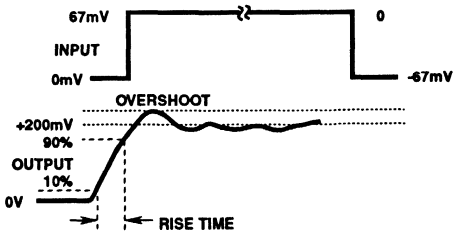


FIGURE 2. TRANSIENT RESPONSE

NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

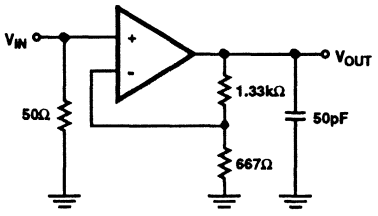


FIGURE 3. SLEW RATE AND TRANSIENT RESPONSE

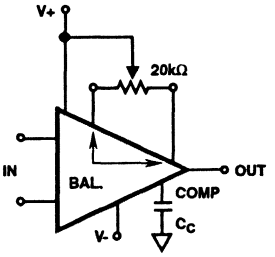
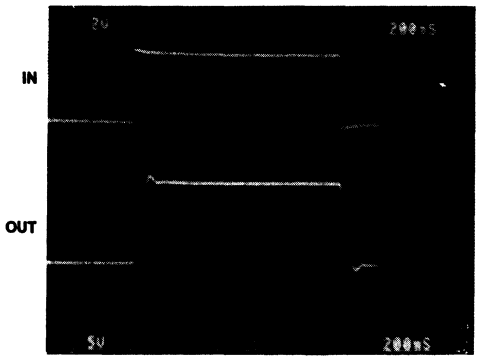


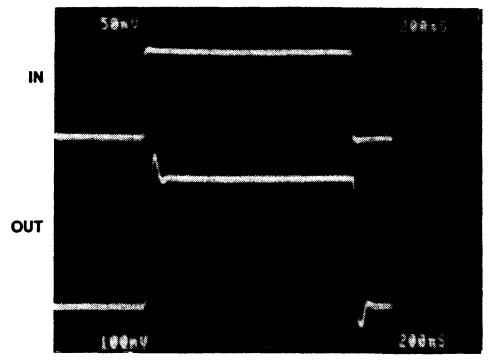
FIGURE 4. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK UP

Tested offset adjustment range is $|V_{OS} + 1mV|$ minimum referred to output. Typical ranges are +28mV to -18mV with $R_T = 20k\Omega$

LARGE SIGNAL RESPONSE
Horizontal Scale: (200ns/Div.)
Vertical Scale: (2V/Div. Input)
(5V/Div. Output).



SMALL SIGNAL RESPONSE
Horizontal Scale: (200ns/Div.)
Vertical Scale: (50mV/Div. Input)
(100mV/Div. Output).



Typical Performance Curves

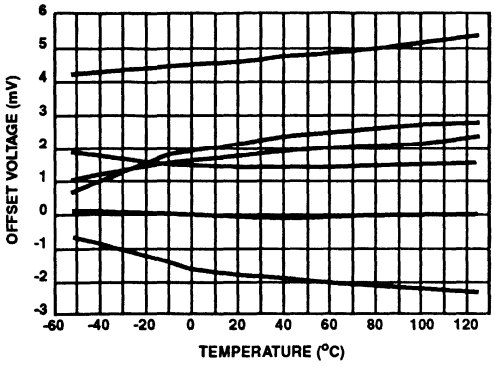


FIGURE 5. OFFSET VOLTAGE vs TEMPERATURE (6 TYPICAL UNITS FROM 3 LOTS AT V_S = ±15V)

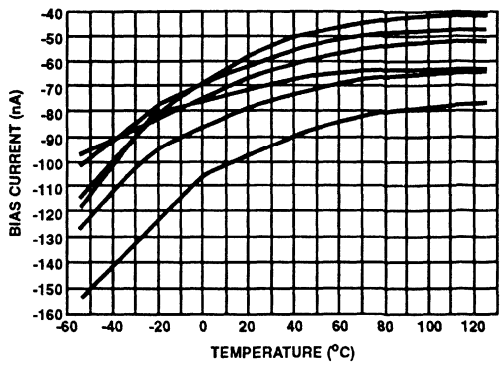


FIGURE 6. BIAS CURRENT vs TEMPERATURE (6 TYPICAL UNITS FROM 3 LOTS AT V_S = ±15V)

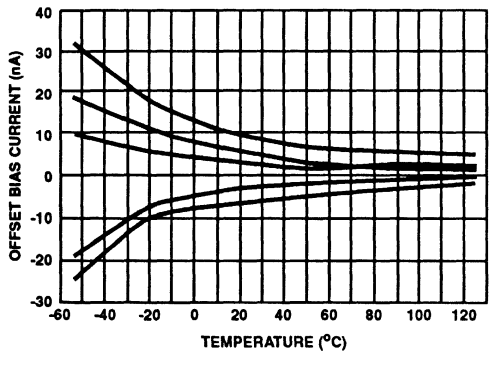


FIGURE 7. OFFSET CURRENT vs TEMPERATURE (5 TYPICAL UNITS FROM 3 LOTS AT V_S = ±15V)

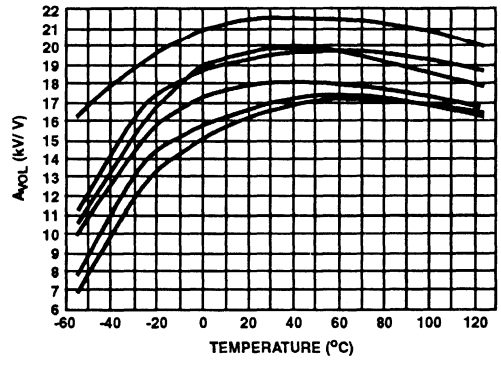


FIGURE 8. OPEN LOOP GAIN vs TEMPERATURE (6 TYPICAL UNITS FROM 3 LOTS AT V_S = ±15V)

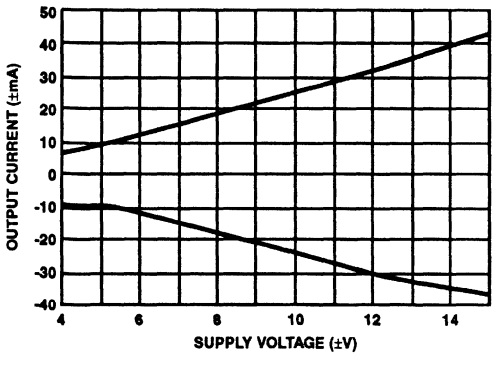


FIGURE 9. OUTPUT CURRENT vs SUPPLY VOLTAGE

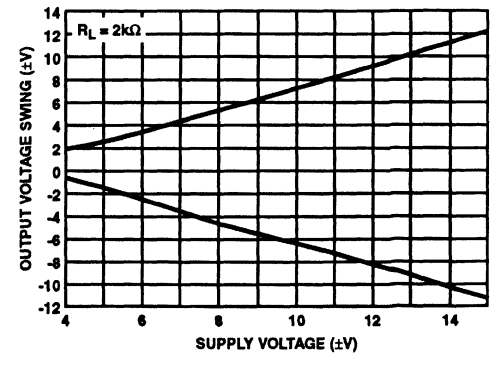


FIGURE 10. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

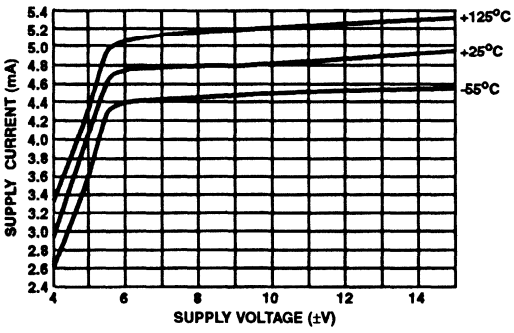


FIGURE 11. SUPPLY CURRENT vs SUPPLY VOLTAGE (OVER FULL TEMPERATURE)

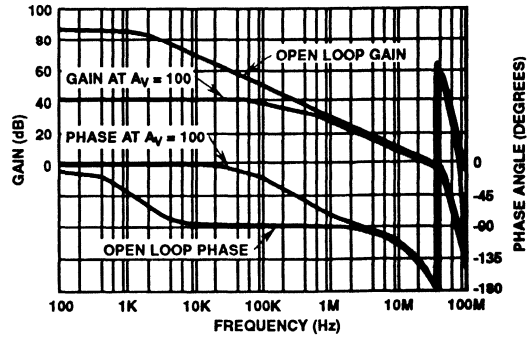


FIGURE 12. FREQUENCY RESPONSE AT VARIOUS GAINS

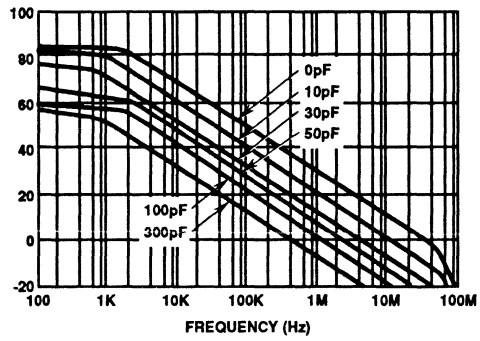


FIGURE 13. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMP PIN TO GROUND

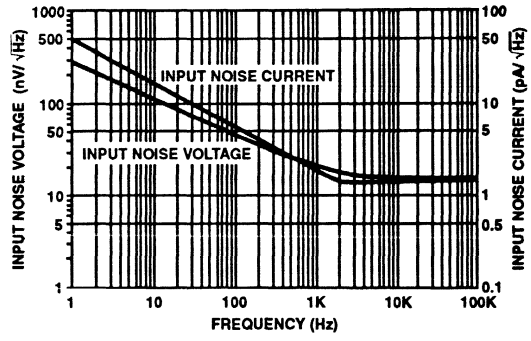


FIGURE 14. INPUT NOISE CHARACTERISTICS

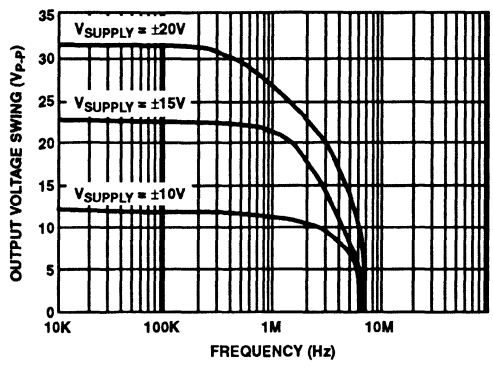


FIGURE 15. OUTPUT VOLTAGE SWING vs FREQUENCY

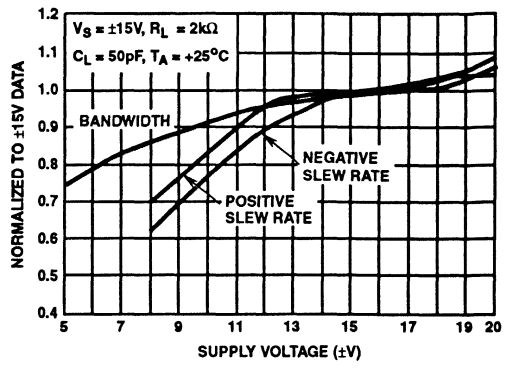
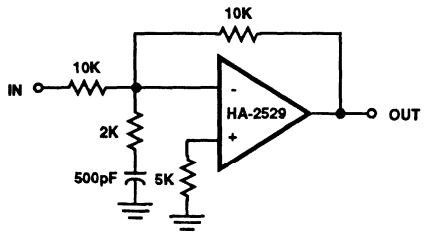
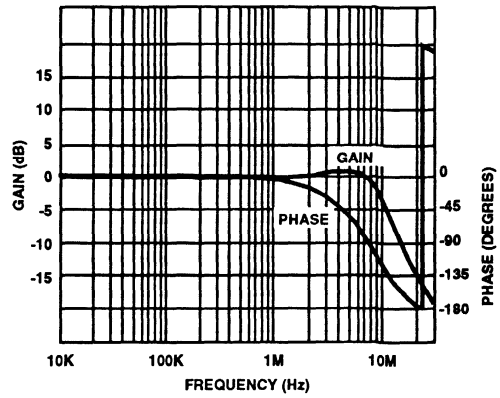


FIGURE 16. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

Typical Applications





NOTES:

- Compensation Circuit for A_V = -1
- Slew Rate ≈ 120V/µs
- Bandwidth ≈ 10MHz
- Settling Time (0.1%) ≈ 500ns
- Capacitance at pin 8 must be minimized for maximum bandwidth.
- Tested and functional with supply voltages from ±4V to ±15V.

FIGURE 17. FREQUENCY RESPONSE FOR INVERTING UNITY GAIN CIRCUIT

HARRIS SEMICONDUCTOR

HA-2539

Very High Slew Rate Wideband Operational Amplifier

March 1993

Features

- Very High Slew Rate 600V/μs
- Open Loop Gain 15kV/V
- Wide Gain-Bandwidth ($A_V \geq 10$) 600MHz
- Power Bandwidth 9.5MHz
- Low Offset Voltage 8mV
- Input Voltage Noise ..... 6nV/√Hz
- Output Voltage Swing ..... ±10V
- Monolithic Bipolar Dielectric Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

Description

The Harris HA-2539 represents the ultimate in high slew rate, wideband, monolithic operational amplifiers. It has been designed and constructed with the Harris High Frequency Bipolar Dielectric Isolation process and features dynamic parameters never before available from a truly differential device.

With a 600V/ms slew rate and a 600MHz gain bandwidth product, the HA-2539 is ideally suited for use in video and RF amplifier designs, in closed loop gains of 10 or greater. Full ±10V swing coupled with outstanding AC parameters and complemented by high open loop gain makes the devices useful in high speed data acquisition systems.

For further design assistance please refer to Application Note 541 (Using the HA-2539 Very High Slew Rate Wideband Operational Amplifiers) and Application Note 556 (Thermal Safe-Operating-Areas For High Current Operational Amplifiers.

For military grade product information, the HA-2539/883 data sheet is available upon request.

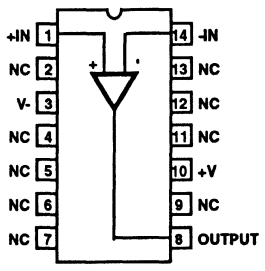
For a lower power version of this product, please see the HA-2839 and HA-2840 data sheets.

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HA1-2539-2	-55°C to +125°C	14 Lead Ceramic DIP
HA1-2539-5	0°C to +75°C	14 Lead Ceramic DIP
HA1-2539-9	-40°C to +85°C	14 Lead Ceramic DIP
HA1-2539C-5	0°C to +75°C	14 Lead Ceramic DIP
HA1-2539C-9	-40°C to +85°C	14 Lead Ceramic DIP
HA3-2539-5	0°C to +75°C	14 Lead Plastic DIP
HA3-2539-9	-40°C to +85°C	14 Lead Plastic DIP
HA3-2539C-5	0°C to +75°C	14 Lead Plastic DIP
HA4P2539-5	0°C to +75°C	20 Lead PLCC
HA9P2539-5	0°C to +75°C	14 Lead SOIC
HA9P2539-9	-40°C to +85°C	14 Lead SOIC
HA9P2539C-5	0°C to +75°C	14 Lead SOIC
HA9P2539C-9	-40°C to +85°C	14 Lead SOIC

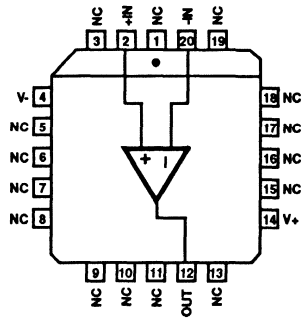
Pinouts

HA-2539
(PDIP, CDIP, SOIC)
TOP VIEW



(NC) No Connection pins may be tied to a ground plane for better isolation and heat dissipation.

HA-2539 (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2896.1**

Absolute Maximum Ratings (Note 1)

Supply Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Peak Output Current 50mA
Continuous Output Current ..... $33mA_{rms}$
Internal Quiescent Power Dissipation (Note 2)
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-2539-2 ..... $-55°C \le T_A \le +125°C$
HA-2539/2539C-5 ..... $0°C \le T_A \le +75°C$
HA-2539-9 ..... $-40°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified.

PARAMETER	TEMP	HA-2539-2 LIMITS			HA-2539-5, -9 LIMITS			HA-2539C-5, -9 LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	-	8	10	-	8	15	-	8	15	mV
	Full	-	13	15	-	13	20	-	13	20	mV
Average Offset Voltage Drift	Full	-	20	-	-	20	-	-	20	-	µV/°C
Bias Current	+25°C	-	5	20	-	5	20	-	5	20	µA
	Full	-	-	25	-	-	25	-	-	25	µA
Offset Current	+25°C	-	1	6	-	1	6	-	1	6	µA
	Full	-	-	8	-	-	8	-	-	8	µA
Input Resistance	+25°C	-	10	-	-	10	-	-	10	-	kΩ
Input Capacitance	+25°C	-	1	-	-	1	-	-	1	-	pF
Common Mode Range	Full	±10.0	-	-	±10.0	-	-	±10.0	-	-	V
Input Current Noise ($f = 1kHz$, $R_{SOURCE} = 0\Omega$)	+25°C	-	6	-	-	6	-	-	6	-	$pA/\sqrt{Hz}$
Input Voltage Noise ($f = 1kHz$, $R_{SOURCE} = 0\Omega$)	+25°C	-	6	-	-	6	-	-	6	-	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 3)	+25°C	10	15	-	10	15	-	7	10	-	kV/V
	Full	5	-	-	5	-	--	5	-	-	kV/V
Common Mode Rejection Ratio (Note 4)	Full	60	72	-	60	72	-	60	72	-	dB
Minimum Stable Gain	+25°C	10	-	-	10	-	-	10	-	-	V/V
Gain Bandwidth (Notes 5, 6)	+25°C	-	600	-	-	600	0	0	600	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 3, 10)	Full	±10.0	–	-	±10.0	–	-	±10.0	–	-	V
Output Current (Note 3)	+25°C	±10	±20	-	±10	±20	-	±10	±20	-	mA
Output Resistance	+25°C	-	30	-	-	30	-	-	30	-	Ω
Full Power Bandwidth (Notes 3, 7)	+25°C	8.7	9.5	-	8.7	9.5	-	8.7	9.5	-	MHz
TRANSIENT RESPONSE (Note 8)											
Rise Time	+25°C	-	7	-	-	7	-	-	7	-	ns
Overshoot	+25°C	-	15	-	-	15	-	-	15	-	%
Slew Rate	+25°C	550	600	-	550	600	-	550	600	-	V/µs
Settling Time: 10V Step to 0.1%	+25°C	-	180	-	-	180	-	-	200	-	ns
POWER REQUIREMENTS											

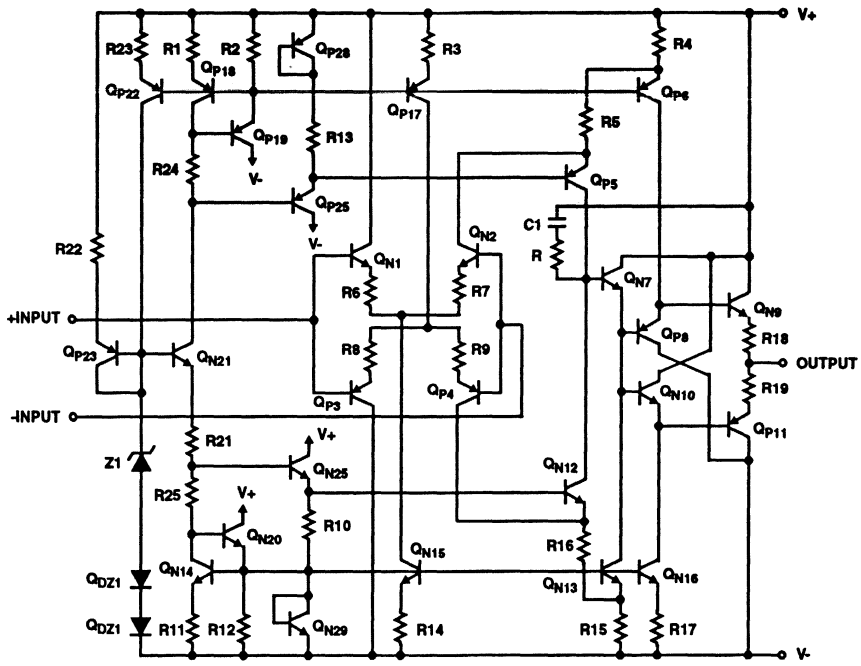
Electrical Specifications V_{SUPPLY} = ±15V, R_L = 1kΩ, C_L < 10pF, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEMP	HA-2539-2 LIMITS			HA-2539-5, -9 LIMITS			HA-2539C-5, -9 LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	Full	-	20	25	-	20	25	-	20	25	mA
Power Supply Rejection Ratio (Note 9)	Full	60	70	-	60	70	-	60	70	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C for the ceramic package and below +150°C for the plastic packages. By using Application Note 556 on Safe Operating Area equations, along with the packaging thermal resistances listed in the Die Characteriistics section, proper load conditions can be determined. Heat sinking is recommended above +75°C with suggested models:
   Thermalloy #6007 (θ_{SA} = 40°C/W) or AAVID #5602B (θ_{SA} = 16°C/W).
3. R_L = 1kΩ, V_O = ±10V
4. V_{CM} = ±10.0V
5. V_O = 90mV
6. A_V = 10
7. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Refer to Test Circuits section of data sheet.
9. V_{SUPPLY} = +5V, -15V and +15V, -5V
10. Guaranteed range for output voltage is ±10V. Functional operation outside of this range is not guaranteed.

Schematic Diagram



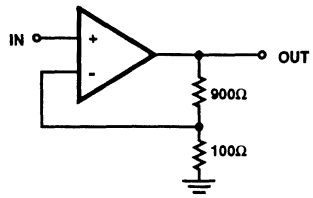
Die Characteristics

Transistor Count 30
Die Dimensions ..... 75 x 61 x 19 mils (1910µm x 1550µm x 483µm)
Substrate Potential (Power Up)* ..... V-
Process ..... High Frequency Bipolar-DI
Passivation ..... Nitride

* The substrate may be left floating (Insulating Die Mount) or it may be mounted on conductor at V- potential.

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	71	14
Plastic DIP	107	38
SOIC	119	36
PLCC	74	33

Test Circuits



$V_S = \pm 15V$
$A_V = +10$
$C_L \leq 10pF$

FIGURE 1. TEST CIRCUIT

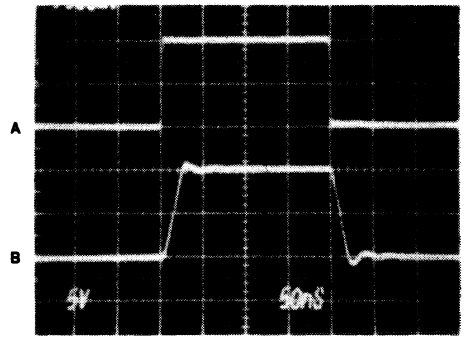


FIGURE 2. LARGE SIGNAL RESPONSE
Vertical Scale: A = 0.5V/Div., B = 5.0V/Div.
Horizontal Scale: Time: 50ns/Div.

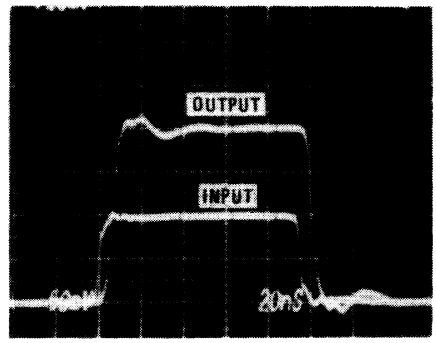
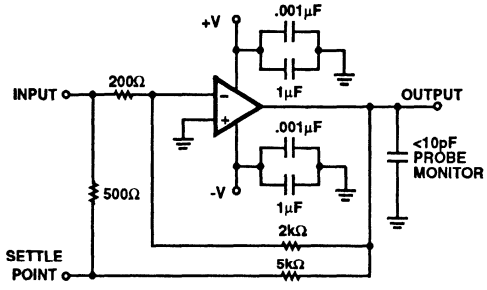


FIGURE 3. SMALL SIGNAL RESPONSE
Vertical Scale: Input = 10mV/Div., Output = 50mV/Div.
Horizontal Scale: 20ns/Div.



- $A_V = -10$
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

FIGURE 4. SETTLING TIME CIRCUIT

Typical Performance Curves

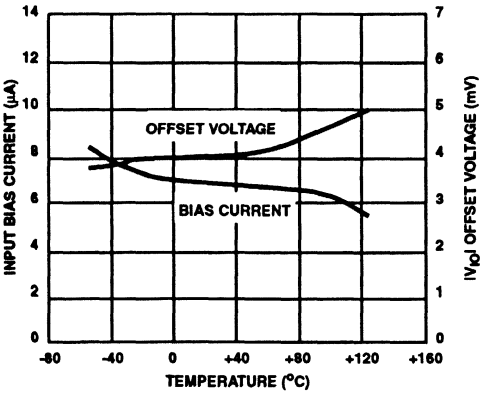


FIGURE 5. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs TEMPERATURE

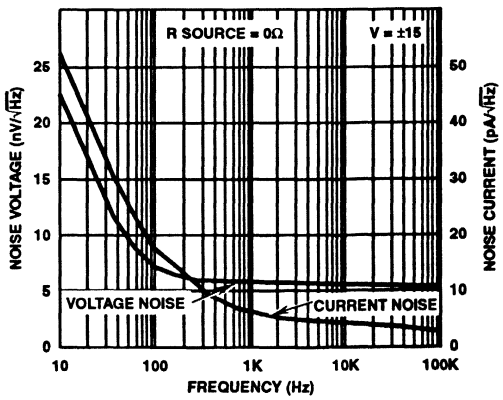


FIGURE 6. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY

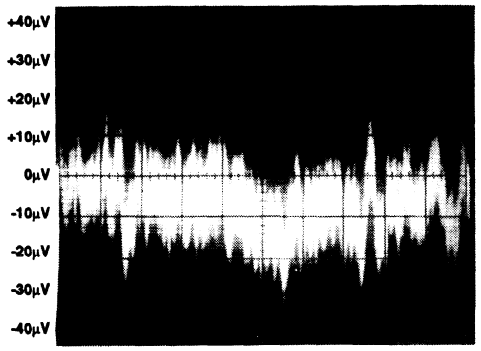


FIGURE 7. BROADBAND NOISE (0.1HZ TO 1MHZ)
Vertical Scale: 10mV/Div.
Horizontal Scale: 50ms/Div.

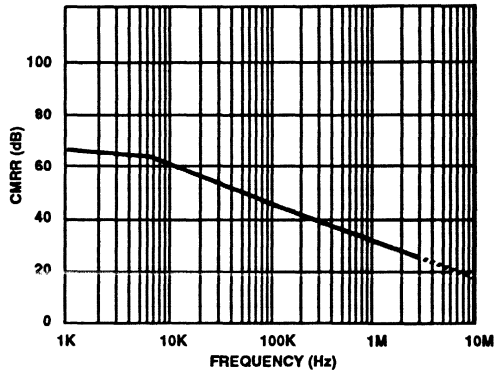


FIGURE 8. COMMON MODE REJECTION RATIO vs FREQUENCY

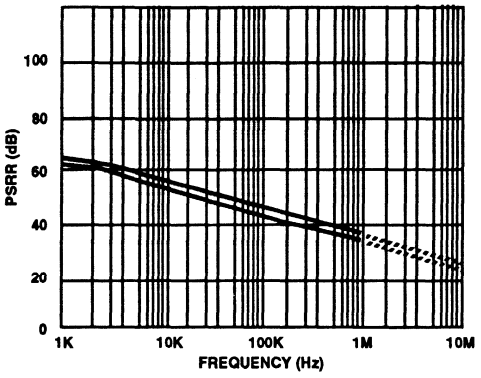


FIGURE 9. POWER SUPPLY REJECTION RATIO vs FREQUENCY

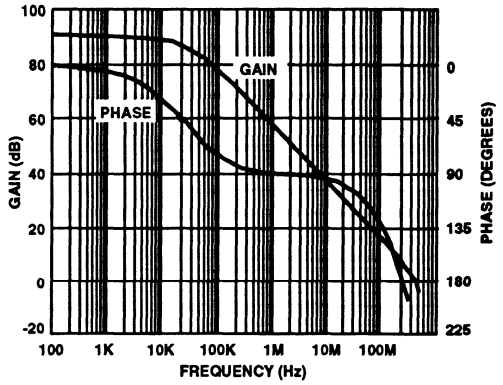


FIGURE 10. OPEN LOOP GAIN/PHASE vs FREQUENCY

Typical Performance Curves (Continued)

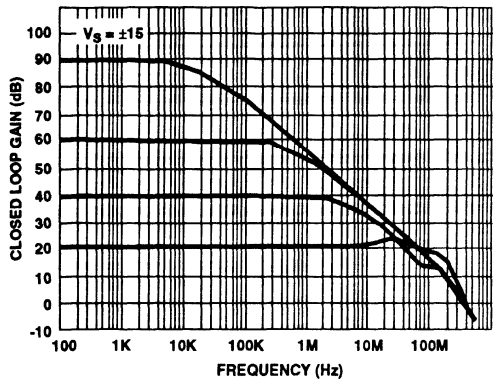


FIGURE 11. CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS

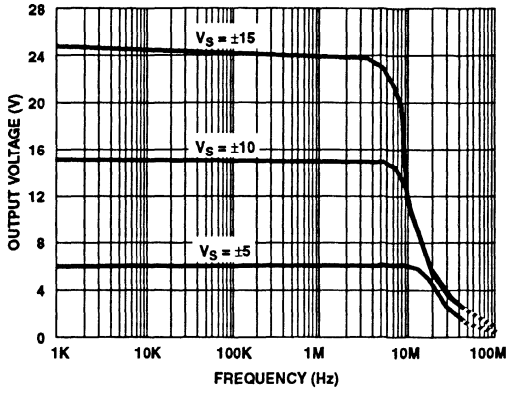


FIGURE 12. OUTPUT VOLTAGE SWING vs FREQUENCY

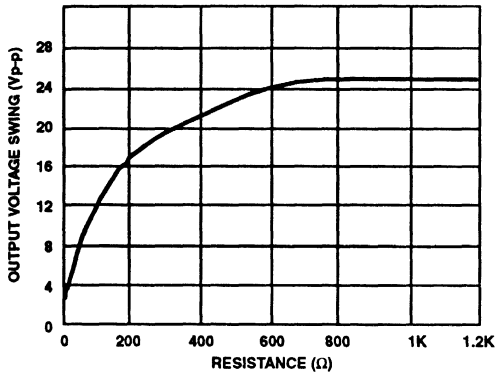


FIGURE 13. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

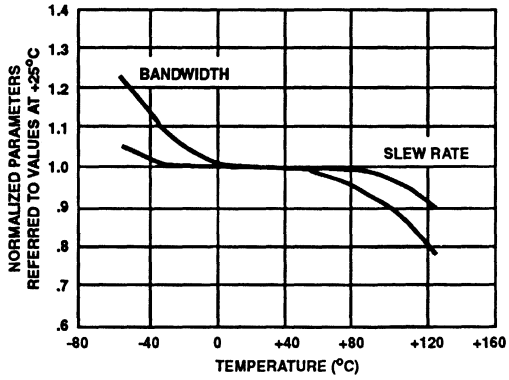


FIGURE 14. NORMALIZED AC PARAMETERS vs TEMPERATURE

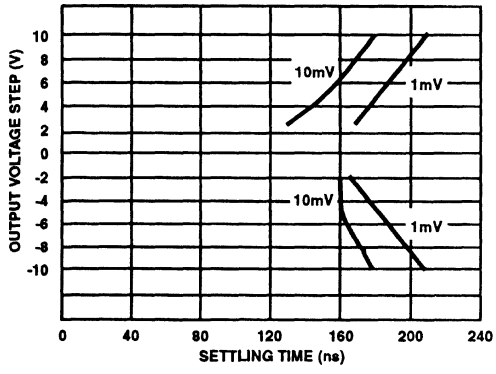


FIGURE 15. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

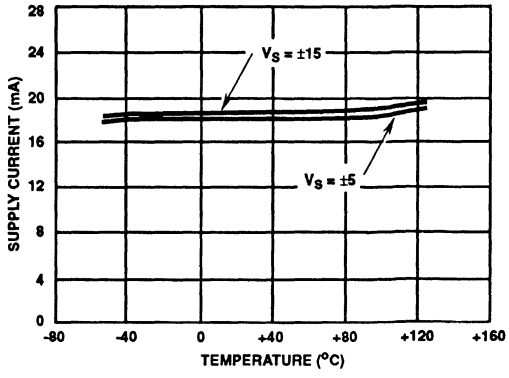


FIGURE 16. POWER SUPPLY CURRENT vs TEMPERATURE AND SUPPLY VOLTAGE

Typical Applications

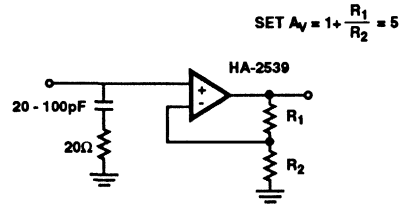


FIGURE 17. FREQUENCY COMPENSATION BY OVERDAMPING

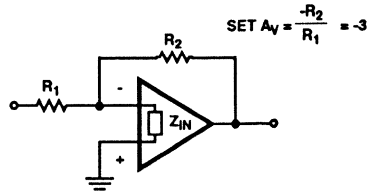


FIGURE 18. STABILIZATION USING Z_{IN}

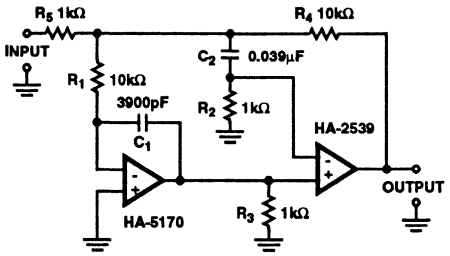


FIGURE 19. REDUCING DC ERRORS; COMPOSITE AMPLIFIER

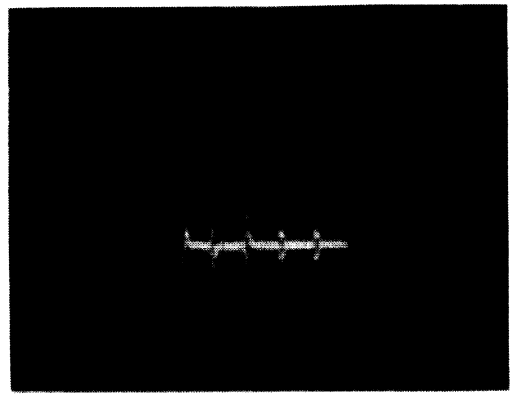


FIGURE 20. DIFFERENTIAL GAIN ERROR (3%) HA-2539 20dB VIDEO GAIN BLOCK

HARRIS SEMICONDUCTOR

HA-2540

Wideband, Fast Settling Operational Amplifier

March 1993

Features

- Very High Slew Rate 400V/µs
- Fast Settling Time 140ns
- Wide Gain Bandwidth ($A_V \geq 10$) 400MHz
- Power Bandwidth 6MHz
- Low Offset Voltage 8mV
- Input Voltage Noise ..... 6nV/$\sqrt{Hz}$
- Output Voltage Swing ..... ±10V
- Monolithic Bipolar Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-2540-2	-55°C to +125°C	14 Lead Ceramic DIP
HA1-2540-5	0°C to +75°C	14 Lead Ceramic DIP
HA1-2540-9	-40°C to +85°C	14 Lead Ceramic DIP
HA1-2540C-5	0°C to +75°C	14 Lead Ceramic DIP
HA1-2540C-9	-40°C to +85°C	14 Lead Ceramic DIP
HA3-2540-5	0°C to +75°C	14 Lead Plastic DIP
HA3-2540-9	-40°C to +85°C	14 Lead Plastic DIP
HA3-2540C-5	0°C to +75°C	14 Lead Plastic DIP
HA4P2540-5	0°C to +75°C	20 Lead PLCC
HA9P2540-5	0°C to +75°C	14 Lead SOIC
HA9P2540-9	-40°C to +85°C	14 Lead SOIC
HA9P2540C-5	0°C to +75°C	14 Lead SOIC
HA9P2540C-9	-40°C to +85°C	14 Lead SOIC

Description

The Harris HA-2540 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance in circuits where closed loop gain is 10 or greater. Additionally, the HA-2540 has a drive capability of ±10V into a 1kΩ load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

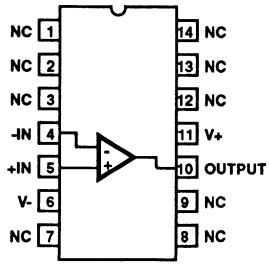
A 400V/µs slew rate ensures high performance in video and pulse amplification circuits, while the 400MHz gain-bandwidth product is ideally suited for wideband signal amplification. A settling time of 140ns also makes the HA-2540 an excellent selection for high speed Data Acquisition Systems.

Refer to Application Note 541 and Application Note 556 for more information on High Speed Op Amp applications. HA-2540/883 MIL-STD-883 data sheet is available on request.

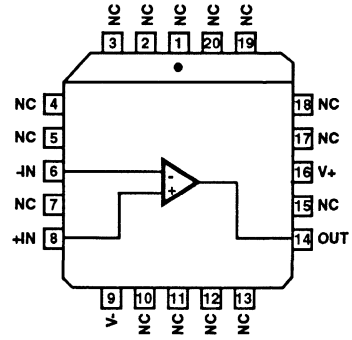
For a lower power version of this product, please see the HA-2840 and HA-2850 datasheets.

Pinouts

HA-2540 (CDIP, PDIP, SOIC)
TOP VIEW



HA-2540 (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2897.1**

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Output Current .....33mArms (Continuous), 50mA (Peak)
Internal Power Dissipation (Note 2)
Junction Temperature ..... +175°C
Junction Temperature (Plastic Packages) ..... +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-2540-2 ..... $-55°C \le T_A \le +125°C$
HA-2540/2540C-5 ..... $0°C \le T_A \le +75°C$
HA-2540/2540C-9 ..... $-40°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified.

PARAMETER	TEMP	HA-2540-2			HA-2540-5, -9			HA-2540C-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	-	8	10	-	8	15	-	8	15	mV
	Full	-	13	15	-	13	20	-	13	20	mV
Average Offset Voltage Drift	Full	-	20	-	-	20	-	-	20	-	µV/°C
Bias Current	+25°C	-	5	20	-	5	20	-	5	20	µA
	Full	-	-	25	-	-	25	-	-	25	µA
Offset Current	+25°C	-	1	6	-	1	6	-	1	6	µA
	Full	-	-	8	-	-	8	-	-	8	µA
Input Resistance	+25°C	-	10	-	-	10	-	-	10	-	kΩ
Input Capacitance	+25°C	-	1	-	-	1	-	-	1	-	pF
Common Mode Range	Full	±10	-	-	±10	-	-	±10	-	-	V
Input Noise Current ($f = 1kHz$, $R_{SOURCE} = 0\Omega$)	+25°C	-	6	-	-	6	-	-	6	-	$pA/\sqrt{Hz}$
Input Noise Voltage ($f = 1kHz$, $R_{SOURCE} = 0\Omega$)	+25°C	-	6	-	-	6	-	-	6	-	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	10	15	-	10	15	-	7	10	-	kV/V
	Full	5	-	-	5	-	-	5	-	-	kV/V
Common-Mode Rejection Ratio (Note 4)	Full	60	72	-	60	72	-	60	72	-	dB
Minimum Stable Gain	+25°C	10	-	-	10	-	-	10	-	-	V/V
Gain Bandwidth Product (Notes 5 & 6)	+25°C	-	400	-	-	400	-	-	400	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 3, 10)	Full	±10	-	-	±10	-	-	±10	-	-	V
Output Current (Note 3)	+25°C	±10	±20	-	±10	±20	-	±10	±20	-	mA
Output Resistance	+25°C	-	30	-	-	30	-	-	30	-	Ω
Full Power Bandwidth (Notes 3, 7)	+25°C	5.5	6	-	5.5	6	-	5.5	6	-	MHz

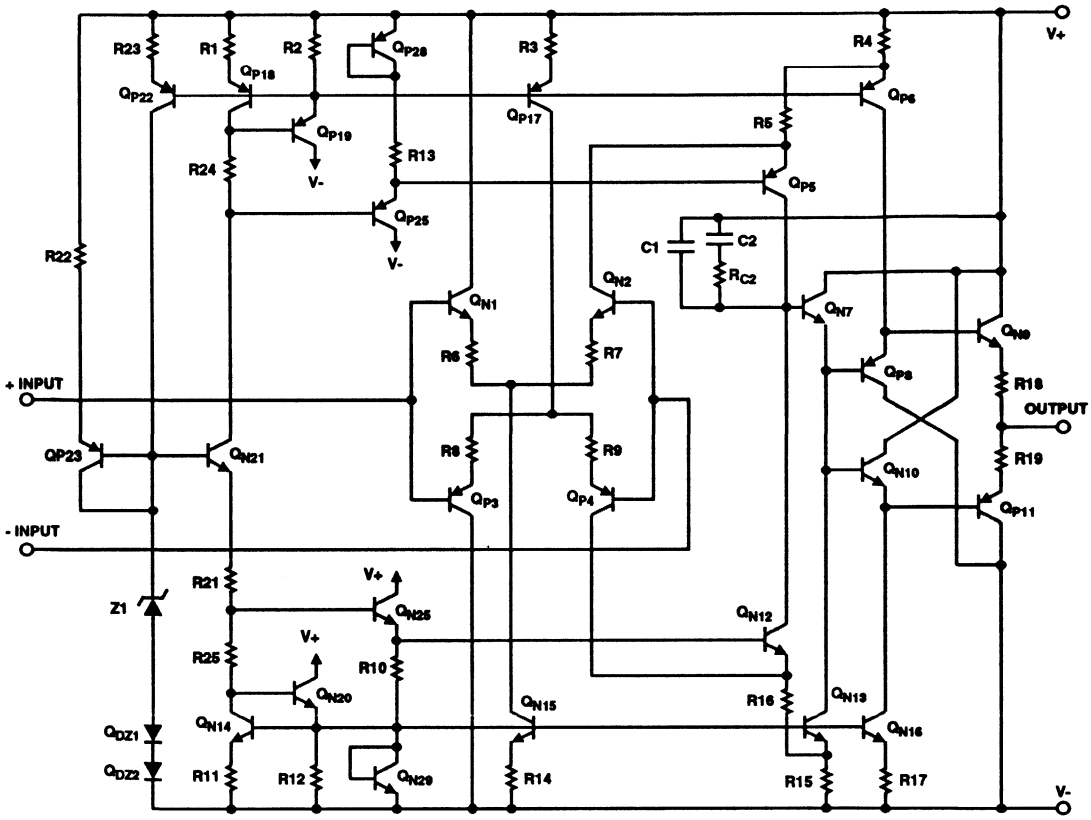
Electrical Specifications V_{SUPPLY} = ±15V, R_L = 1kΩ, C_L < 10pF, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEMP	HA-2540-2			HA-2540-5, -9			HA-2540C-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 8)											
Rise Time	+25°C	-	14	-	-	14	-	-	14	-	ns
Overshoot	+25°C	-	5	-	-	5	-	-	5	-	%
Slew Rate	+25°C	320	400	-	320	400	-	320	400	-	V/µs
Settling Time: 10V Step to 0.1%	+25°C	-	140	-	-	140	-	-	140	-	ns
POWER REQUIREMENTS											
Supply Current	Full	-	20	25	-	20	25	-	20	25	mA
Power Supply Rejection Ratio (Note 9)	Full	60	70	-	60	70	-	60	70	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C for the ceramic package, and below +150°C for the plastic package. By using Application Note 556 on Safe Operating Area Equations, along with the packaging thermal resistances listed in the Die Characteristics section, proper load conditions can be determined. Heat sinking is recommended above +75°C with suggested models:
   Thermalloy #6007 ($\theta_{SA} \cong 40°C/W$) or AAVID #5602B ($\theta_{SA} \cong 16°C/W$).
3. R_L = 1kΩ, V_O = ±10V.
4. V_{CM} = ±10V.
5. V_O = 90mV.
6. A_V = 10.
7. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
8. Refer to Test Circuits section of the data sheet.
9. V_{SUPPLY} = +5V, -15V and +15V, -5V.
10. Guaranteed range for output voltage is ±10V. Functional operation outside of this range is not guaranteed.

Schematic Diagram



Die Characteristics

Transistor Count 30
Die Dimensions ..... 75 x 61 x 19 mils
(1910µm x 1550µm x 483µm)
Substrate Potential (Power Up)* ..... V-
Process ..... High Frequency Bipolar-DI
Passivation ..... Nitride

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	71	14
Plastic DIP	107	38
SOIC	119	36
PLCC	74	33

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Test Circuits

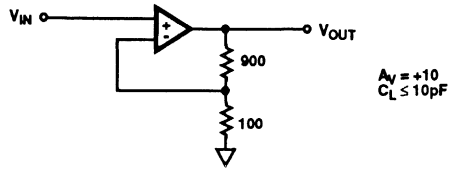
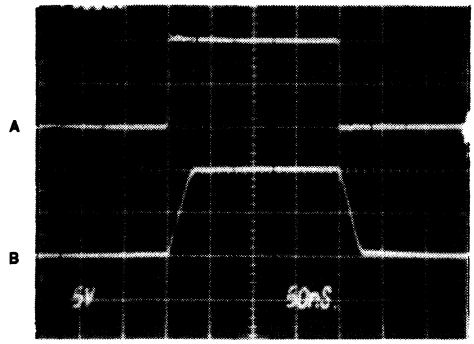
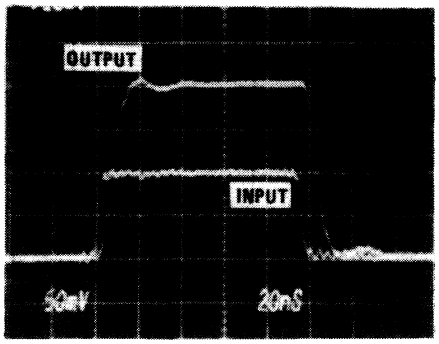


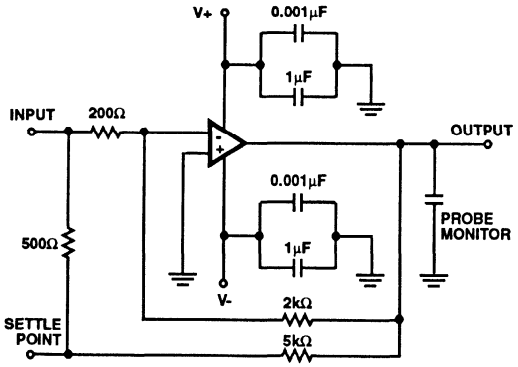
FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: A = 0.5V/Div., B = 5.0V/Div.)
Horizontal Scale: (Time: 50ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale: Input = 10mV/Div.; Output = 50mV/Div.
Horizontal Scale: 20ns/Div.





- A_V = -10.
- Load Capacitance should be less than 10pF. Turn on time delay typically 4ns.
- It is recommended that resistors be carbon composition and the feedback and summing network ratios be matched to 0.1%.
- SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Performance Curves

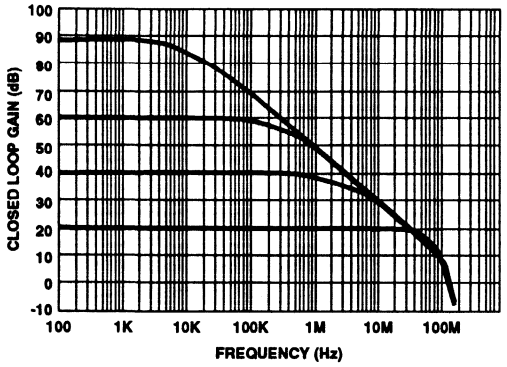


FIGURE 3. CLOSED LOOP FREQUENCY RESPONSE

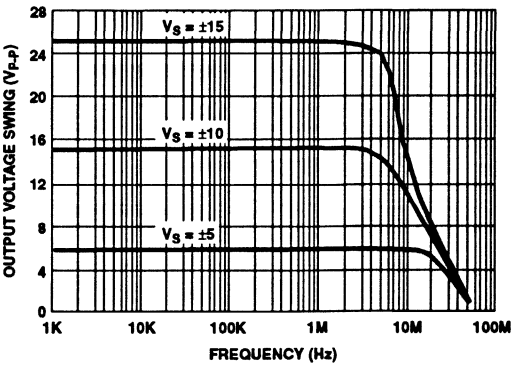


FIGURE 4. OUTPUT VOLTAGE SWING vs FREQUENCY

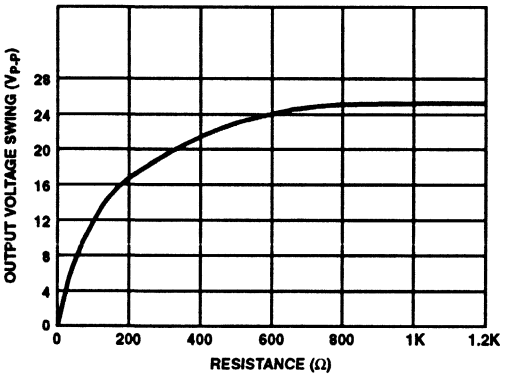


FIGURE 5. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

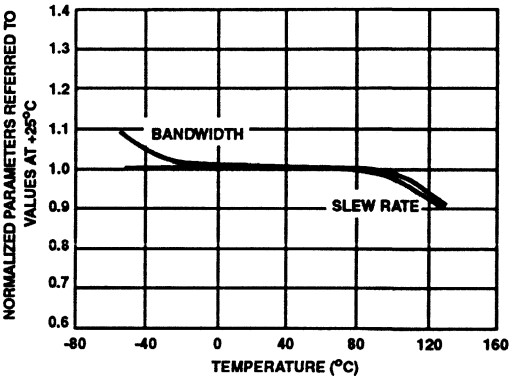


FIGURE 6. NORMALIZED AC PARAMETERS vs TEMPERATURE

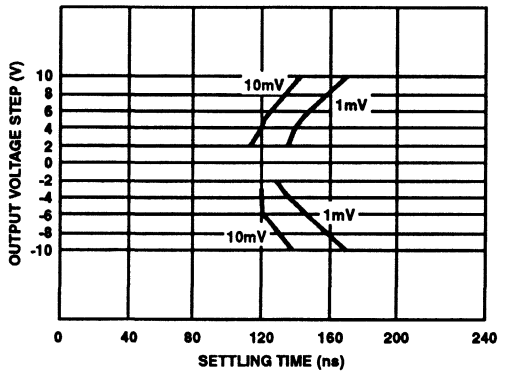


FIGURE 7. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

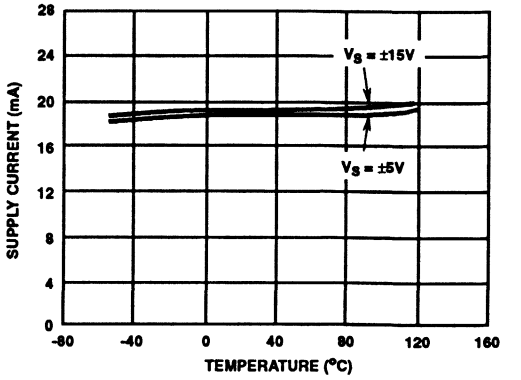


FIGURE 8. POWER SUPPLY CURRENT vs TEMPERATURE AND SUPPLY VOLTAGE

Performance Curves (Continued)

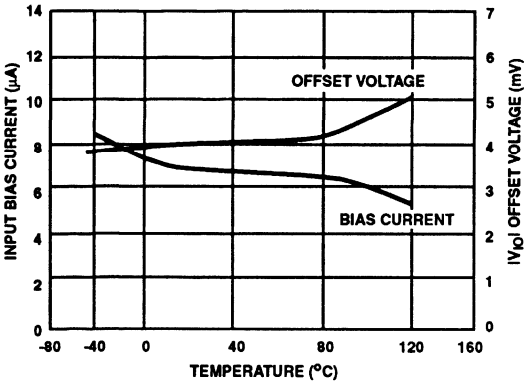


FIGURE 9. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs TEMPERATURE

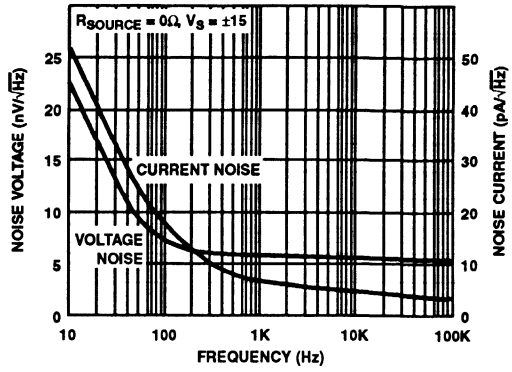


FIGURE 10. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY

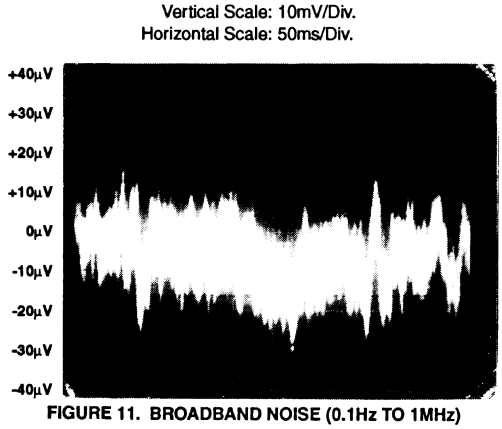


FIGURE 11. BROADBAND NOISE (0.1Hz TO 1MHz)

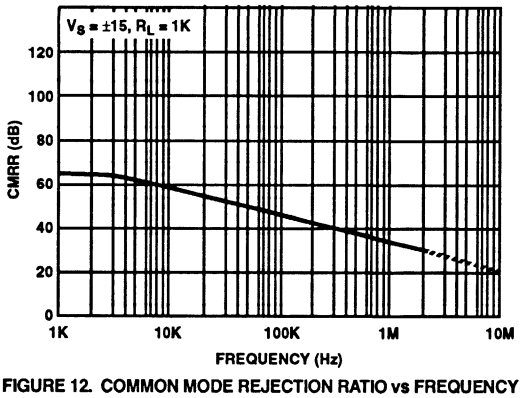


FIGURE 12. COMMON MODE REJECTION RATIO vs FREQUENCY

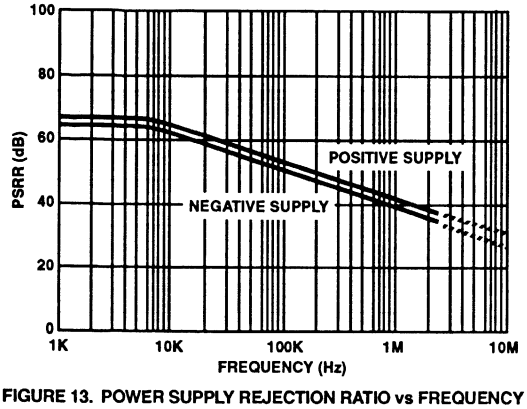


FIGURE 13. POWER SUPPLY REJECTION RATIO vs FREQUENCY

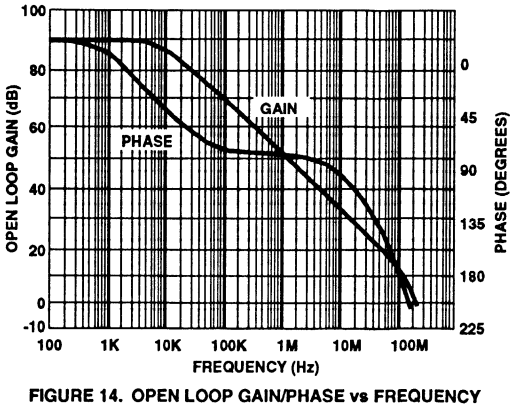


FIGURE 14. OPEN LOOP GAIN/PHASE vs FREQUENCY

Applications

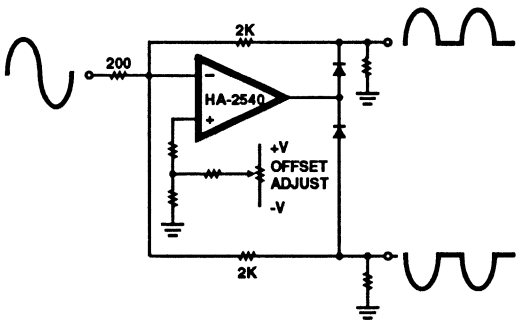


FIGURE 15. WIDEBAND SIGNAL SPLITTER

NOTE: With one HA-2540 and two low capacitance switching diodes, signals exceeding 10MHz can be separated. This circuit is most useful for full wave rectification, AM detectors or sync generation.

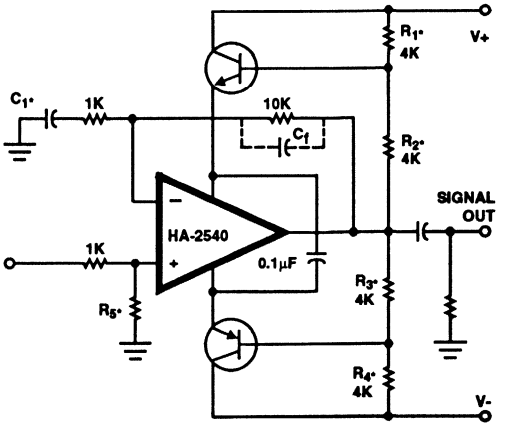


FIGURE 16. BOOTSTRAPPING FOR MORE OUTPUT CURRENT AND VOLTAGE SWING

NOTES:

1. Used for experimental purposes. $C_f \cong 3pF$.
2. C_1 is optional ($0.001\mu F \rightarrow 0.01\mu F$ ceramic).
3. R_5 is optional and can be utilized to reduce input signal amplitude and/or balance input conditions. $R_5 = 500\Omega$ to $1k\Omega$.

Refer to Application Note 541 For Further Applications Information

HARRIS SEMICONDUCTOR

HA-2541

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

March 1993

Features

- Unity Gain Bandwidth 40MHz
- High Slew Rate 250V/μs
- Low Offset Voltage 0.8mV
- Fast Settling Time (0.1%) 90ns
- Power Bandwidth 4MHz
- Output Voltage Swing (Min) ..... ±10V
- Unity Gain Stability
- Monolithic Bipolar Dielectric Isolation Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters
- High Speed A/D Input Buffer

For a lower power version of this product, please see the HA-2841 data sheet.

Description

The HA-2541 is the first unity gain stable monolithic operational amplifier to achieve 40MHz unity gain bandwidth. A major addition to the Harris series of high speed, wideband op amps, the HA-2541 is designed for video and pulse applications requiring stable amplifier response at low closed loop gains.

The uniqueness of the HA-2541 is that its slew rate and bandwidth characteristics are specified at unity gain. Historically, high slew rate, wide bandwidth and unity gain stability have been incompatible features for a monolithic operational amplifier. But features such as 250V/μs slew rate and 40MHz unity gain bandwidth clearly show that this is not the case for the HA-2541. These features, along with 90ns settling time to 0.1%, make this product an excellent choice for high speed data acquisition systems.

Mil-Std-883 product and data sheets are available upon request.

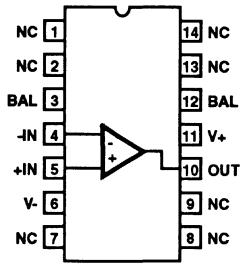
For further application suggestions on the HA-2541, please refer to Application Note 550 (Using the HA-2541), and Application Note 556 (Thermal Safe Operating Areas for High Current Operational Amplifiers). Also see 'Applications' in this data sheet.

Ordering Information

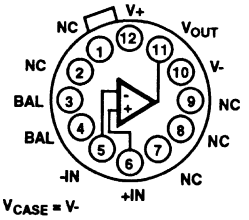
PART NUMBER	TEMP. RANGE	PACKAGE
HA1-2541-2	-55°C to +125°C	14 Lead Ceramic DIP
HA1-2541-5	0°C to +75°C	14 Lead Ceramic DIP
HA2-2541-2	-55°C to +125°C	12 Pin Can
HA2-2541-5	0°C to +75°C	12 Pin Can

Pinouts

HA1-2541 (CDIP)
TOP VIEW

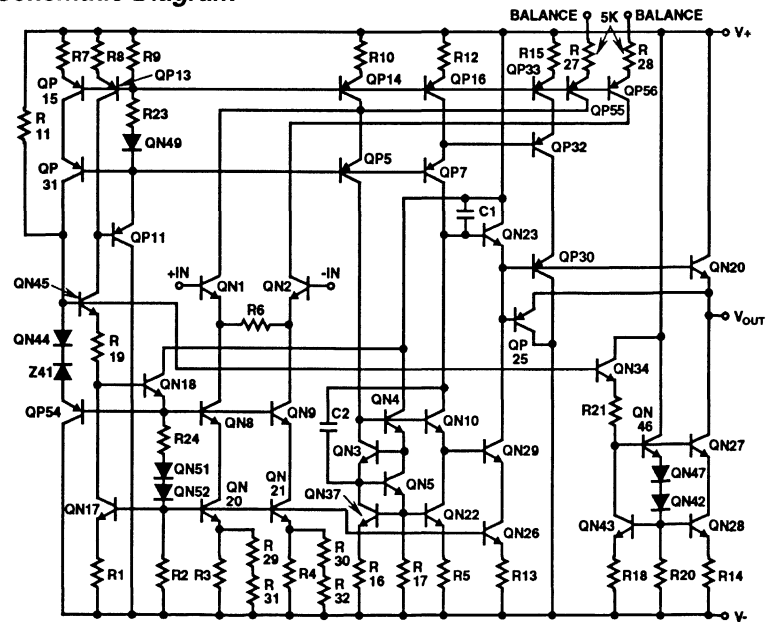


HA2-2541 (TO-8 CAN)
TOP VIEW



VCASE = V-

Schematic Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2898.1**

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Peak Output Current 50mA
Continuous Output Current ..... $28mA_{RMS}$
Junction Temperature (Note 11) ..... +175°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-2541-2 ..... $-55°C \le T_A \le +125°C$
HA-2541-5 ..... $0°C \le T_A \le +75°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V_{SUPPLY} = \pm 15V$, $R_L = 1k\Omega$, $C_L \le 10pF$, Unless Otherwise Specified

PARAMETER	TEMP	HA-2541-2 -55°C to +125°C			HA-2541-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	0.8	2	-	1	2	mV
	Full	-	-	6	-	-	6	mV
Average Offset Voltage Drift	Full	-	9	-	-	9	-	µV/°C
Bias Current	+25°C	-	11	35	-	11	35	µA
	Full	-	-	50	-	-	50	µA
Average Bias Current Drift	Full	-	85	-	-	85	-	nA/°C
Offset Current	+25°C	-	1	7	-	1	7	µA
	Full	-	-	9	-	-	9	µA
Input Resistance	+25°C	-	100	-	-	100	-	kΩ
Input Capacitance	+25°C	-	1	-	-	1	-	pF
Common Mode Range	Full	±10	±11	-	±10	±11	-	V
Input Noise Voltage (f = 1kHz, $R_g = 0\Omega$)	+25°C	-	10	-	-	10	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz, $R_g = 0\Omega$)	+25°C	-	4	-	-	4	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	10	16	-	10	16	-	kV/V
	Full	5	-	-	5	-	-	kV/V
Common Mode Rejection Ratio (Note 5)	Full	70	90	-	70	90	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	V/V
Unity Gain Bandwidth (Note 6)	+25°C	-	40	-	-	40	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 4)	Full	±10	±11	-	±10	±11	-	V
Output Current (Note 4)	+25°C	±10	±15	-	±10	±15	-	mA
Output Resistance	+25°C	-	2	-	-	2	-	Ω
Full Power Bandwidth (Note 3 & 7)	+25°C	3	4	-	3	4	-	MHz
Differential Gain (Note 2)	+25°C	-	0.1	-	-	0.1	-	%
Differential Phase (Note 2)	+25°C	-	0.2	-	-	0.2	-	Degrees
Harmonic Distortion (Note 10)	+25°C	-	<0.01	-	-	<0.01	-	%
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C	-	4	-	-	4	-	ns
Overshoot	+25°C	-	40	-	-	40	-	%
Slew Rate	+25°C	200	250	-	200	250	-	V/µs

Electrical Specifications V_{SUPPLY} = ±15V, R_L = 1kΩ, C_L ≤ 10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	HA-2541-2 -55°C to +125°C			HA-2541-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Settling Time								
10V Step to 0.1%	+25°C	-	90	-	-	90	-	ns
10V Step to 0.01%	+25°C	-	175	-	-	175	-	ns
POWER REQUIREMENTS								
Supply Current	+25°C	-	29	-	-	29	-	mA
	Full	-	-	40	-	-	40	mA
Power Supply Rejection Ratio (Note 9)	Full	70	80	-	70	78	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Differential Gain and Phase are measured with a 1V differential voltage at 5MHz.
3. V_O = ±10V
4. R_L = 1kΩ
5. V_{CM} = ±10V
6. V_O = 90mV.
7. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
8. Refer to Test Circuits section of this data sheet.
9. V_{SUPPLY} = ±5VDC to ±15VDC.
10. f = 10kHz; A_V = 5; V_O = $14V_{P-P}$
11. This value assumes a no load condition: Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C. By using Application Note 556 on Safe operating Area equations, along with the packaging thermal resistances listed in the Die Characteristics section, proper load conditions can be determined. Heat sinking is recommended above +75°C with suggested models:

    14 Lead Ceramic DIP:
    Thermalloy #6007 or AAVID #5602B (θ_{SA} = 16°C/W).

    12 Lead Metal Can (TO-8):
    Thermalloy #2240A (θ_{SA} = 27°C/W) or #2266B (θ_{SA} = 24°C/W)

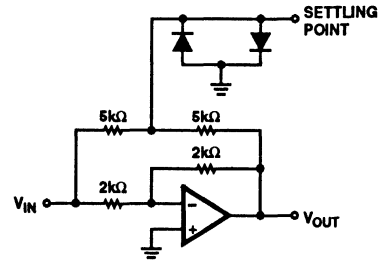
Die Characteristics

Transistor Count 41
Die Dimensions ..... 89 x 79 x 19 mils
Substrate Potential (Power Up)* ..... V-
Process ..... High Frequency Bipolar
Dielectric Isolation Passivation ..... Silox

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	71	13
Metal Can	56	29

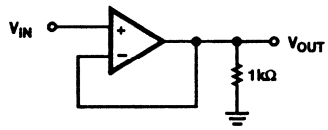
* The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Settling Time Circuit



- A_V = -1
- Feedback and summing resistor ratios should be 0.1% matched.
- HP5082-2810 clipping diodes recommended.
- Tektronix P6201 FET probe used at settling point.

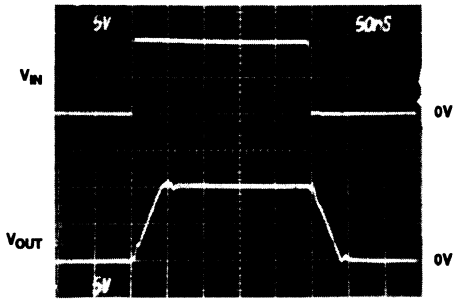
Test Circuits



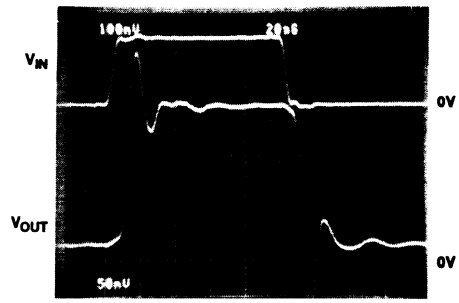
$V_{SS} = \pm 15V$
$A_V = +1$
$C_L \leq 10pF$

FIGURE 1. TEST CIRCUIT

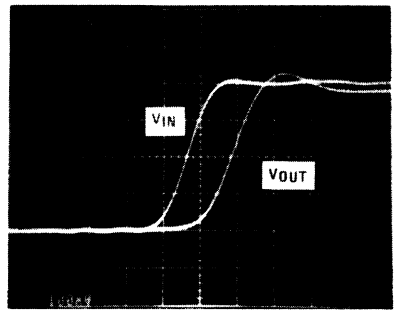
LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: 5V/Div.)
Horizontal Scale: (Time: 50ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale: (V_{IN} = 100mV/Div., V_{OUT} = 50mV/Div.)
Horizontal Scale: (Time: 20ns/Div.).



PROPAGATION DELAY
Vertical Scale: (Volts: = 100mV/Div.)
Horizontal Scale: (Time: 5ns/Div.).



$V_S = \pm 15V$, $R_L = 1k\Omega$
$T = +25°C$
Propagation delay variance is negligible over full temperature range.

Typical Performance Curves

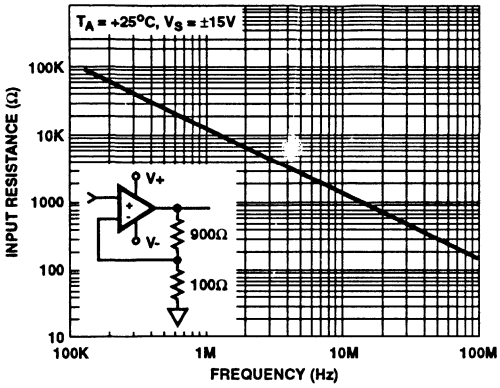


FIGURE 2. INPUT RESISTANCE vs FREQUENCY

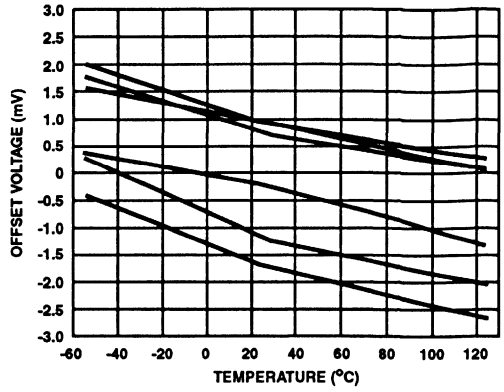


FIGURE 3. OFFSET VOLTAGE DRIFT WITH TEMPERATURE (6 REPRESENTATIVE UNITS)

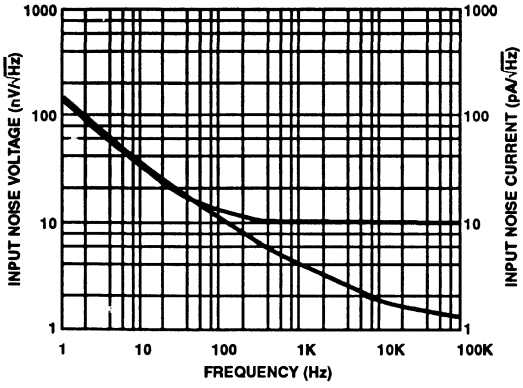


FIGURE 4. NOISE DENSITY vs FREQUENCY (T_A = +25°C)

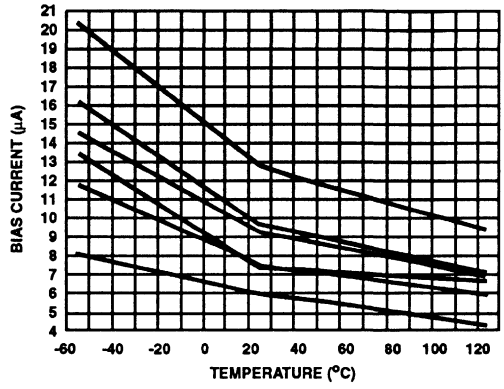


FIGURE 5. BIAS CURRENT DRIFT WITH TEMPERATURE (6 REPRESENTATIVE UNITS)

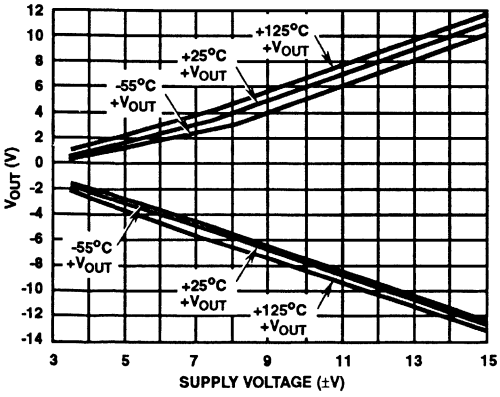


FIGURE 6. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (AT VARIOUS TEMPERATURES)

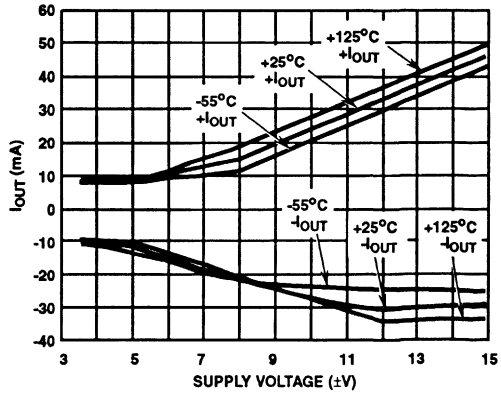


FIGURE 7. OUTPUT CURRENT vs SUPPLY VOLTAGE (AT VARIOUS TEMPERATURES)

Typical Performance Curves (Continued)

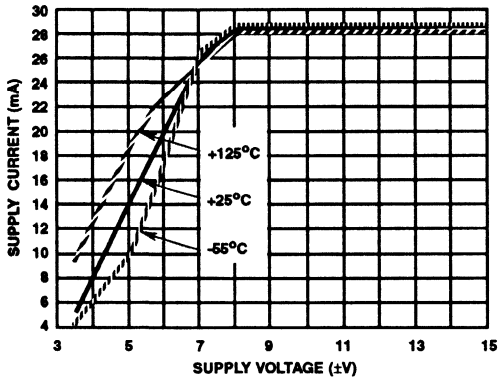


FIGURE 8. SUPPLY CURRENT vs SUPPLY VOLTAGE (AT VARIOUS TEMPERATURES)

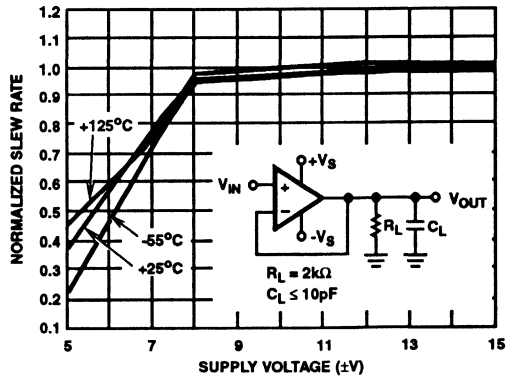


FIGURE 9. SLEW RATE vs SUPPLY VOLTAGE (NORMALIZED WITH V_S = ±15V AT +25°C)

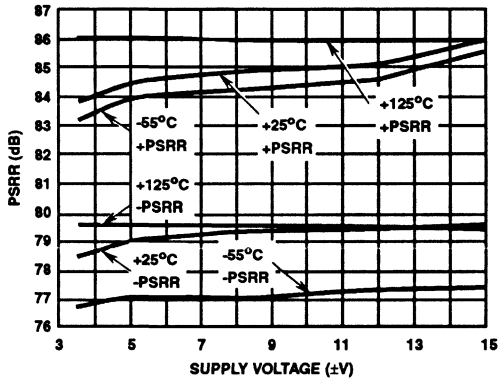


FIGURE 10. PSRR vs SUPPLY VOLTAGE (AVERAGE OF 3 LOTS AT VARIOUS TEMPERATURES)

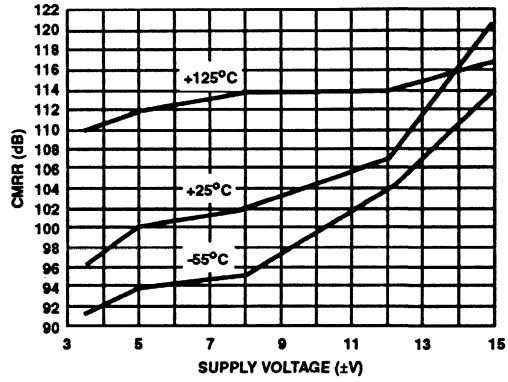


FIGURE 11. CMRR vs SUPPLY VOLTAGE (AVERAGE OF 3 LOTS AT VARIOUS TEMPERATURES)

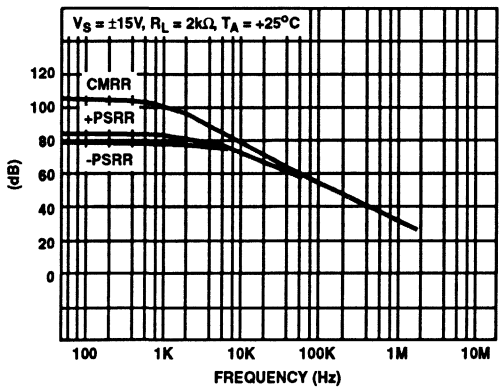


FIGURE 12. REJECTION RATIOS vs FREQUENCY

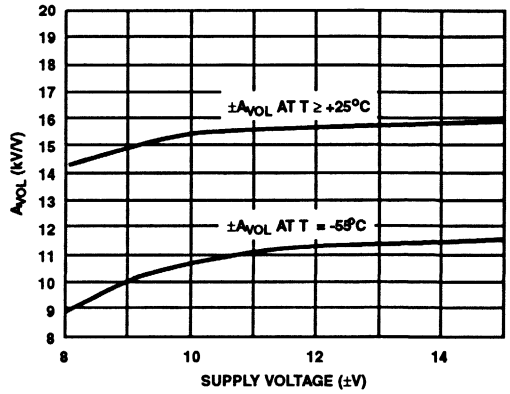


FIGURE 13. ± OPEN LOOP GAIN vs SUPPLY VOLTAGE (AVERAGE OF 3 LOTS OVER TEMPERATURE)

Typical Performance Curves (Continued)

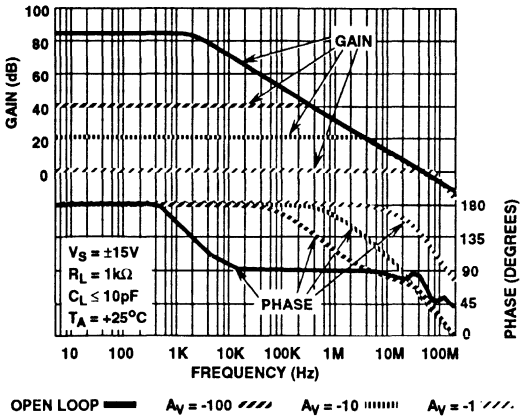


FIGURE 14. GAIN AND PHASE FREQUENCY RESPONSE

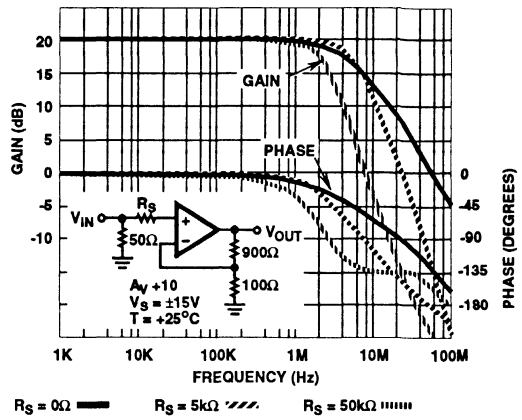


FIGURE 15. SMALL SIGNAL BANDWIDTH vs SOURCE RESISTANCE (V_S = ±15V, R_L = 1kΩ)

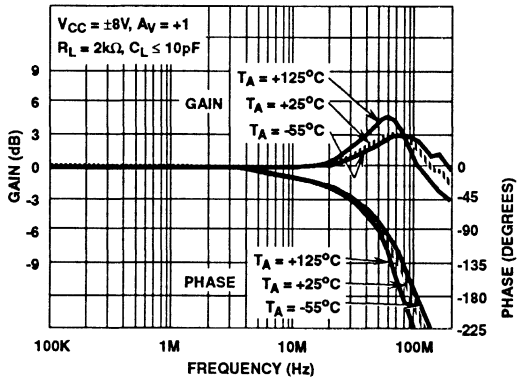
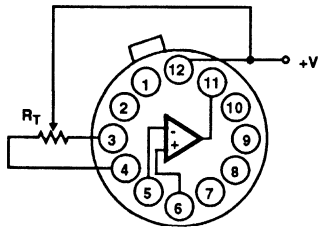


FIGURE 16. CLOSED LOOP FREQUENCY RESPONSE vs TEMPERATURE

Suggested Offset Voltage Adjustment



Tested Offset Adjustment Range is $|V_{OS}|$ + 1mV minimum referred to output. Typical range is ±15mV for R_T = 5kΩ.

Applications (Also see Application Note 550)

Application 1

High power amplifiers and buffers are in use in a wide variety of applications. Many times the "high power" capability is needed to drive large capacitive loads as well as low value resistive loads. In both cases the final driver stage is usually a power transistor of some type, but because of their inherently low gain, several stages of pre-drivers are often required. The HA-2541, with its 10mA output rating, is powerful enough to drive a power transistor without additional stages of current amplification. This capability is well demonstrated with the high power buffer circuit in Figure 17.

The HA-2541 acts as the pre-driver to the output power transistor. Together, they form a unity gain buffer with the ability to drive three 50Ω coaxial cables in parallel, each with a capacitance of 2000pF. The total combined load is 16.6Ω and 6000pF capacitance.

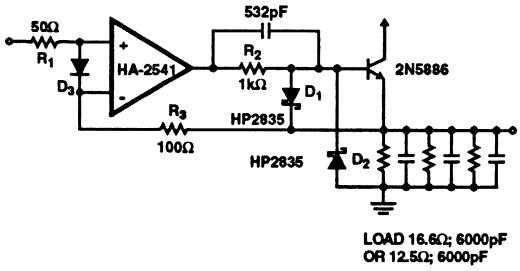


FIGURE 17. DRIVING POWER TRANSISTORS TO GAIN ADDITIONAL CURRENT BOOSTING

Application 2

Video

One of the primary uses of the HA-2541 is in the area of video applications. These applications include signal construction, synchronization addition and removal, as well as signal modification. A wide bandwidth device such as the HA-2541 is well suited for use in this class of amplifier. This, however, is a more involved group of applications than ordinary amplifier applications since video signals contain precise DC levels which must be retained.

The addition of a clamping circuit restores DC levels at the output of an amplifier stage. The circuit shown in Figure 18 utilizes the HA-5320 sample and hold amplifier as the DC clamp. Also shown is a 3.57MHz trap in series, which will block the color burst portion of the video signal and allow the DC level to be amplified and restored.

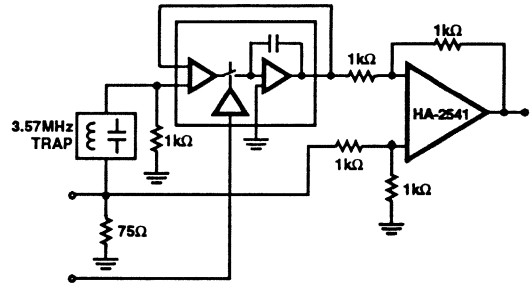


FIGURE 18. VIDEO DC RESTORER

HARRIS SEMICONDUCTOR

HA-2542

Wideband, High Slew Rate, High Output Current Operational Amplifier

March 1993

Features

- Stable at Gains of 2 or Greater
- Gain Bandwidth 70MHz
- High Slew Rate (Min) 300V/μs
- High Output Current (Min) 100mA
- Power Bandwidth (Typ) 5.5MHz
- Output Voltage Swing (Min) ..... ±10V
- Monolithic Bipolar Dielectric Isolation Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- Coaxial Cable Drivers
- Fast Sample-Hold Circuits
- High Frequency Signal Conditioning Circuits

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HA1-2542-2	-55°C to +125°C	14 Lead Ceramic DIP
HA1-2542-5	0°C to +75°C	14 Lead Ceramic DIP
HA2-2542-2	-55°C to +125°C	12 Pin Can
HA2-2542-5	0°C to +75°C	12 Pin Can
HA3-2542-5	0°C to +75°C	14 Lead Plastic DIP

Description

The HA-2542 is a wideband, high slew rate, monolithic operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability.

Utilizing the advantages of the Harris D.I. technology this amplifier offers 350V/μs slew rate, 70MHz gain bandwidth, and ±100mA output current. Application of this device is further enhanced through stable operation down to closed loop gains of 2.

For additional flexibility, offset null and frequency compensation controls are included in the HA-2542 pinout.

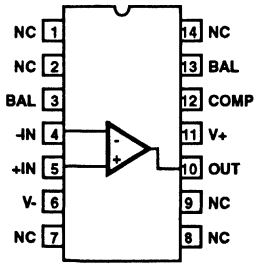
The capabilities of the HA-2542 are ideally suited for high speed coaxial cable driver circuits where low gain and high output drive requirements are necessary. With 5.5MHz full power bandwidth, this amplifier is most suitable for high frequency signal conditioning circuits and pulse video amplifiers. Other applications utilizing the HA-2542 advantages include wideband amplifiers and fast sample-hold circuits.

For more information on the HA-2542, please refer to Application Note 552 (Using the HA-2542), or Application Note 556 (Thermal Safe-Operating-Areas for High Current Op Amps).

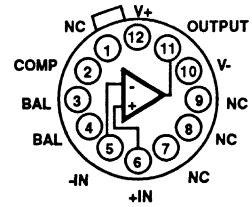
For a lower power version of this product, please see the HA-2842 data sheet.

Pinouts

HA-2542
(PDIP, CDIP)
TOP VIEW



HA-2542
(TO-8 METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2899.1**

Absolute Maximum Ratings (Note 1)

Supply Voltage (Between V+ and V- Terminals) 35V
Differential Input Voltage 6V
Output Current . . . . . 125mA (Peak)
50mA (Continuous)
Junction Temperature (Note 11) . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Operating Temperature Range
HA-2542-2 . . . . . $-55°C \le T_A \le +125°C$
HA-2542-5 . . . . . $0°C \le T_A \le +75°C$
Storage Temperature Range . . . . . $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \le 10pF$, Unless Otherwise Specified.

PARAMETER	TEMPERATURE	HA-2542-2 -55°C to +125°C			HA-2542-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	5	10	-	5	10	mV
	Full	-	8	20	-	8	20	mV
Average Offset Voltage Drift	Full	-	14	-	-	14	-	µV/°C
Bias Current	+25°C	-	15	35	-	15	35	µA
	Full	-	26	50	-	26	50	µA
Average Bias Current Drift	Full	-	66	-	-	45	-	nA/°C
Offset Current	+25°C	-	1	7	-	1	7	µA
	Full	-	-	9	-	-	9	µA
Input Resistance	+25°C	-	100	-	-	100	-	kΩ
Input Capacitance	+25°C	-	1	-	-	1	-	pF
Common Mode Range	Full	±10	-	-	±10	-	-	V
Input Noise Voltage (0.1Hz to 100Hz)	+25°C	-	2.2	-	-	2.2	-	μV_{P-P}
Input Noise Density (f = 1kHz, $R_G = 0\Omega$)	+25°C	-	10	-	-	10	-	$nV/\sqrt{Hz}$
Input Noise Current Density (f = 1kHz, $R_G = 0\Omega$)	+25°C	-	3	-	-	3	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	10	30	-	10	30	-	kV/V
	Full	5	15	-	5	20	-	kV/V
Common Mode Rejection Ratio (Note 4)	Full	70	100	-	70	100	-	dB
Minimum Stable Gain	+25°C	2	-	-	2	-	-	V/V
Gain Bandwidth Product (Note 5)	+25°C	-	70	-	-	70	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10	±11	-	±10	±11	-	V
Output Current (Note 6)	+25°C	100	-	-	100	-	-	mA
Output Resistance	+25°C	-	5	-	-	5	-	Ω
Full Power Bandwidth (Notes 3, 7)	+25°C	4.7	5.5	-	4.7	5.5	-	MHz
Differential Gain (Note 2)	+25°C	-	0.1	-	-	0.1	-	%
Differential Phase (Note 2)	+25°C	-	0.2	-	-	0.2	-	Degree
Harmonic Distortion (Note 10)	+25°C	-	<0.04	-	-	<0.04	-	%
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C	-	4	-	-	4	-	ns
Overshoot	+25°C	-	25	-	-	25	-	%
Slew Rate	+25°C	300	350	-	300	350	-	V/µs

Electrical Specifications V_{SUPPLY} = ±15V, R_L = 1kΩ, C_L ≤ 10pF, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEMPERATURE	HA-2542-2 -55°C to +125°C MIN	TYP	MAX	HA-2542-5 0°C to +75°C MIN	TYP	MAX	UNITS
TRANSIENT RESPONSE (Note 8) Continued								
Settling Time								
10V Step to 0.1%	+25°C	-	100	-	-	100	-	ns
10V Step to 0.01%	+25°C	-	200	-	-	200	-	ns
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	30	-	-	30	-	mA
	Full	-	31	34.5	-	31	40	mA
Power Supply Rejection Ratio (Note 9)	Full	70	79	-	70	79	-	dB

NOTES:

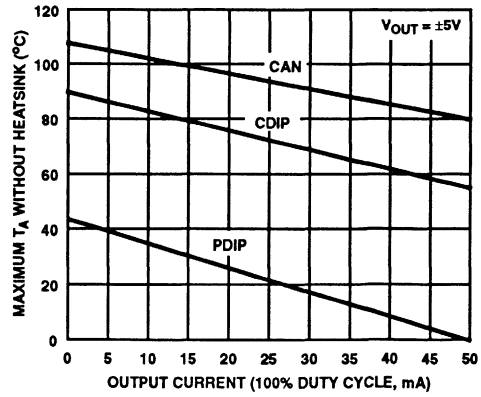
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Differential gain and phase are measured at 5MHz with a 1V differential input voltage.
3. R_L = 1kΩ, V_O = ±10V.
4. V_{CM} = ±10V.
5. A_{VCL} = 100.
6. R_L = 50Ω, V_O = ±5V, Output duty cycle must be reduced for I_{OUT} > 50mA (e.g. ≤50% duty cycle for 100mA).
7. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
8. Refer to Test Circuits section of this data sheet.
9. V_{SUPPLY} = ±5VDC to ±15VDC.
10. V_{IN} = $1V_{RMS}$; f = 10kHz; A_V = 10.
11. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C for ceramic and can packages, and below +150°C for plastic packages. By using Application Note 556 on Safe Operating Area equations, along with the packaging thermal resistances listed in the Die Characteristics section, proper load conditions can be determined. Heatsinking will be required in many applications. See Performance Curve below to determine if heat sinking is required for your application. Some suggested heatsink models are:
    14 Lead Ceramic DIP:
    Thermalloy #6007 or AAVID #5602B (θ_{SA} = 16°C/W)
    12 Pin Metal Can (TO-8):
    Thermalloy #2240A (θ_{SA} = 27°C/W) or #2268B (θ_{SA} = 24°C/W)

Die Characteristics

Transistor Count 43
Die Dimensions ..... 72 x 105 x 19 mils
(1820µm x 2670µm x 485µm)
Substrate Potential* ..... V-
Process ..... High Frequency Bipolar-DI
Passivation ..... Nitride

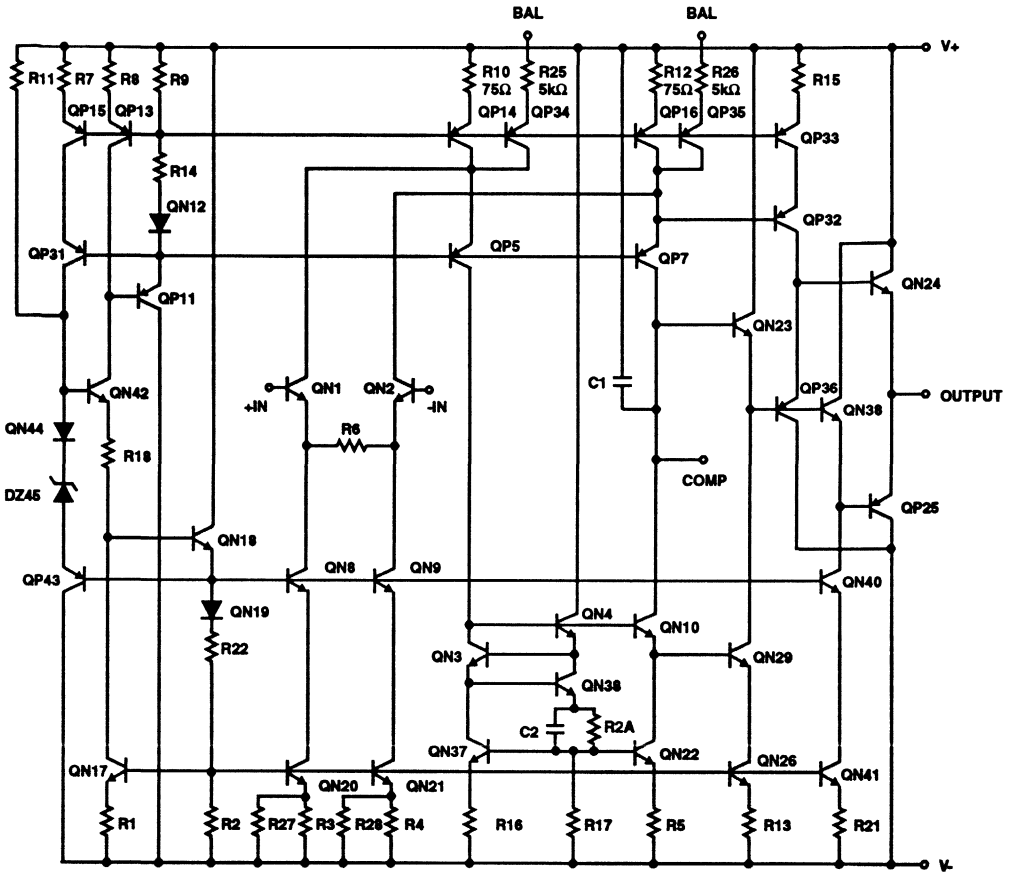
Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	71	13
Plastic DIP	88	27
Metal Can	56	29

* The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.



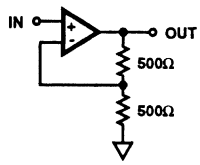
MAXIMUM OPERATING TEMPERATURE vs OUTPUT CURRENT

Schematic Diagram



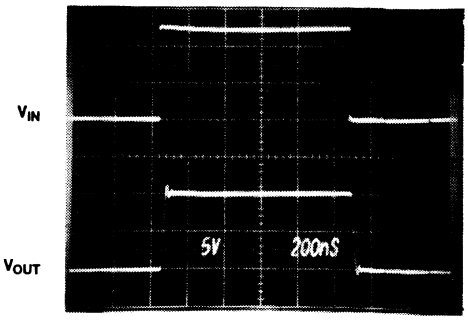
Test Circuits

TEST CIRCUIT

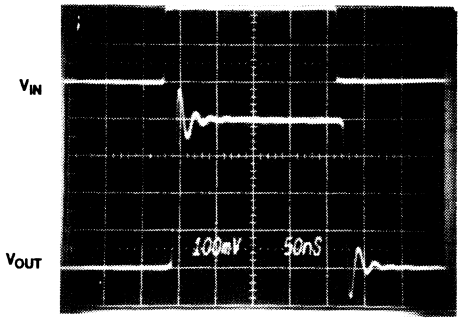


$V_S = \pm 15V$
$A_V = +2$
$C_L \leq 10pF$

LARGE SIGNAL RESPONSE
Vertical Scale (Volts: V_{IN} = 2.0V/Div., V_{OUT} = 5.0V/Div.)
Horizontal Scale (Time: 200ns/Div.)

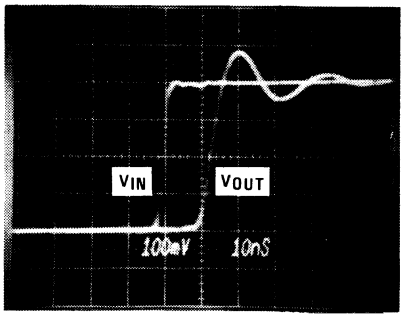


SMALL SIGNAL RESPONSE
Vertical Scale (Volts: 100mV/Div.)
Horizontal Scale (Time: 50ns/Div.)

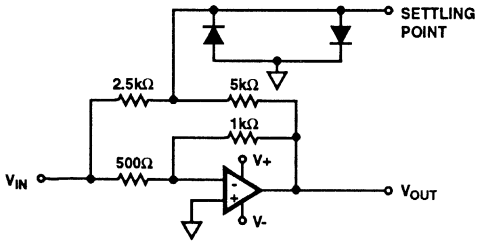


PROPAGATION DELAY
Vertical Scale (Volts: 100mV/Div.)
Horizontal Scale (Time: 10ns/Div.)

$V_S = \pm 15V$, $R_L = 1k\Omega$. Propagation delay variance is negligible over full temperature range



SETTLING TIME TEST CIRCUIT



- $A_V = -2$.
- Feedback and summing resistors must be matched (0.1%).
- HP5082-2810 clipping diodes recommended.
- Tektronix P6201 FET probe used at settling point.
- For 0.01% settling time, heat sinking is suggested to reduce thermal effects and an analog ground plane with supply decoupling is suggested to minimize ground loop errors.

Typical Performance Curves

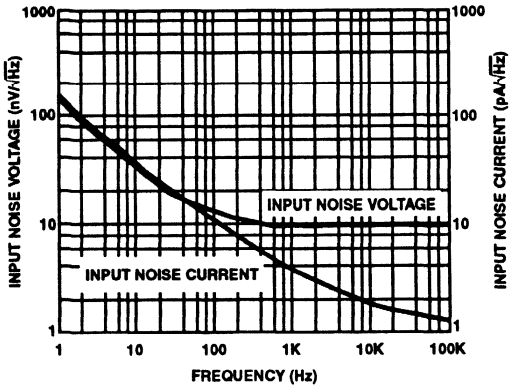


FIGURE 1. INPUT NOISE VOLTAGE AND INPUT NOISE CURRENT vs FREQUENCY

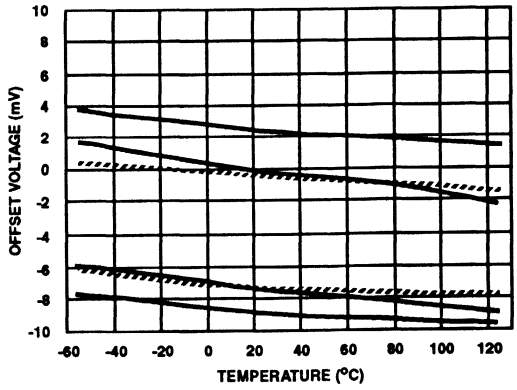


FIGURE 2. OFFSET VOLTAGE DRIFT WITH TEMPERATURE OF SIX REPRESENTATIVE UNITS (V_S = ±12V)

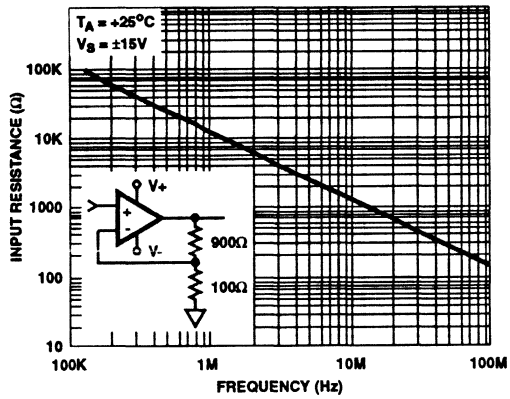


FIGURE 3. INPUT RESISTANCE vs FREQUENCY

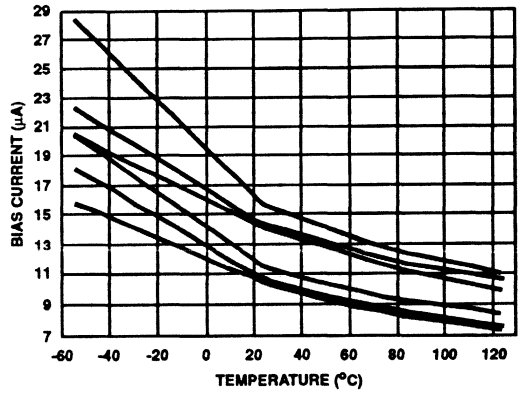


FIGURE 4. BIAS CURRENT DRIFT WITH TEMPERATURE OF SIX REPRESENTATIVE UNITS (V_S = ±12V)

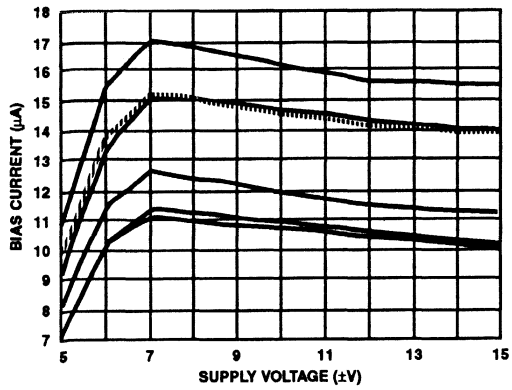


FIGURE 5. BIAS CURRENT vs POWER SUPPLY, SIX UNITS AT VARIOUS SUPPLIES AT +25°C

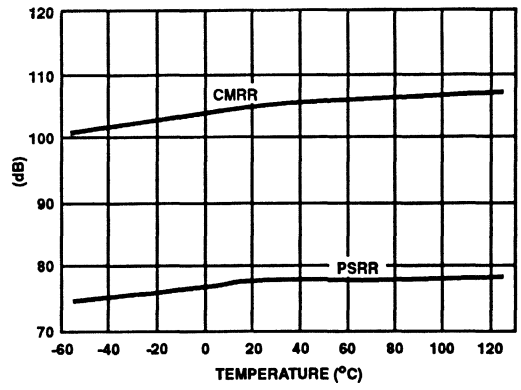


FIGURE 6. PSRR AND CMRR vs TEMPERATURE (V_S = ±15V)

Typical Performance Curves (Continued)

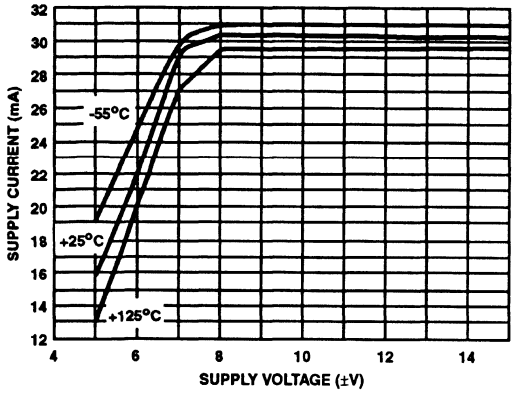


FIGURE 7. SUPPLY CURRENT vs SUPPLY VOLTAGE, AT VARIOUS TEMPERATURES

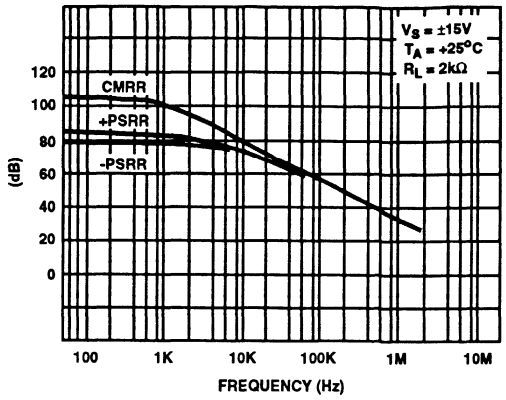


FIGURE 8. PSRR AND CMRR vs FREQUENCY

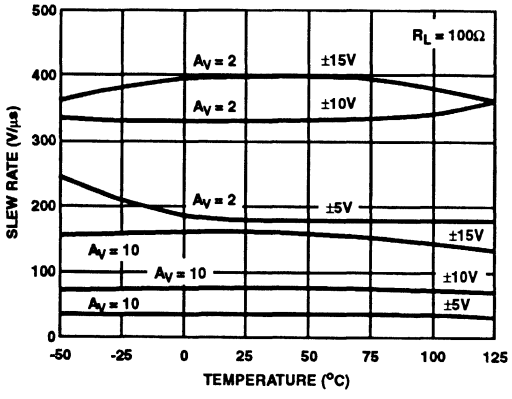


FIGURE 9. SLEW RATE vs TEMPERATURE AT VARIOUS SUPPLY VOLTAGES

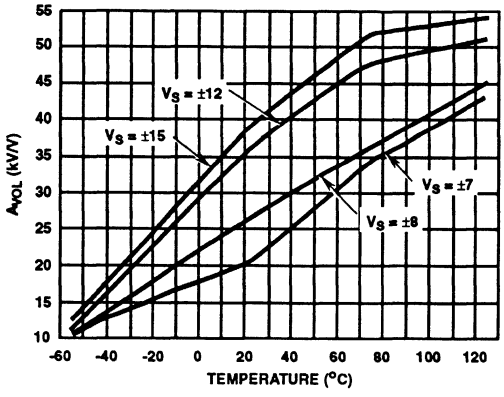


FIGURE 10. OPEN LOOP GAIN vs TEMPERATURE, AT VARIOUS SUPPLY VOLTAGES

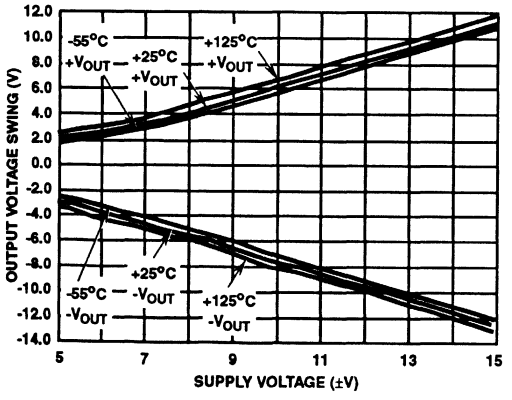


FIGURE 11. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE, AT VARIOUS TEMPERATURES

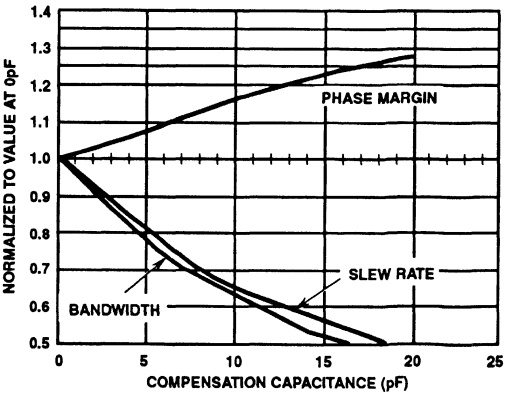


FIGURE 12. NORMALIZED AC PARAMETERS vs COMPENSATION CAPACITANCE

Typical Performance Curves (Continued)

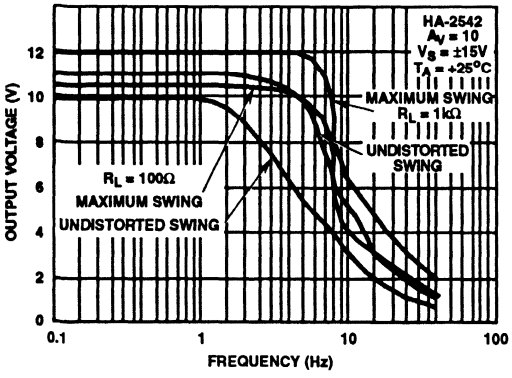


FIGURE 13. OUTPUT VOLTAGE SWING vs FREQUENCY

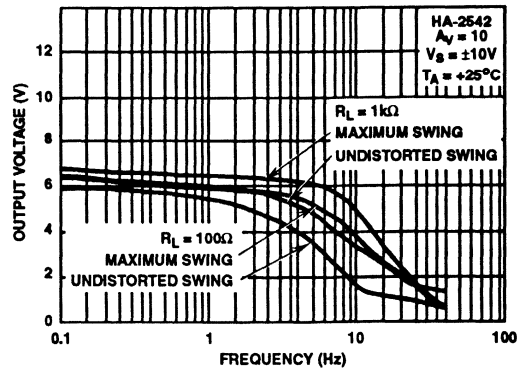


FIGURE 14. OUTPUT VOLTAGE SWING vs FREQUENCY

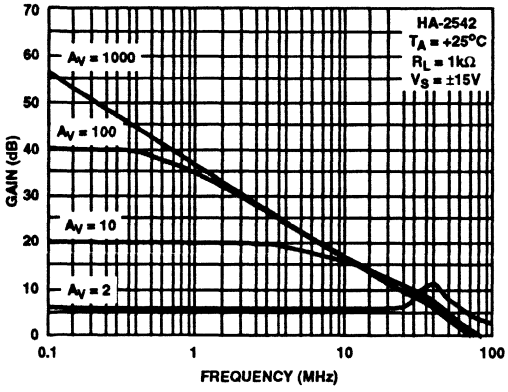


FIGURE 15. FREQUENCY RESPONSE CURVES

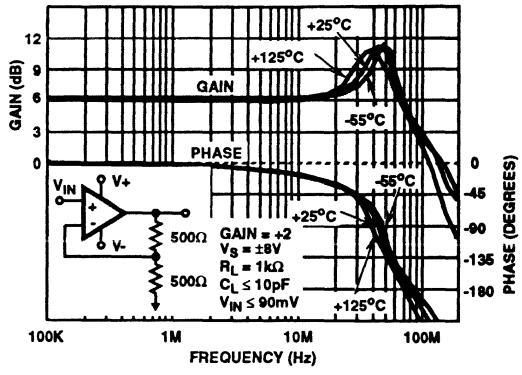


FIGURE 16. HA-2542 CLOSED LOOP GAIN vs TEMPERATURE

Application Information

Typical Applications
(Refer to Application Note 552 for Further Information)

The Harris HA-2542 is a state of the art monolithic device which also approaches the "ALL-IN-ONE" amplifier concept. This device features an outstanding set of AC parameters augmented by excellent output drive capability providing for suitable application in both high speed and high output drive circuits.

Primarily intended to be used in balanced 50Ω and 75Ω coaxial cable systems as a driver, the HA-2542 could also be used as a power booster in audio systems as well as a power amp in power supply circuits. This device would also be suitable as a small DC motor driver.

The applications shown in Figures 17 through Figure 19 demonstrate the HA-2542 at gains of +100 and +2 and as a video cable driver for small signals.

Prototyping Guidelines

For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include: 1) mounting the device through a ground plane: 2) connecting unused pins (N.C.) to the ground: 3) mounting feedback components on Teflon standoffs and or locating these components as close to the device as possible: 4) placing power supply decoupling capacitors from device supply pins to ground.

As a result of speed and bandwidth optimization, the HA-2542 can's case potential, when powered-up, is equal to the V- potential. Therefore, contact with other circuitry or ground should be avoided.

Frequency Compensation

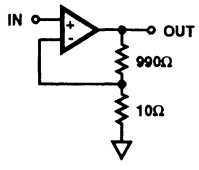
The HA-2542 may be externally compensated with a single capacitor to ground. This provides the user the additional flexibility in tailoring the frequency response of the amplifier. A guideline to the response is demonstrated on the typical performance curve showing the normalized A.C. parameters versus compensation capacitance. It is suggested that the user check and tailor the accurate compensation value for each application. As shown additional phase margin is achieved at the loss of slew rate and bandwidth.

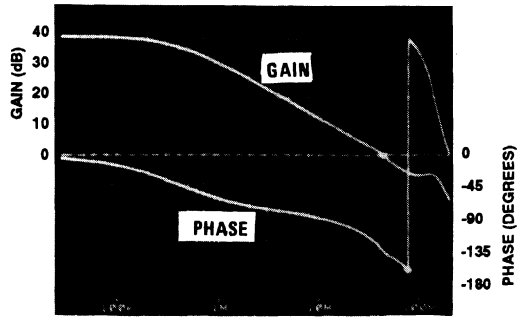
For example, for a voltage gain of +2 (or -1) and a load of 500pF/2kΩ, 20pF is needed for compensation to give a small signal bandwidth of 30MHz with 40° of phase margin. If a full power output voltage of ±10V is needed, this same configuration will provide a bandwidth of 5MHz and a slew rate of 200V/μs.

If maximum bandwidth is desired and no compensation is needed, care must be given to minimize parasitic capacitance at the compensation pin. In some cases where minimum gain applications are desired, bending up or totally removing this pin may be the solution. In this case, care must also be given to minimize load capacitance.

For wideband positive unity gain applications, the HA-2542 can also be over-compensated with capacitance greater than 30pF to achieve bandwidths of around 25MHz. This over-compensation will also improve capacitive load handling or lower the noise bandwidth. This versatility along with the ±100mA output current makes the HA-2542 an excellent high speed driver for many power applications.

Typical Applications

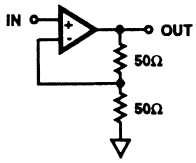




FREQUENCY (0dB) = 44.9MHz, PHASE MARGIN (0dB) = 40°
A_{VCL} = 100 PHASE AND GAIN

FIGURE 17. NONINVERTING CIRCUIT (A_{VCL} = 100)

Typical Applications (Continued)



FREQUENCY (dB) = 56MHz, PHASE MARGIN (3dB) = 40°
A_{VCL} = 2 PHASE AND GAIN

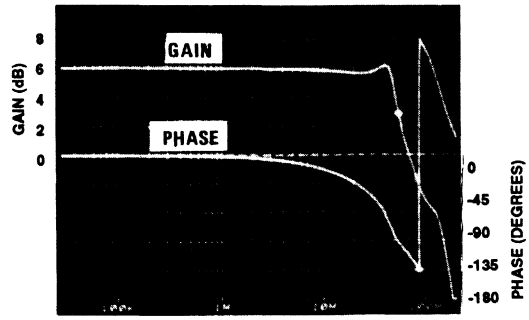
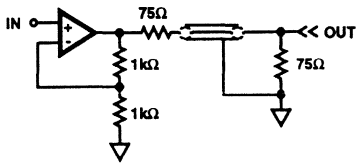


FIGURE 18. NONINVERTING CIRCUIT (A_{VCL} = 2)



VIDEO CABLE DRIVER PULSE RESPONSE (1V/DIV.; 100ns/DIV.)

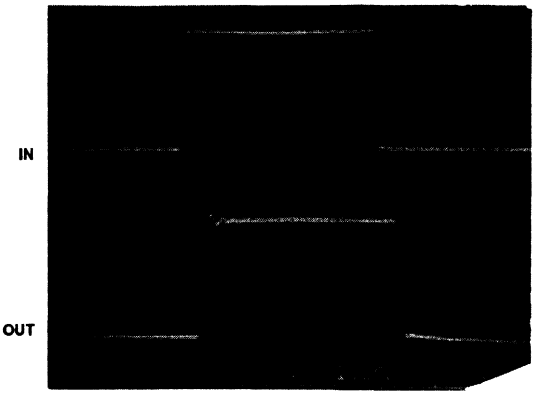
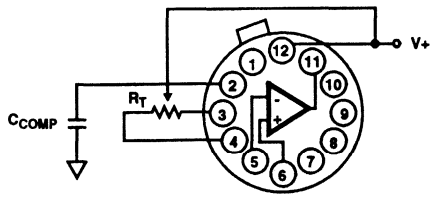


FIGURE 19. VIDEO CABLE DRIVER (A_{VCL} = 2)



Suggested compensation scheme 5pF - 20pF.

Tested Offset Adjustment Range is $|V_{OS}$ +1mV| minimum referred to output.

Typical range is ±20mV with R_T = 5kΩ

FIGURE 20. SUGGESTED OFFSET VOLTAGE ADJUSTMENT AND FREQUENCY COMPENSATION

HARRIS SEMICONDUCTOR

HA-2544

March 1993

Video Operational Amplifier

Features

- Gain Bandwidth 50MHz
- High Slew Rate 150V/μs
- Low Supply Current 10mA
- Differential Gain Error 0.03%
- Differential Phase Error ..... 0.03 Degree
- Gain Flatness at 10MHz 0.12dB

Applications

- Video Systems
- Video Test Equipment
- Radar Displays
- Data Acquisition Systems
- Imaging Systems
- Pulse Amplifiers
- Signal Conditioning Circuits

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HA2-2544-2	-55°C to +125°C	8 Pin TO-99 Can
HA2-2544-5	0°C to +75°C	8 Pin TO-99 Can
HA3-2544-5	0°C to +75°C	8 Lead Plastic DIP
HA3-2544C-5	0°C to +75°C	8 Lead Plastic DIP
HA4P2544-5	0°C to +75°C	20 Lead PLCC
HA4P2544C-5	0°C to +75°C	20 Lead PLCC
HA7-2544-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-2544-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P2544-5	0°C to +75°C	8 Lead SOIC
HA9P2544-9	-40°C to +85°C	8 Lead SOIC
HA9P2544C-5	0°C to +75°C	8 Lead SOIC
HA9P2544C-9	-40°C to +85°C	8 Lead SOIC

Description

The HA-2544 is a fast, unity gain stable, monolithic op amp designed to meet the needs required for accurate reproduction of video or high speed signals. It offers high voltage gain (6kV/V) and high phase margin (65 degrees) while maintaining tight gain flatness over the video bandwidth. Built from high quality Dielectric Isolation, the HA-2544 is another addition to the Harris series of high speed, wideband op amps, and offers true video performance combined with the versatility of an op amp.

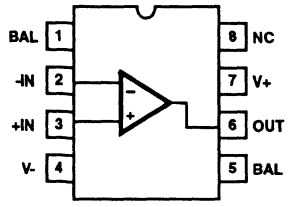
The primary features of the HA-2544 include 50MHz Gain Bandwidth, 150V/μs slew rate, 0.03% differential gain error and gain flatness of just 0.12dB at 10MHz. High performance and low power requirements are met with a supply current of only 10mA.

Uses of the HA-2544 range from video test equipment, guidance systems, radar displays and other precise imaging systems where stringent gain and phase requirements have previously been met with costly hybrids and discrete circuitry. The HA-2544 will also be used in non-video systems requiring high speed signal conditioning such as data acquisition systems, medical electronics, specialized instrumentation and communication systems.

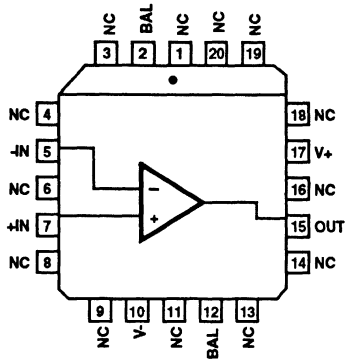
Military (/883) product and data sheets are available upon request.

Pinouts

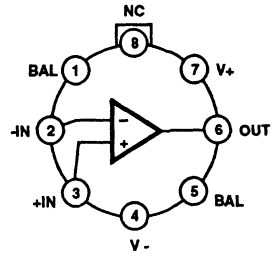
HA-2544 (PDIP, CDIP, SOIC)
HA-2544C (PDIP, SOIC)
TOP VIEW



HA-2544/2544C
(PLCC)
TOP VIEW



HA-2544
(TO-99 CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2900.1**

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage (Note 11) 6V
Peak Output Current ..... ±40mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-2544/2544C-5 ..... $0°C \le T_A \le +75°C$
HA-2544-9 ..... $-40°C \le T_A \le +85°C$
HA-2544-2 ..... $-55°C \le T_A \le +125°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V_S = \pm15V$, $C_L \le 10pF$, $R_L = 1k\Omega$, Unless Otherwise Specified

PARAMETER	TEMP	HA-2544-2/-5			HA-2544C-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	6	15	-	15	25	mV
	-2, -5	-	-	20	-	-	40	mV
	-9	-	-	25	-	-	40	mV
Average Offset Voltage Drift (Note 9)	Full	-	10	-	-	10	-	µV/°C
Bias Current	+25°C	-	7	15	-	9	18	µA
	Full	-	-	20	-	-	30	µA
Average Bias Current Drift (Note 9)	Full	-	0.04	-	-	0.04	-	µA/°C
Offset Current	+25°C	-	0.2	2	-	0.8	2	µA
	Full	-	-	3	-	-	3	µA
Offset Current Drift	Full	-	10	-	-	10	-	nA/°C
Common Mode Range	Full	±10	±11.5	-	±10	±11.5	-	V
Differential Input Resistance	+25°C	50	90	-	50	90	-	kΩ
Differential Input Capacitance	+25°C	-	3	-	-	3	-	pF
Input Noise Voltage (f = 1kHz)	+25°C	-	20	-	-	20	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C	-	2.4	-	-	2.4	-	$pA/\sqrt{Hz}$
Input Noise Voltage								
0.1Hz to 10Hz (Note 9)	+25°C	-	1.5	-	-	1.5	-	μV_{P-P}
0.1Hz to 1MHz	+25°C	-	4.6	-	-	4.6	-	µVRMS
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 4, 9)	+25°C	3.5	6	-	3	6	-	kV/V
	Full	2.5	-	-	2	-	-	kV/V
Common Mode Rejection Ratio (Notes 6, 9)	-2, -5	75	89	-	70	89	-	dB
	-9	75	89	-	65	89	-	dB
Minimum Stable Gain	+25°C	+1	-	-	+1	-	-	V/V
Unity Gain Bandwidth (Notes 3, 9)	+25°C	-	45	-	-	45	-	MHz
Gain Bandwidth Product (Notes 3, 9)	+25°C	-	50	-	-	50	-	MHz
Phase Margin	+25°C	-	65	-	-	65	-	Degrees
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10	±11	-	±10	±11	-	V
Full Power Bandwidth (Note 7)	+25°C	3.2	4.2	-	3.2	4.2	-	MHz
Peak Output Current (Note 9)	+25°C	±25	±35	-	±25	±35	-	mA
Continuous Output Current (Note 9)	+25°C	±10	-	-	±10	-	-	mA
Output Resistance (Open Loop)	+25°C	-	20	-	-	20	-	Ω

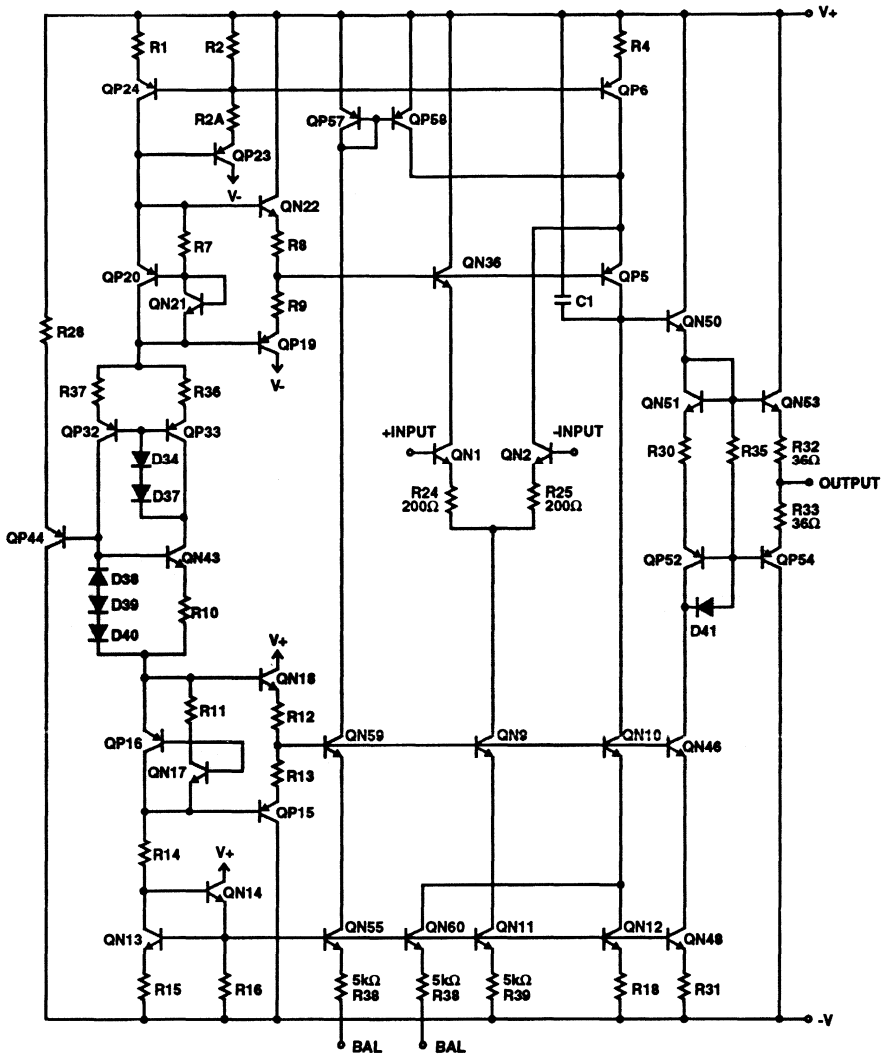
Electrical Specifications $V_S = \pm15V$, $C_L \leq 10pF$, $R_L = 1k\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	HA-2544-2/-5			HA-2544C-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE								
Rise Time (Note 3)	+25°C	-	7	-	-	7	-	ns
Overshoot (Note 3)	+25°C	-	10	-	-	10	-	%
Slew Rate	+25°C	100	150	-	100	150	-	V/µs
Settling Time (Note 5)	+25°C	-	120	-	-	120	-	ns
VIDEO PARAMETERS $R_L = 1k\Omega$ (Note 10)								
Differential Phase (Note 12)	+25°C	-	0.03	-	-	0.03	-	Degree
Differential Gain (Notes 2, 12)	+25°C	-	0.0026	-	-	0.0026	-	dB
	+25°C	-	0.03	-	-	0.03	-	%
Gain Flatness								
5MHz	+25°C	-	0.10	-	-	0.10	-	dB
10MHz	+25°C	-	0.12	-	-	0.12	-	dB
Chrominance to Luminance Gain (Note 13)	+25°C	-	0.1	-	-	0.1	-	dB
Chrominance to Luminance Delay (Note 13)	+25°C	-	7	-	-	7	-	ns
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	10	12	-	10	15	mA
Power Supply Rejection Ratio (Notes 8, 9)	-2, -5	70	80	-	70	80	-	dB
	-9	65	80	-	65	80	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $A_D(\%) = \left[10^{\frac{A_D(dB)}{20}} - 1\right] \times 100$.
3. $V_{OUT} = \pm100mV$. For Rise Time and Overshoot testing, V_{OUT} is measured from 0 to +200mV and 0 to -200mV.
4. $V_{OUT} = \pm5V$
5. Settling Time is specified to 0.1% of final value for a 10V step and $A_V = -1$.
6. $\Delta V_{CM} = \pm10V$
7. Full Power Bandwidth is guaranteed by equation: Full Power Bandwidth $= \frac{\text{Slew Rate}}{2\pi V_{PEAK}} \left(V_{PEAK} = 5V\right)$.
8. $\Delta V_S = \pm10$ to $\pm20V$
9. Refer to typical performance curve in Data Sheet.
10. The video parameter specifications will degrade as the output load resistance decreases.
11. To achieve optimum AC performance, the input stage was designed without protective diode clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of the input transistors and probable degradation of the input parameters especially V_{OS}, I_{OS} and Noise.
12. Tested with a VM700A video tester, using a NTC-7 Composite input signal. For adequate test repeatability, a minimum warm-up of 2 minutes is suggested. $A_V = +1$.
13. C-L Gain and C-L Delay was less than the resolution of the test equipment used which is 0.1dB and 7ns, respectively.

Schematic



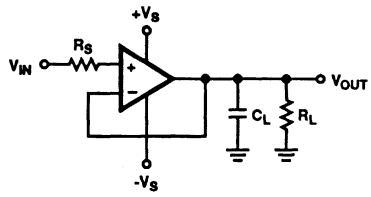
Die Characteristics

Transistor Count	44
Die Dimensions	80 x 65 x 19 mils
Substrate Potential*	V-
Process	High Frequency Bipolar D.I.
Passivation	Nitride

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Metal Can	111	34
Plastic Mini-DIP	92	30
Ceramic Mini-DIP	114	35
SOIC	157	43
PLCC	74	33

* The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Test Circuits

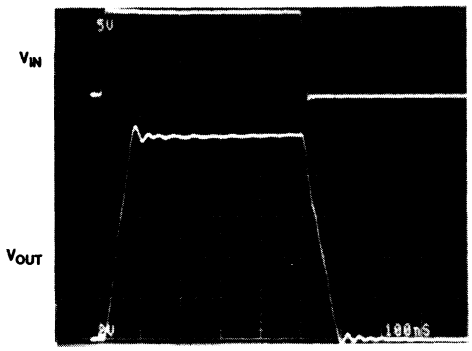


V_S = ±15V
A_V = +1
R_S = 50Ω or 75Ω (Optional)
R_L = 1kΩ
C_L < 10pF

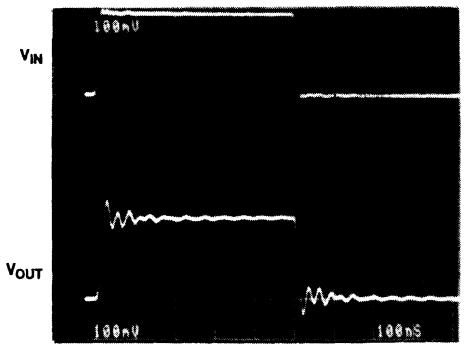
V_{IN} for Large Signal = ±5V
V_{IN} for Small Signal = 0 to +200mV and 0 to -200mV

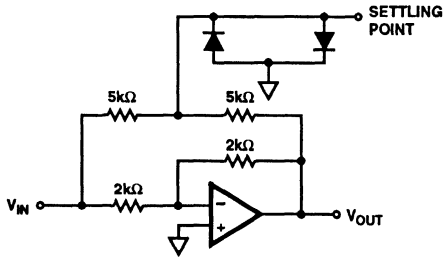
FIGURE 1. TRANSIENT RESPONSE

LARGE SIGNAL RESPONSE
V_{OUT} = 0 to +10V
Vertical Scale: (V_{IN} = 5V/Div.; V_{OUT} = 2V/Div.)
Horizontal Scale: (100ns/Div.)



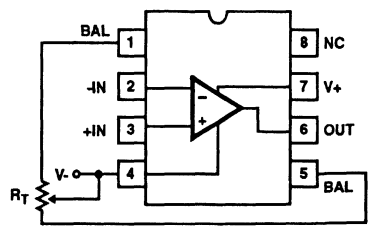
SMALL SIGNAL RESPONSE
V_{OUT} = 0 to +200mV
Vertical Scale: (V_{IN} = 100mV/Div.; V_{OUT} = 100mV/Div.)
Horizontal Scale: (100ns/Div.).





- A_V = -1
- Feedback and summing resistor ratios should be 0.1% matched.
- HP5082-2810 clipping diodes recommended.
- Tektronix P6201 FET probe used at settling point.

FIGURE 2. SETTLING TIME TEST CIRCUIT



Tested offset adjustment range is $|V_{OS}$ + 1mV| minimum referred to output. Typical range for R_T = 20kΩ is approximately ±30mV.

FIGURE 3. OFFSET VOLTAGE ADJUSTMENT

Typical Performance Curves

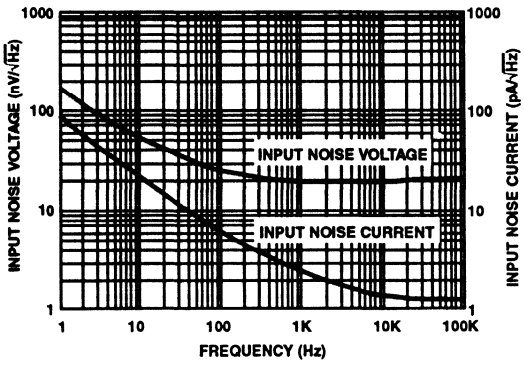


FIGURE 4. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY

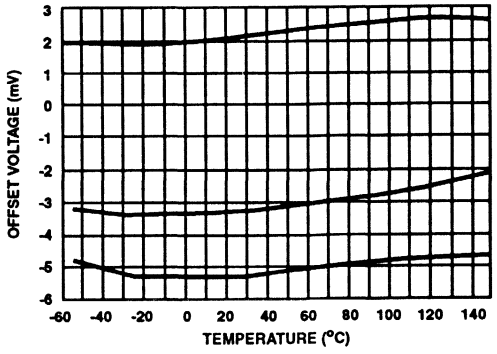
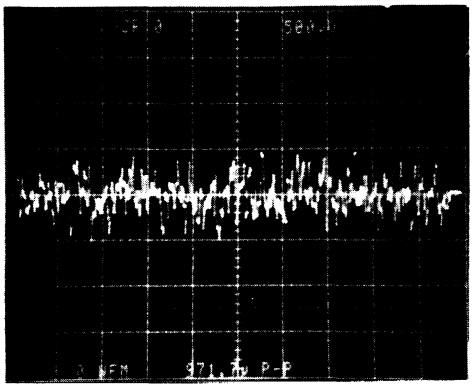


FIGURE 5. INPUT OFFSET VOLTAGE vs TEMPERATURE (3 TYPICAL UNITS)



0.1Hz to 10Hz, Noise Voltage = 0.97μV_{P-P}

FIGURE 6. NOISE VOLTAGE (A_V = 1000)

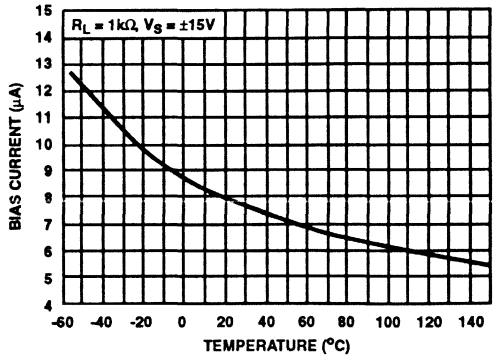


FIGURE 7. INPUT BIAS CURRENT vs TEMPERATURE

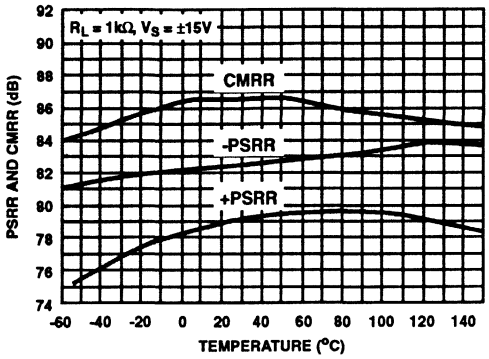


FIGURE 8. PSRR AND CMRR vs TEMPERATURE

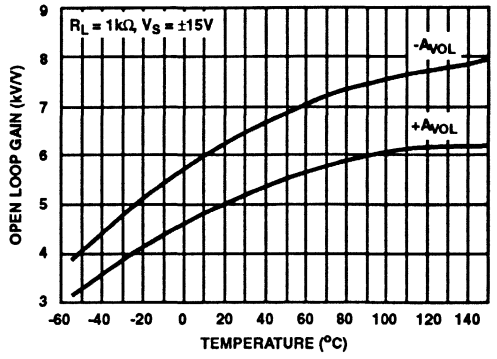


FIGURE 9. OPEN LOOP GAIN vs TEMPERATURE

Typical Performance Curves (Continued)

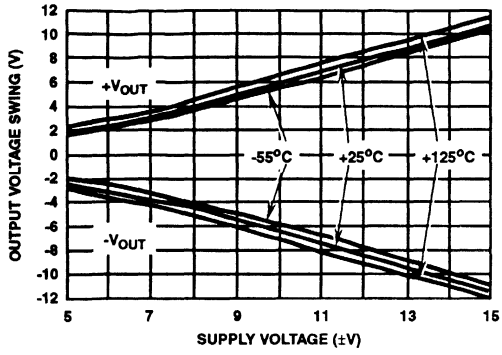


FIGURE 10. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (OVER FULL TEMPERATURE)

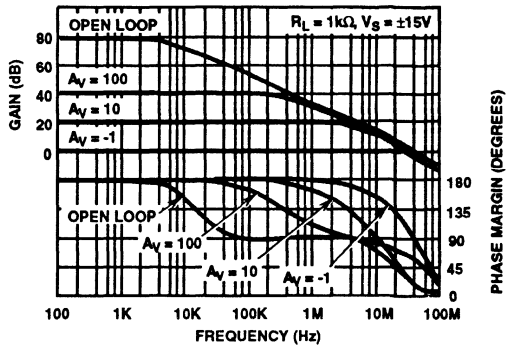


FIGURE 11. FREQUENCY RESPONSE AT VARIOUS GAINS

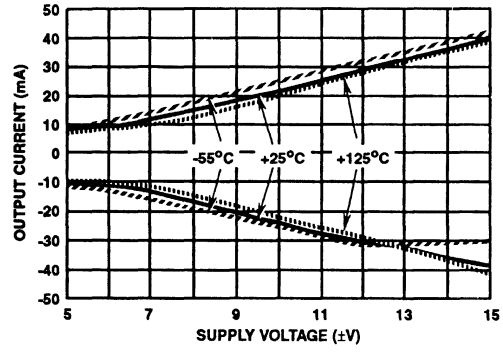


FIGURE 12. OUTPUT CURRENT vs SUPPLY VOLTAGE (OVER FULL TEMPERATURE)

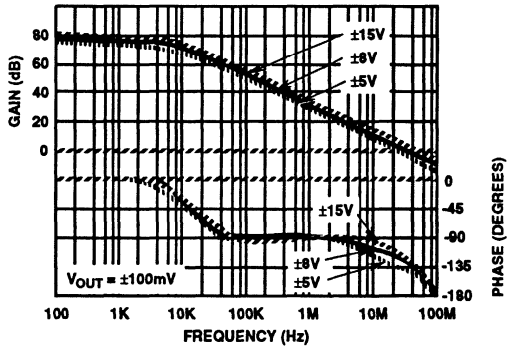


FIGURE 13. OPEN LOOP RESPONSE

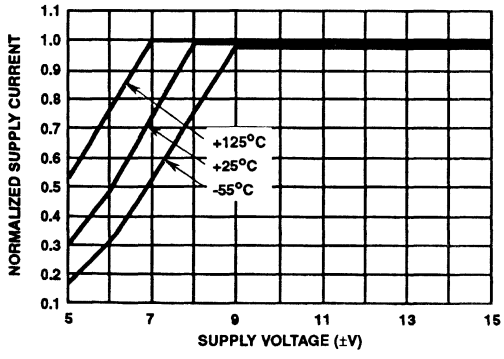


FIGURE 14. SUPPLY CURRENT vs SUPPLY VOLTAGE (NORMALIZED AT V_S = ±15V AT +25°C)

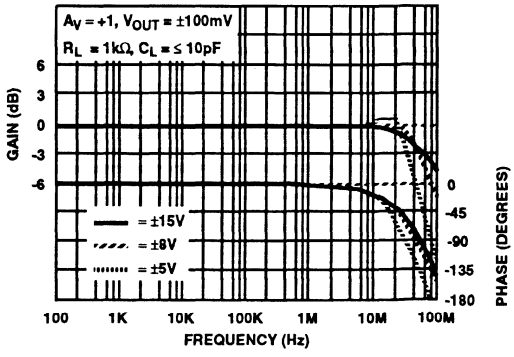


FIGURE 15. VOLTAGE FOLLOWER RESPONSE

Typical Video Performance Curves

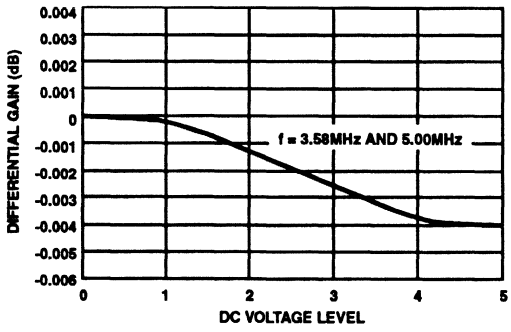


FIGURE 16. AC GAIN VARIATION vs DC OFFSET LEVELS (DIFFERENTIAL GAIN)

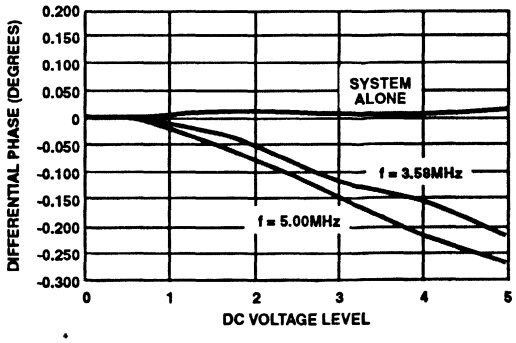
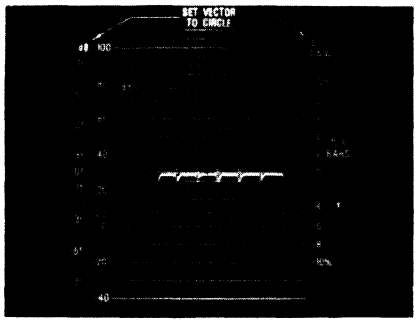
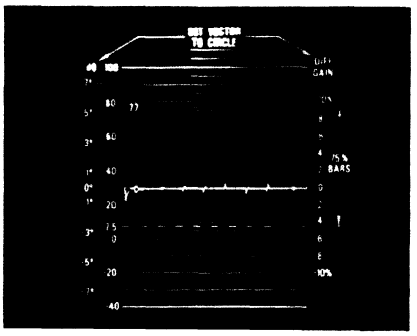


FIGURE 17. AC PHASE VARIATION vs DC OFFSET LEVELS (DIFFERENTIAL PHASE)



NTSC Method, R_L = 1kΩ, Differential Gain < 0.05% at T_A = +75°C
No Visual Difference at T_A = -55°C or +125°C

FIGURE 18. DIFFERENTIAL GAIN



NTSC Method, R_L = 1kΩ, Differential Phase < 0.05 Degree at T_A = +75°C
No Visual Difference at T_A = -55°C or +125°C

FIGURE 19. DIFFERENTIAL PHASE

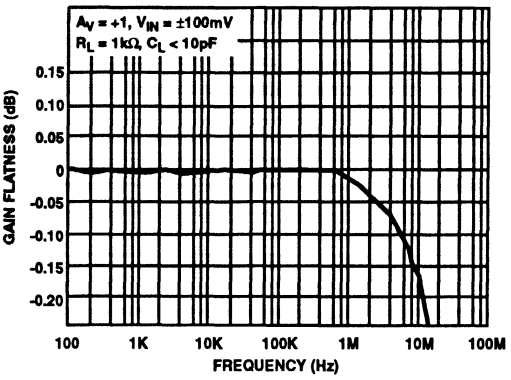
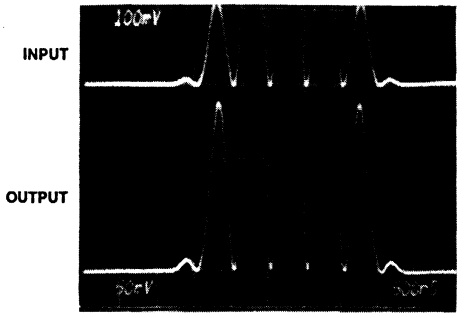


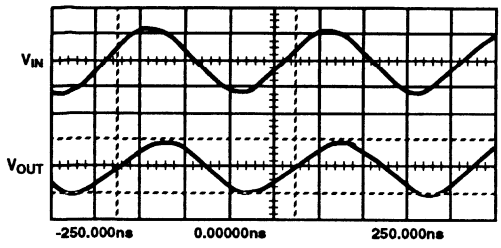
FIGURE 20. GAIN FLATNESS



NTSC Method, R_L = 1kΩ, C-L Delay < 7ns at T_A = +75°C
No Visual Difference at T_A = -55°C or +125°C
Vertical Scale: Input = 100mV/Div., Output = 50mV/Div.
Horizontal Scale: 500ns/Div.

FIGURE 21.CHROMINANCE TO LUMINANCE DELAY

Typical Video Performance Curves (Continued)



V_{IN} = 2.0V/Div., V_{OUT} = 2.0V/Div., Timebase = 50ns

FIGURE 22. ±2V OUTPUT SWING (WITH R_{LOAD} = 75Ω, FREQUENCY = 5.00MHz)

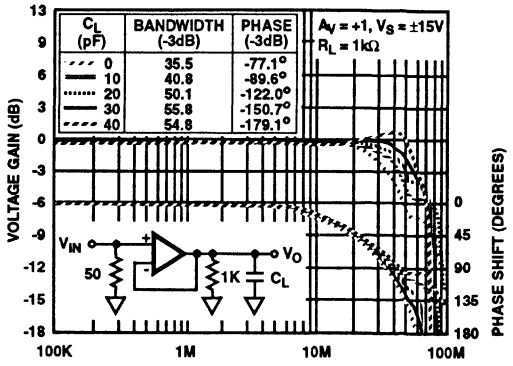


FIGURE 23. BANDWIDTH vs LOAD CAPACITANCE

Applications and Product Guidelines

The HA-2544 is a true differential op amp that is as versatile as any op amp but offers the advantages of high unity gain bandwidth, high speed and low supply current. More important than its general purpose applications is that the HA-2544 was especially designed to meet the requirements found in a video amplifier system. These requirements include fine picture resolution and accurate color rendition, and must meet broadcast quality standards.

In a video signal, the video information is carried in the amplitude and phase as well as in the DC level. The amplifier must pass the 30Hz line rate luminance level and the 3.58MHz (NTSC) or 4.43MHz (PAL) color band without altering phase or gain. The HA-2544's key specifications aimed at meeting this include high bandwidth (50MHz), very low gain flatness (0.12dB at 10MHz), near unmeasurable differential gain and differential phase (0.03% and 0.03 degrees), and low noise (20nV/$\sqrt{Hz}$). The HA-2544 meets these quidelines.

The HA-2544 also offers the advantage of a full output voltage swing of ±10V into a 1kΩ load. This equates to a full power bandwidth of 2.4MHz for this ±10V signal. If video signal levels of ±2V maximum is used (with R_L = 1kΩ), the full power bandwidth would be 11.9MHz without clipping distortion. Another usage might be required for a direct 50Ω or 75Ω load where the HA-2544 will still swing this ±2V signal as shown in the above display. One important note that must be realized is that as load resistance decreases the video parameters are also degraded. For optimal video performance a 1 kΩ load is recommended.

If lower supply voltages are required, such as ±5V, many of the characterization curves indicate where the parameters vary. As shown the bandwidth, slew rate and supply current are still very well maintained.

Prototyping and PC Board Layout

When designing with the HA-2544 video op amp as with any high performance device, care should be taken to use high frequency layout techniques to avoid unwanted parasitic effects. Short lead lengths, low source impedance and lower value feedback resistors help reduce unwanted poles or zeros. This layout would also include ground plane construction and power supply decoupling as close to the supply pins with suggested parallel capacitors of 0.1µF and 0.001µF ceramic to ground.

In the noninverting configuration, the amplifier is sensitive to stray capacitance (<40pF) to ground at the inverting input. Therefore, the inverting node connections should be kept to a minimum. Phase shift will also be introduced as load parasitic capacitance is increased. A small series resistor (20Ω to 100Ω) before the capacitance effectively decouples this effect.

Stability/Phase Margin/Compensation

The HA-2544 has not sacrificed unity gain stability in achieving its superb AC performance. For this device, the phase margin exceeds 60 degrees at the unity crossing point of the open loop frequency response. Large phase margin is critical in order to reduce the differential phase and differential gain errors caused by most other op amps. Because this part is unity gain stable, no compensation pin is brought out. If compensation is desired to reduce the noise bandwidth, most standard methods may be used. One method suggested for an inverting scheme would be a series R-C from the inverting node to ground which will reduce bandwidth, but not effect slew rate. If the user wishes to achieve even higher bandwidth (>50MHz), and can tolerate some slight gain peaking and lower phase margin, experimenting with various load capacitance can be done.

Shown in Application 1 is an excellent Differential Input, Unity Gain Buffer which also will terminate a cable to 75Ω and reject common mode voltages. Application 2 is a method of separating a video signal up into the Sync. only signal and the Video and Blanking signal. Application 3 shows the HA-2544 being used as a 100kHz High Pass 2-Pole Butterworth Filter. Also shown is the measured frequency response curves.

Typical Applications

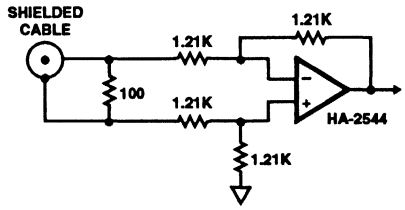


FIGURE 24. APPLICATION 1, 75Ω DIFFERENTIAL INPUT BUFFER

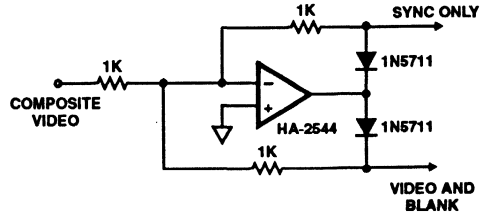


FIGURE 25. APPLICATION 2, COMPOSITE VIDEO SYNC. SEPARATOR

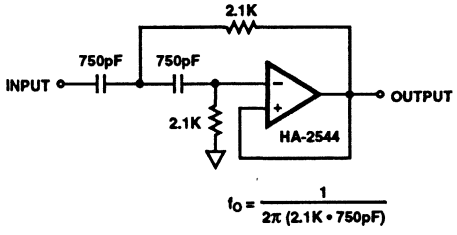


FIGURE 26. APPLICATION 3, 100kHz HIGH PASS 2-POLE BUTTERWORTH FILTER

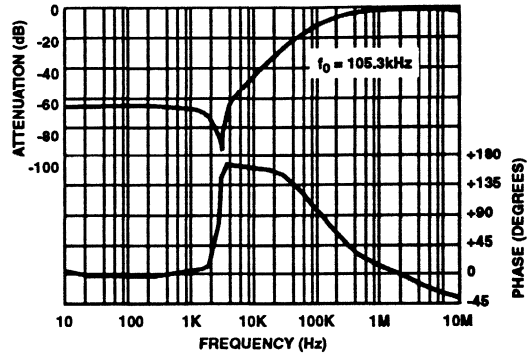


FIGURE 27. MEASURED FREQUENCY RESPONSE OF APPLICATION 3

HARRIS SEMICONDUCTOR

HA-2548

Precision, High Slew Rate, Wideband Operational Amplifier

March 1993

Features

- High Slew Rate 120V/μs
- Low Offset Voltage 300μV
- High Open Loop Gain 130dB
- Gain Bandwidth Product 150MHz
- Low Noise Voltage at 1kHz ..... 8.3nV/√Hz
- Minimum Gain Stability ..... ≥5

Applications

- High Speed Instrumentation
- Data Acquisition Systems
- Analog Signal Conditioning
- Precision, Wideband Amplifiers
- Pulse/RF Amplifiers

Description

The HA-2548 is a monolithic op amp that offers a unique combination of bandwidth, slew rate, and precision specifications. These features can eliminate the need for composite op amp designs and external calibration circuitry.

Optimized for gains ≥5, the HA-2548 has a gain-bandwidth product of 150MHz and a slew rate of 120V/μs while maintaining extremely high open loop gain (130dB typ) and low offset voltage (300μV typ). These specifications are achieved through uniquely designed input circuitry and a single ultra-high gain stage that minimizes the AC signal path. Capable of delivering over 30mA of output current, the HA-2548 is ideal for precision, high speed applications such as signal conditioning, instrumentation, video/pulse amplifiers and buffers.

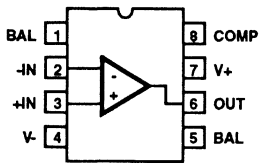
For information on the military version of this device please refer to the HA-2548/883 datasheet.

Ordering Information

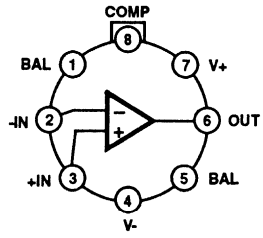
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-2548-5	0°C to +75°C	8 Pin CAN
HA2-2548-9	-40°C to +85°C	8 Pin CAN
HA3-2548-5	0°C to +75°C	8 Lead Plastic DIP
HA7-2548-5	0°C to +75°C	8 Lead Ceramic Sidebraze DIP
HA7-2548-9	-40°C to +85°C	8 Lead Ceramic Sidebraze DIP
HA9P2548-5	0°C to +75°C	16 Lead Wide Body SOIC

Pinouts

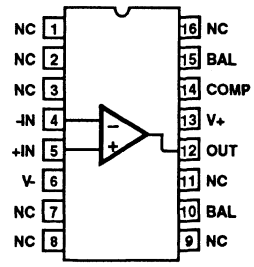
HA-2548
(PDIP, CDIP)
TOP VIEW



HA-2548
(TO-99 CAN)
TOP VIEW



HA-2548
(300 mil SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2901.1**

Absolute Maximum Ratings (Note 1)

Supply Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 5V
Output Current 40mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-2548-5 ..... $0°C \le T_A \le +75°C$
HA-2548-9 ..... $-40°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +15V, V- = -15V, R_L = 1K, C_L = 10pF, Unless Otherwise Specified.

PARAMETER	TEMP	HA-2548-5, -9 LIMITS			HA-2548A-5 LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Offset Voltage	+25°C	-	300	900	-	100	300	µV
	Full	-	400	1200	-	200	600	µV
Average Offset Voltage Drift (Note 12)	Full	-	4	9	-	3	7	µV/°C
Input Bias Current	+25°C	-	5	50	-	5	50	nA
	Full	-	20	100	-	20	100	nA
Input Offset Current	+25°C	-	5	50	-	5	50	nA
	Full	-	20	100	-	20	100	nA
Common Mode Range	+25°C	±7	±10	-	±7	±10	-	V
Differential Input Resistance	+25°C	-	1	-	-	1	-	MΩ
Input Noise Voltage (f = 0.1Hz to 10Hz)	+25°C	-	0.2	-	-	0.2	-	µVrms
(f = 0.1Hz to 1MHz)	+25°C	-	0.8	-	-	0.8	-	µVrms
Input Noise Voltage Density (Note 2) (f = 10Hz)	+25°C	-	30	-	-	30	-	$nV/\sqrt{Hz}$
(f = 100Hz)	+25°C	-	12	-	-	12	-	$nV/\sqrt{Hz}$
(f = 1000Hz)	+25°C	-	8.3	-	-	8.3	-	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 2) (f = 10Hz)	+25°C	-	1.9	-	-	1.9	-	$pA/\sqrt{Hz}$
(f = 100Hz)	+25°C	-	0.7	-	-	0.7	-	$pA/\sqrt{Hz}$
(f = 1000Hz)	+25°C	-	0.4	-	-	0.4	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	114	130	-	120	130	-	dB
	Full	108	125	-	118	125	-	dB
Common Mode Rejection Ratio (Note 4)	Full	80	90	-	80	90	-	dB
Gain Bandwidth Product (Notes 5, 12)	+25°C	130	150	-	130	150	-	MHz
	Full	110	125	-	110	125	-	MHz
Minimum Stable Gain	Full	5	-	-	5	-	-	V/V
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±11	±12	-	±11	±12	-	V
Output Current (Note 6)	Full	±30	±33	-	±30	±33	-	mA
Output Resistance	+25°C	-	5	-	-	5	-	Ω
Full Power Bandwidth (Note 7)	+25°C	-	1.91	-	-	1.91	-	MHz

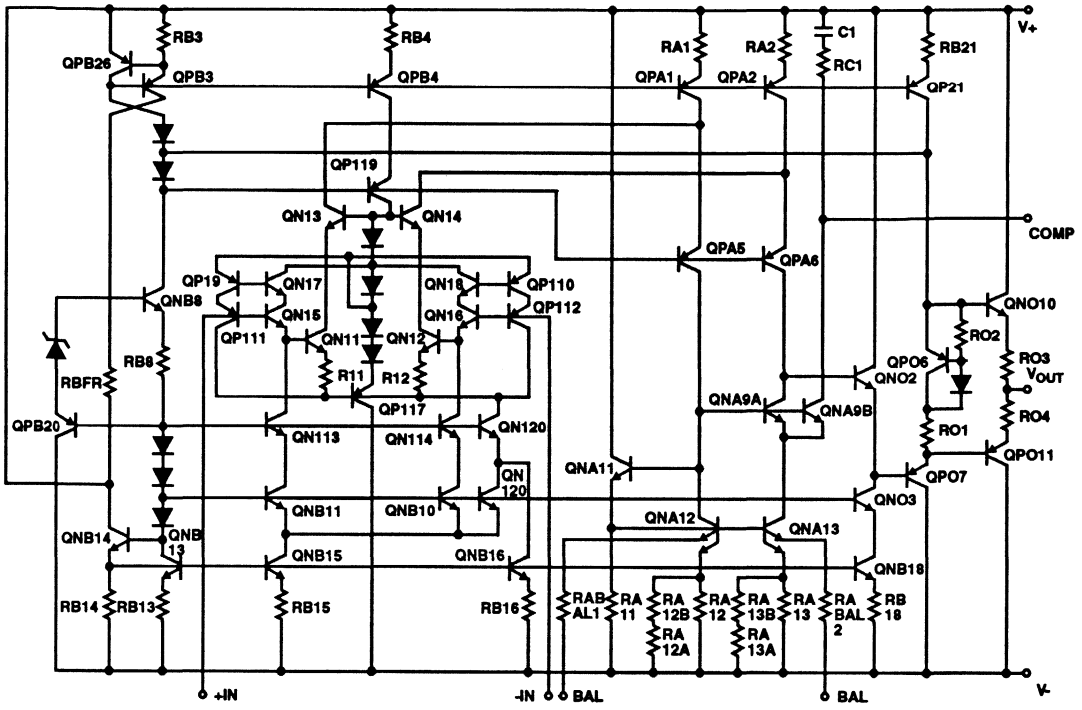
Electrical Specifications V+ = +15V, V- = -15V, R_L = 1K, C_L = 10pF, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEMP	HA-2548-5, -9 LIMITS			HA-2548A-5 LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE								
Slew Rate (Notes 8, 12) Positive	+25°C	80	120	-	80	120	-	V/µs
	Full	70	105	-	70	105	-	V/µs
Slew Rate (Notes 8, 12) Negative	+25°C	70	110	-	70	110	-	V/µs
	Full	60	105	-	60	105	-	V/µs
Rise Time (Notes 9, 12)	+25°C	-	16.5	20	-	16.5	20	ns
	Full	-	19	23	-	19	23	ns
Fall Time (Notes 9, 12)	+25°C	-	16	20	-	16	20	ns
	Full	-	18	23	-	18	23	ns
Overshoot (Notes 9, 12) Positive	+25°C	-	15	25	-	15	25	%
	Full	-	25	35	-	25	35	%
Overshoot (Notes 9, 12) Negative	+25°C	-	8	15	-	8	15	%
	Full	-	20	30	-	20	30	%
Settling Time (Notes 10, 12)	+25°C	-	200	260	-	200	260	ns
POWER SUPPLY								
Power Supply Rejection Ratio (Note 11)	Full	86	95	-	86	95	-	dB
I_{CC}	Full	-	12	18	-	12	18	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceable of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Refer to typical performance curve in data sheet.
3. V_{OUT} = ±10V.
4. V_{CM} = ±2V.
5. Characterized in an A_V = -100 configuration from 100kHz to 10MHz.
6. R_L = 1kΩ, V_{OUT} > 10V.
7. Full Power Bandwidth is calculated by: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$, V_{PEAK} = 10V
8. V_{OUT} = ±5V, A_V = +5.
9. V_{OUT} = ±100mV, A_V = +5.
10. Settling time is specified to 0.01% with a 10V step and A_V = -5.
11. Delta V_S = ±10V to ±20V.
12. These parameters are not tested. The limits are guaranteed based on lab characterization and reflect lot to lot variation.

Schematic Diagram



Die Characteristics

Transistor Count 60
Die Dimensions ..... 85 x 91 x 19 mils (2160 x 2320 x 482µm)
Substrate Potential* ..... V-
Process ..... High Frequency Bipolar DI
Metallization:
- Type: ..... Aluminum, 1% Copper
- Thickness: ..... 16kÅ ± 2kÅ

Glassivation:
- Type: ..... Nitride over Silox
- Silox Thickness: ..... 12kÅ ± 2kÅ
- Nitride Thickness: ..... 3.5kÅ ± 1kÅ

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Sidebrazed Ceramic DIP	75	12
Plastic DIP	92	30
SOIC	96	26
CAN	105	32

* The substrate may be left floating (Insulating Die Mount) or it may be mounted on conductor at V- potential.

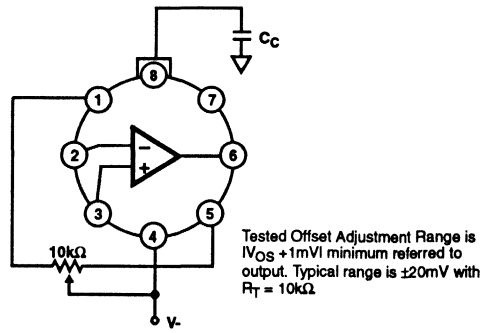
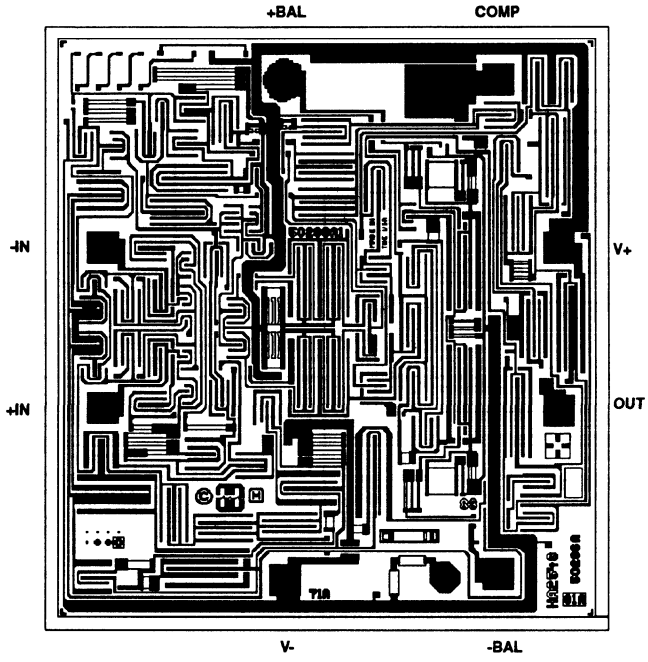


FIGURE 1. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK UP

Metallization Mask Layout

HA-2548



Test Circuits and Waveforms

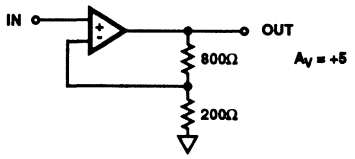


FIGURE 2. LARGE AND SMALL SIGNAL RESPONSE CIRCUIT

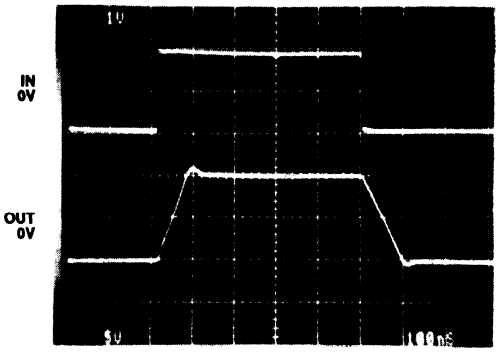


FIGURE 3. LARGE SIGNAL RESPONSE
V_{OUT} = ±5V, A_V = +5, R_L = 1K, C_L ≤ 10pF

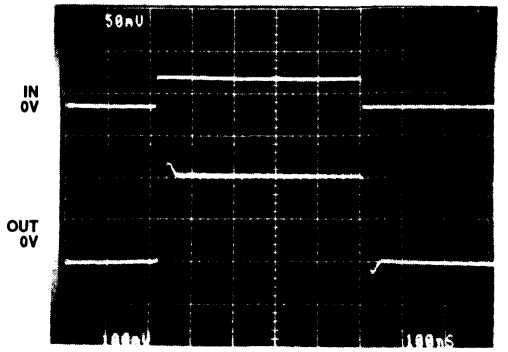
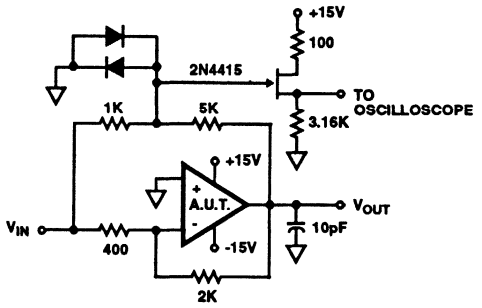


FIGURE 4. SMALL SIGNAL RESPONSE
V_{OUT} = ±100mV, A_V = +5, R_L = 1K, C_L ≤ 10pF



- A_V = -5
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 5. SETTLING TIME TEST CIRCUIT

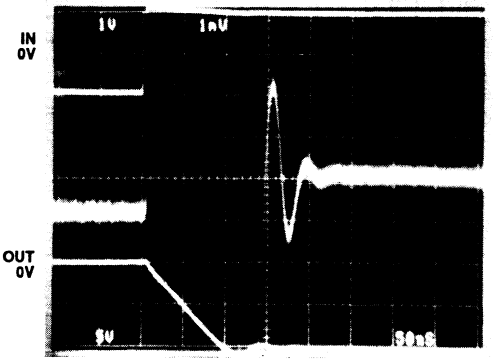


FIGURE 6. HA-2548 SETTLING TIME
A_V = -5, Output = -10V Output Scale Vertical: 1mV/Div, Horizontal: 50ns/Div

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$

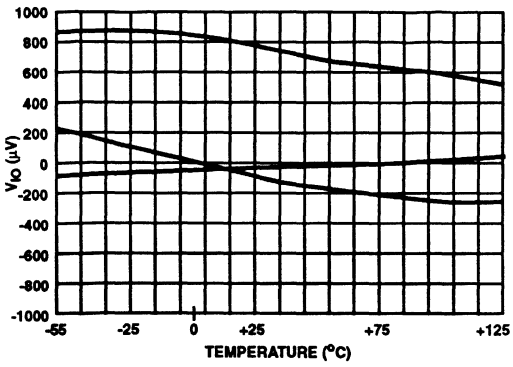


FIGURE 7. V_{IO} vs TEMPERATURE
(3 Representative Units)

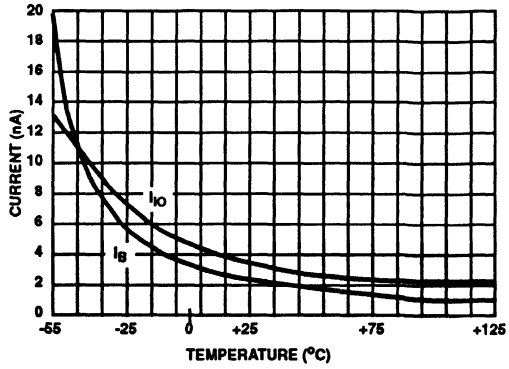


FIGURE 8. OFFSET CURRENT/BIAS CURRENT vs TEMPERATURE

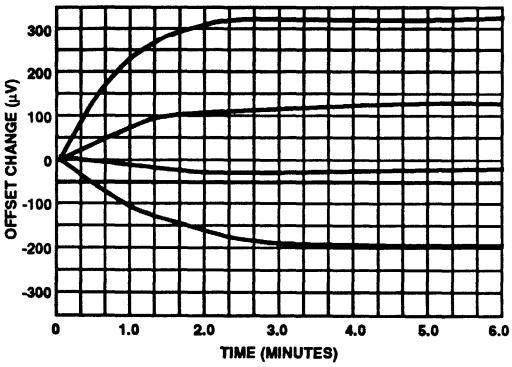


FIGURE 9. V_{IO} WARM-UP DRIFT (NORMALIZED FROM ZERO)
(4 Representative Units)

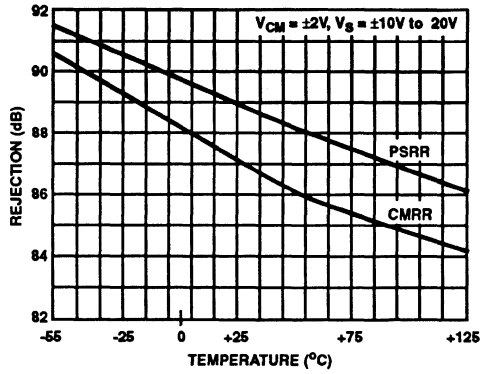


FIGURE 10. PSRR/CMRR vs TEMPERATURE

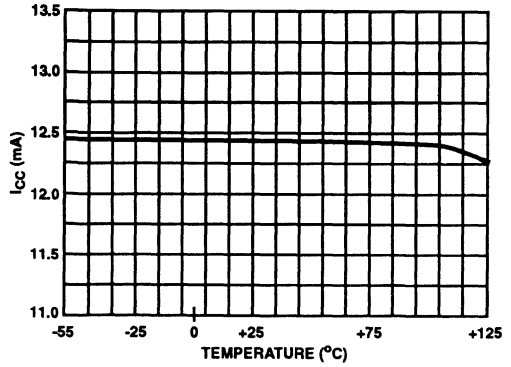


FIGURE 11. I_{CC} vs TEMPERATURE

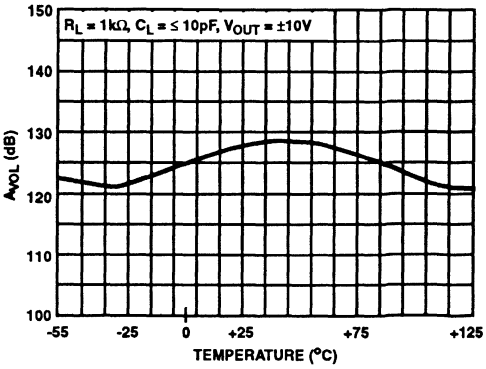


FIGURE 12. A_{VOL} vs TEMPERATURE

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$ (Continued)

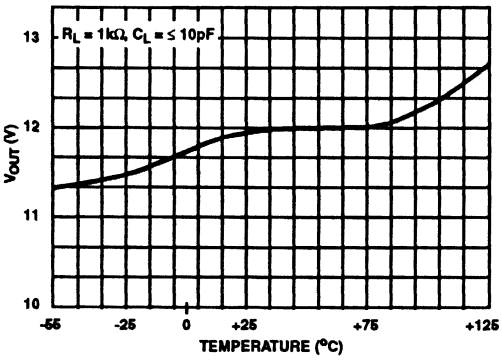


FIGURE 13. V_{OUT} vs TEMPERATURE

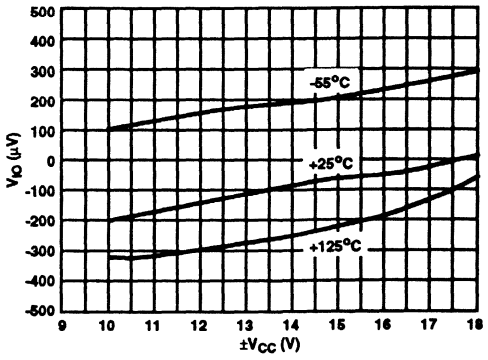


FIGURE 14. V_{IO} vs ±V_{CC} vs TEMPERATURE

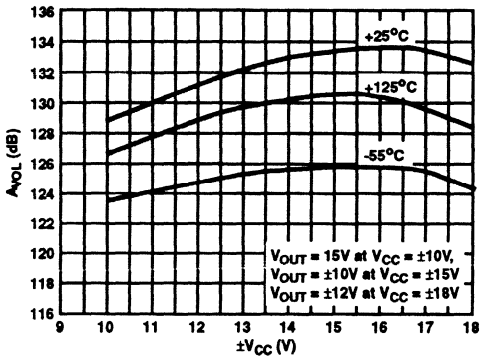


FIGURE 15. A_{VOL} vs ±V_{CC} vs TEMPERATURE

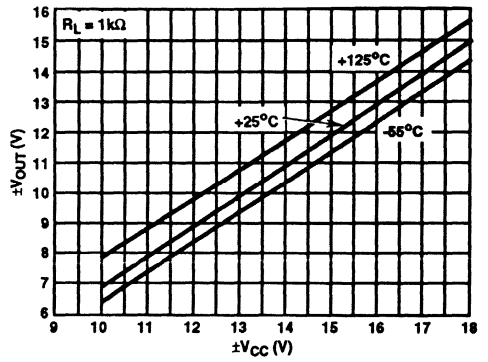


FIGURE 16. ±V_{OUT} vs ±V_{CC} vs TEMPERATURE

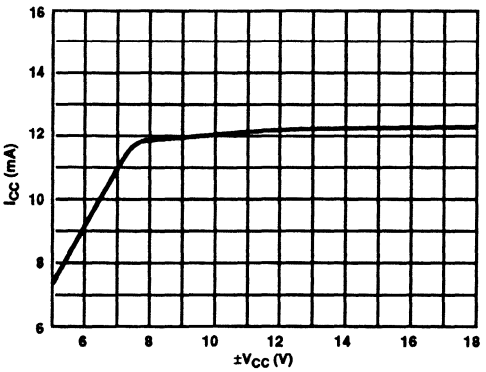


FIGURE 17. SUPPLY CURRENT vs SUPPLY VOLTAGE

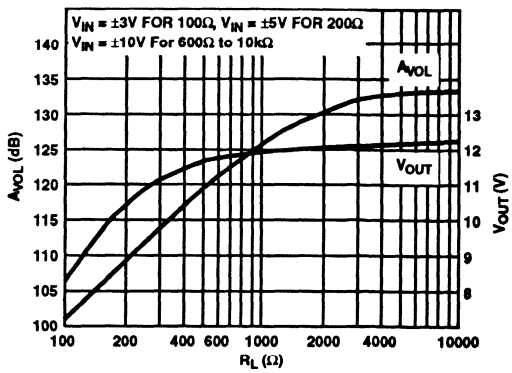


FIGURE 18. A_{VOL}/V_{OUT} vs R_L

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$ (Continued)

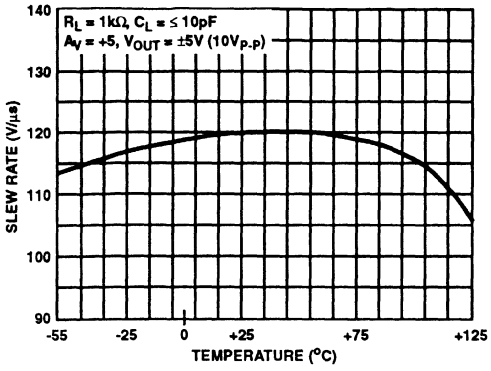


FIGURE 19. SLEW RATE vs TEMPERATURE

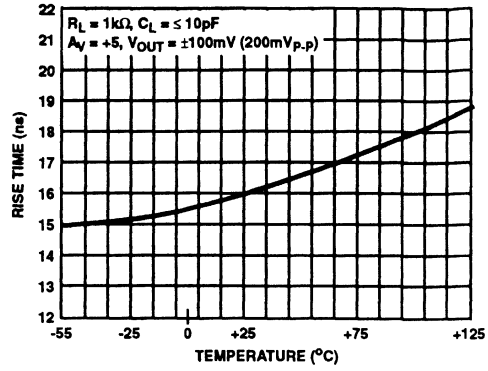


FIGURE 20. RISE TIME vs TEMPERATURE

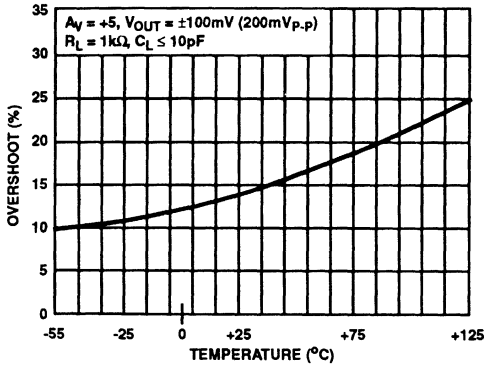


FIGURE 21. OVERSHOOT vs TEMPERATURE

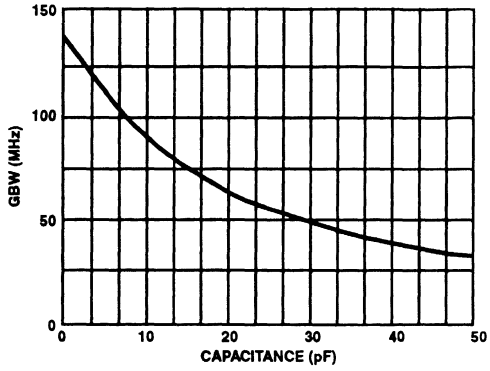


FIGURE 22. GAIN BANDWIDTH PRODUCT vs COMPENSATION CAPACITANCE TO GND

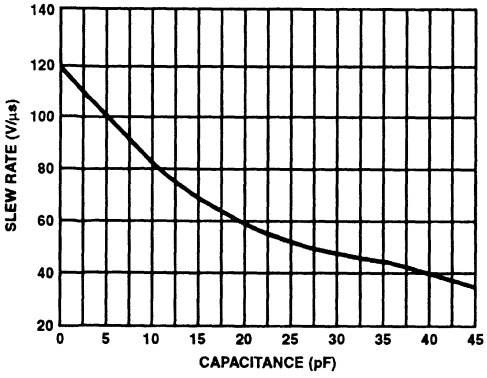


FIGURE 23. SLEW RATE vs COMPENSATION CAPACITANCE TO GND

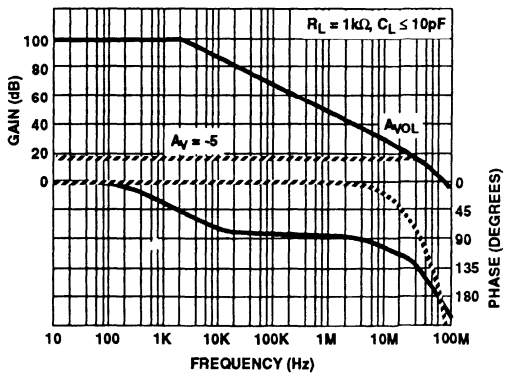


FIGURE 24. GAIN AND PHASE vs FREQUENCY

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$ (Continued)

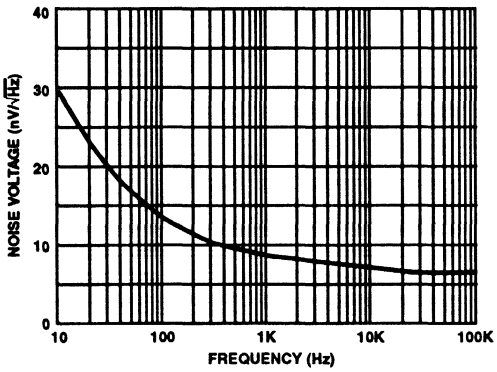


FIGURE 25. INPUT NOISE VOLTAGE DENSITY

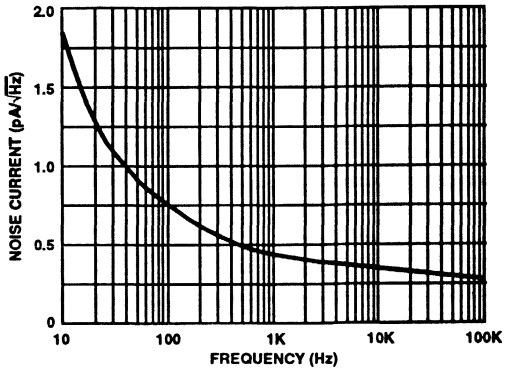


FIGURE 26. INPUT NOISE CURRENT DENSITY

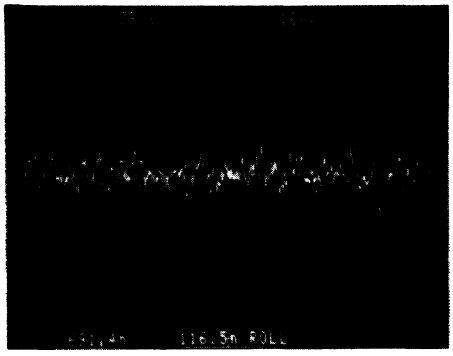


FIGURE 27. PEAK TO PEAK NOISE 0.1HZ TO 10HZ
p-p(RTI) = 691.4nV, rms(RTI) = 116.5nV, A_V = 25000

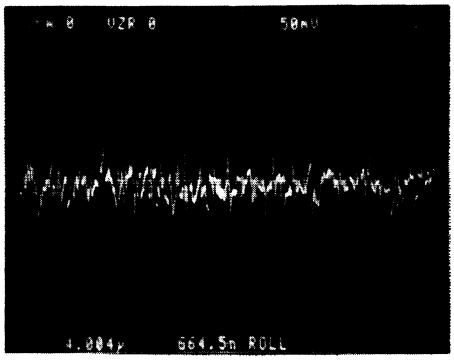


FIGURE 28. PEAK TO PEAK NOISE 0.1HZ TO 1MHZ
p-p(RTI) = 4.004µV, rms(RTI) = 664.5nV, A_V = 25000

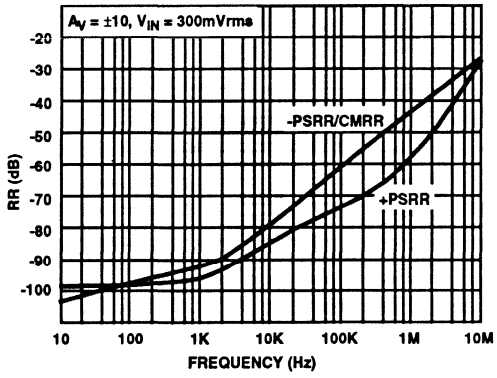


FIGURE 29. REJECTION RATIOS vs FREQUENCY

HARRIS SEMICONDUCTOR

HA-2600, HA-2602 HA-2605

Wideband, High Impedance Operational Amplifiers

March 1993

Features

- Wide Bandwidth 12MHz
- High Input Impedance 500MΩ
- Low Input Bias Current 1nA
- Low Input Offset Current 1nA
- Low Input Offset Voltage 0.5mV
- High Gain 150kV/V
- High Slew Rate 7V/μs
- Output Short Circuit Protection
- Unity Gain Stable

Applications

- Video Amplifier
- Pulse Amplifier
- Audio Amplifiers and Filters
- High-Q Active Filters
- High-Speed Comparators
- Low Distortion Oscillators

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-2600-2	-55°C to +125°C	8 Pin Can
HA2-2602-2	-55°C to +125°C	8 Pin Can
HA2-2605-5	0°C to +75°C	8 Pin Can
HA3-2605-5	0°C to +75°C	8 Lead Plastic DIP
HA4P2605-5	0°C to +75°C	20 Lead PLCC
HA7-2600-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-2602-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-2605-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P2605-5	0°C to +75°C	8 Lead SOIC
HA9P2605-9	-40°C to +85°C	8 Lead SOIC

Description

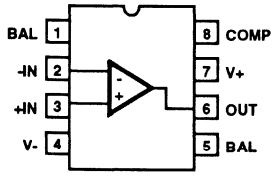
HA-2600/2602/2605 are internally compensated bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2600) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2600) and low bias and offset current (1nA, HA-2600) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 12MHz unity gain-bandwidth, 7V/μs slew rate and 150kV/V open-loop gain enables HA-2600/2602/2605 to perform high-gain amplification of fast, wideband signals. These dynamic characteristics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs, HA-2600/2602/2605 are particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators. For more information, please refer to Application Note 515.

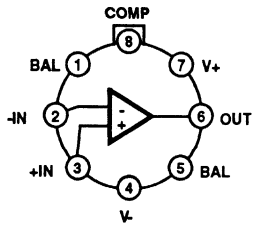
The HA-2600 and HA-2602 are offered as /883 Military Grade; product and data sheets are available upon request.

Pinouts

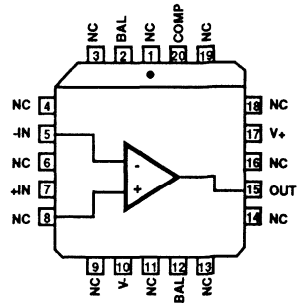
HA-2600/02 (CDIP)
HA-2605 (PDIP, CDIP, SOIC)
TOP VIEW



HA-2600/02/05
(TO-99 METAL CAN)
TOP VIEW



HA-2605, (PLCC)
TOP VIEW



File Number 2902.1

Absolute Maximum Ratings (Note 13)

Supply Voltage Between V+ and V- Terminals 45.0V
Differential Input Voltage 12.0V
Peak Output Current . . . . . Full Short Circuit Protection
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Operating Temperature Range
HA-2600/HA-2602-2 . . . . . $-55°C \leq T_A \leq +125°C$
HA-2605-5 . . . . . $0°C \leq T_A \leq +75°C$
HA-2605-9 . . . . . $-40°C \leq T_A \leq +85°C$
Storage Temperature Range . . . . . $-65°C \leq T_A \leq +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_S = \pm 15V$ D.C., Unless Otherwise Specified

PARAMETER	TEMP	HA-2600-2			HA-2602-2			HA-2605-5			(NOTE 15) HA-2605-9	UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MAX	
INPUT CHARACTERISTICS												
Offset Voltage	+25°C	-	0.5	4	-	3	5	-	3	5	5	mV
	Full	-	2	6	-	-	7	-	-	7	7	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-	-	5	-	-	µV/°C
Bias Current	+25°C	-	1	10	-	15	25	-	5	25	25	nA
	Full	-	10	30	-	-	60	-	-	40	70	nA
Offset Current	+25°C	-	1	10	-	5	25	-	5	25	25	nA
	Full	-	5	30	-	-	60	-	-	40	70	nA
Differential Input Resistance (Note 10)	+25°C	100	500	-	40	300	-	40	300	-	-	MΩ
Input Noise Voltage Density f = 1kHz	+25°C	-	11	-	-	11	-	-	11	-	-	$nV/\sqrt{Hz}$
Input Noise Current Density f = 1kHz	+25°C	-	0.16	-	-	0.16	-	-	0.16	-	-	$pA/\sqrt{Hz}$
Common Mode Range	Full	±11	±12	-	±11	±12	-	±11	±12	-	-	V
TRANSFER CHARACTERISTICS												
Large Signal Voltage Gain (Notes 1, 4)	+25°C	100	150	-	80	150	-	80	150	-	-	kV/V
	Full	70	-	-	60	-	-	70	-	-	-	kV/V
Common Mode Rejection Ratio (Note 2)	Full	80	100	-	74	100	-	74	100	-	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	1	-	-	-	V/V
Gain Bandwidth Product (Note 3)	+25°C	-	12	-	-	12	-	-	12	-	-	MHz
OUTPUT CHARACTERISTICS												
Output Voltage Swing (Note 1)	Full	±10	±12	-	±10	±12	-	±10	±12	-	-	V
Output Current (Note 4)	+25°C	±15	±22	-	±10	±18	-	±10	±18	-	-	mA
Full Power Bandwidth (Notes 4, 11)	+25°C	50	75	-	50	75	-	50	75	-	-	kHz

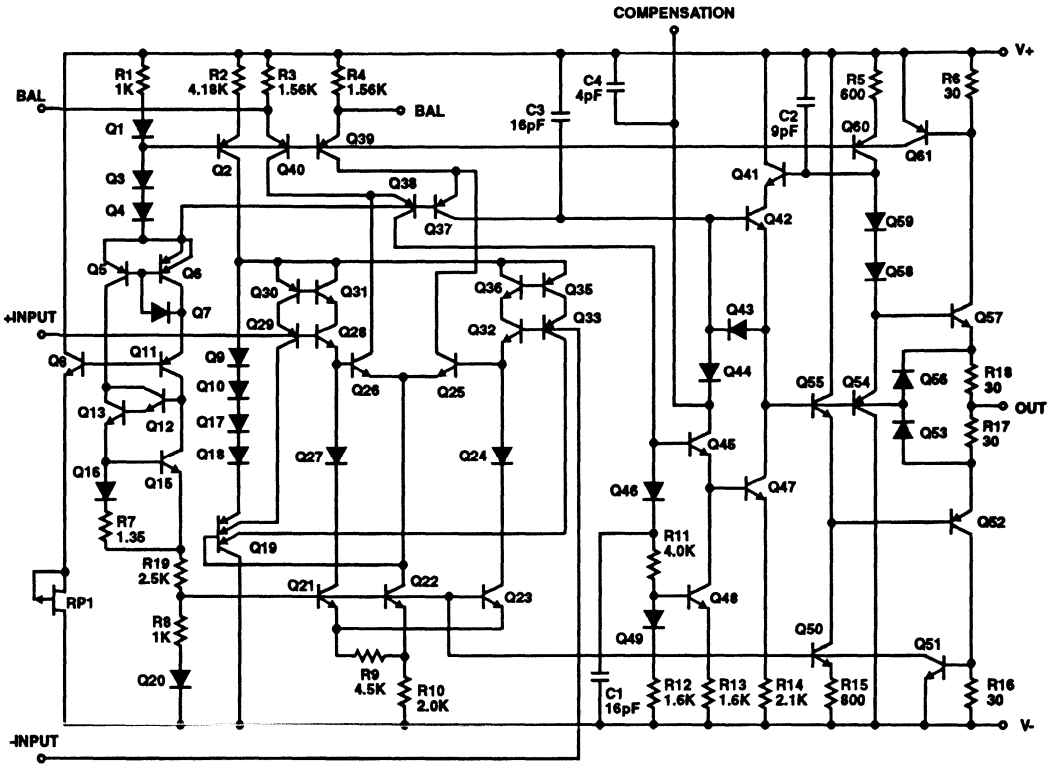
Electrical Specifications $V_S = \pm 15V$ D.C., Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	HA-2600-2			HA-2602-2			HA-2605-5			(NOTE 15) HA-2605-9	UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MAX	
TRANSIENT RESPONSE (Note 8)												
Rise Time (Notes 1, 5, 6 & 7)	+25°C	-	30	60	-	30	60	-	30	60	60	ns
Overshoot (Notes 1, 5, 6 & 7)	+25°C	-	25	40	-	25	40	-	25	40	40	%
Slew Rate (Notes 1, 5, 7 & 12)	+25°C	±4	±7	-	±4	±7	-	±4	±7	-	-	V/µs
Settling Time (Notes 1, 5 & 14)	+25°C	-	1.5	-	-	1.5	-	-	1.5	-	-	µs
POWER SUPPLY CHARACTERISTICS												
Supply Current	+25°C	-	3	3.7	-	3	4	-	3	4	4	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90	-	74	90	-	74	90	-	-	dB

NOTES:

1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 10V$
3. $V_{OUT} < 90mV$
4. $V_{OUT} = \pm 10V$
5. $C_L = 100pF$
6. $V_{OUT} = \pm 200mV$
7. $A_V = +1$
8. See Transient Response Test Circuits and Waveforms
9. $\Delta V_S = \pm 5V$
10. This parameter value guaranteed by design calculations.
11. Full Power Bandwidth guaranteed by slew rate measurement: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
12. $V_{OUT} = \pm 5V$
13. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
14. Settling time is characterized at $A_V = -1$ to 0.1% of a 10 Volt step.
15. Typical and minimum specifications for -9 are identical to those of -5.

Schematic Diagram



Die Characteristics

Transistor Count	140
Die Dimensions	69 x 56 x 19 mils
Substrate Potential	Unbiased

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Metal Can	117	36
Plastic DIP	96	34
Ceramic DIP	115	36
SOIC	157	43
PLCC	74	33

Test Circuits

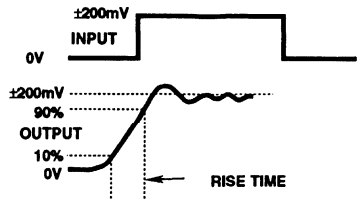


FIGURE 1. TRANSIENT RESPONSE

NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

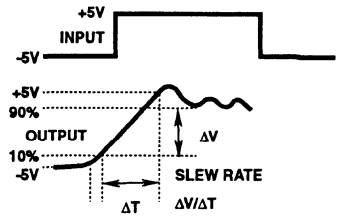


FIGURE 2. SLEW RATE

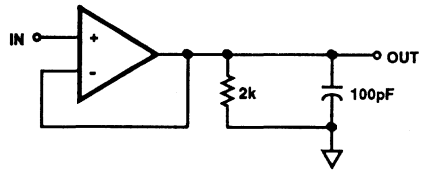


FIGURE 3. SLEW RATE AND TRANSIENT RESPONSE

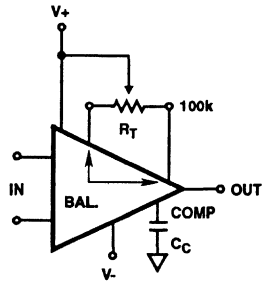


FIGURE 4. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK UP

NOTE: Tested offset adjustment range is $|V_{OS}| + 1mV|$ minimum referred to output. Typical ranges are ±10mV with $R_T = 100k\Omega$

Typical Performance Curves $V_S = \pm15VDC$, $T_A = +25°C$, Unless Otherwise Specified

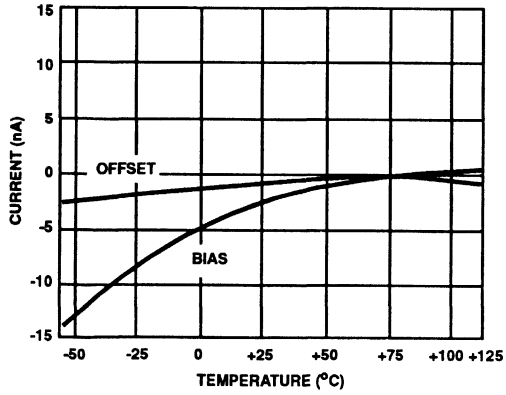


FIGURE 5. INPUT BIAS CURRENT AND OFFSET CURRENT vs TEMPERATURE

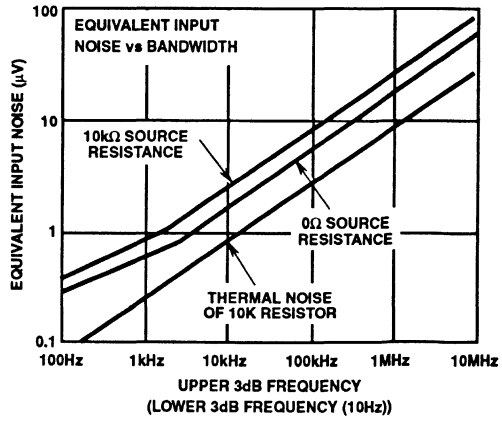


FIGURE 6. BROADBAND NOISE CHARACTERISTICS

Typical Performance Curves $V_S = \pm15VDC$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

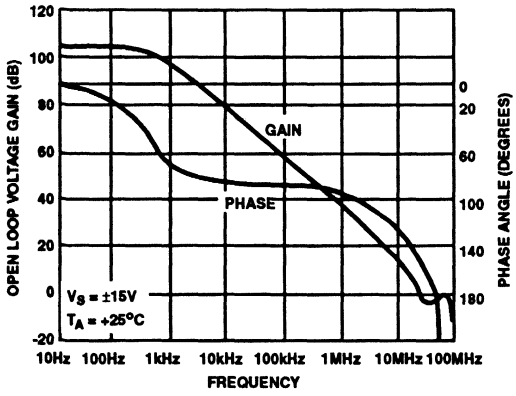


FIGURE 7. OPEN LOOP FREQUENCY AND PHASE RESPONSE

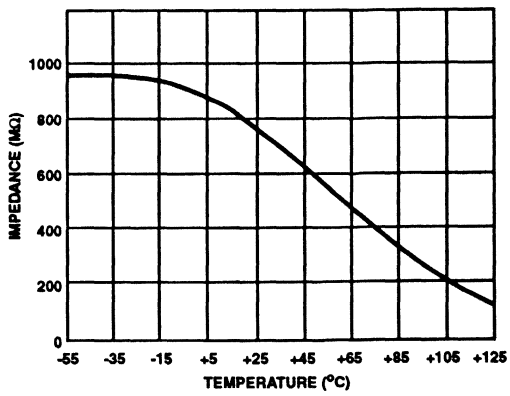


FIGURE 8. INPUT IMPEDANCE vs TEMPERATURE (100Hz)

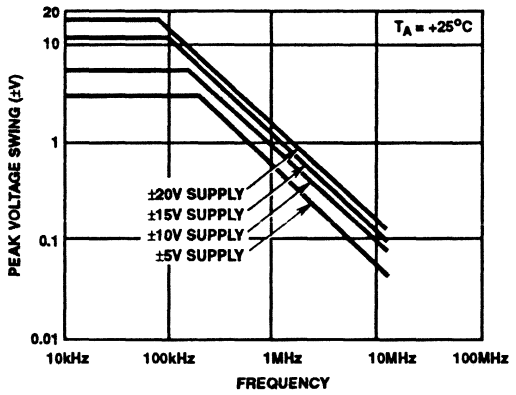


FIGURE 9. OUTPUT VOLTAGE SWING vs FREQUENCY

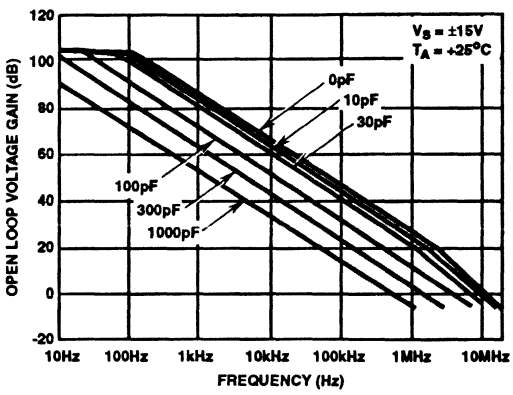


FIGURE 10. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired. If External Compensation is used, also connect 100pF capacitor from output to ground.

Typical Performance Curves $V_S = \pm15VDC$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

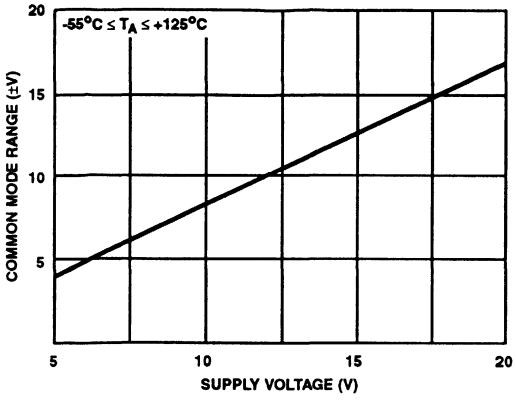


FIGURE 11. COMMON MODE VOLTAGE RANGE vs SUPPLY VOLTAGE

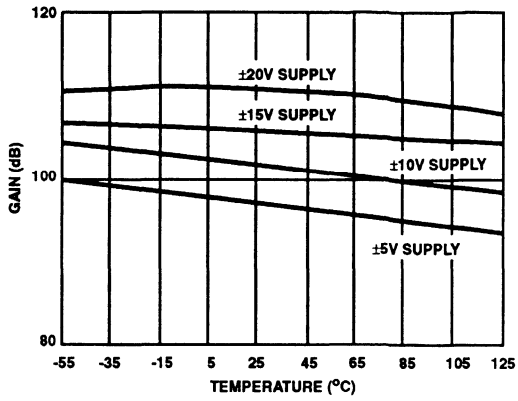


FIGURE 12. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

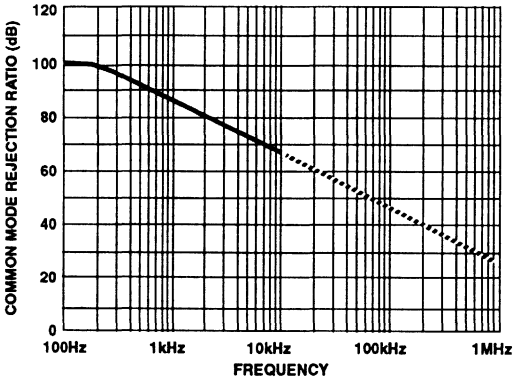


FIGURE 13. COMMON MODE REJECTION RATIO vs FREQUENCY

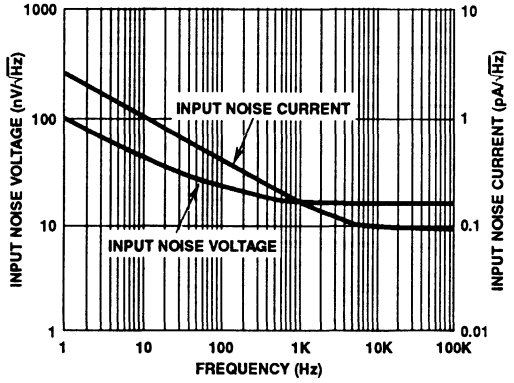
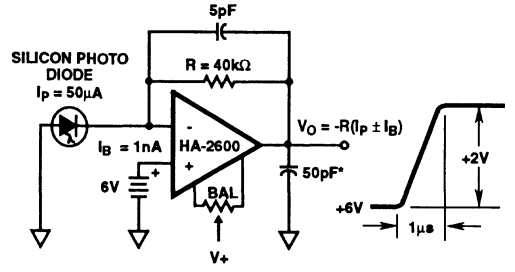


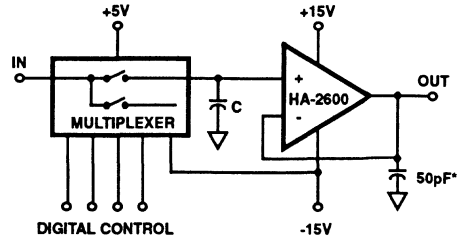
FIGURE 14. NOISE DENSITY vs FREQUENCY

Typical Applications



FEATURES:
1. Constant cell voltage
2. Minimum bias current error

FIGURE 15. PHOTO CURRENT TO VOLTAGE CONVERTER

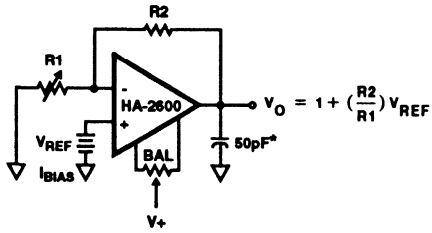


DRIFT RATE = $\frac{I_{BIAS}}{C}$

If C = 1000pF
Then DRIFT = 0.01V/µs Max

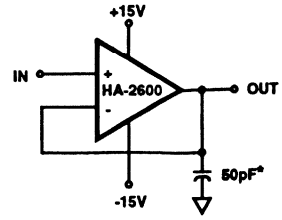
FIGURE 16. SAMPLE AND HOLD

Typical Applications (Continued)



FEATURES:
1. Minimum bias current in reference cell
2. Short Circuit Protection

FIGURE 17. REFERENCE VOLTAGE AMPLIFIER



$Z_{IN} = 10^{12}\Omega$ Min.
$Z_{OUT} = 0.01\Omega$ Max. B.W. = 12MHz. Typ.
Slew Rate = 4V/µs Min. Output Swing = ±10V Min. to 50kHz

FIGURE 18. VOLTAGE FOLLOWER

* A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

HARRIS SEMICONDUCTOR

HA-2620, HA-2622 HA-2625

Very Wideband, Uncompensated Operational Amplifiers

March 1993

Features

- Gain Bandwidth Product ($A_V \geq 5$) 100MHz
- High Input Impedance 500MΩ
- Low Input Bias Current 1nA
- Low Input Offset Current 1nA
- Low Input Offset Voltage 0.5mV
- High Gain 150kV/V
- High Slew Rate 35V/μs
- Output Short Circuit Protection

Applications

- Video and R.F. Amplifier
- Pulse Amplifier
- Audio Amplifiers and Filters
- High-Q Active Filters
- High Speed Comparators
- Low Distortion Oscillator

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-2620-2	-55°C to +125°C	8 Pin Can
HA2-2622-2	-55°C to +125°C	8 Pin Can
HA2-2625-5	0°C to +75°C	8 Pin Can
HA3-2625-5	0°C to +75°C	8 Lead Plastic DIP
HA4P2625-5	0°C to +75°C	20 Lead PLCC
HA7-2620-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-2622-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-2625-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P2625-5	0°C to +75°C	8 Lead SOIC
HA9P2625-9	-40°C to +85°C	8 Lead SOIC

Description

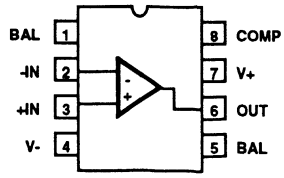
HA-2620/2622/2625 are bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. The 100MHz gain bandwidth product (HA-2620/2622/2625 are stable for closed loop gains greater than 5), 35V/μs slew rate and 150kV/V open loop gain enables HA-2620/2622/2625 to perform high gain amplification of very fast, wideband signals. These dynamic characteristics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor connected from the Comp pin to GND.

In addition to its application in pulse and video amplifier designs, HA-2620/2622/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators. For more information, please refer to Application Notes 509, 519 and 546.

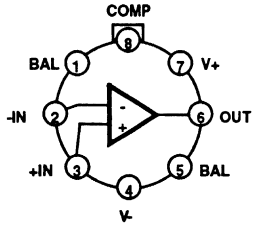
The HA-2620 and HA-2622 are both offered as /883 Military Grade with the HA-2622 also available in LCC packages. MIL-STD-883 data sheets are available upon request.

Pinouts

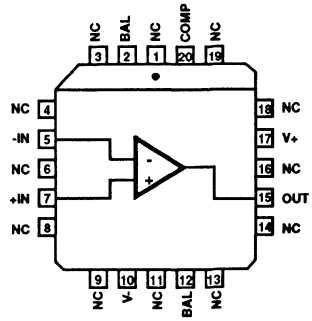
HA-2620/22 (CDIP)
HA-2526 (CDIP, PDIP, SOIC)
TOP VIEW



HA-2620, HA-2622, HA-2625
(CAN)
TOP VIEW



HA-2625, (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2903.1**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 45V
Differential Input Voltage 12.0V
Peak Output Current ..... Full Short Circuit Protection
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Temperature Ranges

Operating Temperature Range
HA-2620/HA-2622-2 ..... $-55°C \le T_A \le +125°C$
HA-2625-5 ..... $0°C \le T_A \le +75°C$
HA-2625-9 ..... $-40°C \le T_A \le +80°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_S = \pm 15VDC$, Unless Otherwise Specified.

PARAMETER	TEMP	HA-2620-2			HA-2622-2			HA-2625-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage (Note 1)	+25°C	-	0.5	4	-	3	5	-	3	5	mV
	Full	-	2	6	-	-	7	-	-	7	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-	-	5	-	µV/°C
Bias Current	+25°C	-	1	15	-	5	25	-	5	25	nA
	Full	-	10	35	-	-	60	-	-	40	nA
Offset Current	+25°C		1	15	-	5	25	-	5	25	nA
	Full	-	5	35	-	-	60	-	-	40	nA
Differential Input Resistance (Note 11)	+25°C	65	500	-	40	300	-	40	300	-	MΩ
Input Noise Voltage Density f = 1kHz	+25°C	-	11	-	-	11	-	-	11	-	$nV/\sqrt{Hz}$
Input Noise Current Density f = 1kHz	+25°C	-	0.16	-	-	0.16	-	-	0.16	-	$pA/\sqrt{Hz}$
Common Mode Range	Full	±11	±12	-	±11	±12	-	±11	±12	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 2, 3)	+25°C	100	150	-	80	150	-	80	150	-	kV/V
	Full	70	-	-	60	-	-	70	-	-	kV/V
Common Mode Rejection Ratio (Note 4)	Full	80	100	-	74	100	-	74	100	-	dB
Minimum Stable Gain	+25°C	5	-	-	5	-	-	5	-	-	V/V
Gain Bandwidth Product (Notes 2, 5, 6)	+25°C	-	100	-	-	100	-	-	100	-	MHz

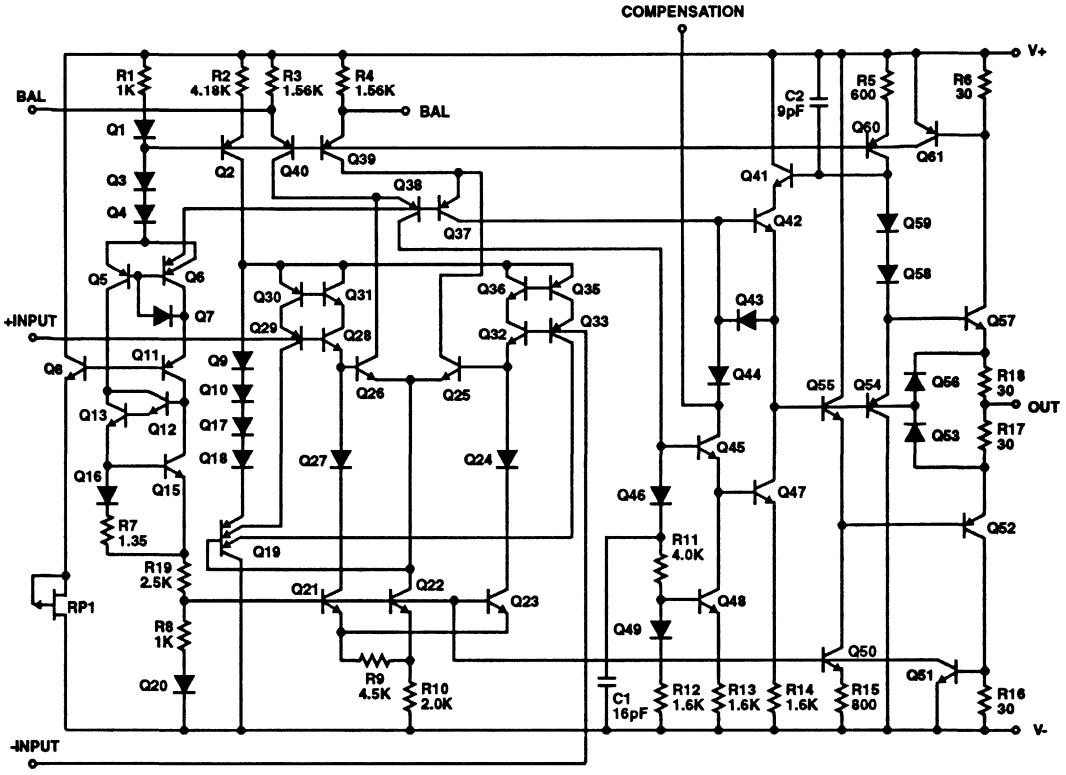
Electrical Specifications V_S = ±15VDC, Unless Otherwise Specified.

PARAMETER	TEMP	HA-2620-2			HA-2622-2			HA-2625-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10	±12	-	±10	±12	-	±10	±12	-	V
Output Current (Note 3)	+25°C	±15	±22	-	±10	±18	-	±10	±18	-	mA
Full Power Bandwidth (Notes 2, 3, 7, 12)	+25°C	400	600	-	320	600	-	320	600	-	kHz
TRANSIENT RESPONSE (Note 8)											
Rise Time (Notes 2, 7, 8)	+25°C	-	17	45	-	17	45	-	17	45	ns
Slew Rate (Notes 2, 7, 8, 10)	+25°C	±25	±35	-	±20	±35	-	±20	±35	-	V/µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C	-	3	3.7	-	3	4	-	3	4	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90	-	74	90	-	74	90	-	dB

NOTES:

1. Offset may be externally adjusted to zero.
2. $R_L = 2k\Omega$.
3. $V_{OUT} = \pm 10.0V$.
4. $V_{CM} = \pm 10V$.
5. $V_{OUT} < 90mV$.
6. 40dB Gain.
7. See Transient Response Test Circuits & Waveforms.
8. $A_V = 5$ (The HA-2620 family is not stable at unity gain without external compensation).
9. $\Delta V_S = \pm 5V$.
10. $V_{OUT} = \pm 5V$.
11. This parameter value guaranteed by design calculations.
12. Full Power Bandwidth guaranteed by slew rate measurement: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
13. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

Schematic Diagram



Die Characteristics

Transistor Count 140

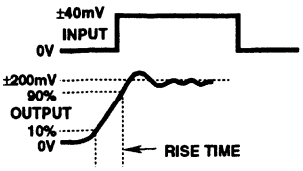
Die Dimensions ..... 73 x 52 x 19 mils

Substrate Potential ..... Unbiased

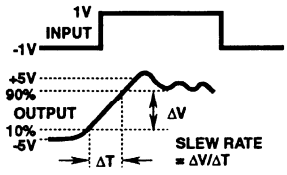
Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Metal Can	117	36
Plastic DIP	96	34
Ceramic DIP	115	36
SOIC	157	43
PLCC	74	33

Test Circuits

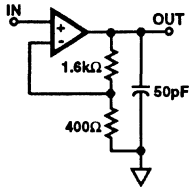
TRANSIENT RESPONSE



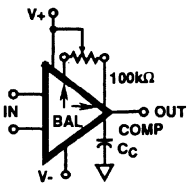
SLEW RATE



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK-UP



NOTE: Measured on both positive and negative transistions from 0V to +200mV and 0V to -200mV at output.

Tested Offset Adjustment is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is ±10mV with R_T = 100kΩ.

Typical Performance Curves V_S = ±15VDC, T_A = +25°C, Unless Otherwise Specified.

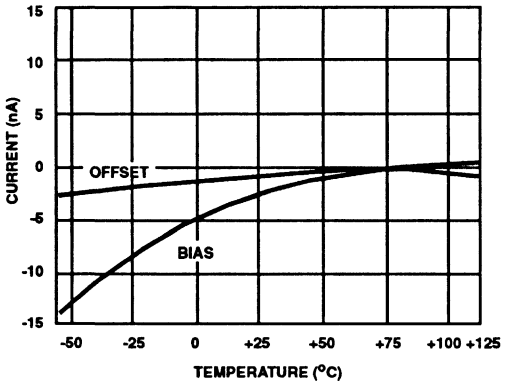


FIGURE 1. INPUT BIAS CURRENT AND OFFSET CURRENT vs TEMPERATURE

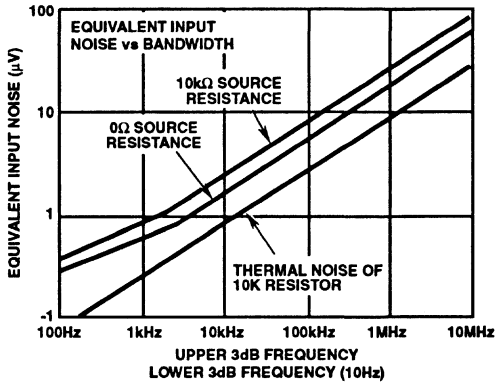


FIGURE 2. BROADBAND NOISE CHARACTERISTICS

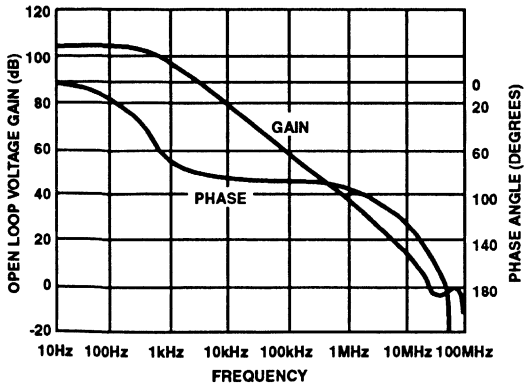


FIGURE 3. OPEN LOOP FREQUENCY AND PHASE RESPONSE

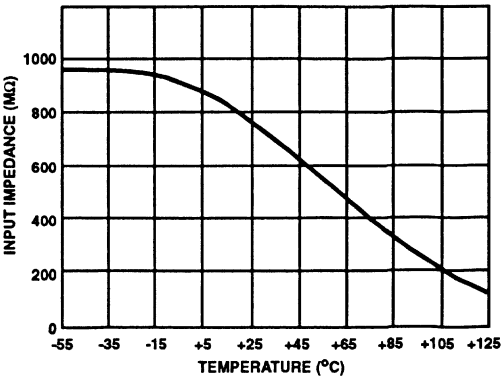


FIGURE 4. INPUT IMPEDANCE vs TEMPERATURE, 100Hz

Typical Performance Curves $V_S = \pm15VDC$, $T_A = +25°C$, Unless Otherwise Specified. (Continued)

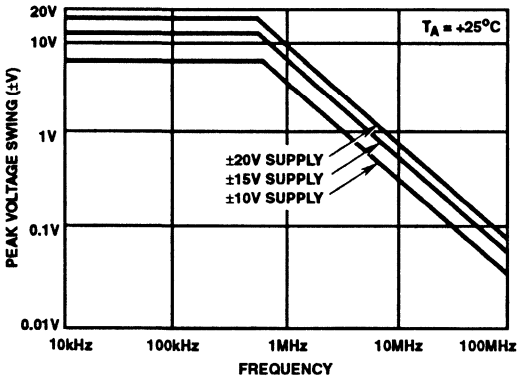


FIGURE 5. OUTPUT VOLTAGE SWING vs FREQUENCY

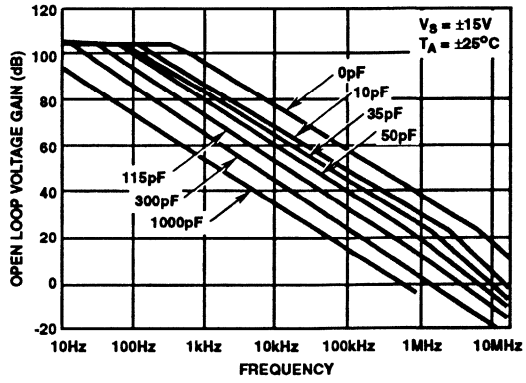


FIGURE 6. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMP. PIN TO GND

NOTE: External Compensation is required for closed loop gain < 5. If external compensation is used, also connect 100pF capacitor from output to ground.

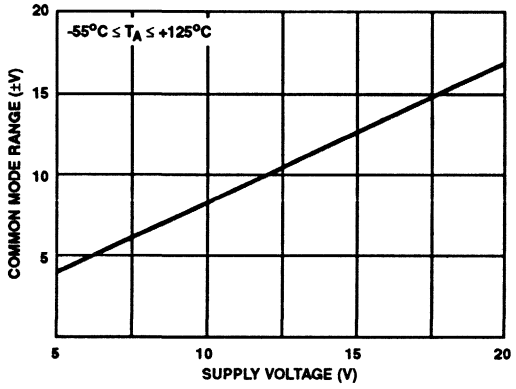


FIGURE 7. COMMON MODE VOLTAGE RANGE vs SUPPLY VOLTAGE

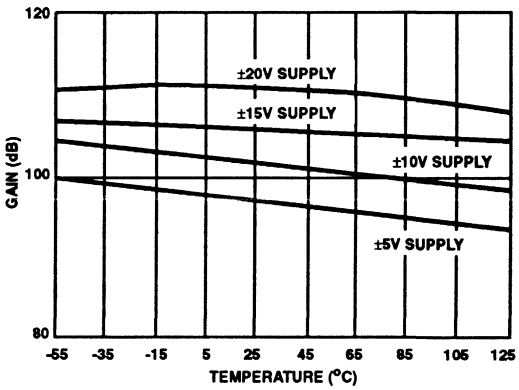


FIGURE 8. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

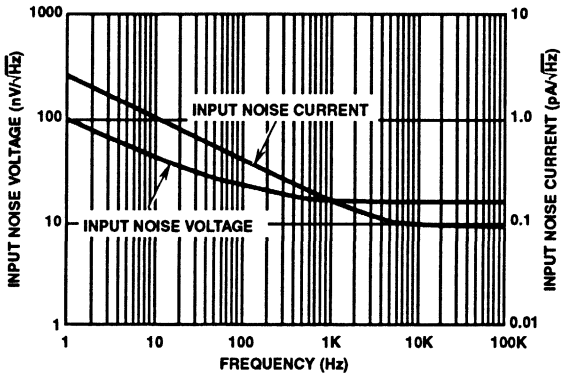


FIGURE 9. NOISE DENSITY vs FREQUENCY

Typical Applications

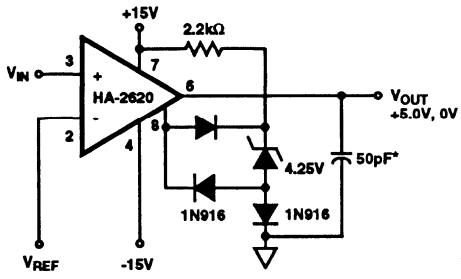


FIGURE 10. HIGH IMPEDANCE COMPARATOR

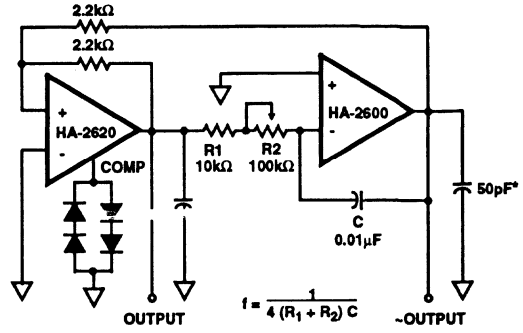
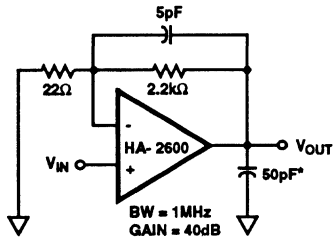


FIGURE 11. FUNCTION GENERATOR



*A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent possible high frequency oscillations.

FIGURE 12. VIDEO AMPLIFIER

HA-2640, HA-2645

March 1993

High Voltage Operational Amplifiers

Features

- Output Voltage Swing ..... ±35V
- Supply Voltage ..... ±10V to ±40V
- Offset Current 5nA
- Bandwidth 4MHz
- Slew Rate 5V/μs
- Common Mode Input Voltage Range ..... ±35V
- Output Overload Protection

Applications

- Industrial Control Systems
- Power Supplies
- High Voltage Regulators
- Resolver Excitation
- Signal Conditioning

Description

HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

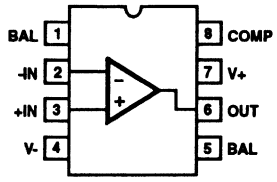
These amplifiers deliver ±35V common mode input voltage range, ±35V output voltage swing, and up to ±40V supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and 5V/μs slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excellent components for resolver excitation designs.

Ordering Information

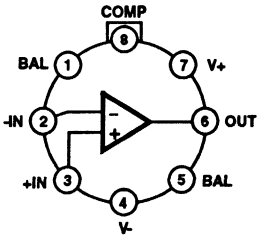
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-2640-2	-55°C to +125°C	8 Pin TO-99 Can
HA2-2645-5	0°C to +75°C	8 Pin TO-99 Can
HA7-2640-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-2645-5	0°C to +75°C	8 Lead Ceramic DIP

Pinouts

HA-2640/2645
(CDIP)
TOP VIEW



HA-2640/2645
(TO-99 CAN)
TOP VIEW



(TO-99 CASE VOLTAGE = V-)

File Number 2904.1

Absolute Maximum Ratings (Note 12)

Voltage Between V+ and V- Terminals 100V
Differential Input Voltage Range 37V
Output Current ..... Full Short Circuit Protection
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-2640-2 ..... $-55°C \le T_A \le +125°C$
HA-2645-5 ..... $0°C \le T_A \le +75°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	114	34
Can	108	33

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V_{SUPPLY} = \pm 40V$, $R_L = 5k\Omega$, Unless Otherwise Specified

PARAMETER	TEMP	HA-2640-2 -55°C to +125°C			HA-2645-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	2	4	-	2	6	mV
	Full		-	6	-	-	7	mV
Average Offset Voltage Drift	Full	-	15	-	-	15	-	µV/°C
Bias Current	+25°C	-	10	25	-	12	30	nA
	Full	-	-	50	-	-	50	nA
Offset Current	+25°C	-	5	12	-	15	30	nA
	Full	-	-	35	-	-	50	nA
Input Resistance (Note 10)	+25°C	50	250	-	40	200	-	MΩ
Common Mode Range	Full	±35	-	-	±35	-	-	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 8)	+25°C	100	200	-	100	200	-	kV/V
	Full	75	-	-	75	-	-	kV/V
Common Mode Rejection Ratio (Note 1)	Full	80	100	-	74	100	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	V/V
Unity Gain Bandwidth (Note 2)	+25°C	-	4	-	-	4	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±35	-	-	±35	-	-	V
Output Current (Note 9)	+25°C	±12	±15	-	±10	±12	-	mA
Output Resistance	+25°C	-	500	-	-	500	-	Ω
Full Power Bandwidth (Notes 3 & 11)	+25°C	-	23	-	-	23	-	kHz
TRANSIENT RESPONSE (Note 7)								
Rise Time (Notes 4 & 6)	+25°C	-	60	135	-	60	135	ns
Overshoot (Notes 4 & 6)	+25°C	-	15	30		15	40	%
Slew Rate (Note 6)	+25°C	±3	±5	-	±2.5	±5	-	V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	3.2	3.8	-	3.2	4.5	mA

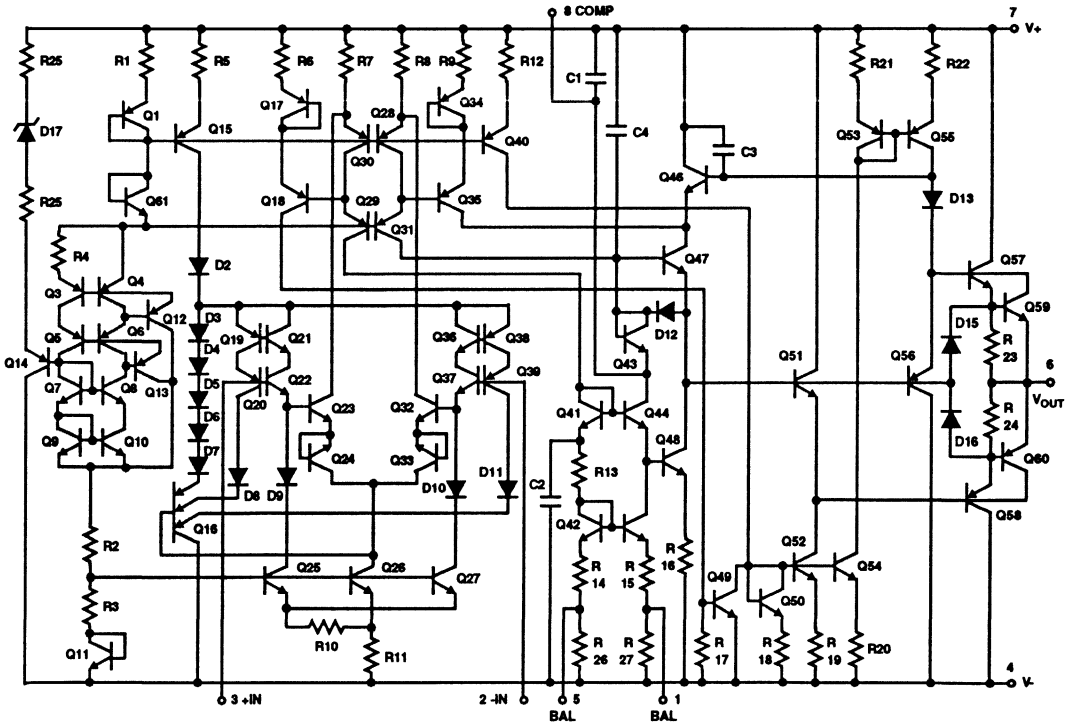
Electrical Specifications V_{SUPPLY} = ±40V, R_L = 5kΩ, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	HA-2640-2 -55°C to +125°C			HA-2645-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage Range	Full	±10	-	±40	±10	-	±40	V
Power Supply Rejection Ratio (Note 5)	Full	80	90	-	74	90	-	dB

NOTES:

1. V_{CM} = ±20V
2. V_{OUT} = 90mV
3. V_{OUT} = ±35V
4. V_{OUT} = ±200mV
5. V_S = ±10V to ±40V
6. A_V = +1
7. C_L = 50pF, R_L = 5kΩ
8. V_{OUT} = ±30V
9. R_L = 1kΩ
10. This parameter based upon design calculations.
11. Full Power Bandwidth guaranteed based upon slew rate measurement: FPBW = S.R./2πV_{PEAK}; V_{PEAK} = 35V.
12. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

Schematic Diagram



Test Circuits and Switching Waveform

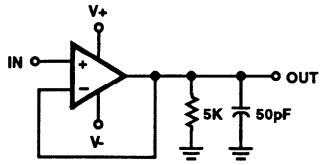
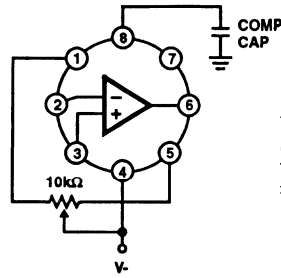
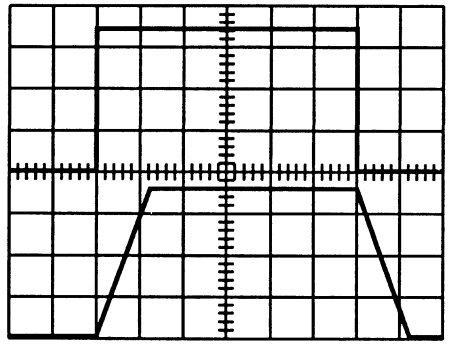


FIGURE 1. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



Tested offset adjustment range is $|V_{OS}$ +1mV| minimum referred to output. Typical range is ±20mV with R_T = 10kΩ.

FIGURE 2. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK UP



R_L = 5K, C_L = 50pF, T_A = +25°C, V_S = ±40V
Vertical = 10V/Div.
Horizontal = 5µs/Div.

FIGURE 3. VOLTAGE FOLLOWER PULSE RESPONSE

Typical Performance Curves V+ = V- = 40VDC, T_A = +25°C, Unless Otherwise Specified

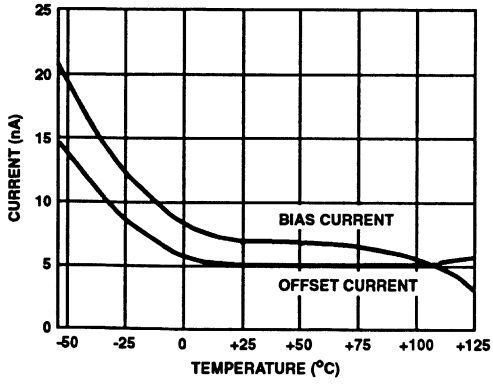


FIGURE 4. INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

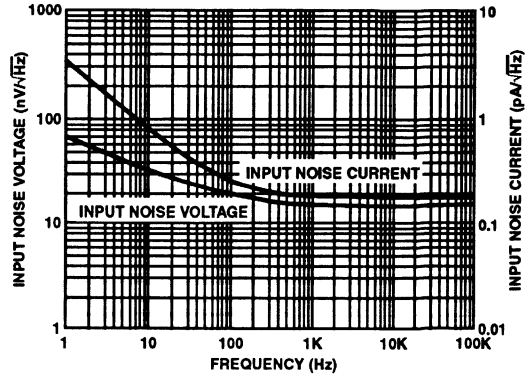


FIGURE 5. INPUT NOISE CHARACTERISTICS

Typical Performance Curves V+ = V- = 40VDC, T_A = +25°C, Unless Otherwise Specified (Continued)

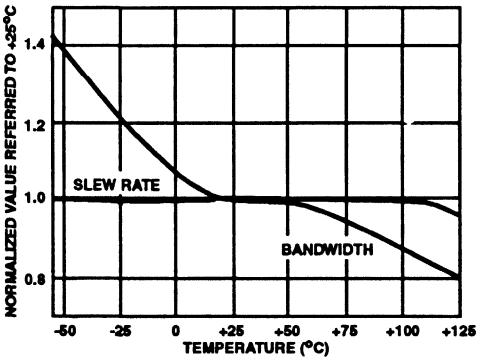


FIGURE 6. NORMALIZED AC PARAMETERS vs TEMPERATURE

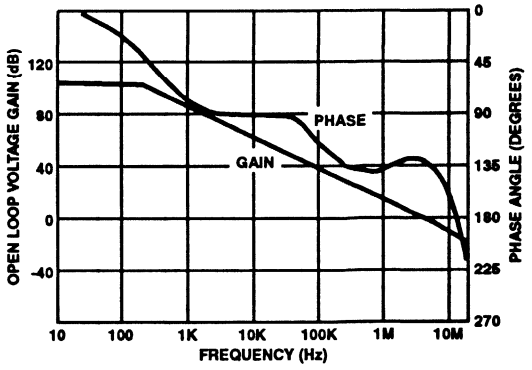


FIGURE 7. OPEN LOOP FREQUENCY AND PHASE RESPONSE

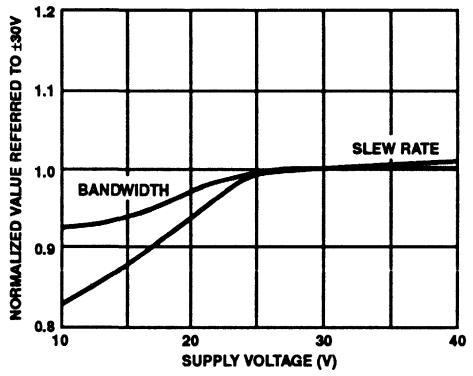


FIGURE 8. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C

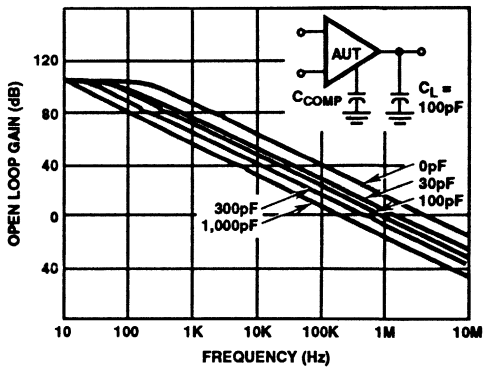


FIGURE 9. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

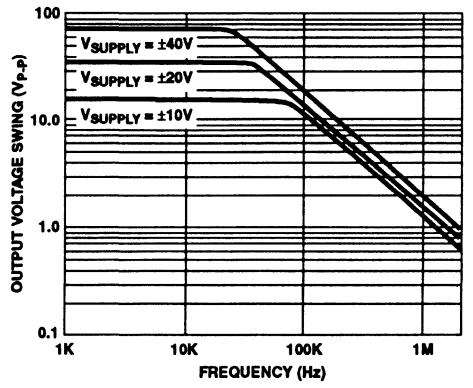


FIGURE 10. OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C

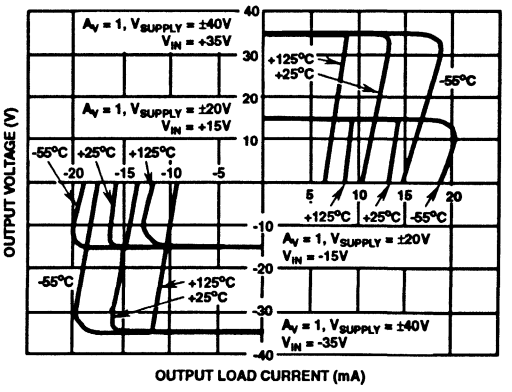


FIGURE 11. OUTPUT CURRENT CHARACTERISTIC

Typical Performance Curves $V+ = V- = 40VDC$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

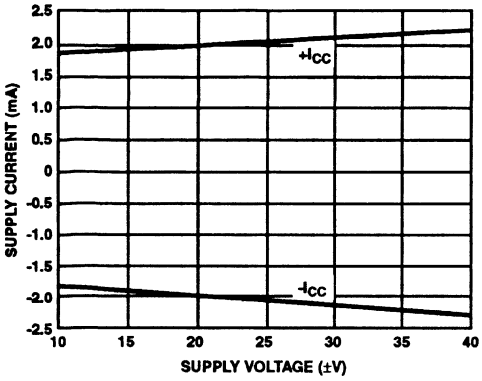


FIGURE 12. SUPPLY CURRENT vs SUPPLY VOLTAGE

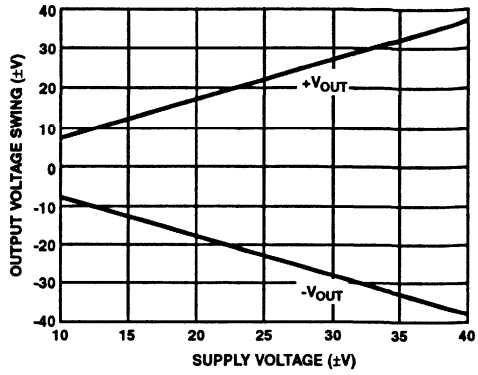


FIGURE 13. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

HARRIS SEMICONDUCTOR

HA-2705

Low Power, High Performance Operational Amplifier

March 1993

Features

- High Slew Rate 20V/μs
- Low Power Dissipation ..... 2.25mW at ±15.0V
- High Open Loop Gain ..... 300kV/V (R_L = 2kΩ)
- Low Input Bias Current 5nA
- Low Offset Voltage 1mV
- High CMRR 106dB
- Wide Power Supply Range ..... ±5.5V to ±20.0V
- Fully Internally Compensated
- Output Short Circuit Protected
- Offset Null Capability

Applications

- Instrumentation
- Battery Powered Circuits
- Portable Instruments
- Remote Data Logging

Description

The HA-2705 is a general purpose amplifier which operates at very low power levels without compromising large signal response characteristics or output drive capability. Advanced circuit design techniques and the use of vertical NPN and PNP transistors make possible the attainment of very high gain with a single stage of voltage amplification. This ensures closed loop stability even in the critical unity gain follower mode, without the use of external compensation components.

The circuit is intended for use in applications that require fast large signal response with low power dissipation and for instrumentation applications in which low offset voltage, low bias current drift, large voltage gain and high common mode rejection are necessary. Full output short circuit protection and the large differential input breakdown enable the device to withstand a variety of fault conditions.

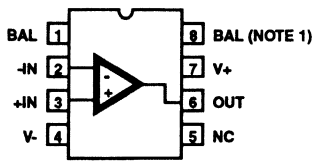
For military grade product, please refer to the HA-2700/883 datasheet.

Ordering Information

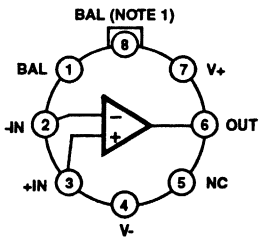
PART NUMBER	TEMPERATURE RANGE	PRODUCT DESCRIPTION
HA3-2705-5	0°C to +70°C	8 Lead Plastic DIP
HA9P2705-5	0°C to +70°C	8 Lead SOIC
HA2-2705-5	0°C to +70°C	8 Pin TO-99 Metal Can

Pinouts

HA-2705
(PDIP, SOIC)
TOP VIEW



HA-2705
(TO-99 METAL CAN)
TOP VIEW



File Number 3391

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44.0V
Differential Input Voltage 18V
Input Voltage . . . . . V+ to V-
Junction Temperature (Hermetic) . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C

Operating Conditions

HA-2705-5 . . . . . $0°C \le T_A \le +75°C$
Storage Temperature Range . . . . . $-65°C \le T_A \le +150°C$

Thermal Resistance (°C/W)	θ_{JA}	θ_{JC}
Plastic DIP Package	94	32
SOIC Package	157	43
TO-99 Metal Can	114	35

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = +15V, V- = -15V, R_L = 5kΩ Unless Otherwise Specified.

PARAMETER	TEMP	HA-2705-5 MIN	HA-2705-5 TYP	HA-2705-5 MAX	UNITS
INPUT CHARACTERISTICS					
Offset Voltage (Note 1)	+25°C	-	1.0	5.0	mV
	Full	-	-	7.0	mV
Bias Current	+25°C	-	5.0	40.0	nA
	Full	-	-	70.0	nA
Offset Current	+25°C	-	2.5	15.0	nA
	Full	-	-	40.0	nA
Common Mode Range	Full	±11.0	-	-	V
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Notes 2 and 3)	+25°C	200	300	-	kV/V
	Full	100	-	-	kV/V
Common Mode Rejection Ratio (Note 4)	Full	80	106	-	dB
Gain Bandwidth Product (Note 2)	+25°C	-	1.0	-	MHz
Minimum Stable Gain	Full	1	-	-	V/V
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 2)	+25°C	±12.0	±13.0	-	V
	Full	±11.0	-	-	V
Output Current (Note 3)	+25°C	-	10	-	mA
TRANSIENT RESPONSE CHARACTERISTICS					
Slew Rate (Notes 2 and 6)	+25°C	10	20	-	V/µs
POWER SUPPLY CHARACTERISTICS					
Supply Current	+25°C	-	75	150	µA
	Full	-	-	200	µA
Power Supply Rejection Ratio (Note 5)	Full	80	100	-	dB

NOTES:

1. Can be adjusted to zero with 1MΩ potentiometer between Pins 1 and 8 with the wiper to V+.
2. R_L = 2kΩ, C_L = 100pf
3. V_O = ±10.0V
4. V_{CM} = ±5.0V
5. V_S = ±10.0V to ±20.0V
6. A_V = 5

Die Characteristics

DIE DIMENSIONS:
70 x 60 x 19 ± 1mils

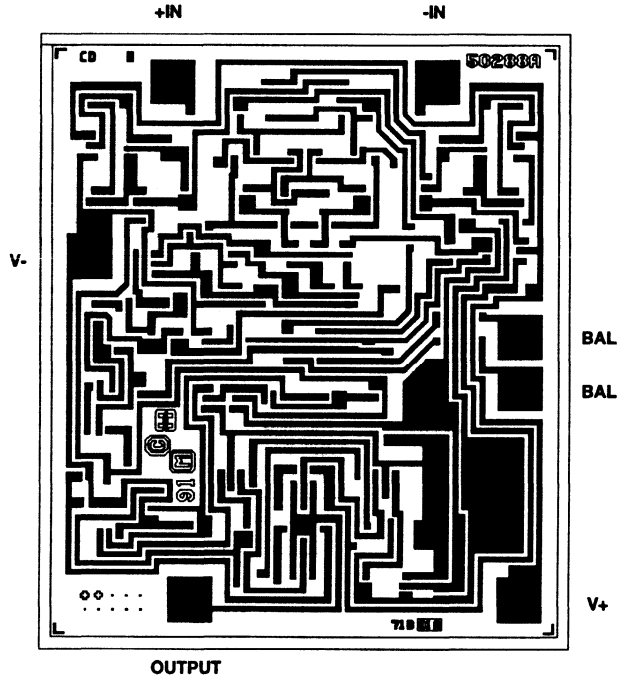
METALLIZATION:
Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos)
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 2kÅ

DIE ATTACH:
Material: Silver Epoxy - Plastic DIP and SOIC
Silver Epoxy - TO-99 Metal Can

Metallization Mask Layout

HA-2705



HARRIS SEMICONDUCTOR

HA-2839

Very High Slew Rate Wideband Operational Amplifier

March 1993

Features

- Low Supply Current 13mA
- Very High Slew Rate 625V/µs
- Open Loop Gain 25kV/V
- Wide Gain-Bandwidth ($A_V \geq 10$) 600MHz
- Full Power Bandwidth 10MHz
- Low Offset Voltage 0.6mV
- Differential Gain/Phase . . . . . 0.03%/0.03°
- Enhanced Replacement for EL2039

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

Description

The HA-2839 is a wideband, very high slew rate, operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction, coupled with dielectric isolation, delivers outstanding performance in circuits with a closed loop gain of 10 or greater.

A 625V/µs slew rate and a 600MHz gain bandwidth product ensure high performance in video and RF amplifier designs. Differential gain and phase are a low 0.03% and 0.03° respectively, making the HA-2839 ideal for video applications. A full ±10V output swing, high open loop gain, and outstanding AC parameters, make the HA-2839 an excellent choice for high speed Data Acquisition Systems.

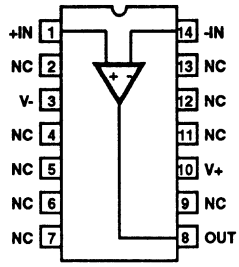
The HA-2839 is available in commercial and industrial temperature ranges, and a choice of packages. For military grade product, refer to the HA-2839/883 data sheet.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-2839-5	0°C to +75°C	14 Lead Ceramic DIP
HA3-2839-5	0°C to +75°C	14 Lead Plastic DIP
HA1-2839-9	-40°C to +85°C	14 Lead Ceramic DIP
HA3-2839-9	-40°C to +85°C	14 Lead Plastic DIP

Pinout

HA-2839
(CDIP, PDIP)
TOP VIEW



NOTE: (NC) No Connection pins may be tied to a ground plane for better isolation and heat dissipation.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2841.1**

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Output Current 50mA
Internal Quiescent Power Dissipation (Note 2)
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-2839-5 ..... $0°C \le T_A \le +75°C$
HA-2839-9 ..... $-40°C \le T_A \le +85°C$
Recommended Supply Voltage Range ..... ±7V to ±15V
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP Package	71	14
Plastic Dip Package	107	38

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \le 10pF$, Unless Otherwise Specified.

PARAMETER	TEMPERATURE	HA-2839-5, -9 MIN	HA-2839-5, -9 TYP	HA-2839-5, -9 MAX	UNITS
INPUT CHARACTERISTICS					
Offset Voltage (Note 13)	+25°C	-	0.6	2	mV
	Full	-	2	6	mV
Average Offset Voltage Drift	Full	-	20	-	µV/°C
Bias Current (Note 13)	+25°C	-	5	14.5	µA
	Full	-	8	20	µA
Offset Current	+25°C	-	1	4	µA
	Full	-	-	8	µA
Input Resistance	+25°C	-	10	-	kΩ
Input Capacitance	+25°C	-	1	-	pF
Common Mode Range	Full	±10	-	-	V
Input Noise Voltage (f = 1kHz, $R_{SOURCE} = 0\Omega$, Note 13)	+25°C	-	6	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz, $R_{SOURCE} = 10k\Omega$, Note 13)	+25°C	-	6	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Note 3)	+25°C	20	25	-	kV/V
	Full	15	20	-	kV/V
Common-Mode Rejection Ratio (Notes 4, 13)	Full	75	80	-	dB
Minimum Stable Gain	+25°C	10	-	-	V/V
Gain Bandwidth Product (Notes 5, 12, 13)	+25°C	-	600	-	MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Notes 3, 13)	Full	±10	-	-	V
Output Current (Notes 3, 13)	Full	±10	±20	-	mA
Output Resistance	+25°C	-	30	-	Ω
Full Power Bandwidth (Notes 3, 7)	+25°C	8.7	10	-	MHz
Differential Gain (Notes 6, 11)	+25°C	-	0.03	-	%
Differential Phase (Notes 6, 11)	+25°C	-	0.03	-	Degrees
Harmonic Distortion (Notes 6, 13, 14)	+25°C	-	-79	-	dBc

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified. **(Continued)**

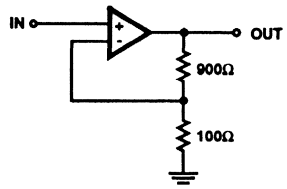
PARAMETER	TEMPERATURE	HA-2839-5, -9			UNITS
		MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 8)					
Rise Time	+25°C	-	4	-	ns
Overshoot	+25°C	-	20	-	%
Slew Rate (Notes 3, 10, 13)	+25°C	550	625	-	V/µs
Settling Time: 10V Step to 0.1%	+25°C	-	180	-	ns
POWER REQUIREMENTS					
Supply Current (Note 13)	Full	-	13	15	mA
Power Supply Rejection Ratio (Notes 9, 13)	Full	75	90	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C for ceramic packages and below +150°C for plastic packages.
3. $R_L = 1k\Omega$, $V_O = \pm10V$, 0V to $\pm10V$ for slew rate.
4. $V_{CM} = \pm10V$.
5. $V_O = 90mV$.
6. $A_V = +10$.
7. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $(V_{PEAK} = 10V)$.
8. Refer to Test Circuit section of data sheet.
9. $V_{SUPPLY} = \pm10VDC$ to $\pm20VDC$.
10. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
11. Differential gain and phase are measured with a VM700A video tester, using a NTC-7 composite VITS.
12. $A_V = +100$.
13. See "Typical Performance Curves" for more information.
14. $V_O = 2V_{P-P}$, f = 1MHz.

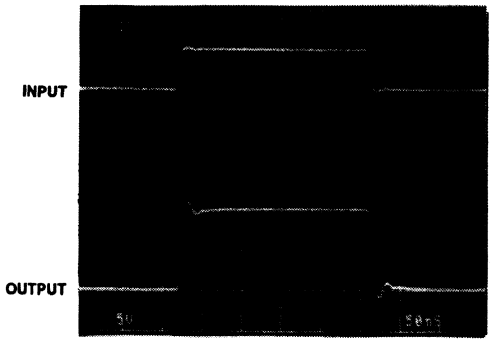
Test Circuit

TEST CIRCUIT

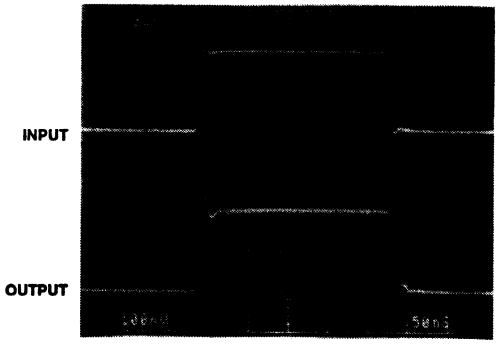


NOTE:
$V_S = \pm 15V$
$A_V = +10$
$C_L < 10pF$

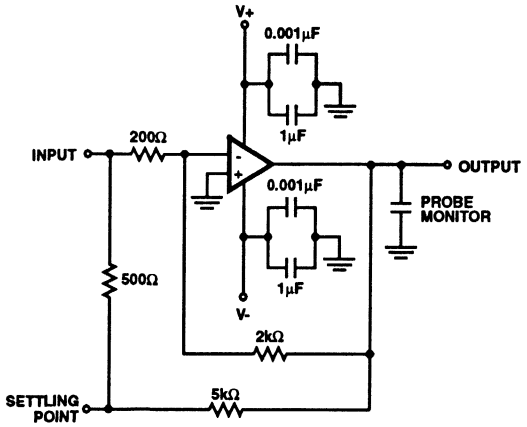
LARGE SIGNAL RESPONSE
Input = 1V/Div.
Output = 5V/Div.
50ns/Div.



SMALL SIGNAL RESPONSE
Input = 10mV/Div.
Output = 100mV/Div.
50ns/Div.



SETTLING TIME TEST CIRCUIT



- $A_V = -10$
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- SETTLING POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

Die Characteristics

DIE DIMENSIONS:
65 x 52 x 19 ± 1mils
(1650 x 1310 x 483µm)

METALLIZATION:
Type: Aluminum, 1% Copper
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride thickness: 3.5kÅ ± 1kÅ

DIE ATTACH:
Material: Epoxy-Plastic DIP
Gold Eutectic-Ceramic DIP

WORST CASE CURRENT DENSITY:
1.3×10^5 A/cm^2 at 3.4mA

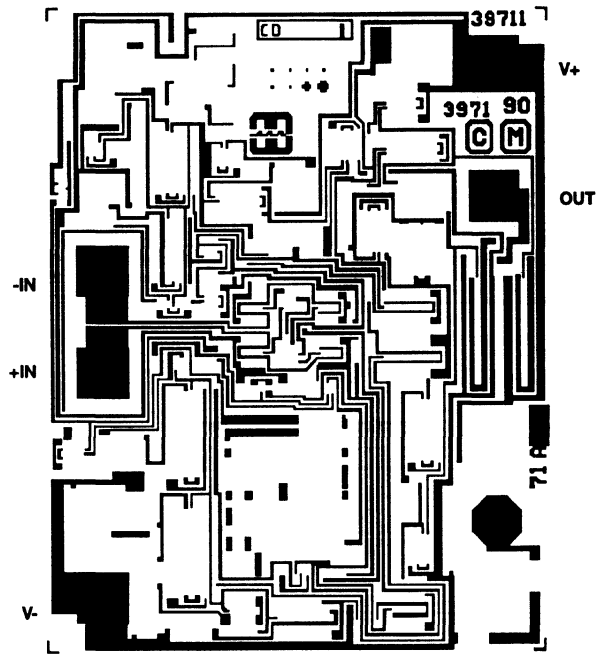
SUBSTRATE POTENTIAL (POWERED UP): V-

TRANSISTOR COUNT: 34

PROCESS: High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2839



Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified

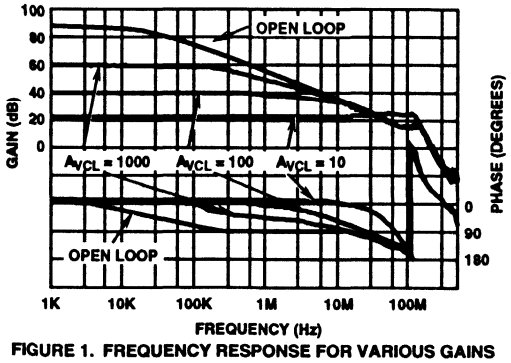


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS GAINS

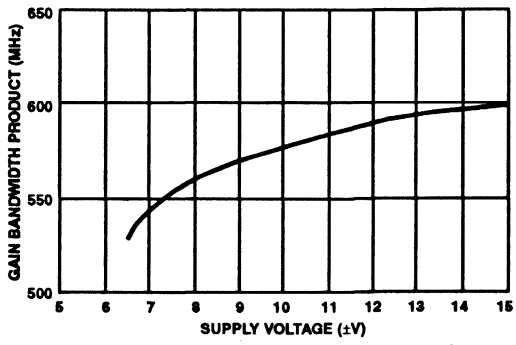


FIGURE 2. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

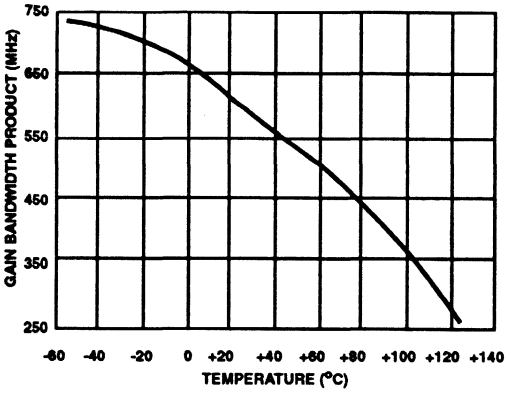


FIGURE 3. GAIN BANDWIDTH PRODUCT vs TEMPERATURE

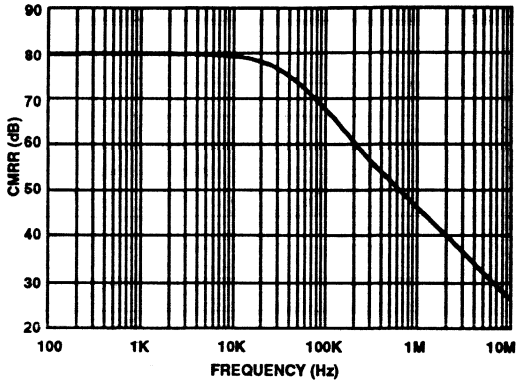


FIGURE 4. CMRR vs FREQUENCY

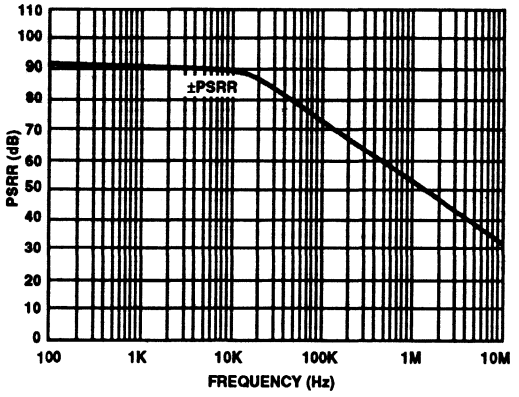


FIGURE 5. PSRR vs FREQUENCY

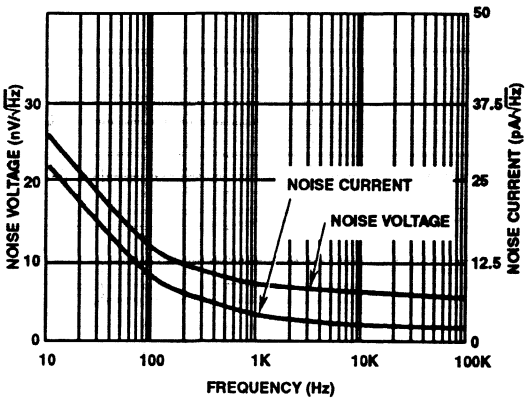


FIGURE 6. INPUT NOISE vs FREQUENCY

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified (Continued)

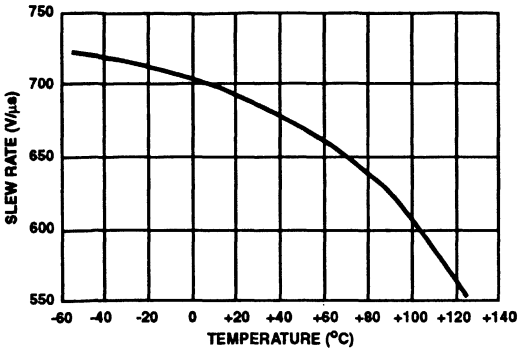


FIGURE 7. SLEW RATE vs TEMPERATURE

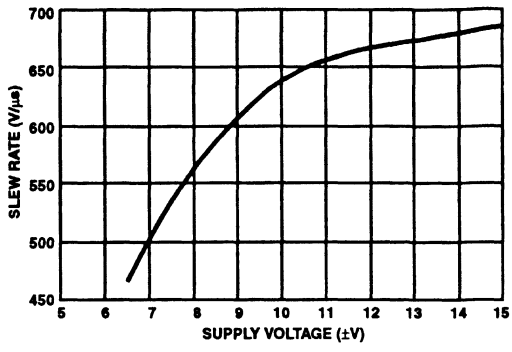


FIGURE 8. SLEW RATE vs SUPPLY VOLTAGE

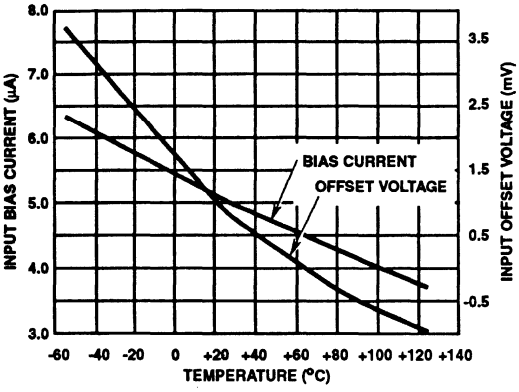


FIGURE 9. INPUT OFFSET VOLTAGE AND INPUT BIAS CURRENT vs TEMPERATURE

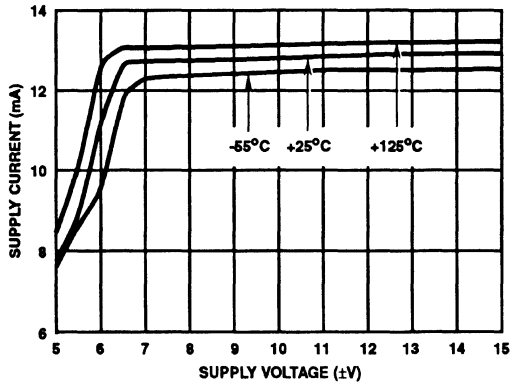


FIGURE 10. SUPPLY CURRENT vs SUPPLY VOLTAGE

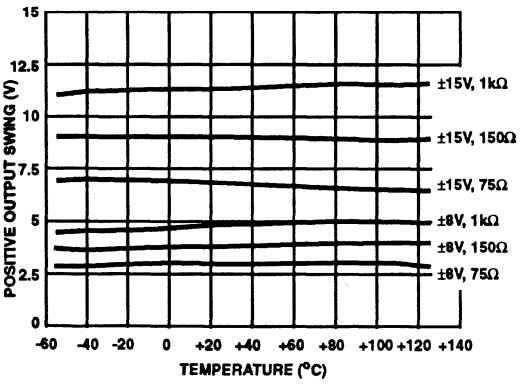


FIGURE 11. POSITIVE OUTPUT SWING vs TEMPERATURE

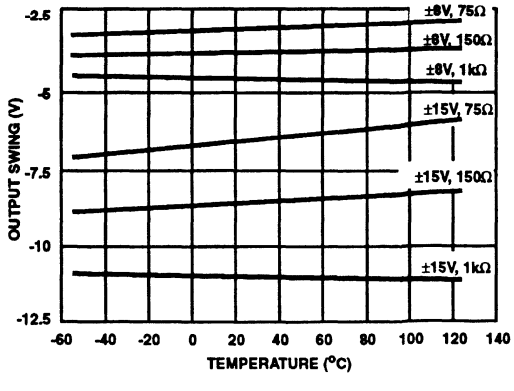


FIGURE 12. NEGATIVE OUTPUT SWING vs TEMPERATURE

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified (Continued)

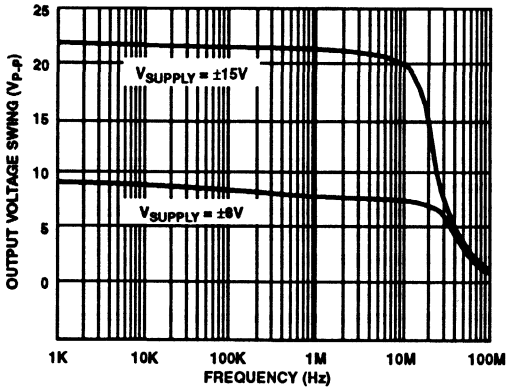


FIGURE 13. MAXIMUM UNDISTORTED OUTPUT SWING vs FREQUENCY

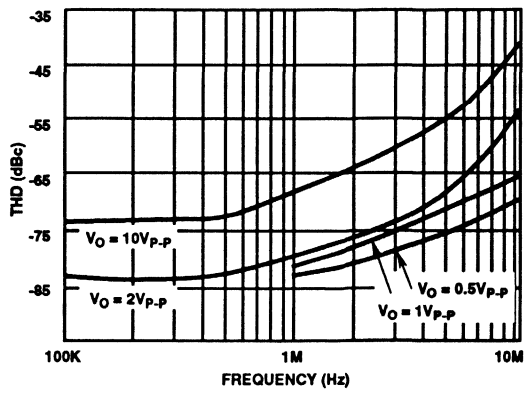


FIGURE 14. TOTAL HARMONIC DISTORTION vs FREQUENCY

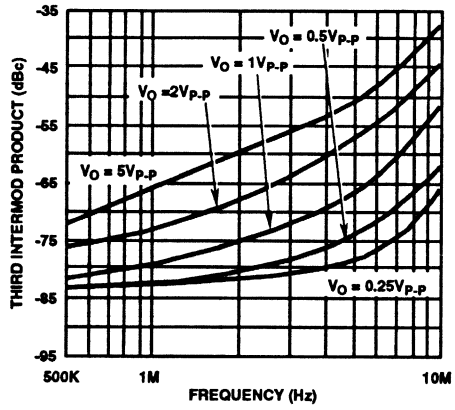


FIGURE 15. INTERMODULATION DISTORTION vs FREQUENCY TWO TONE

HARRIS SEMICONDUCTOR

HA-2840

Very High Slew Rate Wideband Operational Amplifier

March 1993

Features

- Low Supply Current 13mA
- Very High Slew Rate 625V/μs
- Open Loop Gain 25kV/V
- Wide Gain-Bandwidth ($A_V \geq 10$) 600MHz
- Full Power Bandwidth 10MHz
- Low Offset Voltage 0.6mV
- Differential Gain/Phase . . . . . 0.03%/0.03°
- Enhanced Replacement for EL2039

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

Description

The HA-2840 is a wideband, very high slew rate, operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction, coupled with dielectric isolation, delivers outstanding performance in circuits with a closed loop gain of 10 or greater.

A 625V/μs slew rate and a 600MHz gain bandwidth product ensure high performance in video and RF amplifier designs. Differential gain and phase are a low 0.03% and 0.03° respectively, making the HA-2840 ideal for video applications. A full ±10V output swing, high open loop gain, and outstanding AC parameters, make the HA-2840 an excellent choice for high speed Data Acquisition Systems.

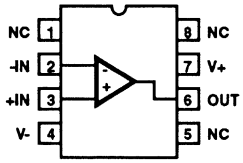
The HA-2840 is available in commercial and industrial temperature ranges, and a choice of packages. See the "Ordering Information" below for more information. For military grade product, refer to the HA-2840/883 data sheet.

Ordering Information

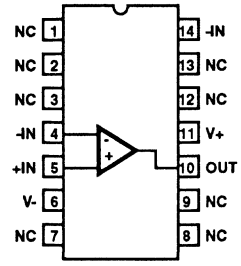
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-2840-5	0°C to +75°C	14 Lead Ceramic DIP
HA3B2840-5	0°C to +75°C	14 Lead Plastic DIP
HA7-2840-5	0°C to +75°C	8 Lead Ceramic DIP
HA3-2840-5	0°C to +75°C	8 Lead Plastic DIP
HA9P2840-5	0°C to +75°C	8 Lead SOIC
HA1-2840-9	-40°C to +85°C	14 Lead Ceramic DIP
HA3B2840-9	-40°C to +85°C	14 Lead Plastic DIP
HA7-2840-9	-40°C to +85°C	8 Lead Ceramic DIP
HA3-2840-9	-40°C to +85°C	8 Lead Plastic DIP

Pinouts

HA-2840
(CDIP, PDIP, SOIC)
TOP VIEW



HA-2840
(CDIP, PDIP)
TOP VIEW



NOTE: (NC) No Connection pins may be tied to a ground plane for better isolation and heat dissipation.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2842.1**

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Output Current 50mA
Internal Quiescent Power Dissipation (Note 2)
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Operating Temperature Range
HA-2840-5 . . . . . $0°C \le T_A \le +75°C$
HA-2840-9 . . . . . $-40°C \le T_A \le +85°C$
Recommended Supply Voltage Range . . . . . ±7V to ±15V
Storage Temperature Range . . . . . $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
14 Lead Ceramic DIP Package	71	14
14 Lead Plastic DIP Package	107	38
8 Lead Ceramic DIP Package	115	36
8 Lead Plastic DIP Package	96	34
8 Lead SOIC	157	43

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{SUPPLY} = ±15V, R_L = 1kΩ, $C_L \le$ 10pF, Unless Otherwise Specified.

PARAMETER	TEMPERATURE	HA-2840-5, -9 MIN	HA-2840-5, -9 TYP	HA-2840-5, -9 MAX	UNITS
INPUT CHARACTERISTICS					
Offset Voltage (Note 13)	+25°C	-	0.6	2	mV
	Full	-	2	6	mV
Average Offset Voltage Drift	Full	-	20	-	µV/°C
Bias Current (Note 13)	+25°C	-	5	14.5	µA
	Full	-	8	20	µA
Offset Current	+25°C	-	1	4	µA
	Full	-	-	8	µA
Input Resistance	+25°C	-	10	-	kΩ
Input Capacitance	+25°C	-	1	-	pF
Common Mode Range	Full	±10	-	-	V
Input Noise Voltage (f = 1kHz, R_{SOURCE} = 0Ω, Note 13)	+25°C	-	6	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz, R_{SOURCE} = 10kΩ, Note 13)	+25°C	-	6	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Note 3)	+25°C	20	25	-	kV/V
	Full	15	20	-	kV/V
Common-Mode Rejection Ratio (Notes 4, 13)	Full	75	80	-	dB
Minimum Stable Gain	+25°C	10	-	-	V/V
Gain Bandwidth Product (Notes 5, 12, 13)	+25°C	-	600	-	MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Notes 3, 13)	Full	±10	-	-	V
Output Current (Notes 3, 13)	Full	±10	±20	-	mA
Output Resistance	+25°C	-	30	-	Ω
Full Power Bandwidth (Notes 3, 7)	+25°C	8.7	10	-	MHz
Differential Gain (Notes 6, 11)	+25°C	-	0.03	-	%
Differential Phase (Notes 6, 11)	+25°C	-	0.03	-	Degrees
Harmonic Distortion (Notes 6, 13, 14)	+25°C	-	-79	-	dBc

Electrical Specifications V_{SUPPLY} = ±15V, R_L = 1kΩ, C_L ≤ 10pF, Unless Otherwise Specified. **(Continued)**

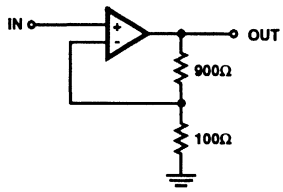
PARAMETER	TEMPERATURE	HA-2840-5, -9			UNITS
		MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 8)					
Rise Time	+25°C	-	4	-	ns
Overshoot	+25°C	-	20	-	%
Slew Rate (Notes 3, 10, 13)	+25°C	550	625	-	V/µs
Settling Time: 10V Step to 0.1%	+25°C	-	180	-	ns
POWER REQUIREMENTS					
Supply Current (Note 13)	Full	-	13	15	mA
Power Supply Rejection Ratio (Notes 9, 13)	Full	75	90	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C for ceramic packages and below +150°C for plastic packages.
3. R_L = 1kΩ, V_O = ±10V, 0V to ±10V for slew rate.
4. V_{CM} = ±10V.
5. V_O = 90mV.
6. A_V = +10.
7. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $(V_{PEAK} = 10V)$.
8. Refer to Test Circuit section of data sheet.
9. V_{SUPPLY} = ±10VDC to ±20VDC.
10. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
11. Differential gain and phase are measured with a VM700A video tester, using a NTC-7 composite VITS.
12. A_V = +100.
13. See "Typical Performance Curves" for more information.
14. $V_O = 2V_{P-P}$, f = 1MHz.

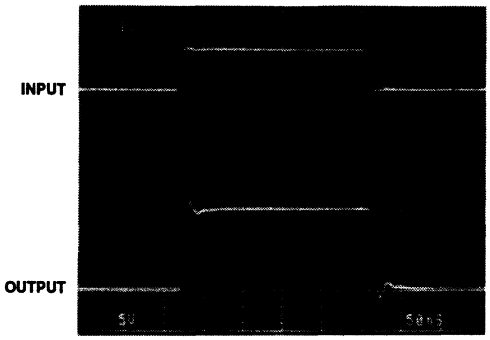
Test Circuit

TEST CIRCUIT

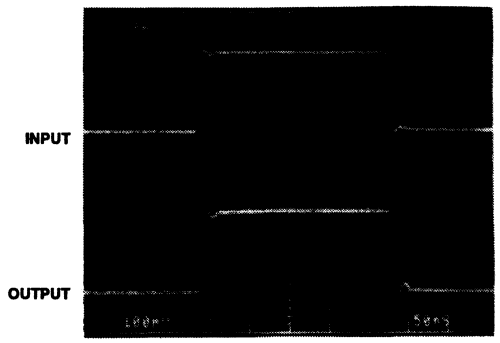


NOTE:
$V_S = \pm 15V$
$A_V = +10$
$C_L < 10pF$

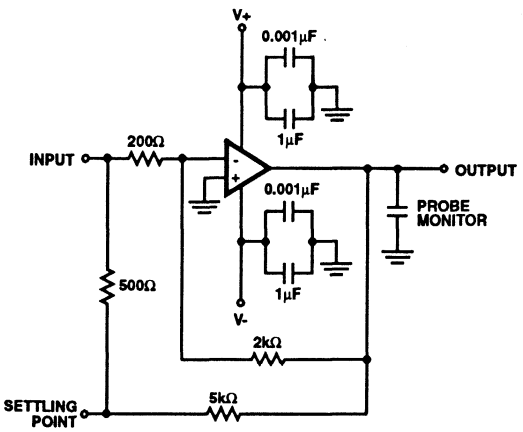
LARGE SIGNAL RESPONSE
Input = 1V/Div.
Output = 5V/Div.
50ns/Div.



SMALL SIGNAL RESPONSE
Input = 10mV/Div.
Output = 100mV/Div.
50ns/Div.



SETTLING TIME TEST CIRCUIT



- $A_V = -10$
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- SETTLING POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

Die Characteristics

DIE DIMENSIONS:
65 x 52 x 19 ± 1mils
(1650 x 1310 x 483µm)

METALLIZATION:
Type: Aluminum, 1% Copper
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride thickness: 3.5kÅ ± 1kÅ

DIE ATTACH:
Material: Epoxy-Plastic DIP
Gold Eutectic-Ceramic DIP

WORST CASE CURRENT DENSITY:
1.3×10^5 A/cm^2 at 3.4mA

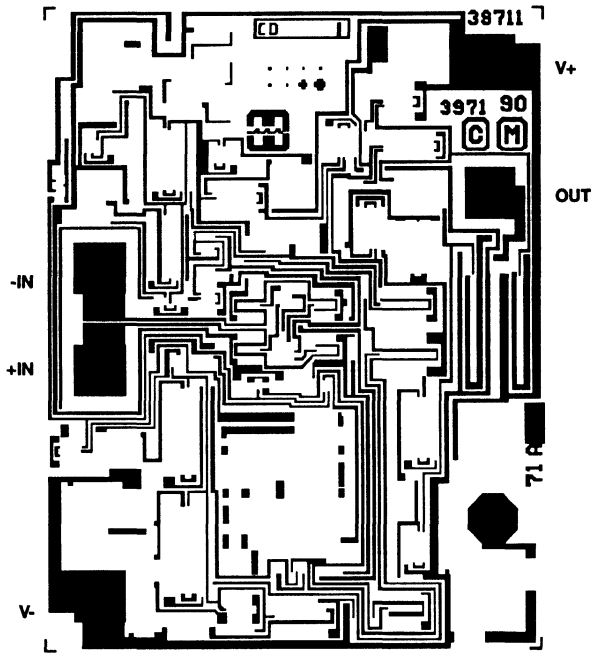
SUBSTRATE POTENTIAL (POWERED UP): V-

TRANSISTOR COUNT: 34

PROCESS: High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2840



Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified

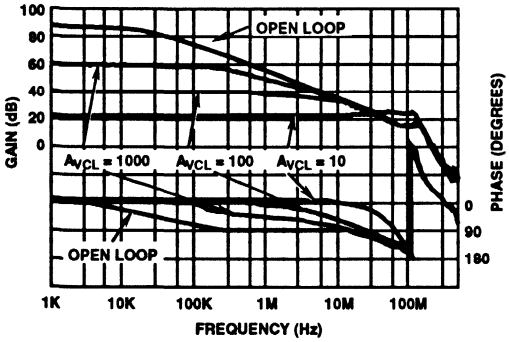


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS GAINS

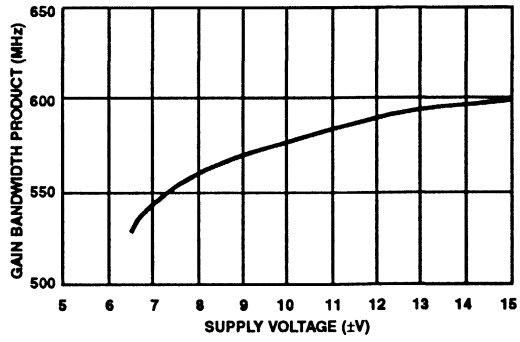


FIGURE 2. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

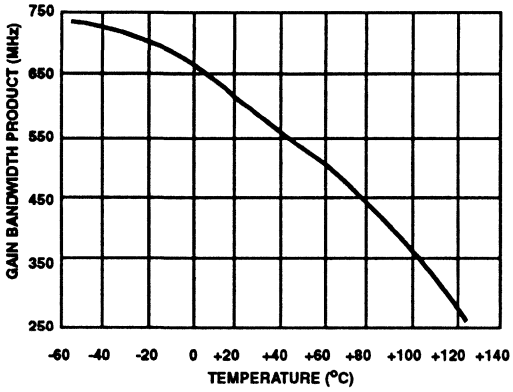


FIGURE 3. GAIN BANDWIDTH PRODUCT vs TEMPERATURE

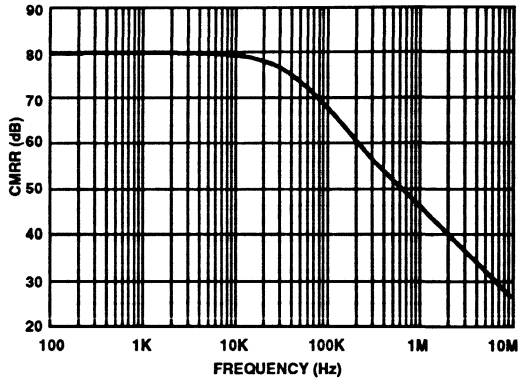


FIGURE 4. CMRR vs FREQUENCY

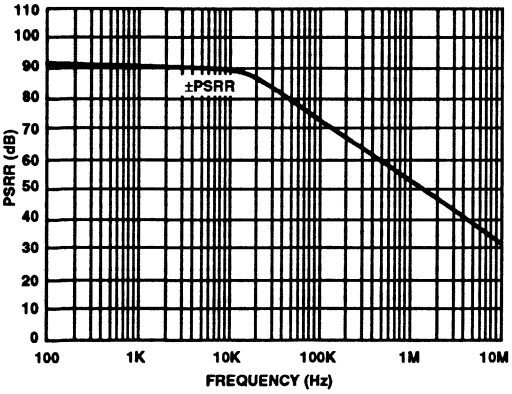


FIGURE 5. PSRR vs FREQUENCY

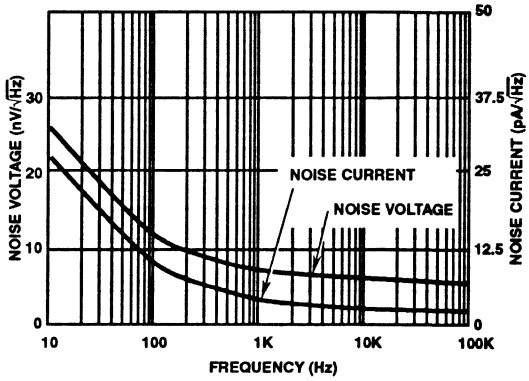


FIGURE 6. INPUT NOISE vs FREQUENCY

Typical Performance Curves T_A = +25°C, V_{SUPPLY} = ±15V, R_L = 1kΩ, C_L < 10pF, Unless Otherwise Specified (Continued)

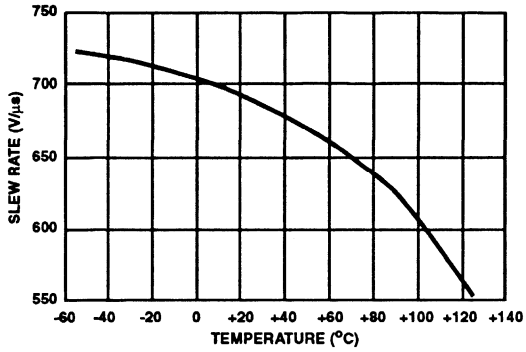


FIGURE 7. SLEW RATE vs TEMPERATURE

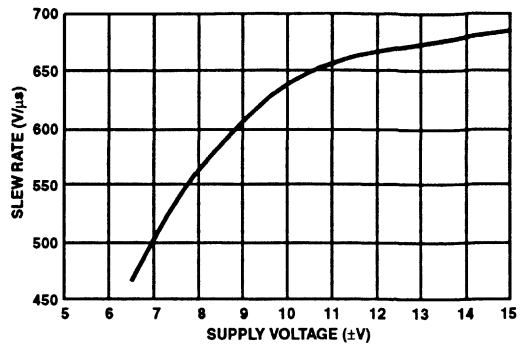


FIGURE 8. SLEW RATE vs SUPPLY VOLTAGE

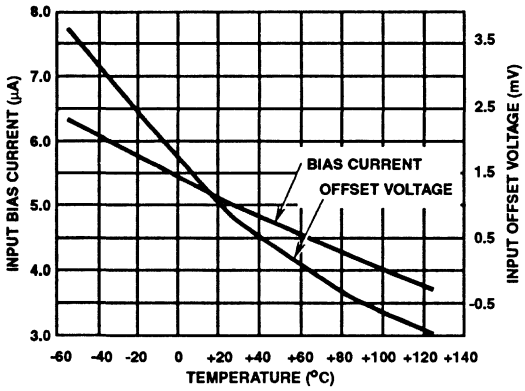


FIGURE 9. INPUT OFFSET VOLTAGE AND INPUT BIAS CURRENT vs TEMPERATURE

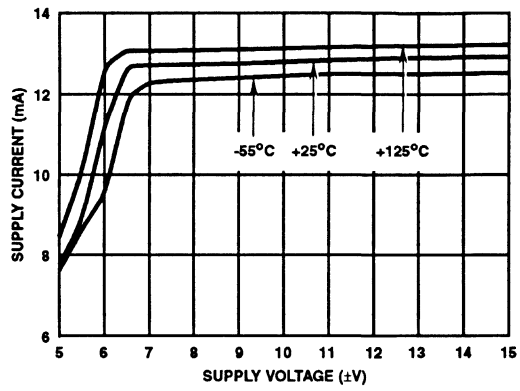


FIGURE 10. SUPPLY CURRENT vs SUPPLY VOLTAGE

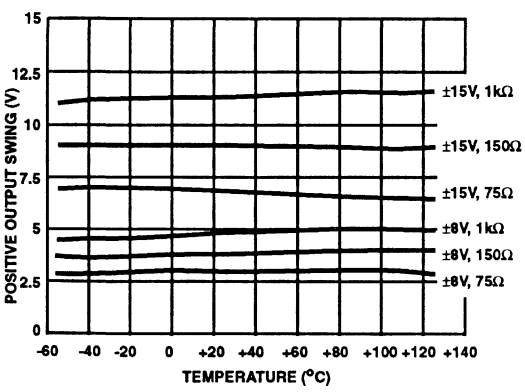


FIGURE 11. POSITIVE OUTPUT SWING vs TEMPERATURE

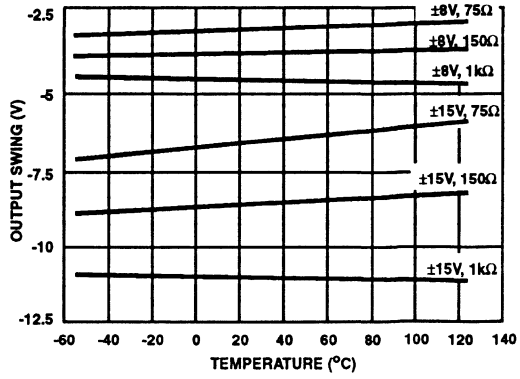


FIGURE 12. NEGATIVE OUTPUT SWING vs TEMPERATURE

Typical Performance Curves T_A = +25°C, V_{SUPPLY} = ±15V, R_L = 1kΩ, C_L < 10pF, Unless Otherwise Specified (Continued)

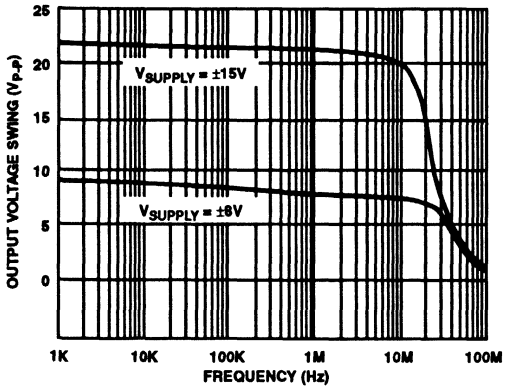


FIGURE 13. MAXIMUM UNDISTORTED OUTPUT SWING vs FREQUENCY

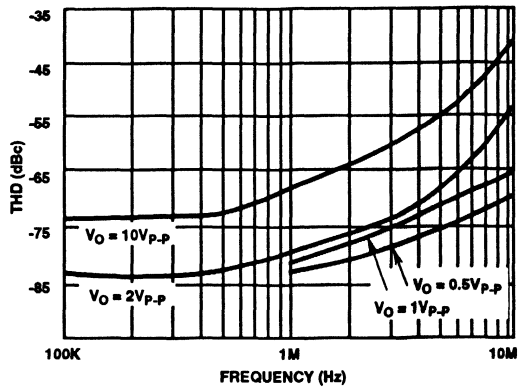


FIGURE 14. TOTAL HARMONIC DISTORTION vs FREQUENCY

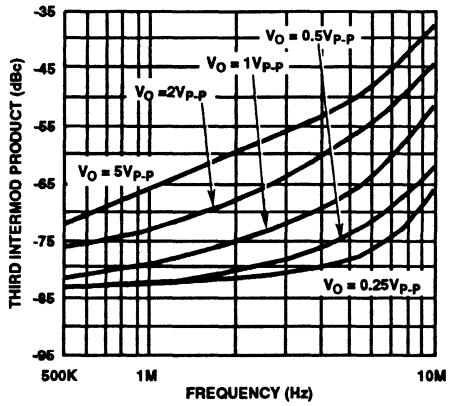


FIGURE 15. INTERMODULATION DISTORTION vs FREQUENCY TWO TONE

HARRIS SEMICONDUCTOR

HA-2841

Wideband, Fast Settling, Unity Gain Stable, Video Operational Amplifier

March 1993

Features

- Low Supply Current 10mA
- Low AC Variability Over Process and Temperature
- Unity Gain Bandwidth 50MHz
- Gain Flatness to 10MHz 0.05dB
- High Slew Rate 240V/μs
- Low Offset Voltage 1mV
- Fast Settling Time (0.1%) 90ns
- Differential Gain/Phase . . . . . 0.03%/0.03°
- Enhanced Replacement for AD841 and EL2041

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters
- High Speed A/D Input Buffer

Description

The HA-2841 is a wideband, unity gain stable, operational amplifier featuring a 50MHz unity gain bandwidth, and excellent DC specifications. This amplifier's performance is further enhanced through stable operation down to closed loop gains of +1, the inclusion of offset null controls, and by its excellent video performance.

The capabilities of the HA-2841 are ideally suited for high speed pulse and video amplifier circuits, where high slew rates and wide bandwidth are required. Gain flatness of 0.05dB, combined with differential gain and phase specifications of 0.03%, and 0.03 degrees, respectively, make the HA-2841 ideal for component and composite video applications.

A zener/nichrome based reference circuit, coupled with advanced laser trimming techniques, yields a supply current with a low temperature coefficient and low lot-to-lot variability. Tighter Icc control translates to more consistent AC parameters ensuring that units from each lot perform the same way, and easing the task of designing systems for wide temperature ranges. Critical AC parameters, Slew Rate and Bandwidth, each vary by less than ±5% over the industrial temperature range (see characteristic curves).

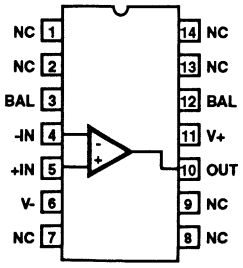
For military grade product, refer to the HA-2841/883 data sheet.

Ordering Information

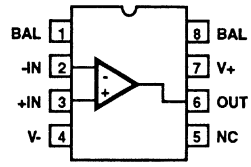
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA3B2841-5	0°C to +75°C	14 Lead Plastic DIP
HA3-2841-5	0°C to +75°C	8 Lead Plastic DIP
HA9P2841-5	0°C to +75°C	8 Lead SOIC
HA3B2841-9	-40°C to +85°C	14 Lead Plastic DIP
HA3-2841-9	-40°C to +85°C	8 Lead Plastic DIP

Pinouts

HA-2841
(PDIP)
TOP VIEW



HA-2841
(PDIP, SOIC)
TOP VIEW



NOTE: (NC) No Connection pins may be tied to a ground plane for better isolation and heat dissipation.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2843.1**

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Output Current (Note 6) 50mA
10mA (50% Duty Cycle)
Junction Temperature (Note 11) ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-2841-5 ..... $0°C \le T_A \le +75°C$
HA-2841-9 ..... $-40°C \le T_A \le +85°C$
Recommended Supply Voltage Range ..... ±6.5V to ±15V
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
14 Lead Plastic DIP Package	89	28
8 Lead Plastic Dip Package	92	30
8 Lead SOIC Package	157	42

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \le 10pF$, Unless Otherwise Specified.

PARAMETER	TEMPERATURE	HA-2841-5, -9			UNITS
		MIN	TYP	MAX	
INPUT CHARACTERISTICS					
Offset Voltage (Note 13)	+25°C	-	1	3	mV
	Full	-	-	6	mV
Average Offset Voltage Drift	Full	-	14	-	µV/°C
Bias Current (Note 13)	+25°C	-	5	10	µA
	Full	-	8	15	µA
Average Bias Current Drift	Full	-	45	-	nA/°C
Offset Current	+25°C	-	0.5	1.0	µA
	Full	-	-	1.5	µA
Input Resistance	+25°C	-	170	-	kΩ
Input Capacitance	+25°C	-	1	-	pF
Common Mode Range	Full	±10	-	-	V
Input Noise Voltage (10Hz to 1MHz)	+25°C	-	16	-	µVrms
Input Noise Voltage (f = 1kHz, $R_{SOURCE} = 0\Omega$) (Note 13)	+25°C	-	16	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz, $R_{SOURCE} = 10k\Omega$) (Note 13)	+25°C	-	2	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Note 3)	+25°C	25	50	-	kV/V
	Full	10	30	-	kV/V
Common-Mode Rejection Ratio (Notes 4, 13)	Full	80	95	-	dB
Minimum Stable Gain	+25°C	1	-	-	V/V
Gain Bandwidth Product (Notes 5, 13)	+25°C	-	50	-	MHz
Gain Flatness to 5MHz ($R_L \ge 75\Omega$) (Note 13)	+25°C	-	±0.015	-	dB
Gain Flatness to 10MHz ($R_L \ge 500\Omega$) (Note 13)	+25°C	-	±0.05	-	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 13)	Full	±10	±10.5	-	V
Output Current (Notes 6, 13)	Full	15	30	-	mA
Output Resistance	+25°C	-	8.5	-	Ω
Full Power Bandwidth (Notes 3 and 7)	+25°C	3.2	3.8	-	MHz
Differential Gain (Notes 2, 13)	+25°C	-	0.03	-	%
Differential Phase (Notes 2, 13)	+25°C	-	0.03	-	Degrees

Electrical Specifications V_{SUPPLY} = ±15V, R_L = 1kΩ, C_L ≤ 10pF, Unless Otherwise Specified. **(Continued)**

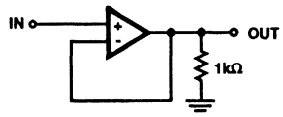
PARAMETER	TEMPERATURE	HA-2841-5, -9			UNITS
		MIN	TYP	MAX	
OUTPUT CHARACTERISTICS (Continued)					
Harmonic Distortion (Notes 10, 13)	+25°C	-	>83	-	dBc
TRANSIENT RESPONSE (Note 8)					
Rise Time	+25°C	-	3	-	ns
Overshoot	+25°C	-	33	-	%
Slew Rate (Notes 12, 13)	+25°C	200	240	-	V/µs
Settling Time: 10V Step to 0.1%	+25°C	-	90	-	ns
POWER REQUIREMENTS					
Supply Current (Note 13)	+25°C	-	10	-	mA
	Full	-	10	11	mA
Power Supply Rejection Ratio (Notes 9, 13)	Full	70	80	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Differential gain and end phase are measured with a VM700A video tester, using a NTC-7 composite VITS. $R_F = R_1$ = 1K, R_L = 700Ω.
3. V_O = ±10V.
4. V_{CM} = ±10V.
5. A_{VCL} = 1000, Measured at unity gain crossing.
6. V_O = ±10V, R_L unconnected. Output duty cycle must be reduced if I_{OUT} >10mA.
7. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; (V_{PEAK} = 10V).
8. Refer to Test Circuit section of data sheet.
9. V_{SUPPLY} = ±10VDC to ±20VDC.
10. V_O = 2Vp-p; f = 1MHz; A_V = +1.
11. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below +150°C for plastic packages.
12. A_V = +1. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
13. See "Typical Performance Curves" for more information.

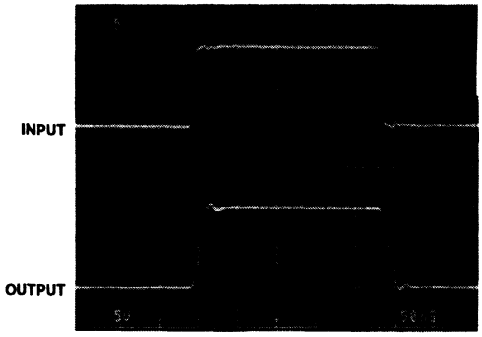
Test Circuit

TEST CIRCUIT

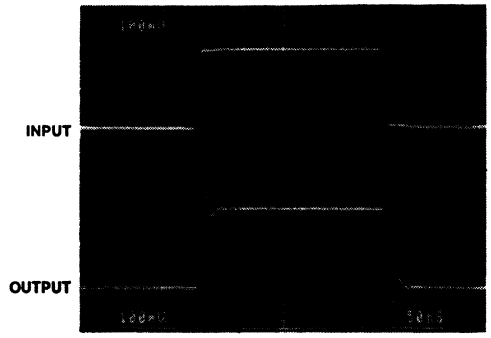


NOTE:
$V_S = \pm 15V$
$A_V = +1$
$C_L < 10pF$

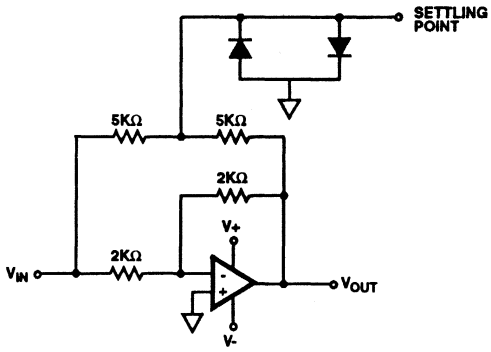
LARGE SIGNAL RESPONSE
Input = 5V/Div.
Output = 5V/Div.
50ns/Div.



SMALL SIGNAL RESPONSE
Input = 100mV/Div.
Output = 100mV/Div.
50ns/Div.

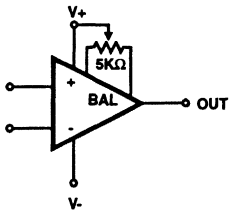


Settling Time Test Circuit



- $A_V = -1$
- Load Capacitance should be less than 10pF.
- Feedback and summing resistors must be matched to 0.1%.
- Tektronix P6201 FET probe used at settling point.
- HP5082-2810 clipping diodes recommended.

Suggested Offset Voltage Adjustment



Die Characteristics

DIE DIMENSIONS:
77 x 81 x 19 ± 1mils
(1960 x 2060 x 483µm)

METALLIZATION:
Type: Aluminum, 1% Copper
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride thickness: 3.5kÅ ± 1kÅ

DIE ATTACH:
Material: Epoxy-Plastic DIP and SOIC

WORST CASE CURRENT DENSITY:
1.2×10^5 A/cm^2 at 9.7mA

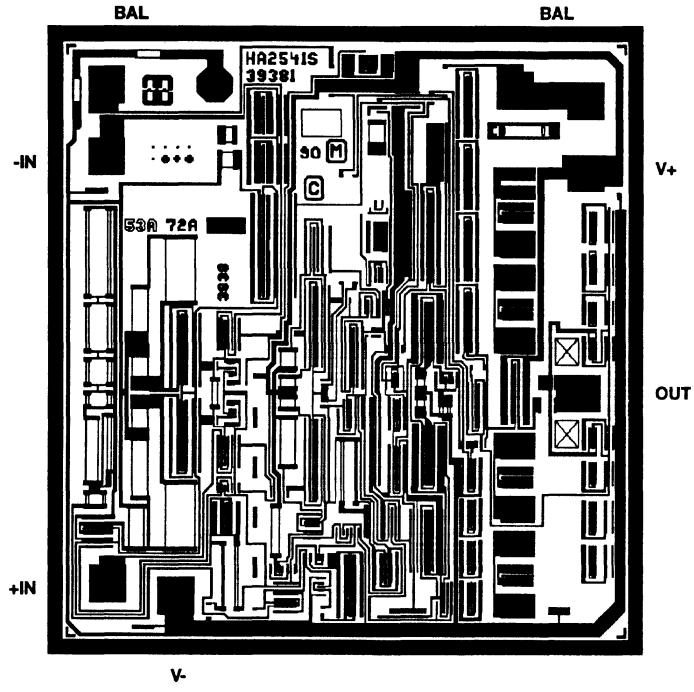
SUBSTRATE POTENTIAL (POWERED UP): V-

TRANSISTOR COUNT: 43

PROCESS: High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2841



Typical Performance Curves $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$, $R_L = 1K\Omega$, $C_L < 10pF$, Unless Otherwise Specified

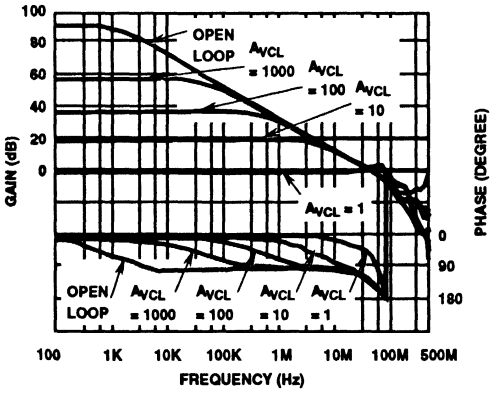


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS GAINS

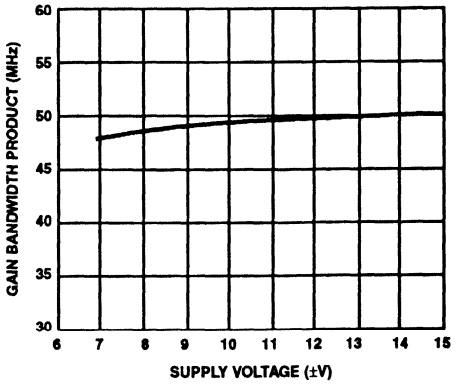


FIGURE 2. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

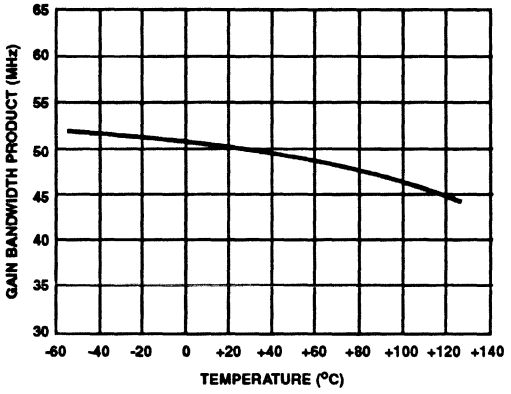


FIGURE 3. GAIN BANDWIDTH PRODUCT vs TEMPERATURE

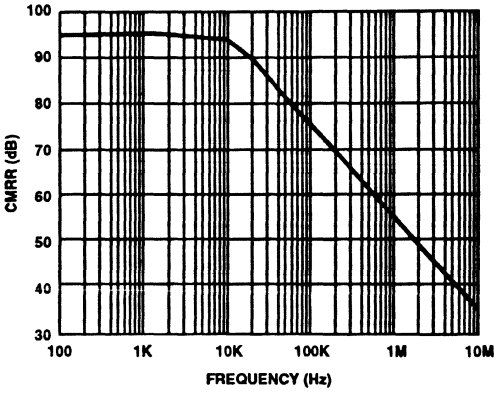


FIGURE 4. CMRR vs FREQUENCY

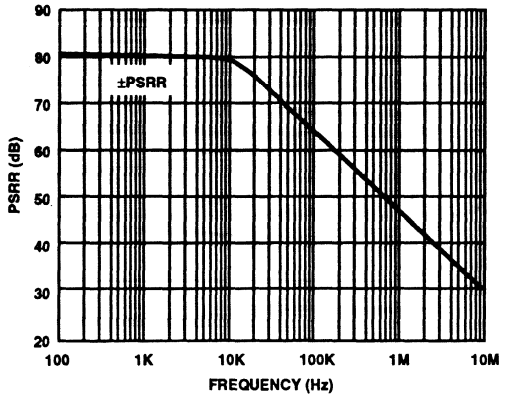


FIGURE 5. PSRR vs FREQUENCY

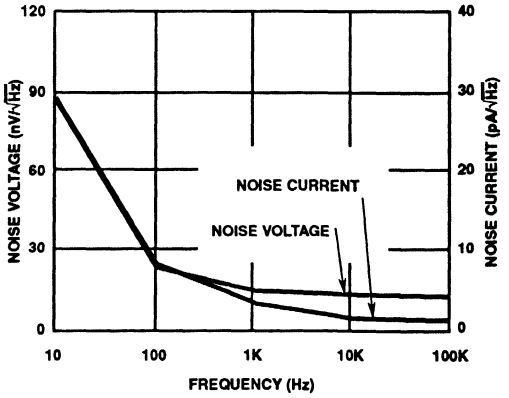


FIGURE 6. INPUT NOISE vs FREQUENCY

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $R_L = 1K\Omega$, $C_L < 10pF$, Unless Otherwise Specified (Continued)

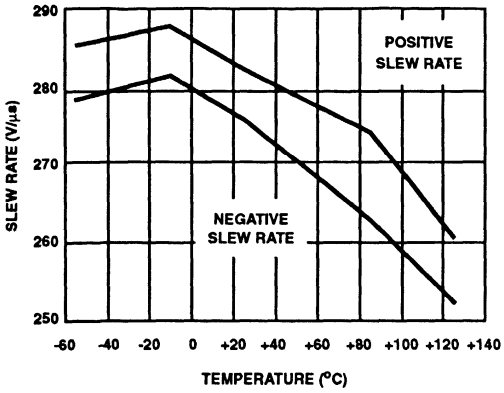


FIGURE 7. SLEW RATE vs TEMPERATURE

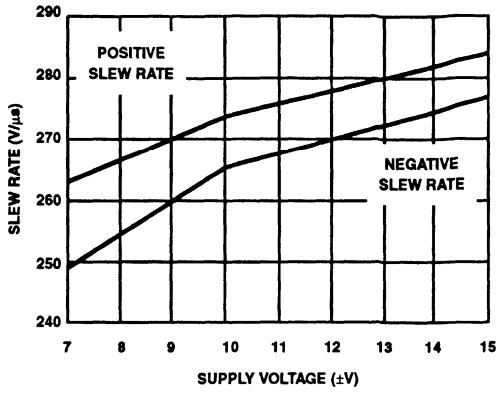


FIGURE 8. SLEW RATE vs SUPPLY VOLTAGE

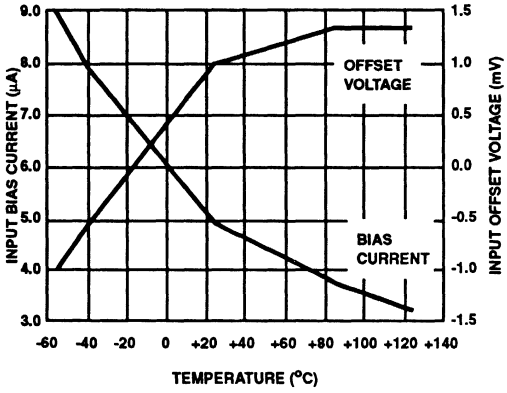


FIGURE 9. INPUT OFFSET VOLTAGE AND INPUT BIAS CURRENT vs TEMPERATURE

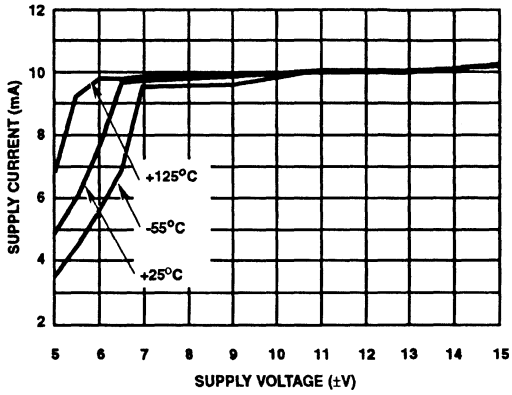


FIGURE 10. SUPPLY CURRENT vs SUPPLY VOLTAGE

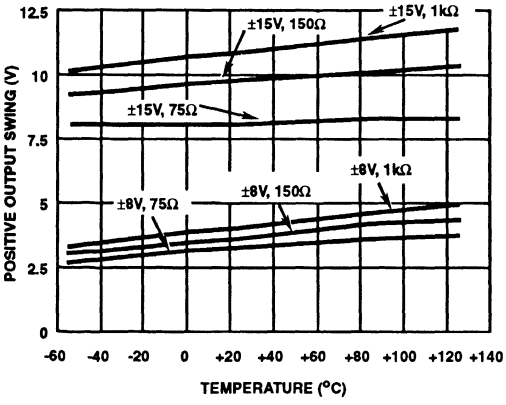


FIGURE 11. POSITIVE OUTPUT SWING vs TEMPERATURE

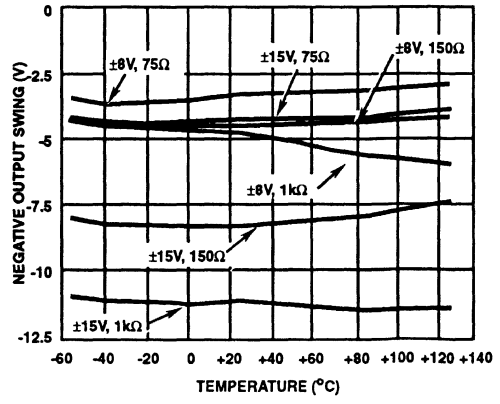


FIGURE 12. NEGATIVE OUTPUT SWING vs TEMPERATURE

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $R_L = 1K\Omega$, $C_L < 10pF$, Unless Otherwise Specified (Continued)

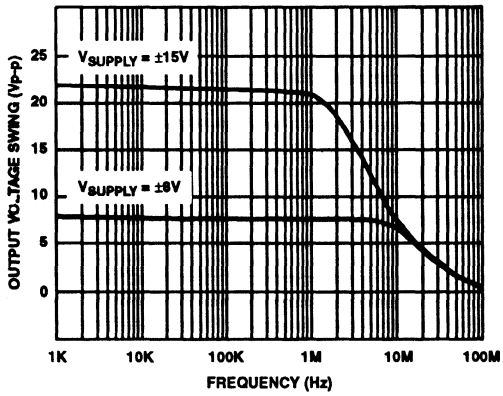


FIGURE 13. MAXIMUM UNDISTORTED OUTPUT SWING vs FREQUENCY

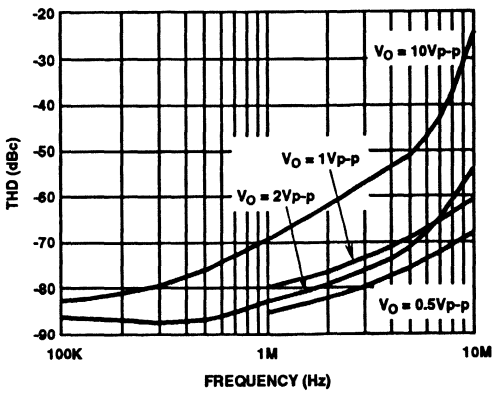


FIGURE 14. TOTAL HARMONIC DISTORTION vs FREQUENCY

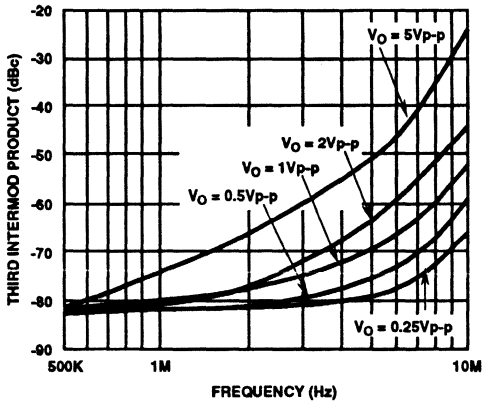


FIGURE 15. INTERMODULATION DISTORTION vs FREQUENCY (TWO TONE)

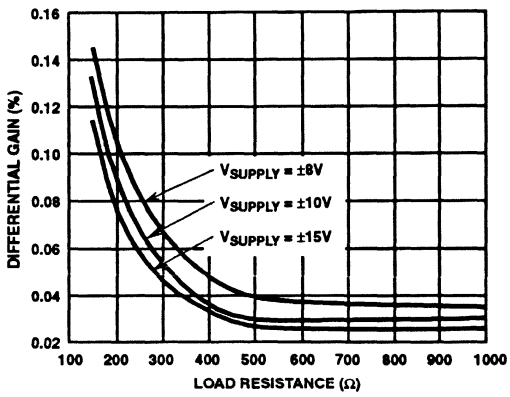


FIGURE 16. DIFFERENTIAL GAIN vs LOAD RESISTANCE

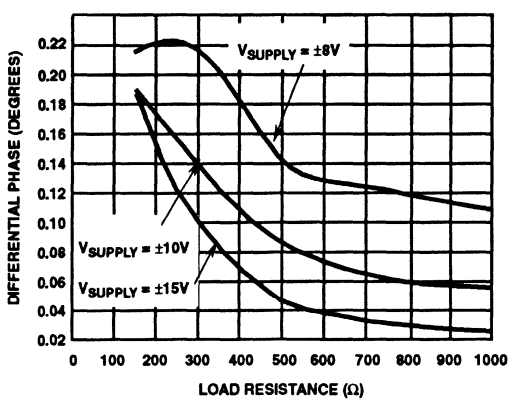


FIGURE 17. DIFFERENTIAL PHASE vs LOAD RESISTANCE

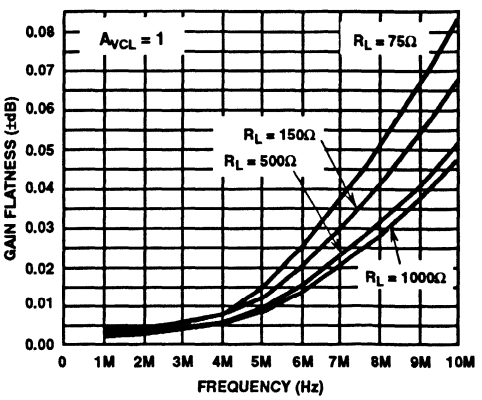


FIGURE 18. GAIN FLATNESS vs FREQUENCY

Typical Applications (Also see Application Note 550)

Application 1

High power amplifiers and buffers are in use in a wide variety of applications. Many times the "high power" capability is needed to drive large capacitive loads as well as low value resistive loads. In both cases the final driver stage is usually a power transistor of some type, but because of their inherently low gain, several stages of pre-drivers are often required. The HA-2841, with its 15mA output rating, is powerful enough to drive a power transistor without additional stages of current amplification. This capability is well demonstrated with the high power buffer circuit in Figure 19.

The HA-2841 acts as the pre-driver to the output power transistor. Together, they form a unity gain buffer with the ability to drive three 50Ω coaxial cables in parallel, each with a capacitance of 2000pF. The total combined load is 16.6Ω and 6000pF capacitance.

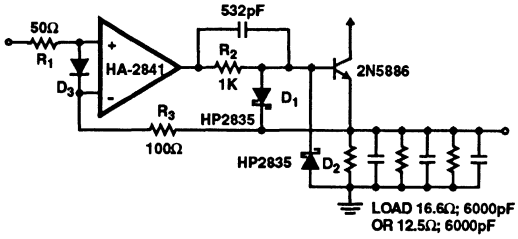


FIGURE 19. DRIVING POWER TRANSISTORS TO GAIN ADDITIONAL CURRENT BOOSTING

Application 2

Video

One of the primary uses of the HA-2841 is in the area of video applications. These applications include signal construction, synchronization addition and removal, as well as signal modification. A wide bandwidth device such as the HA-2841 is well suited for use in this class of amplifier. This, however, is a more involved group of applications than ordinary amplifier applications since video signals contain precise DC levels which must be retained.

The addition of a clamping circuit restores DC levels at the output of an amplifier stage. The circuit shown in Figure 20 utilizes the HA-5320 sample and hold amplifier as the DC clamp. Also shown is a 3.57MHz trap in series, which will block the color burst portion of the video signal and allow the DC level to be amplified and restored.

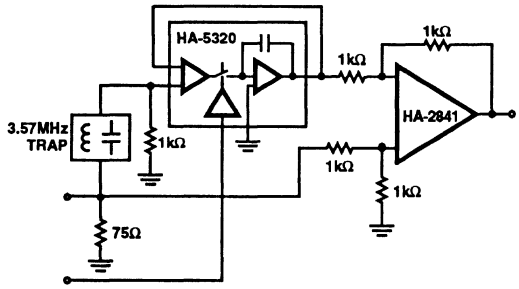


FIGURE 20. VIDEO DC RESTORER

Prototyping Guidelines

For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include:

1. Mounting the device through a ground plane.
2. Connecting unused pins (NC) to the ground plane.
3. Mounting feedback components on Teflon standoffs and/or locating these components as close to the device as possible.
4. Placing power supply decoupling capacitors from device supply pins to ground.

HARRIS SEMICONDUCTOR

HA-2842

Wideband, High Slew Rate, High Output Current, Video Operational Amplifier

March 1993

Features

- Stable at Gains of 2 or Greater
- Low AC Variability Over Process and Temperature
- Gain Bandwidth 80MHz
- Gain Flatness to 10MHz. 0.035dB
- High Slew Rate 400V/µs
- High Output Current (Min). 100mA
- Differential Gain/Phase ..... 0.02%/0.03°
- Low Supply Current (Max) 15mA
- Enhanced Replacement for AD842

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- Coaxial Cable Drivers
- Fast Sample-Hold Circuits
- High Frequency Signal Conditioning Circuits

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA3B2842-5	0°C to +75°C	14 Lead Plastic DIP
HA3-2842-5	0°C to +75°C	8 Lead Plastic DIP
HA9P2842-5	0°C to +75°C	8 Lead SOIC
HA3-2842C-5	0°C to +75°C	8 Lead Plastic DIP
HA9P2842C-5	0°C to +75°C	8 Lead SOIC
HA3B2842-9	-40°C to +85°C	14 Lead Plastic DIP
HA3-2842-9	-40°C to +85°C	8 Lead Plastic DIP

Description

The HA-2842 is a wideband, high slew rate, operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability. This amplifier's performance is further enhanced through stable operation down to closed loop gains of +2, the inclusion of offset null controls, and by its excellent video performance.

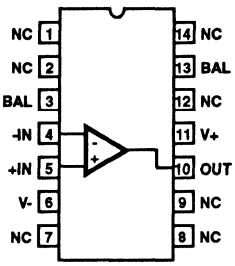
The capabilities of the HA-2842 are ideally suited for high speed cable driver circuits, where low closed loop gains and high output drive are required. With a 6MHz full power bandwidth, this amplifier is well suited for high frequency signal conditioning circuits and video amplifiers. Gain flatness of 0.035dB, combined with differential gain and phase specifications of 0.02%, and 0.03 degrees, respectively, make the HA-2842 ideal for component and composite video applications.

A zener/nichrome based reference circuit, coupled with advanced laser trimming techniques, yields a supply current with a low temperature coefficient and low lot-to-lot variability. For example, the average Icc variation from +85°C to -40°C is <600µA (±2%),while the standard deviation of the I_{CC} distribution is <0.1mA (0.8%) at +25°C. Tighter I_{CC} control translates to more consistent AC parameters ensuring that units from each lot perform the same way, and easing the task of designing systems for wide temperature ranges. Critical AC parameters, Slew Rate and Bandwidth, each vary by less than ±5% over the industrial temperature range (see Typical Performance Curves).

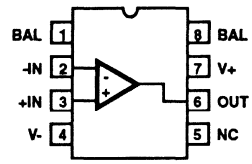
The HA-2842C is the same amplifier with a compensation pin available to the user. By connecting a capacitor from pin 8 to GND, the HA-2842C can be compensated for unity gain operation, or the bandwidth can be limited to reduce total noise.

Pinouts

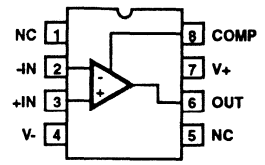
HA-2842 (PDIP) TOP VIEW



HA-2842 (PDIP, SOIC) TOP VIEW



HA-2842C (PDIP, SOIC) TOP VIEW



NOTE: (NC) No Connection pins may be tied to a ground plane for better isolation and heat dissipation.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2766.3**

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Output Current 125mA
100mA (50% Duty Cycle)
Junction Temperature (Note 11) ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-2842-5 ..... $0°C \le T_A \le +75°C$
HA-2842-9 ..... $-40°C \le T_A \le +85°C$
Recommended Supply Voltage Range ..... ±6.5V to ±15V
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
14 Lead Plastic DIP Package	89	28
8 Lead Plastic Dip Package	92	30
8 Lead SOIC Package	157	42

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{SUPPLY} = ±15V, R_L = 1kΩ, $C_L \le$ 10pF, Unless Otherwise Specified.

PARAMETER	TEMPERATURE	HA-2842-5, -9			UNITS
		MIN	TYP	MAX	
INPUT CHARACTERISTICS					
Offset Voltage (Note 13)	+25°C	-	1	3	mV
	Full	-	-	6	mV
Average Offset Voltage Drift	Full	-	13	-	µV/°C
Bias Current (Note 13)	+25°C	-	5	10	µA
	Full	-	-	15	µA
Average Bias Current Drift	Full	-	20	-	nA/°C
Offset Current	+25°C	-	0.5	1.0	µA
	Full	-	-	1.5	µA
Average Offset Current Drift	Full	-	1.3	-	nA/°C
Input Resistance	+25°C	-	170	-	kΩ
Input Capacitance	+25°C	-	1	-	pF
Common Mode Range	Full	±10	-	-	V
Input Noise Voltage (10Hz to 1MHz)	+25°C	-	16	-	µVrms
Input Noise Voltage Density (f = 1kHz, R_{SOURCE} = 0Ω) (Note 13)	+25°C	-	16	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz, R_{SOURCE} = 100kΩ) (Note 13)	+25°C	-	2	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Note 3)	+25°C	50	100	-	kV/V
	Full	30	60	-	kV/V
Common-Mode Rejection Ratio (Notes 4, 13)	Full	80	110	-	dB
Minimum Stable Gain	+25°C	2	-	-	V/V
Gain Bandwidth Product (Notes 5, 13)	+25°C	-	80	-	MHz
Gain Flatness to 10MHz ($R_L \ge$ 75Ω) (Note 13)	+25°C	-	±0.035	-	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Notes 3, 13)	Full	±10	±11	-	V
Output Current (Notes 6, 13)	Full	100	-	-	mA
Output Resistance	+25°C	-	8.5	-	Ω
Full Power Bandwidth (Notes 3 and 7)	+25°C	5.2	6	-	MHz
Differential Gain (Notes 2, 13)	+25°C	-	0.02	-	%
Differential Phase (Notes 2, 13)	+25°C	-	0.03	-	Degrees
Harmonic Distortion (Notes 10, 13)	+25°C	-	>81	-	dBc

Electrical Specifications V_{SUPPLY} = ±15V, R_L = 1kΩ, C_L ≤ 10pF, Unless Otherwise Specified. **(Continued)**

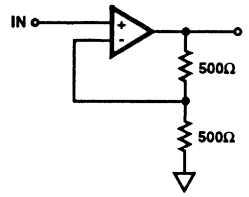
PARAMETER	TEMPERATURE	HA-2842-5, -9			UNITS
		MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 9)					
Rise Time	+25°C	-	4	-	ns
Overshoot	+25°C	-	25	-	%
Slew Rate (Notes 12, 13)	+25°C	325	400	-	V/µs
Settling Time: 10V Step to 0.1%	+25°C	-	100	-	ns
POWER REQUIREMENTS					
Supply Current (Note 13)	+25°C	-	14.2	-	mA
	Full	-	14.3	15	mA
Power Supply Rejection Ratio (Notes 9, 13)	Full	70	80	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Differential gain and phase are measured with a VM700A video tester, using a NTC-7 composite VITS. $R_F = R_1 = 1K$, $R_L = 700\Omega$.
3. $R_L = 1k\Omega$, $V_O = \pm 10V$.
4. $V_{CM} = \pm 10V$.
5. $A_{VCL} = 100$.
6. $V_O = \pm 5V$, R_L Unconnected, Duty cycle ≤ 50%. For information about using high output current amplifiers, please refer to Application Note 556 (Thermal Safe-Operating-Areas For High Current Op Amps)
7. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $V_{PEAK} = 10V$.
8. Refer to Test Circuits section of this data sheet.
9. V_{SUPPLY} = ±10VDC to ±20VDC.
10. V_O = 2Vp-p; f = 1MHz; A_V = +2.
11. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below +150°C for plastic packages. By using Application Note 556 on Safe Operating Area equations, along with the packaging thermal resistances listed in the Operating Conditions section, proper load conditions can be determined.
12. A_V = +2. This parameter is not tested. The limits are guaranteed based on lab characterization and reflect lot-to-lot variation.
13. See "Typical Performance Curves" for more information.

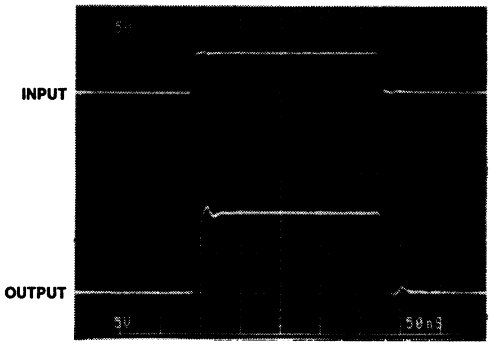
Test Circuits

TEST CIRCUIT

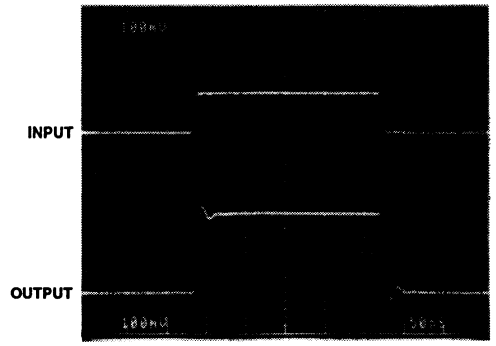


NOTE:
$V_S = \pm 15V$
$A_V = +2$
$C_L \leq 10pF$

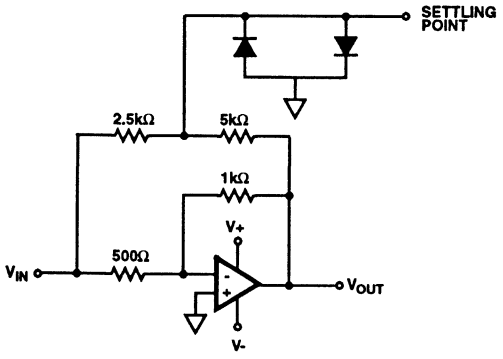
LARGE SIGNAL RESPONSE
Input = 5V/Div.
Output = 5V/Div.
50ns/Div.



SMALL SIGNAL RESPONSE
Input = 100mV/Div.
Output = 100mV/Div.
50ns/Div.

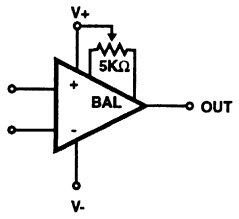


SETTLING TIME TEST CIRCUIT



- $A_V = -2$
- Feedback and summing resistors must be matched (0.1%)
- HP5082-2810 clipping diodes recommended
- Tektronix P6201 FET probe used at settling point
- For 0.01% settling time, heat sinking is suggested to reduce thermal effects and an analog ground plane with supply decoupling is suggested to minimize ground loop errors.

SUGGESTED OFFSET VOLTAGE ADJUSTMENT



Metallization Topology

DIE DIMENSIONS:
77 x 81 x 19 ± 1mils
(1960 x 2060 x 483µm)

METALLIZATION:
Type: Aluminum, 1% Copper
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride thickness: 3.5kÅ ± 1kÅ

DIE ATTACH:
Material: Epoxy-Plastic DIP and SOIC

WORST CASE CURRENT DENSITY:
1.83×10^5 A/cm^2 at 56mA

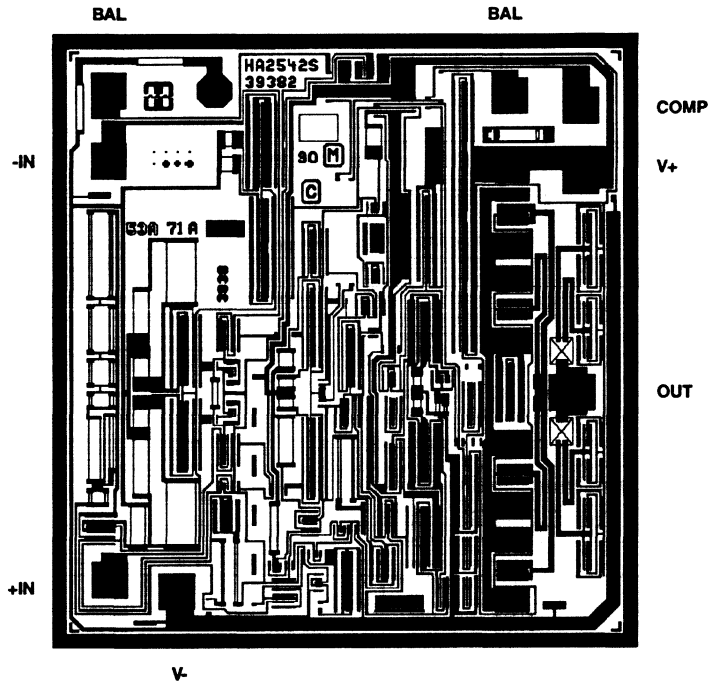
SUBSTRATE POTENTIAL (POWERED UP): V-

TRANSISTOR COUNT: 58

PROCESS: High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2842



Typical Performance Curves T_A = +25°C, V_{SUPPLY} = ±15V, R_L = 1KΩ, C_L < 10pF, Unless Otherwise Specified

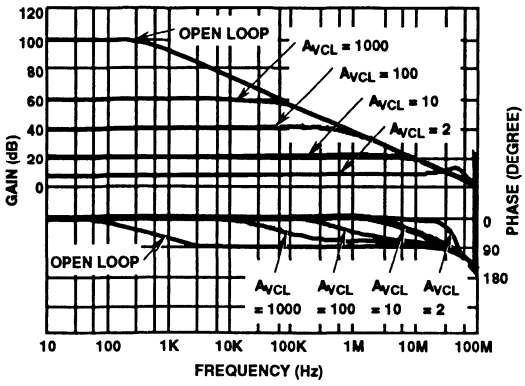


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS GAINS

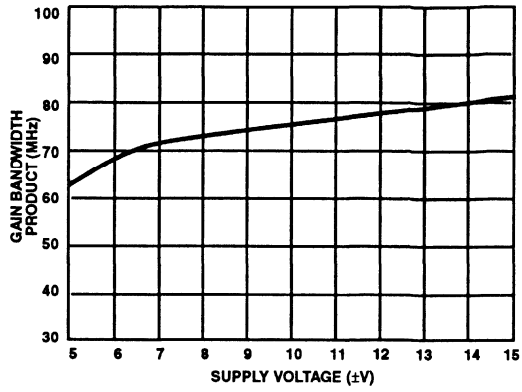


FIGURE 2. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

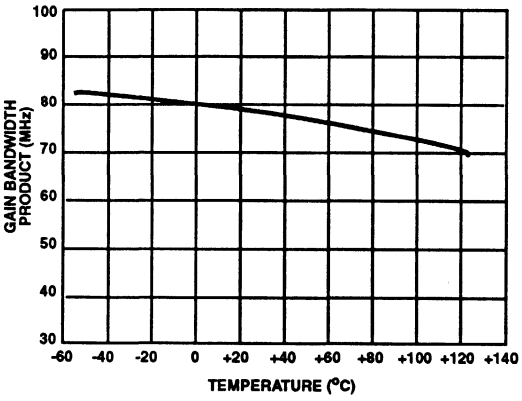


FIGURE 3. GAIN BANDWIDTH PRODUCT vs TEMPERATURE

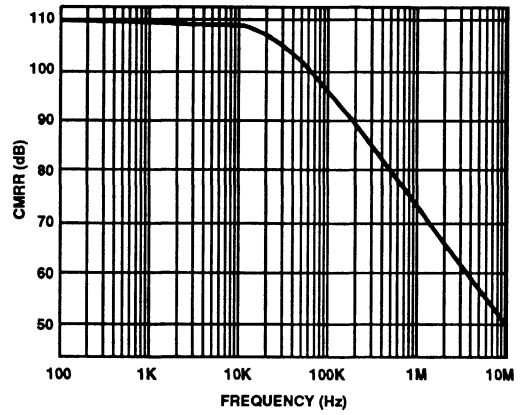


FIGURE 4. CMRR vs FREQUENCY

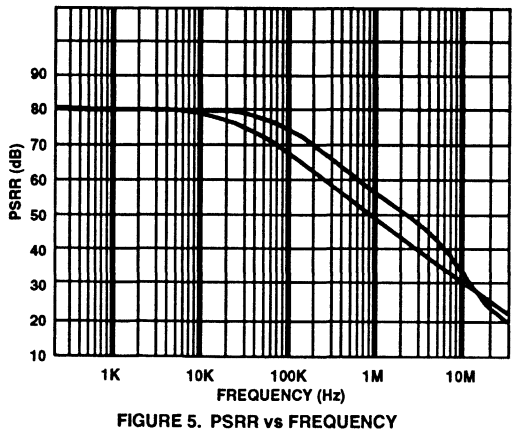


FIGURE 5. PSRR vs FREQUENCY

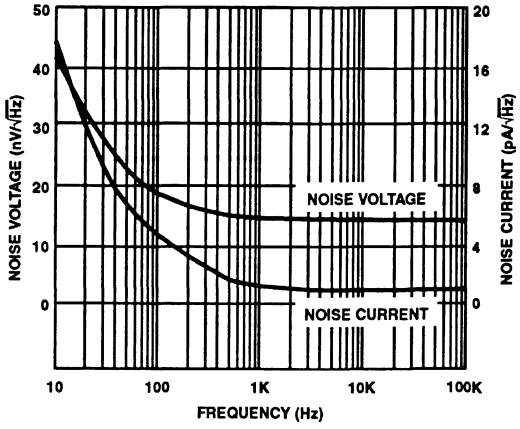


FIGURE 6. INPUT NOISE vs FREQUENCY

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $R_L = 1K\Omega$, $C_L < 10pF$, Unless Otherwise Specified (Continued)

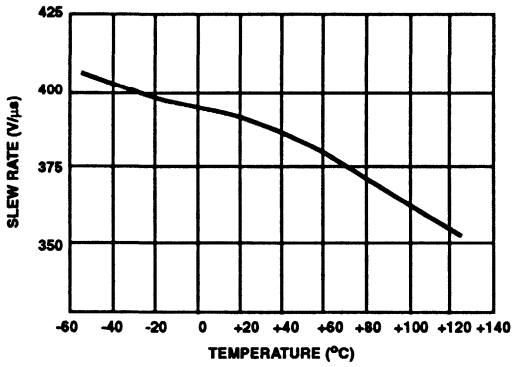


FIGURE 7. SLEW RATE vs TEMPERATURE

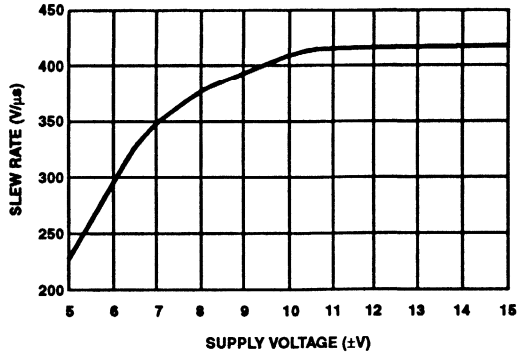


FIGURE 8. SLEW RATE vs SUPPLY VOLTAGE

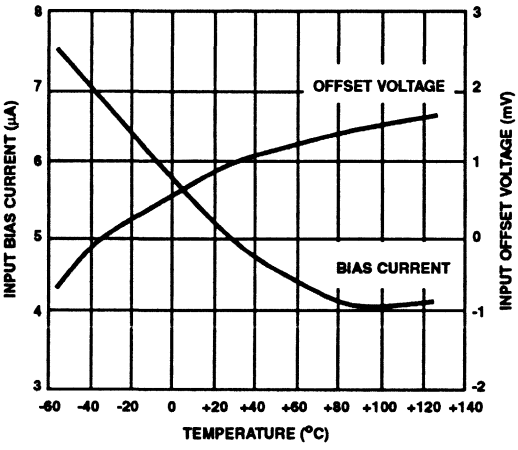


FIGURE 9. INPUT OFFSET VOLTAGE AND INPUT BIAS CURRENT vs TEMPERATURE

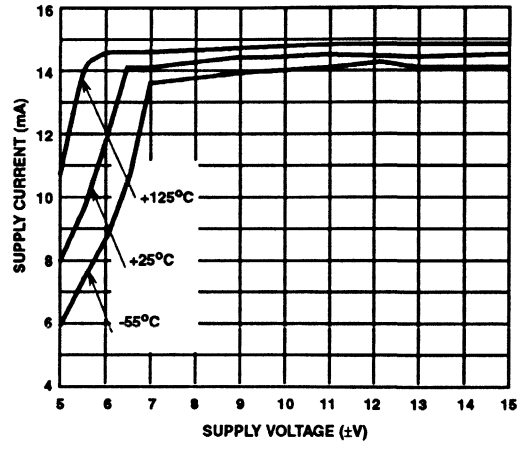


FIGURE 10. SUPPLY CURRENT vs SUPPLY VOLTAGE

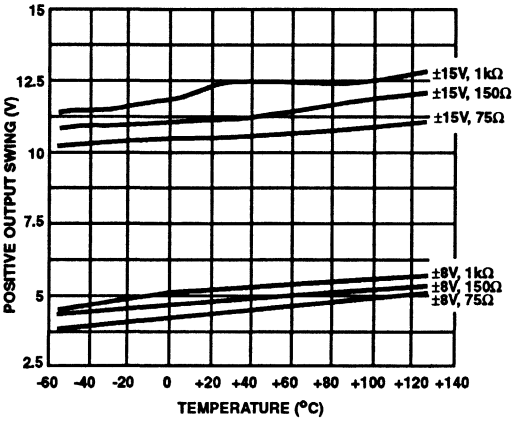


FIGURE 11. POSITIVE OUTPUT SWING vs TEMPERATURE

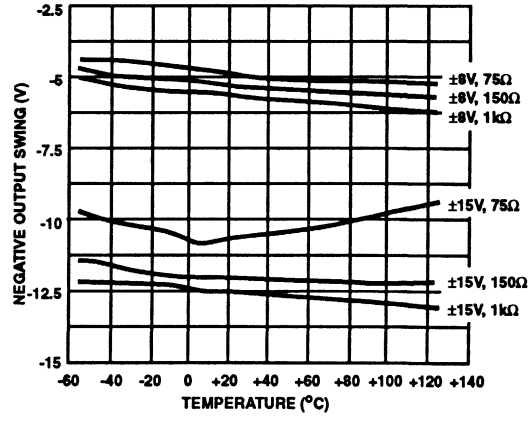


FIGURE 12. NEGATIVE OUTPUT SWING vs TEMPERATURE

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $R_L = 1K\Omega$, $C_L < 10pF$, Unless Otherwise Specified (Continued)

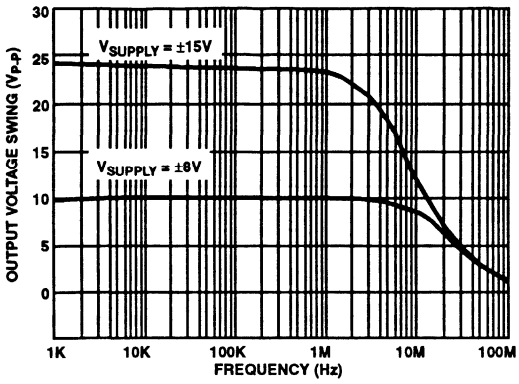


FIGURE 13. MAXIMUM UNDISTORTED OUTPUT SWING vs FREQUENCY

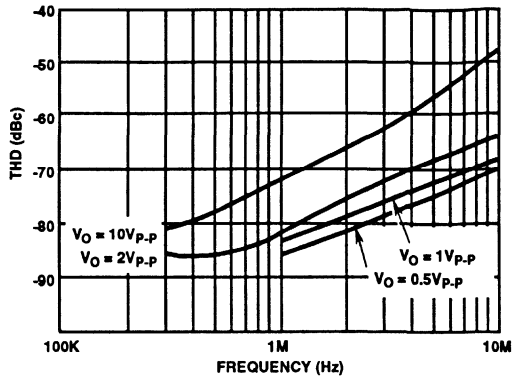


FIGURE 14. TOTAL HARMONIC DISTORTION vs FREQUENCY

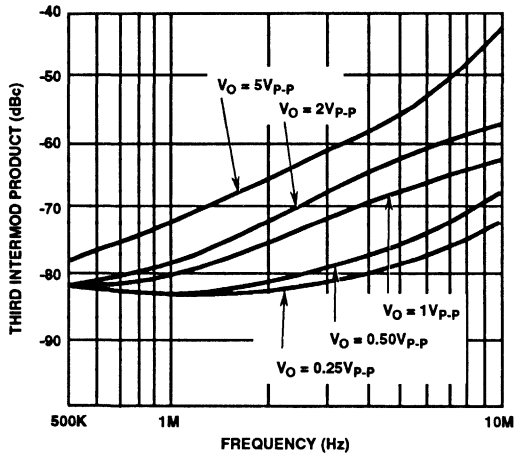


FIGURE 15. INTERMODULATION DISTORTION vs FREQUENCY (TWO TONE)

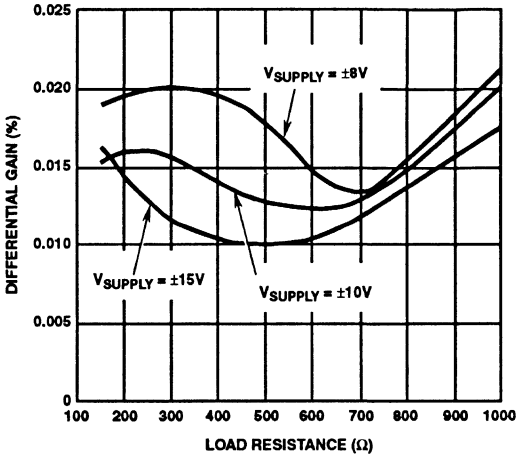


FIGURE 16. DIFFERENTIAL GAIN vs LOAD RESISTANCE

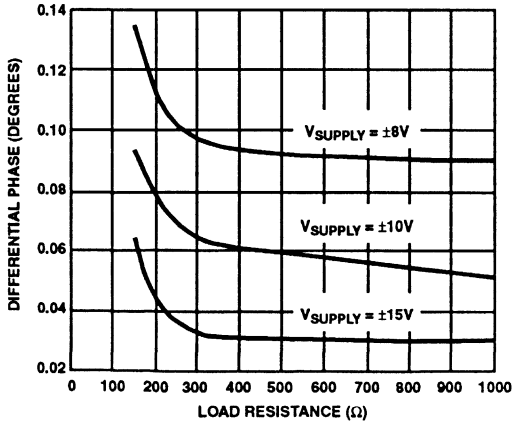


FIGURE 17. DIFFERENTIAL PHASE vs LOAD RESISTANCE

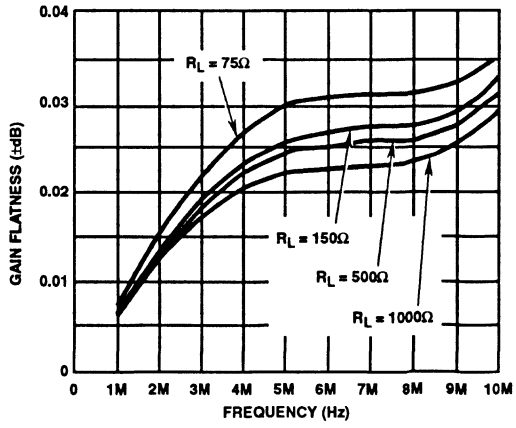


FIGURE 18. GAIN FLATNESS vs FREQUENCY ($A_{VCL} = 2$)

Typical Performance Curves T_A = +25°C, V_{SUPPLY} = ±15V, R_L = 1KΩ, C_L < 10pF, Unless Otherwise Specified (Continued)

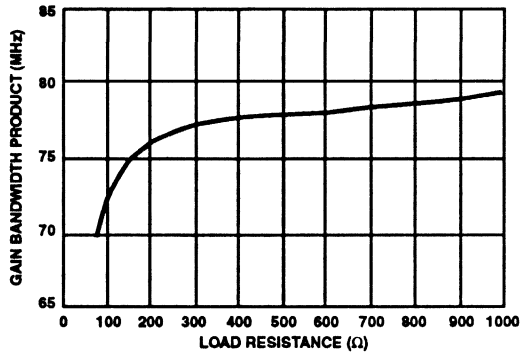


FIGURE 19. GAIN BANDWIDTH PRODUCT vs LOAD RESISTANCE

Typical Applications

The Harris HA-2842 is a state of the art monolithic device which also approaches the "ALL-IN-ONE" amplifier concept. This device features an outstanding set of AC parameters augmented by excellent output drive capability providing for suitable application in both high speed and high output drive circuits.

Primarily intended to be used in balanced 50Ω and 75Ω coaxial cable systems as a driver, the HA-2842 could also be used as a power booster in audio systems as well as a power amp in power supply circuits. This device would also be suitable as a small DC motor driver.

Prototyping Guidelines

For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include:

1. Mounting the device through a ground plane.
2. Connecting unused pins (NC) to the ground plane.
3. Mounting feedback components on Teflon standoffs and/or locating these components as close to the device as possible.
4. Placing power supply decoupling capacitors from device supply pins to ground.

Power Dissipation Considerations

At high output currents, especially with the 8 lead SOIC package, care must be taken to ensure that the Maximum Junction Temperature (T_J, see "Absolute Maximum Ratings" table) isn't exceeded. As an example consider the HA-2842 in the SOIC package, with a required output current of 50mA at V_{OUT} = 10V. The power dissipation is the quiescent power (450mW = 30V • 15mA) plus the power dissipated in the output stage (P_{OUT} = 250mW = 50mA • (15V - 10V)), or a total of 700mW. The thermal resistance (θ_{JA}) of the SOIC package is +157°C/W, which increases the junction temperature by 110°C over the ambient temperature (T_A). Remaining below T_{JMAX} requires that T_A be restricted to ≤ +40°C (+150°C - +110°C). Heatsinking would be required for operation at ambient temperatures greater than +40°C.

Note that the problem isn't as severe with either of the PDIP packages due to their lower thermal resistances, however it is recommended that the above analysis be performed for any package if operating outside the conditions listed below:

MAX P_{OUT} WITHOUT HEATSINK (V_S = ±15V)

T_A	14 LEAD PDIP (θ_{JA} = 89°C/W)	8 LEAD PDIP (θ_{JA} = 92°C/W)	8 LEAD SOIC (θ_{JA} = 157°C/W)
+85°C	280mW	260mW	Heatsink Required
+70°C	450mW	420mW	60mW
+25°C	950mW	910mW	350mW

Allowable output power can be increased by decreasing the quiescent dissipation via lower supply voltages.

For more information please refer to Application Note 556, Thermal Safe Operating Areas for High Current Op Amps.

HARRIS SEMICONDUCTOR

HA-2850

Low Power, High Slew Rate Wideband Operational Amplifier

March 1993

Features

- Low Supply Current 7.5mA
- High Slew Rate 340V/μs
- Open Loop Gain 25kV/V
- Wide Gain-Bandwidth ($A_V \geq 10$) 470MHz
- Full Power Bandwidth 5.4MHz
- Low Offset Voltage 0.6mV
- Input Noise Voltage . . . . . $11nV/\sqrt{Hz}$
- Differential Gain/Phase . . . . . 0.04%/0.04°
- Lower Power Enhanced Replacement for AD840 and EL2040

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters

Description

The HA-2850 is a wideband, high slew rate, operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction, coupled with dielectric isolation, delivers outstanding performance in circuits with a closed loop gain of 10 or greater.

A 340V/μs slew rate and a 470MHz gain bandwidth product ensure high performance in video and wideband amplifier designs. Differential gain and phase are a low 0.04% and 0.04° respectively, making the HA-2850 ideal for video applications. A full ±10V output swing, high open loop gain, and outstanding AC parameters, make the HA-2850 an excellent choice for high speed Data Acquisition Systems.

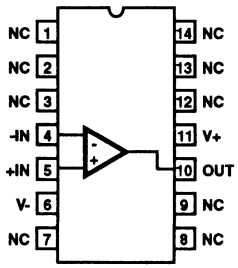
The HA-2850 is available in commercial and industrial temperature ranges, and a choice of packages. For military grade product, refer to the HA-2850/883 data sheet.

Ordering Information

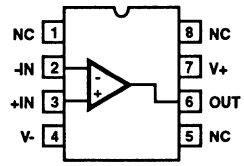
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-2850-5	0°C to +75°C	14 Lead Ceramic DIP
HA3B2850-5	0°C to +75°C	14 Lead Plastic DIP
HA7-2850-5	0°C to +75°C	8 Lead Ceramic DIP
HA3-2850-5	0°C to +75°C	8 Lead Plastic DIP
HA9P2850-5	0°C to +75°C	8 Lead SOIC
HA1-2850-9	-40°C to +85°C	14 Lead Ceramic DIP
HA3B2850-9	-40°C to +85°C	14 Lead Plastic DIP
HA7-2850-9	-40°C to +85°C	8 Lead Ceramic DIP
HA3-2850-9	-40°C to +85°C	8 Lead Plastic DIP

Pinouts

HA-2850
(CDIP, PDIP)
TOP VIEW



HA-2850
(CDIP, PDIP, SOIC)
TOP VIEW



NOTE: (NC) No Connection pins may be tied to a ground plane for better isolation and heat dissipation.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2844.2**

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Operating Temperature Range
HA-2850-5 . . . . . $0°C \le T_A \le +75°C$
HA-2850-9 . . . . . $-40°C \le T_A \le +85°C$
Recommended Supply Voltage Range . . . . . ±6V To ±15V
Storage Temperature Range . . . . . $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
14 Lead Plastic DIP Package	107	38
14 Lead Ceramic DIP Package	71	14
8 Lead Plastic DIP Package	96	34
8 Lead Ceramic DIP Package	115	36
8 Lead SOIC Package	157	43

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{SUPPLY} = ±15V, R_L = 1kΩ, $C_L \le$ 10pF, Unless Otherwise Specified.

PARAMETER	TEMPERATURE	HA-2850-5, -9 MIN	HA-2850-5, -9 TYP	HA-2850-5, -9 MAX	UNITS
INPUT CHARACTERISTICS					
Offset Voltage (Note 13)	+25°C	-	0.6	2	mV
	Full	-	2	6	mV
Average Offset Voltage Drift	Full	-	20	-	µV/°C
Bias Current (Note 13)	+25°C	-	5	14.5	µA
	Full	-	8	20	µA
Offset Current	+25°C	-	1	4	µA
	Full	-	-	8	µA
Input Resistance	+25°C	-	10	-	kΩ
Input Capacitance	+25°C	-	1	-	pF
Common Mode Range	Full	±10	-	-	V
Input Noise Voltage (f = 1kHz, R_{SOURCE} = 0Ω, Note 13)	+25°C	-	11	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz, R_{SOURCE} = 10kΩ, Note 13)	+25°C	-	6	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Note 3)	+25°C	20	25	-	kV/V
	Full	15	20	-	kV/V
Common-Mode Rejection Ratio (Notes 4, 13)	Full	75	80	-	dB
Minimum Stable Gain	+25°C	10	-	-	V/V
Gain Bandwidth Product (Notes 5, 11, 13)	+25°C	-	470	-	MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Notes 3, 13)	Full	±10	±11	-	V
Output Current (Notes 3, 13)	Full	±10	±20	-	mA
Output Resistance	+25°C	-	30	-	Ω
Full Power Bandwidth (Notes 3, 7)	+25°C	4.8	5.4	-	MHz
Differential Gain (Notes 2, 6)	+25°C	-	0.04	-	%
Differential Phase (Notes 2, 6)	+25°C	-	0.04	-	Degrees
Harmonic Distortion (Notes 6, 12, 13)	+25°C	-	-74	-	dBc

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified. **(Continued)**

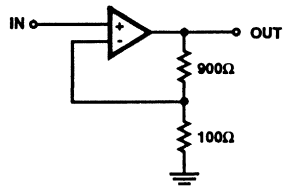
PARAMETER	TEMPERATURE	HA-2850-5, -9			UNITS
		MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 8)					
Rise Time	+25°C	-	5	-	ns
Overshoot	+25°C	-	25	-	%
Slew Rate (Notes 3, 10, 13)	+25°C	300	340	-	V/µs
Settling Time: 10V Step to 0.1%	+25°C	-	200	-	ns
POWER REQUIREMENTS					
Supply Current (Note 13)	Full	-	7.5	8.0	mA
Power Supply Rejection Ratio (Notes 9, 13)	Full	75	90	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Differential gain and phase are measured with a VM700A video tester, using a NTC-7 composite VITS.
3. $R_L = 1k\Omega$, $V_O = \pm10V$, 0V to $\pm10V$ for slew rate.
4. $V_{CM} = \pm10V$.
5. $V_O = 90mV$.
6. $A_V = +10$.
7. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $(V_{PEAK} = 10V)$.
8. Refer to Test Circuit section of data sheet.
9. $V_{SUPPLY} = \pm10VDC$ to $\pm20VDC$.
10. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
11. $A_V = +100$.
12. $V_O = 2V_{P-P}$, f = 1MHz
13. See "Typical Performance Curves" for more information.

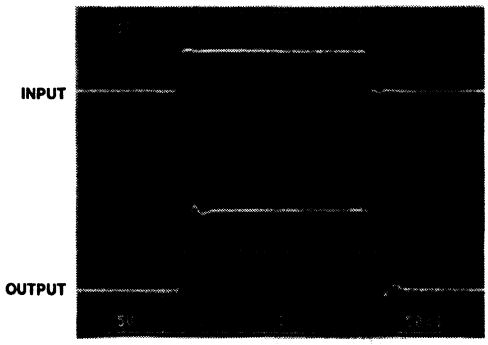
Test Circuit

TEST CIRCUIT

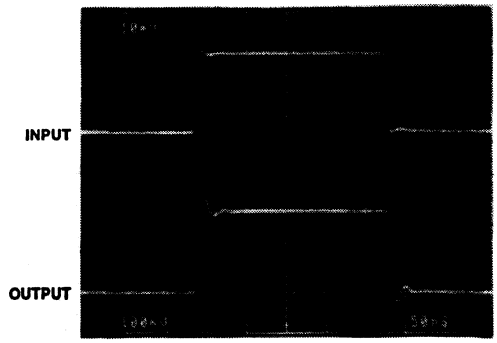


NOTE:
$V_S = \pm 15V$
$A_V = +10$
$C_L < 10pF$

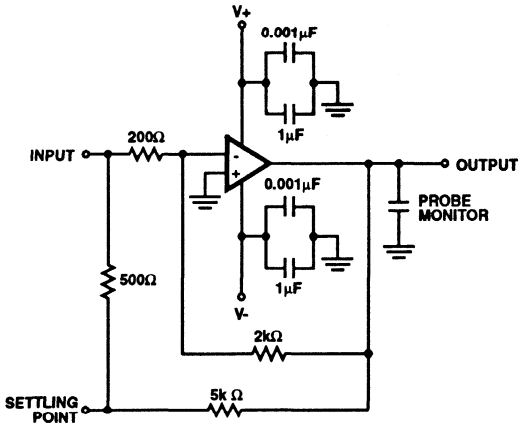
LARGE SIGNAL RESPONSE
Input = 1V/Div.
Output = 5V/Div.
50ns/Div.



SMALL SIGNAL RESPONSE
Input = 10mV/Div.
Output = 100mV/Div.
50ns/Div.



SETTLING TIME TEST CIRCUIT



- $A_V = -10$
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- SETTLING POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

Die Characteristics

DIE DIMENSIONS:
65 x 52 x 19 ± 1mils
(1650 x 1310 x 483µm)

METALLIZATION:
Type: Aluminum, 1% Copper
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride thickness: 3.5kÅ ± 1kÅ

DIE ATTACH:
Material: Epoxy-Plastic DIP and SOIC
Gold Eutectic-Ceramic DIP

WORST CASE CURRENT DENSITY:
0.7×10^5 A/cm^2 at 1.8mA

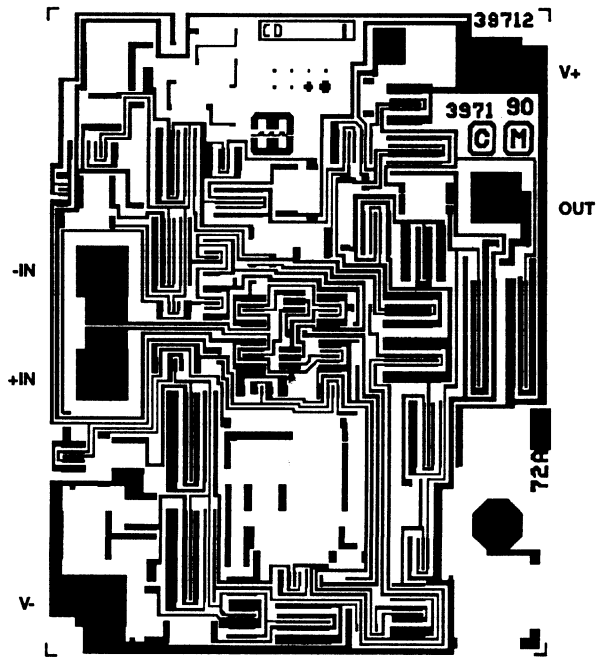
SUBSTRATE POTENTIAL (POWERED UP): V-

TRANSISTOR COUNT: 34

PROCESS: High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2850



Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified

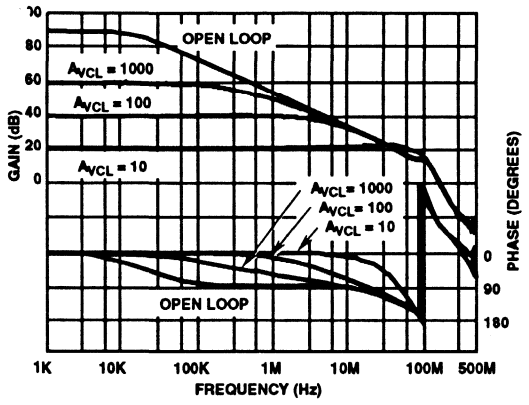


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS GAINS

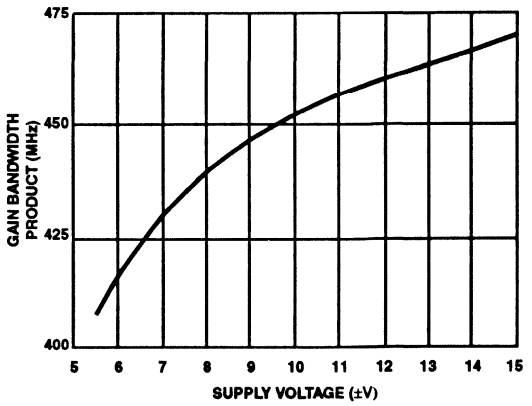


FIGURE 2. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

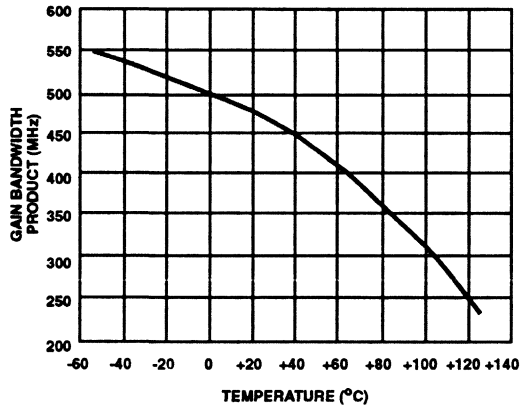


FIGURE 3. GAIN BANDWIDTH PRODUCT vs TEMPERATURE

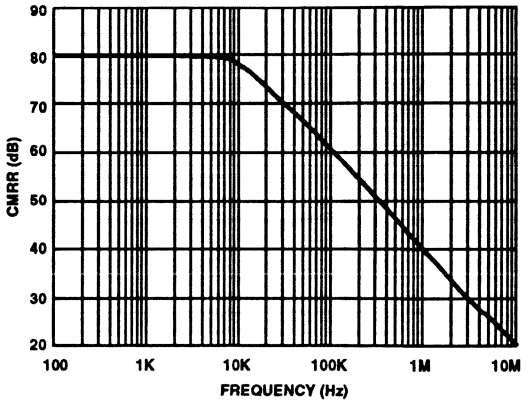


FIGURE 4. CMRR vs FREQUENCY

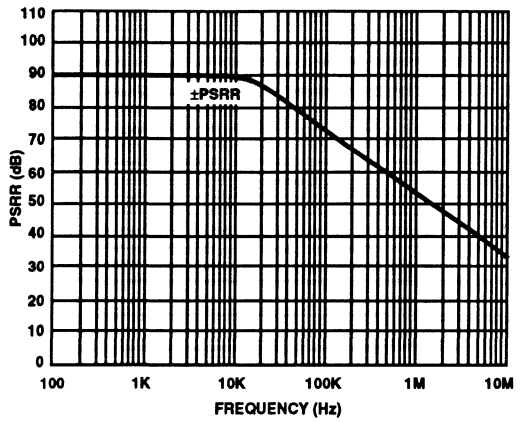


FIGURE 5. PSRR vs FREQUENCY

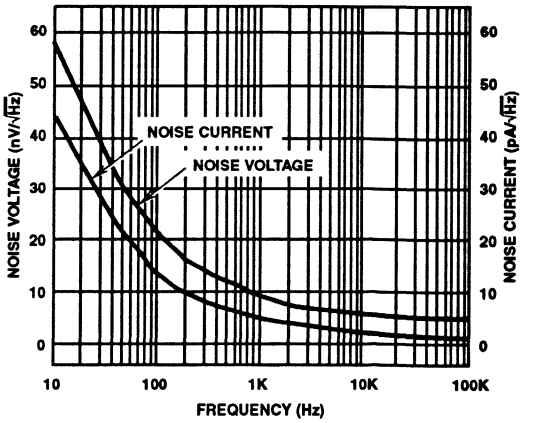


FIGURE 6. INPUT NOISE vs FREQUENCY

Typical Performance Curves T_A = +25°C, V_{SUPPLY} = ±15V, R_L = 1kΩ, C_L < 10pF, Unless Otherwise Specified (Continued)

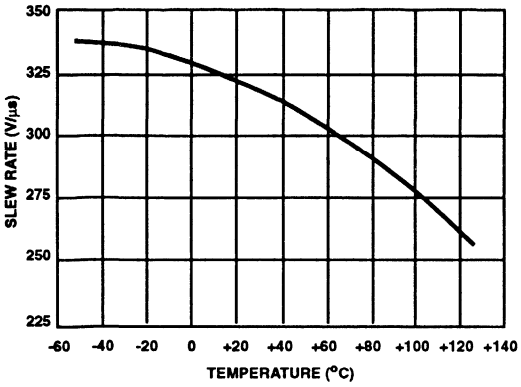


FIGURE 7. SLEW RATE vs TEMPERATURE

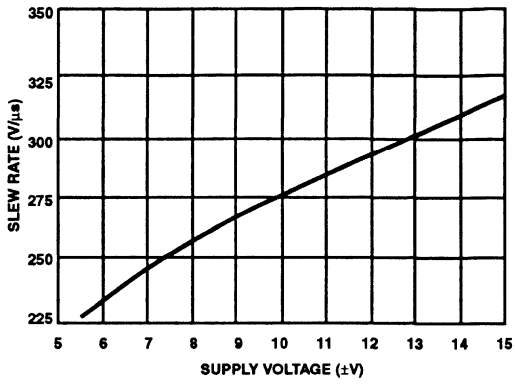


FIGURE 8. SLEW RATE vs SUPPLY VOLTAGE

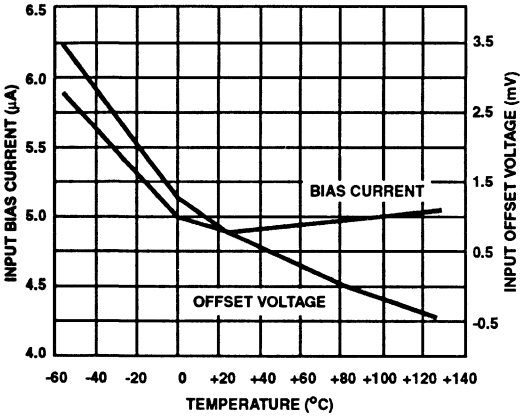


FIGURE 9. INPUT OFFSET VOLTAGE AND INPUT BIAS CURRENT vs TEMPERATURE

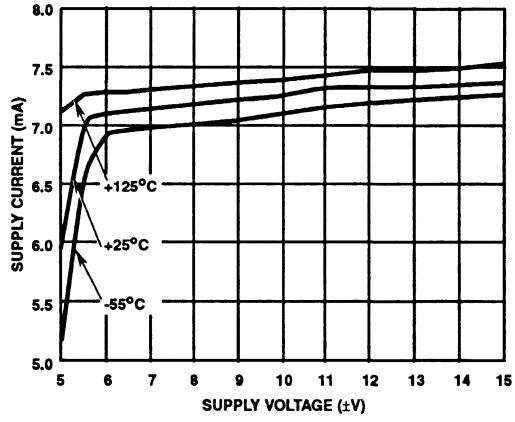


FIGURE 10. SUPPLY CURRENT vs SUPPLY VOLTAGE

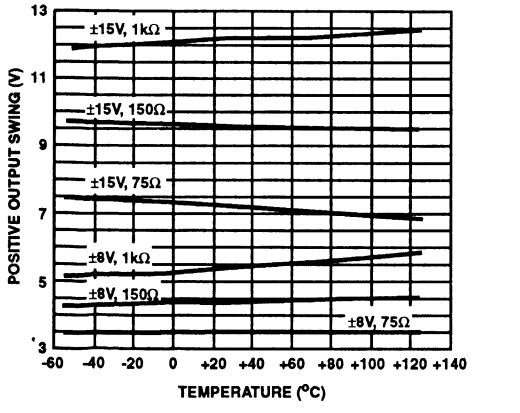


FIGURE 11. POSITIVE OUTPUT SWING vs TEMPERATURE

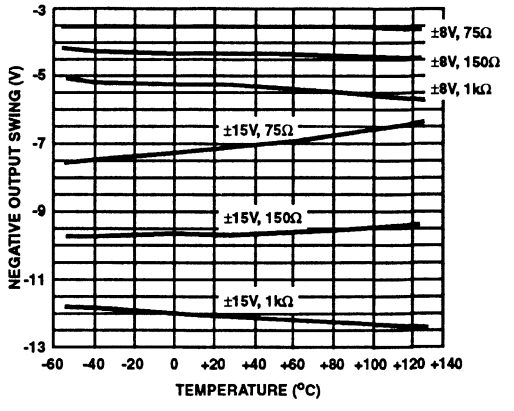


FIGURE 12. NEGATIVE OUTPUT SWING vs TEMPERATURE

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified (Continued)

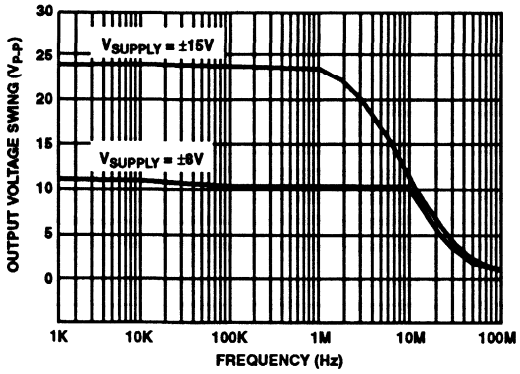


FIGURE 13. MAXIMUM UNDISTORTED OUTPUT SWING vs FREQUENCY

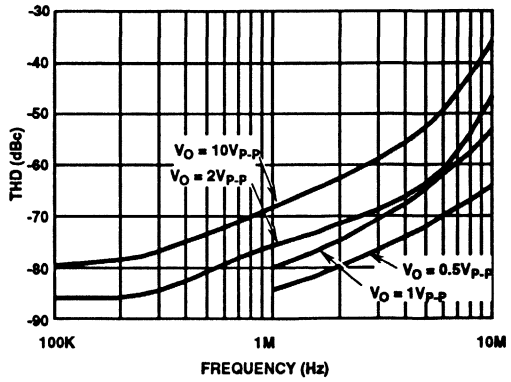


FIGURE 14. TOTAL HARMONIC DISTORTION vs FREQUENCY

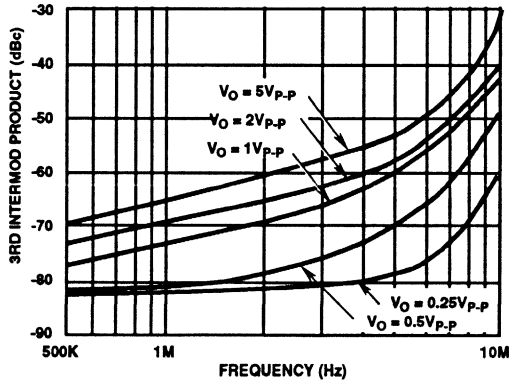


FIGURE 15. INTERMODULATION DISTORTION vs FREQUENCY (2 TONE)

HARRIS SEMICONDUCTOR

HA-4741

March 1993

Quad Operational Amplifier

Features

- Slew Rate 1.6V/μs
- Bandwidth 3.5MHz
- Input Voltage Noise ..... 9nV/√Hz
- Input Offset Voltage 0.5mV
- Input Bias Current 60nA
- Supply Range ..... ±2V to ±20V
- No Crossover Distortion
- Standard Quad Pinout

Applications

- Universal Active Filters
- D3 Communications Filters
- Audio Amplifiers
- Battery-Powered Equipment

Description

HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/√Hz at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion.

These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier -to-amplifier isolation (69dB at 10kHz).

A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

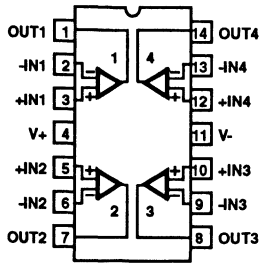
HA-4741/883 product and data sheets available upon request.

Ordering Information

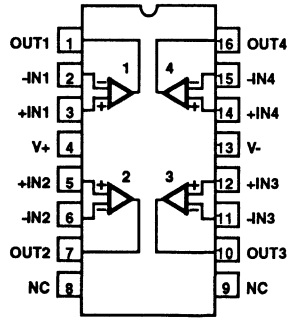
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-4741-2	-55°C to +125°C	14 Lead Ceramic DIP
HA1-4741-5	0°C to +75°C	14 Lead Ceramic DIP
HA3-4741-5	0°C to +75°C	14 Lead Plastic DIP
HA4P4741-5	0°C to +75°C	20 Lead PLCC
HA9P4741-5	0°C to +75°C	16 Lead Wide Body SOIC
HA9P4741-9	-40°C to +85°C	16 Lead Wide Body SOIC

Pinouts

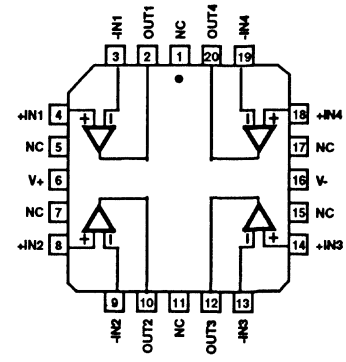
HA-4741 (PDIP, CDIP) TOP VIEW



HA-4741 (300 mil SOIC) TOP VIEW



HA-4741 (PLCC) TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2922.1**

Absolute Maximum Ratings (Note 13)

T_A = +25°C Unless Otherwise Stated

Supply Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage 30.0V
Input Voltage (Note 1) ..... ±15.0V
Output Short Circuit Duration (Note 2) ..... Indefinite
Junction Temperature (Note 3) ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range:
HA-4741-2 ..... -55°C ≤ T_A ≤ +125°C
HA-4741-5 ..... 0°C ≤ T_A ≤ +75°C
HA-4741-9 ..... -40°C ≤ T_A ≤ +85°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP Package	71	13
Plastic DIP Package	107	38
SOIC	96	26
PLCC	74	33

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified.

PARAMETER	TEMP	HA-4741-2 LIMITS			HA-4741-5 LIMITS			(NOTE 14) HA-4741-9	UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MAX	
INPUT CHARACTERISTICS									
Offset Voltage	+25°C	-	0.5	3	-	1	5	5	mV
	Full	-	4	5	-	4	6.5	8.5	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-		µV/°C
Bias Current	+25°C	-	60	200	-	60	300	300	nA
	Full	-	-	325	-	-	400	400	nA
Offset Current	+25°C	-	15	30	-	30	50	50	nA
	Full	-	-	75	-	-	100	100	nA
Common Mode Range	Full	±12	–	-	±12	–	-	-	V
Differential Input Resistance	+25°C	-	0.5	-	-	0.5	-	-	MΩ
Input Voltage Noise (f = 1kHz)	+25°C	-	9	-	-	9	-	-	nV/√Hz
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain (Note 4)	+25°C	50	100	-	25	50	-	-	kV/V
	Full	25	-	-	15	-	-	-	kV/V
Common Mode Rejection Ratio	+25°C	80	95	-	80	95	-	-	dB
	Full	74	-	-	74	-	-	-	dB
Channel Separation (Note 5)	+25°C	66	69	-	66	69	-	-	dB
Small Signal Bandwidth	+25°C	2.5	3.5	-	2.5	3.5	-		MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing (R_L = 10kΩ)	Full	±12	±13.7	-	±12	±13.7	-	-	V
Output Voltage Swing (R_L = 2kΩ)	Full	±10	±12.5	-	±10	±12.5	-	-	V
Full Power Bandwidth (Notes 4, 9)	+25°C	14	25	-	14	25	-	-	kHz
Output Current (Note 6)	Full	±5	±15	-	±5	±15	-	-	mA
Output Resistance	+25°C	-	300	-	-	300	-	-	Ω
TRANSIENT RESPONSE (Notes 7, 10)									
Rise Time (Note 11)	+25°C	-	75	140	-	75	140	140	ns
Overshoot (Note11)	+25°C	-	25	40	-	25	40	40	%
Slew Rate (Note 12)	+25°C	-	±1.6	-	-	±1.6	-	-	V/µs

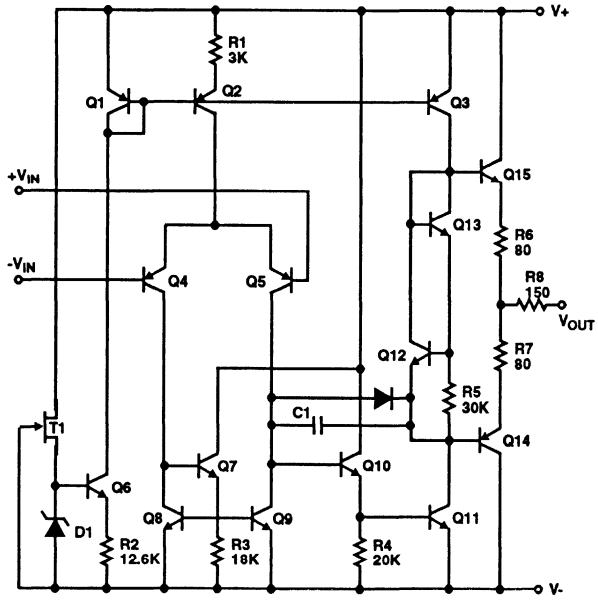
Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEMP	HA-4741-2 LIMITS			HA-4741-5 LIMITS			(NOTE 14) HA-4741-9	UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MAX	
POWER SUPPLY CHARACTERISTICS									
Supply Current	+25°C	-	4.5	5	-	5	7	7	mA
Power Supply Rejection Ratio (Note 8)	Full	80	95	-	80	95	-	-	dB

NOTES:

1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Maximum power dissipation, including output load, must be designed to maintain junction temperature below +175°C for the ceramic package, and below +150°C for the plastic packages.
4. V_{OUT} = ±10V, R_L = 2kΩ.
5. Referred to input; f = 10kHz, R_S = 1K, V_{IN} = 100mV_{PEAK}.
6. V_{OUT} = ±10V.
7. See Pulse Response Characteristics.
8. ΔV = ±5V.
9. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./2π V_{PEAK}.
10. R_L = 2kΩ, C_L = 50pF.
11. V_{OUT} = ±200mV.
12. V_{OUT} = ±5V.
13. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
14. Typical and Minimum specifications for the -9 version are the same as those for the -5 version.

Schematic Diagram



Typical Performance Curves V+ = +15V, V- = -15V, T_A = +25°C, Unless Otherwise Specified

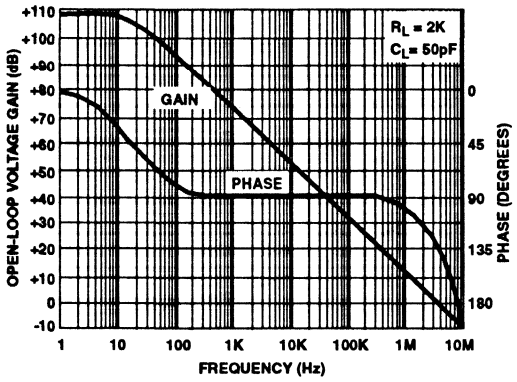


FIGURE 1. OPEN LOOP FREQUENCY RESPONSE

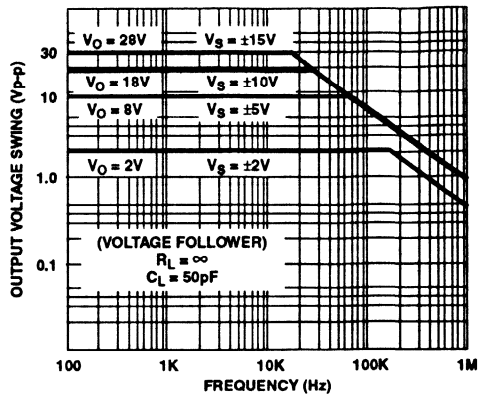


FIGURE 2. OUTPUT VOLTAGE SWING vs FREQUENCY

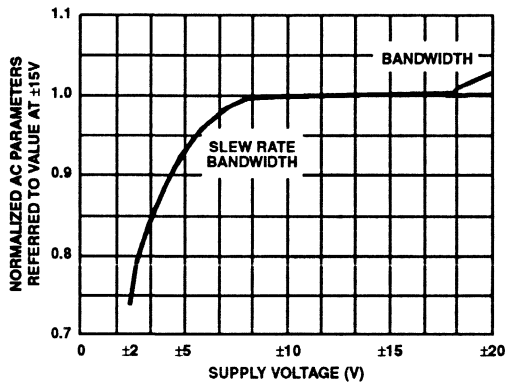


FIGURE 3. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

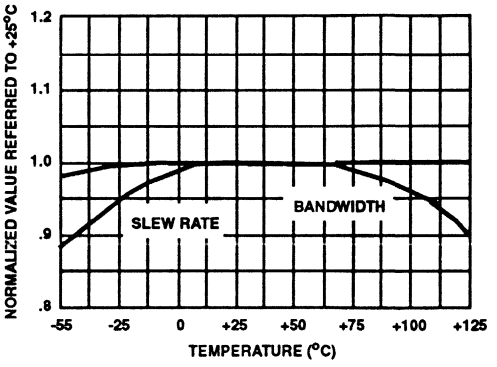


FIGURE 4. NORMALIZED AC PARAMETERS vs TEMPERATURE

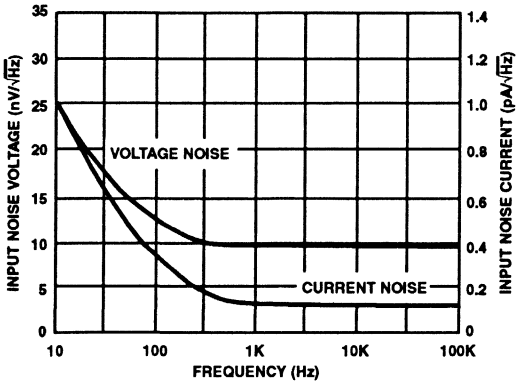


FIGURE 5. INPUT NOISE vs FREQUENCY

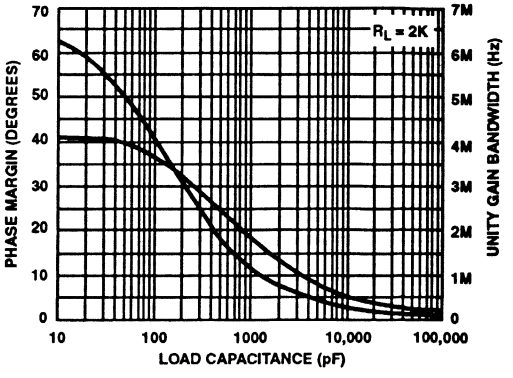


FIGURE 6. SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE

Typical Performance Curves V+ = +15V, V- = -15V, T_A = +25°C, Unless Otherwise Specified (Continued)

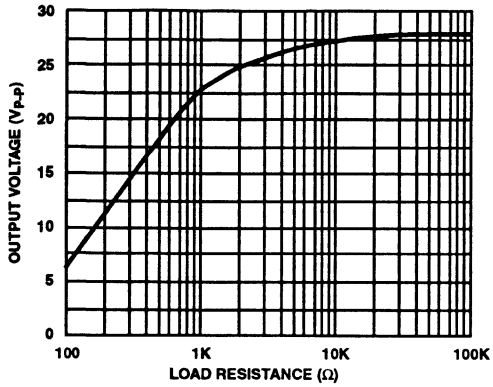


FIGURE 7. MAXIMUM OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

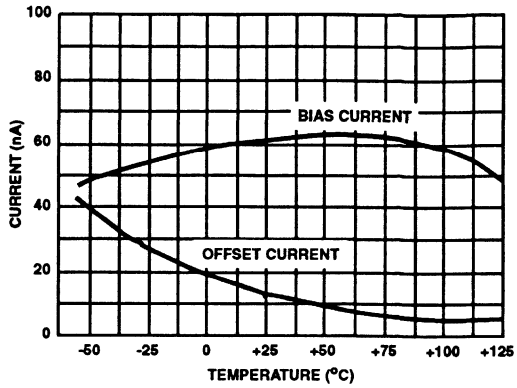


FIGURE 8. INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

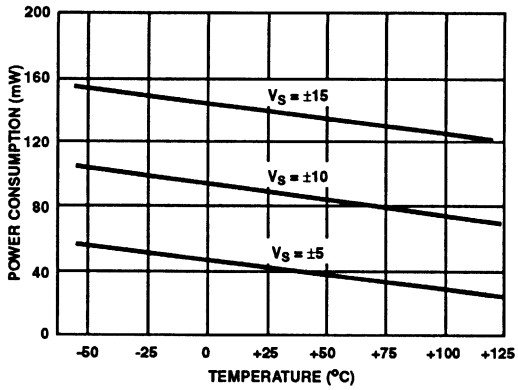


FIGURE 9. POWER CONSUMPTION vs TEMPERATURE

Pulse Response

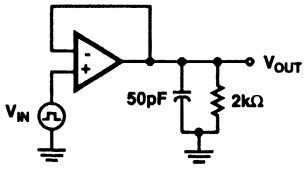


FIGURE 10. TRANSIENT RESPONSE/SLEW RATE CIRCUIT

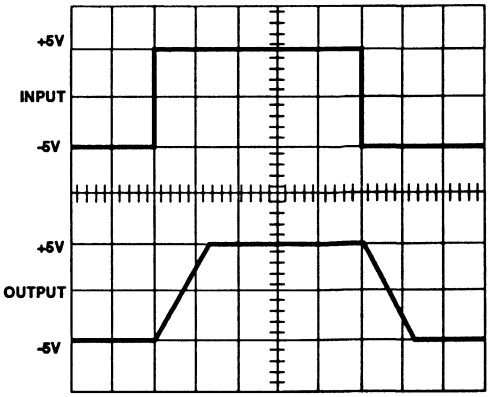


FIGURE 11. SLEW RESPONSE
(Volts: 5V/Div., Time: 5µs/Div.)

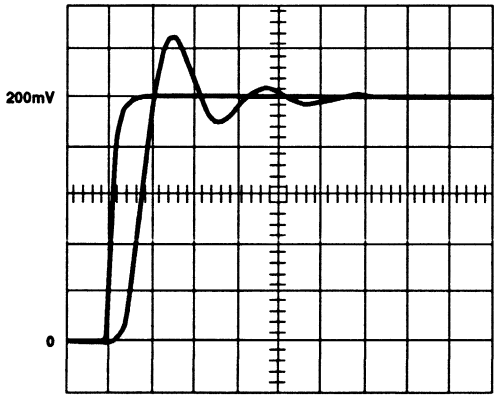


FIGURE 12. TRANSIENT RESPONSE
(Volts: 40mV/Div., Time 100ns/Div.)

HARRIS SEMICONDUCTOR

HA-5002

Monolithic, Wideband, High Slew Rate, High Output Current Buffer

March 1993

Features

- Voltage Gain 0.995
- High Input Impedance 3000kΩ
- Low Output Impedance 3Ω
- Very High Slew Rate 1300V/μs
- Very Wide Bandwidth 110MHz
- High Output Current ..... ±200mA
- Pulsed Output Current 400mA
- Monolithic Construction

Applications

- Line Driver
- Data Acquisition
- 110MHz Buffer
- High Power Current Booster
- High Power Current Source
- Sample and Holds
- Radar Cable Driver
- Video Products

Description

The HA-5002 is a monolithic, wideband, high slew rate, high output current, buffer amplifier.

Utilizing the advantages of the Harris D.I. technologies, the HA-5002 current buffer offers 1300V/μs slew rate with 110MHz of bandwidth. The ±200mA output current capability is enhanced by a 3Ω output impedance.

The monolithic HA-5002 will replace the hybrid LH0002 with corresponding performance increases. These characteristics range from the 3000kΩ input impedance to the increased output voltage swing. Monolithic design technologies have allowed a more precise buffer to be developed with more than an order of magnitude smaller gain error.

The HA-5002 will provide many present hybrid users with a higher degree of reliability and at the same time increase overall circuit performance.

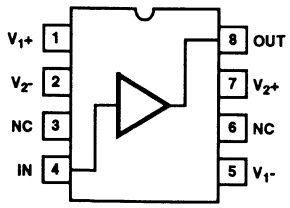
For the military grade product, refer to the HA-5002/883 datasheet.

Ordering Information

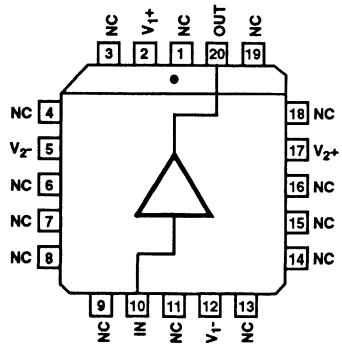
PART NUMBER	TEMP. RANGE	PACKAGE
HA2-5002-2	-55°C to +125°C	8 Pin Can
HA2-5002-5	0°C to +75°C	8 Pin Can
HA3-5002-5	0°C to +75°C	8 Lead Plastic DIP
HA4P5002-5	0°C to +75°C	20 Lead PLCC
HA7-5002-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5002-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P5002-5	0°C to +75°C	8 Lead SOIC
HA9P5002-9	-40°C to +85°C	8 Lead SOIC

Pinouts

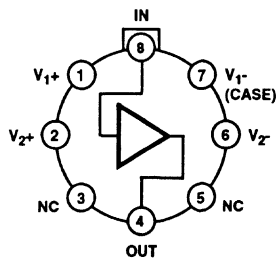
HA-5002
(PDIP, CDIP, SOIC)
TOP VIEW



HA-5002
(PLCC)
TOP VIEW



HA-5002
(TO-99 CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2921.1**

Specifications HA-5002

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 44V
Input Voltage ..... V_1+ to V_1-
Output Current (Continuous) ..... ±200mA
Output Current (50ms On, 1s Off) ..... ±400mA
Internal Power Dissipation (Note 2)
TO-99 (+25°C) 1.39W
Ceramic DIP (+25°C) 1.32W
Plastic DIP (+25°C) 1.36W
SOIC (+25°C) 0.80W
PLCC (+25°C) 1.69W
Maximum Junction Temperature ..... +175°C
Maximum Junction Temperature (Note 2)
Plastic Packages ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-5002-2 ..... -55°C ≤ T_A ≤ +125°C
HA-5002-5 ..... 0°C ≤ T_A ≤ +75°C
HA-5002-9 ..... -40°C ≤ T_A ≤ +85°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{SUPPLY} = ±12V to ±15V, R_S = 50Ω, R_L = 1kΩ, C_L = 10pF, Unless Otherwise Specified.

PARAMETER		TEMP	HA-5002-2 MIN	HA-5002-2 TYP	HA-5002-2 MAX	HA-5002-5, -9 MIN	HA-5002-5, -9 TYP	HA-5002-5, -9 MAX	UNITS
INPUT CHARACTERISTICS									
Offset Voltage		+25°C	-	5	20	-	5	20	mV
		Full	-	10	30	-	10	30	mV
Average Offset Voltage Drift		Full	-	30	-	-	30	-	µV/°C
Bias Current		+25°C	-	2	7	-	2	7	µA
		Full	-	3.4	10	-	2.4	10	µA
Input Resistance		Full	1.5	3	-	1.5	3	-	MΩ
Input Noise Voltage (10Hz-1MHz)		+25°C	-	4	-	-	4	-	μV_{P-P}
TRANSFER CHARACTERISTICS									
Voltage Gain (Note 7)	R_L = 50Ω	+25°C	-	0.900	-	-	0.900	-	V/V
	R_L = 100Ω	+25°C	-	0.971	-	-	0.971	-	V/V
	R_L = 1kΩ	+25°C	-	0.995	-	-	0.995	-	V/V
	R_L = 1kΩ	Full	0.980	-	-	0.980	-	-	V/V
-3dB Bandwidth (Note 4)		+25°C	-	110	-	-	110	-	MHz
AC Current Gain		+25°C	-	40	-	-	40	-	A/mA
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 100Ω	+25°C	±10	±10.7	-	±10	±11.2	-	V
	R_L = 1kΩ (Note 3)	Full	±10	±13.5	-	±10	±13.9	-	V
	R_L = 1kΩ (Note 5)	Full	±10	±10.5	-	±10	±10.5	-	V
Output Current (Note 10)		+25°C	-	220	-	-	220	-	mA
Output Resistance		Full	-	3	10	-	3	10	Ω
Harmonic Distortion (Note 6)		+25°C	-	<0.005	-	-	<0.005	-	%
TRANSIENT RESPONSE									
Full Power Bandwidth (Note 8)		+25°C	-	41	-	-	41	-	MHz
Rise Time		+25°C	-	3.6	-	-	3.6	-	ns
Propagation Delay		+25°C	-	2	-	-	2	-	ns
Overshoot		+25°C	-	30	-	-	30	-	%
Slew Rate		+25°C	1.0	1.3	-	1.0	1.3	-	V/ns
Settling Time to 0.1%		+25°C	-	50	-	-	50	-	ns

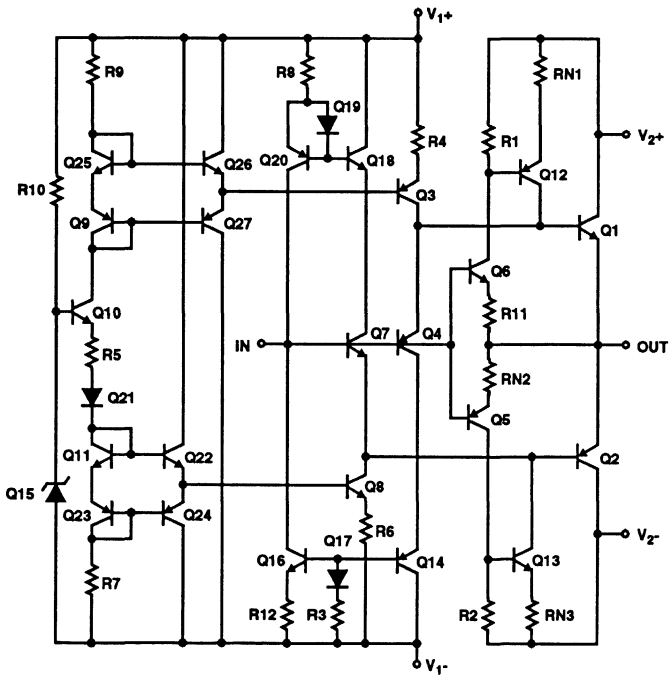
Electrical Specifications V_{SUPPLY} = ±12V to ±15V, R_S = 50Ω, R_L = 1kΩ, C_L = 10pF, Unless Otherwise Specified. **(Continued)**

PARAMETER		TEMP	HA-5002-2 MIN	HA-5002-2 TYP	HA-5002-2 MAX	HA-5002-5, -9 MIN	HA-5002-5, -9 TYP	HA-5002-5, -9 MAX	UNITS
Differential Gain	R_L = 500Ω	+25°C	-	0.06	-	-	0.06	-	%
Differential Phase	R_L = 500Ω	+25°C	-	0.22	-	-	0.22	-	Degrees
POWER REQUIREMENTS									
Supply Current		+25°C	-	8.3	-	-	8.3	-	mA
		Full	-	-	10	-	-	10	mA
Power Supply Rejection Ratio (Note 9)		Full	54	64	-	54	64	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. See thermal constants data in Die Characteristics section. Maximum power dissipation, including load conditions, must be designed to maintain the maximum junction temperature below +175°C for the ceramic and can packages, and below +150°C for the plastic packages.
3. V_{SUPPLY} = ±15V
4. V_{IN} = $1V_{P-P}$
5. V_{SUPPLY} = ±12V
6. V_{IN} = $1V_{RMS}$; f = 10kHz.
7. V_{OUT} = ±10V
8. $FPBW = \frac{\text{Slew Rate}}{2\pi V_P}$; V_P = 5V
9. ΔV_{SUPPLY} = 10V
10. V_{IN} = ±10V, R_L = 40Ω.

Schematic Diagram



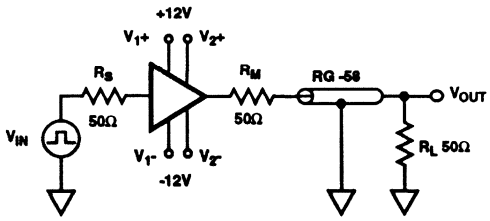
Die Characteristics

Transistor Count 27
Die Dimensions . . . . . 80 x 81 x 19 mils
(2030µm x 2050µm x 480µm)
Substrate Potential* . . . . . V_1-
Process . . . . . Bipolar-DI

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
HA7-5002 (Ceramic Mini DIP)	114	34
HA3-5002 (Plastic DIP)	92	30
HA2-5002 (Metal Can)	108	33
HA4P5002 (PLCC)	74	33
HA9P5002 (SOIC)	157	42

* The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Test Circuits



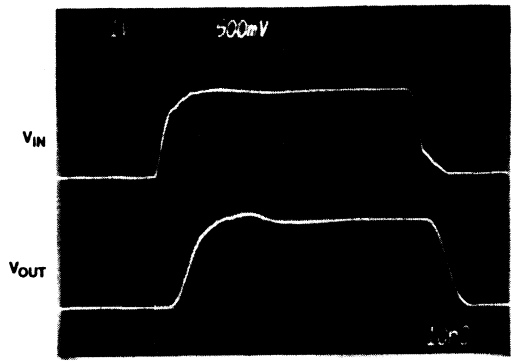


FIGURE 1. COAXIAL CABLE DRIVER - 50Ω SYSTEM

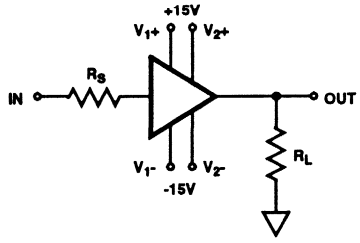
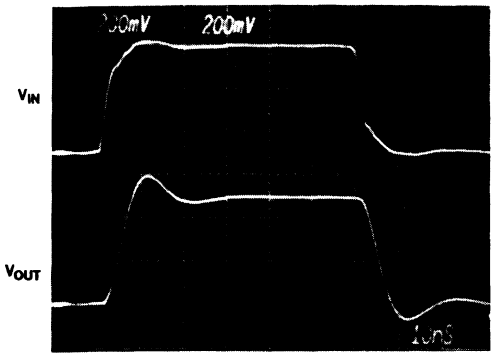


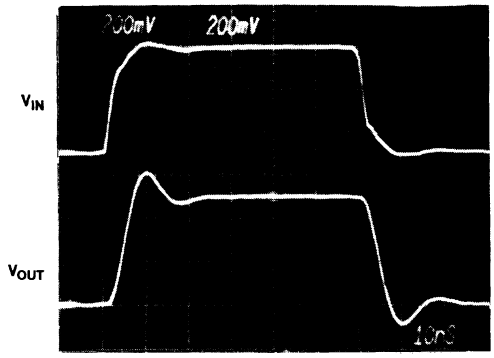
FIGURE 2. LARGE AND SMALL SIGNAL RESPONSE

Test Circuits (Continued)

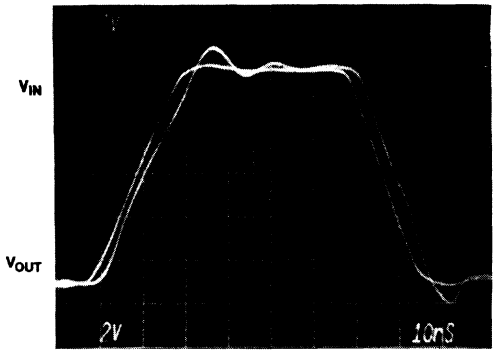
SMALL SIGNAL WAVEFORMS
$R_S = 50\Omega$, $R_L = 100\Omega$



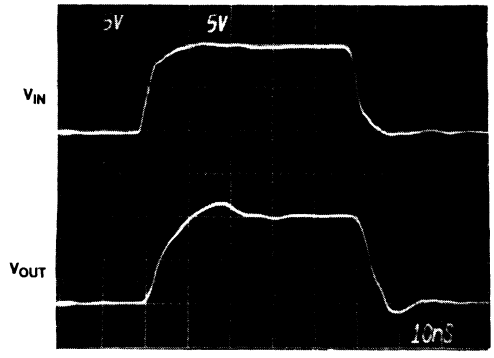
SMALL SIGNAL WAVEFORMS
$R_S = 50\Omega$, $R_L = 1k\Omega$



LARGE SIGNAL WAVEFORMS
$R_S = 50\Omega$, $R_L = 1k\Omega$



LARGE SIGNAL WAVEFORMS
$R_S = 50\Omega$, $R_L = 1k\Omega$



Typical Performance Curves

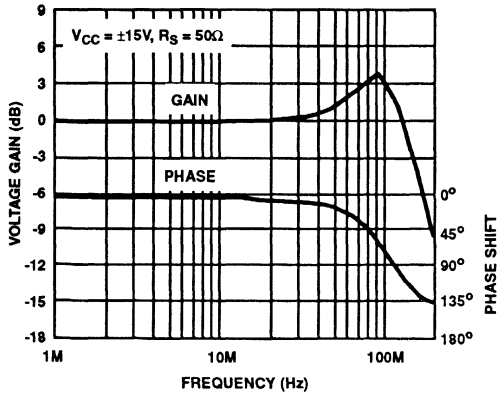


FIGURE 3. GAIN/PHASE vs FREQUENCY ($R_L = 1k\Omega$)

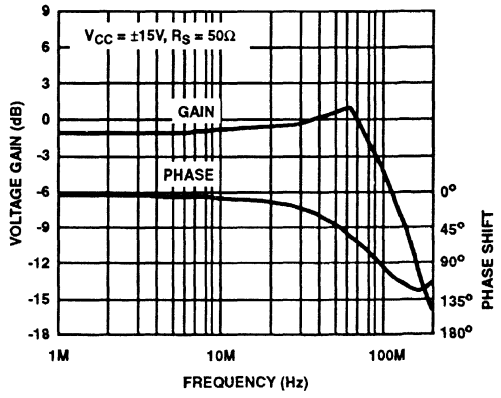


FIGURE 4. GAIN/PHASE vs FREQUENCY ($R_L = 50\Omega$)

Typical Performance Curves (Continued)

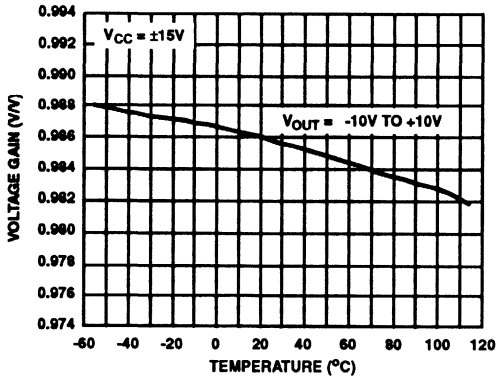


FIGURE 5. VOLTAGE GAIN vs TEMPERATURE (R_L = 100Ω)

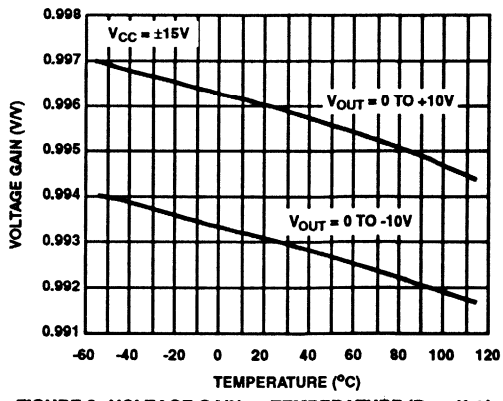


FIGURE 6. VOLTAGE GAIN vs TEMPERATURE (R_L = 1kΩ)

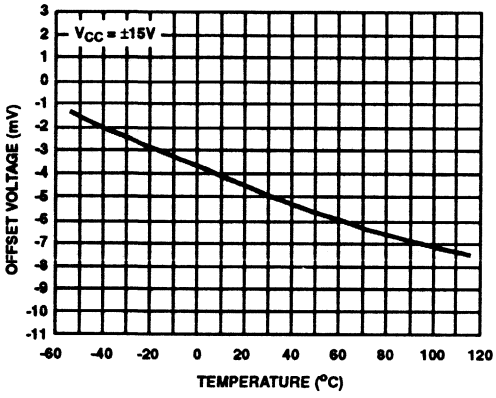


FIGURE 7. OFFSET VOLTAGE vs TEMPERATURE

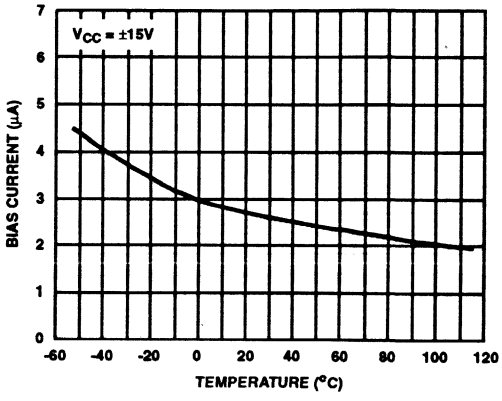


FIGURE 8. BIAS CURRENT vs TEMPERATURE

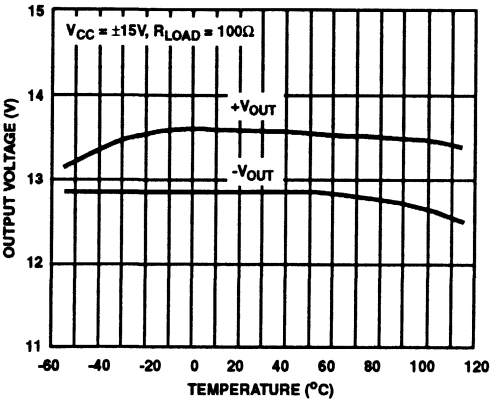


FIGURE 9. MAXIMUM OUTPUT VOLTAGE vs TEMPERATURE

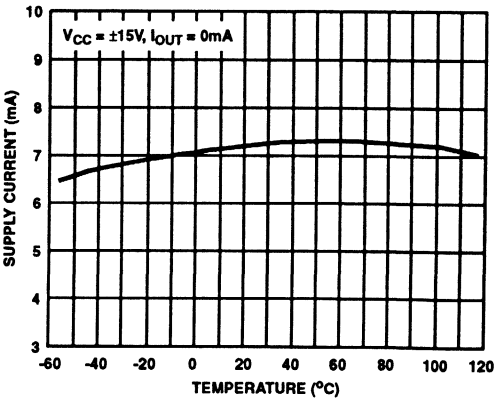


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

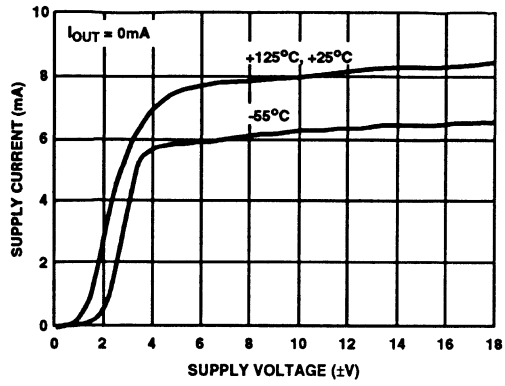


FIGURE 11. SUPPLY CURRENT vs SUPPLY VOLTAGE

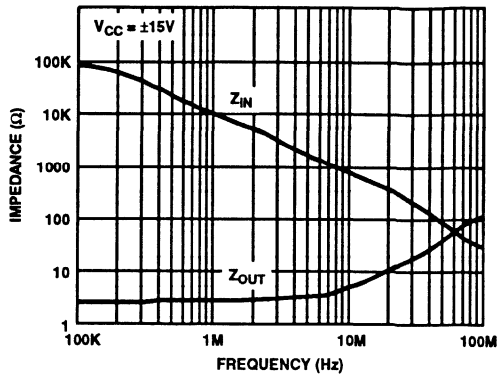


FIGURE 12. INPUT/OUTPUT IMPEDANCE vs FREQUENCY

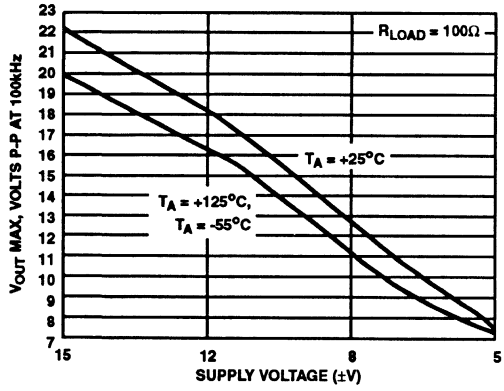


FIGURE 13. V_{OUT} MAXIMUM vs V_{SUPPLY}

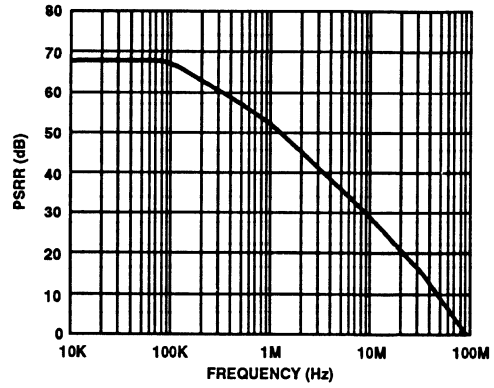


FIGURE 14. PSRR vs FREQUENCY

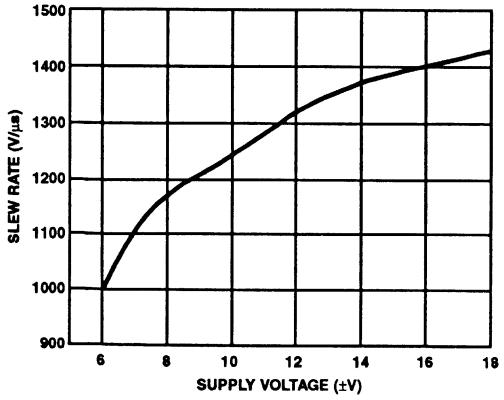


FIGURE 15. SLEW RATE vs SUPPLY VOLTAGE

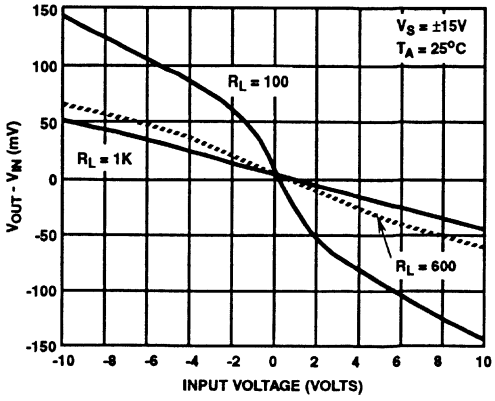


FIGURE 16. GAIN ERROR vs INPUT VOLTAGE

Operating Instructions

Layout Considerations

The wide bandwidth of the HA-5002 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

Power Supply Decoupling

For optimal device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1µF will minimize high frequency variations in supply voltage, while low frequency bypassing requires larger valued capacitors since the impedance of the capacitor is dependent on frequency.

It is also recommended that the bypass capacitors be connected close to the HA-5002 (preferably directly to the supply pins).

Typical Applications

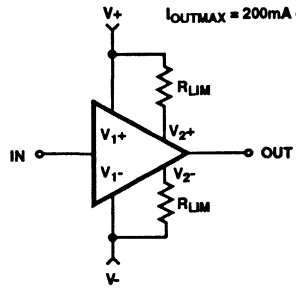
Operation at Reduced Supply Levels

The HA-5002 can operate at supply voltage levels as low as ±5V and lower. Output swing is directly affected as well as slight reductions in slew rate and bandwidth.

Short Circuit Protection

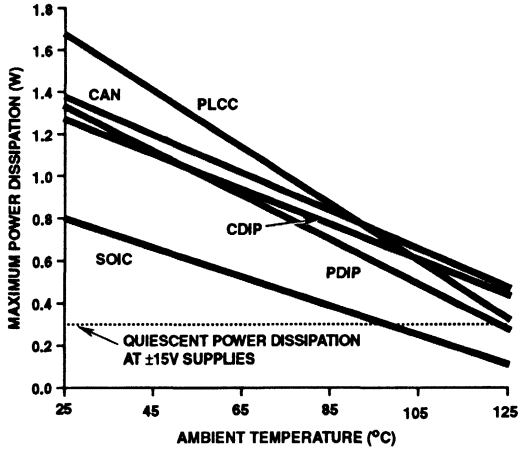
The output current can be limited by using the following circuit:

$$R_{LIM} = \frac{V+}{I_{OUTMAX}} = \frac{V-}{I_{OUTMAX}}$$



Capacitive Loading

The HA-5002 will drive large capacitive loads without oscillation but peak current limits should not be exceeded. Following the formula $I = C^{dv}/_{dt}$ implies that the slew rate or the capacitive load must be controlled to keep peak current below the maximum or use the current limiting approach as shown. The HA-5002 can become unstable with small capacitive loads (50pF) if certain precautions are not taken. Stability is enhanced by any one of the following: a source resistance in series with the input of 50Ω to 1kΩ; increasing capacitive load to 150pF or greater; decreasing C_{LOAD} to 20pF or less; adding an output resistor of 10Ω to 50Ω; or adding feedback capacitance of 50pF or greater. Adding source resistance generally yields the best results.



$$P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

Where: T_{jmax} = Maximum Junction Temperature of the Device

T_A = Ambient

θ_{JC} = Junction to Case Thermal Resistance

θ_{CS} = Case to Heat Sink Thermal Resistance

θ_{SA} = Heat Sink to Ambient Thermal Resistance

Graph is based on: $P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}}$

FIGURE 17. FREE AIR POWER DISSIPATION

HARRIS SEMICONDUCTOR

HA-5004

March 1993

100MHz Current Feedback Amplifier

Features

- Slew Rate 1200V/µs
- Output Current ..... ±100mA
- Drives ..... ±9V into 100Ω
- V_{SUPPLY} ..... ±5V to ±18V
- Thermal Overload Protection and Output Flag
- Bandwidth Nearly Independent of Gain
- Output Enable/Disable

Applications

- Unity Gain Video/Wideband Buffer
- Video Gain Block
- High Speed Peak Detector
- Fiber Optic Transmitters
- Zero Insertion Loss Transmission Line Drivers
- Current to Voltage Converter
- Radar Systems

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HA1-5004-5	-40°C to +85°C	14 Lead Ceramic DIP
HA1-5004-9	-40°C to +85°C	14 Lead Ceramic DIP
HA3-5004-5	0°C to +75°C	14 Lead Plastic DIP
HA9P5004-5	0°C to +75°C	14 Lead SOIC

Description

The HA-5004 current feedback amplifier is a video/wideband amplifier optimized for low gain applications. The design is based on current-mode feedback which allows the amplifier to achieve higher closed loop bandwidth than voltage-mode feedback operational amplifiers. Since feedback is employed, the HA-5004 can offer better gain accuracy and lower distortion than open loop buffers. Unlike conventional op amps, the bandwidth and rise time of the HA-5004 are nearly independent of closed loop gain. The 100MHz bandwidth at unity gain reduces to only 65MHz at a gain of 10. The HA-5004 may be used in place of a conventional op amp with a significant improvement in speed power product.

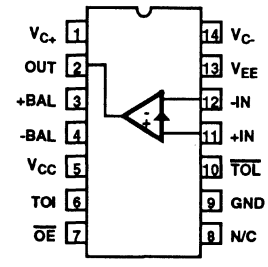
Several features have been designed in for added value. A thermal overload feature protects the part against excessive junction temperature by shutting down the output. If this feature is not needed, it can be inhibited via a TTL input (TOI). A TTL chip enable/disable ($\overline{OE}$) is also provided; when the chip is disabled its output is high impedance. Finally, an open collector output flag ($\overline{TOL}$) is provided to indicate the status of the chip. The status flag goes low to indicate when the chip is disabled due to either the internal Thermal Overload shutdown or the external disable.

In order to maximize bandwidth and output drive capacity, internal current limiting is not provided. However, current limiting may be applied via the V_C+ and V_C- pins which provide power separately to the output stage.

For Military grade product refer to the HA-5004/883 data sheet.

Pinout

HA-5004
(PDIP, CDIP, SOIC)
TOP VIEW



INPUTS		TEMP	$\overline{TOL}$ OUTPUT (OPEN COLLECTOR)	OPERATION
$\overline{OE}$	TOI	T_J		
0	0	Normal	1	Normal
0	0	High*	0	Auto Shutdown, Hi-Z OUT
0	1	X	1	Normal
1	X	X	0	Manual Shutdown, Hi-Z OUT

* > 180°C Typical

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2923.1**

Absolute Maximum Ratings (Note 1)

Supply Voltage (Between V+ and V- Terminals) 40V
Differential Input Voltage 5V
DC Input Voltage ..... $\pm V_{SUPPLY}$
Output Current ..... ±120mA Max (≤25% Duty Cycle)
Junction Temperature (Note 10) ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-5004-9 ..... $-40°C \le T_A \le +85°C$
HA-5004-5 ..... $0°C \le T_A \le +75°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V_{CC} = V_{C+} = +15V$, $V_{EE} = V_{C-} = -15V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $A_V = +1$, $R_F = 250\Omega$, $\overline{OE} = 0.8V$, TOI = 0.8V or 2.0V, Unless Otherwise Specified

PARAMETER		TEMP	HA-5004-5, -9 LIMITS MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Offset Voltage		+25°C	-	1	5	mV
		Full	-	-	20	mV
Average Offset Voltage Drift		Full	-	10	-	µV/°C
Bias Current (+Input Only) (Note 2)		+25°C	-	2	5	µA
		Full	-	-	20	µA
Input Resistance (-Input)		+25°C	-	6.5	-	Ω
Input Resistance (+Input)		+25°C	-	3	-	MΩ
Input Capacitance		+25°C	-	3	-	pF
Common Mode Range		Full	±10	-	-	V
DISTORTION AND NOISE						
Total Harmonic Distortion $2V_{P-P}$, 200kHz	$A_{VCL} = +1$	+25°C	-	-72	-	dBc
	$A_{VCL} = +2$	+25°C	-	-70	-	dBc
	$A_{VCL} = +5$	+25°C	-	-68	-	dBc
Input Noise Voltage 10Hz to 1MHz		+25°C	-	15	-	μV_{P-P}
Input Noise Voltage Density (Note 3)	$f_O = 10kHz$	+25°C	-	2.2	-	$nV/\sqrt{Hz}$
	$f_O = 100kHz$	+25°C	-	2.2	-	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 3)	$f_O = 10kHz$	+25°C	-	6	-	$pA/\sqrt{Hz}$
	$f_O = 100kHz$	+25°C	-	4	-	$pA/\sqrt{Hz}$
DIGITAL I/O CHARACTERISTICS						
Logic Inputs (OE and TO)	V_{IH}	Full	2.0	-	-	V
	V_{IL}	Full	-	-	0.8	V
	I_{IH} at $V_I = 2.4V$	Full	-	-	1	µA
	I_{IH} at $V_I = 0.4V$	Full	-	-	10	µA
Logic Output (TOL) (Open Collector)	V_{OL} at 800µA	Full	-	0.05	0.4	V

Electrical Specifications $V_{CC} = V_{C+} = +15V$, $V_{EE} = V_{C-} = -15V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $A_V = +1$, $R_F = 250\Omega$, $\overline{OE} = 0.8V$, TOI = 0.8V or 2.0V, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMP	HA-5004-5, -9 LIMITS MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS						
DC Gain Error (Note 4)	Small Signal (±100mV)	+25°C	-	0.25	0.43	%
		Full	-	0.25	0.75	%
	Large Signal (±10V) (R_L = 1K)	+25°C	-	0.25	0.43	%
		Full	-	0.25	0.75	%
DC Voltage Gain (Small and Large Signal)		+25°C	233	400	-	V/V
		Full	133	400	-	V/V
DC Transimpedance (Note 5)		+25°C	-	100	-	V/mA
		Full	33	100	-	V/mA
-3dB Bandwidth A_V = +1 (Note 6)		+25°C	-	100	-	MHz
Gain Flatness	DC to 5MHz	+25°C	-	0.03	-	dB
	DC to 10MHz	+25°C	-	0.05	-	dB
Differential Gain (Notes 6, 7, 8) 3.58MHz	A_{VCL} = +1	+25°C	-	0.035	-	%
	A_{VCL} = +2	+25°C	-	0.058	-	%
Differential Gain (Notes 6, 7, 8) 4.43MHz	A_{VCL} = +1	+25°C	-	0.035	-	%
	A_{VCL} = +2	+25°C	-	0.058	-	%
Differential Phase (Notes 6, 7) 3.58MHz	A_{VCL} = +1	+25°C	-	0.15	-	Degrees
	A_{VCL} = +2	+25°C	-	0.23	-	Degrees
Differential Phase (Notes 6, 7) 4.43MHz	A_{VCL} = +1	+25°C	-	0.17	-	Degrees
	A_{VCL} = +2	+25°C	-	0.24	-	Degrees
Common Mode Rejection Ratio (Note 9)		Full	-	58	-	dB
Minimum Stable Gain		Full	1	-	-	V/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 100Ω	+25°C	±9.0	±9.5	-	V
	R_L = 1kΩ	+25°C	±11.5	±11.8	-	V
	R_L = 100Ω	Full	±8.0	±9.5	-	V
	R_L = 1kΩ	Full	±10.5	±11.8	-	V
Full Power Bandwidth (A_V = +1) ($V_{OUT} = 4V_{P-P}$)		+25°C	-	50	-	MHz
Output Resistance, Open Loop		+25°C	-	5	-	Ω
Output Current		+25°C	±90	±100	-	mA
		Full	±80	±100	-	mA
Output Enable Time (Hi Z to ±2V)		Full	-	100	-	ns
Output Disable Time (±2V to Hi Z)		Full	-	3	-	µs
Output Leakage (Disabled)		Full	-	-	1	µA

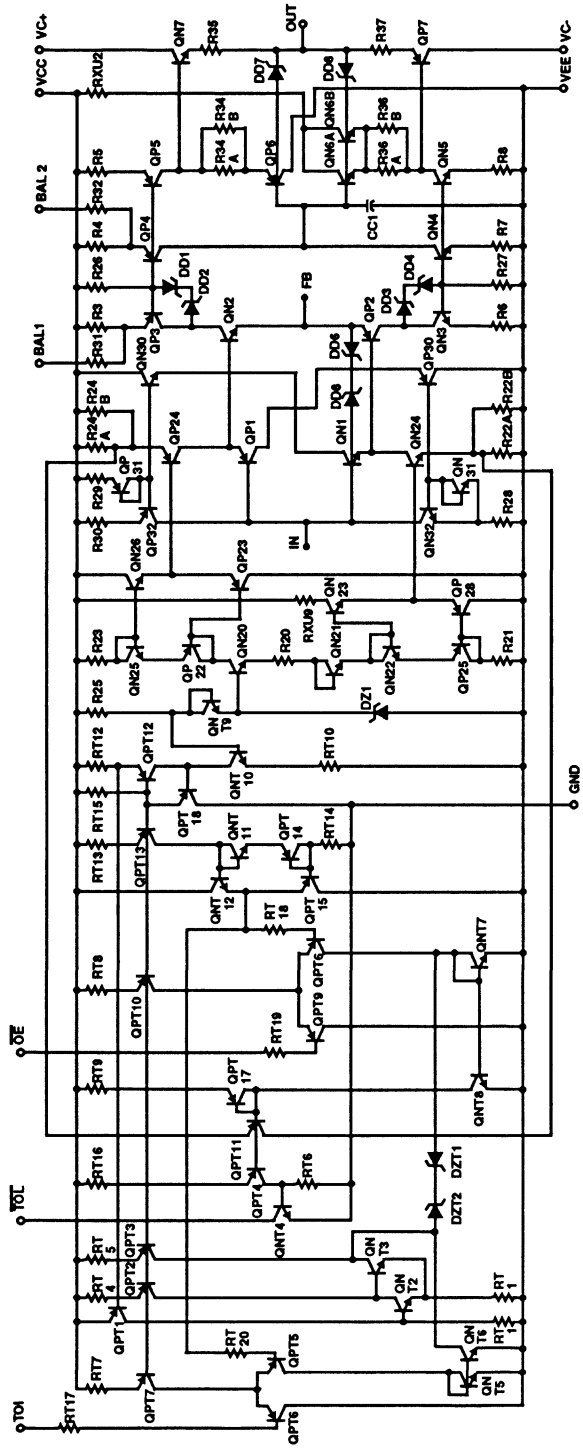
Electrical Specifications $V_{CC} = V_{C+} = +15V$, $V_{EE} = V_{C-} = -15V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $A_V = +1$, $R_F = 250\Omega$, $\overline{OE} = 0.8V$, TOI = 0.8V or 2.0V, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMP	HA-5004-5, -9 LIMITS MIN	TYP	MAX	UNITS
TRANSIENT RESPONSE						
Rise Time/Fall Time (200mV Step)		+25°C	-	6.3	-	ns
Propagation Delay (10V Step)		+25°C	-	7	-	ns
Slew Rate (10V Step)		+25°C	-	1200	-	V/µs
Settling Time (0.1%, 10V Step)		+25°C	-	50	-	ns
Overshoot		+25°C	-	10	-	%
POWER SUPPLY CHARACTERISTICS						
Supply Current	(Enabled)	+25°C	-	12	16	mA
		Full	-	-	22	mA
	(Disabled)	+25°C	-	7	-	mA
Power Supply Rejection Ratio		Full	50	60	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be imparied. Functional operation under any of these conditions is not necessarily implied.
2. The inverting input is a low impedance point; Bias Current and Offset Current, are not specified for this terminal.
3. See typical performance curves.
4. Gain Error $= \frac{1}{\text{DC Voltage Gain}} \times 100\%$
5. DC Transimpedance $= \frac{R_F}{\text{Gain Error}}$, $R_F = 250\,\Omega$
6. $V_{IN} = 300mV_{P-P}$
7. $V_{OFFSET} = 1.0V$
8. Differential Gain (dB) = 0.0869 Differential Gain (%)
9. $V_{CM} = \pm 10V$
10. Maximum power dissipation, including load condition, must be designed to maintain the junction temperature below +175°C for the ceramic DIP, and below +150°C for the plastic packages. See Thermal Resistances in the "Die Characteristics" section.

Schematic Diagram



Die Characteristics

Transistor Count 64
Die Dimensions . . . . . 93 x 63 x 19mils (2370 x 1600 x 480µm)
Substrate Potential . . . . . V_{EE}
Process . . . . . Bipolar DI

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	71	14
Plastic DIP	107	38
SOIC	118	36

Typical Performance Curves

V_{SUPPLY} = ±15V, T_A = +25°C, Unless Otherwise Specified.

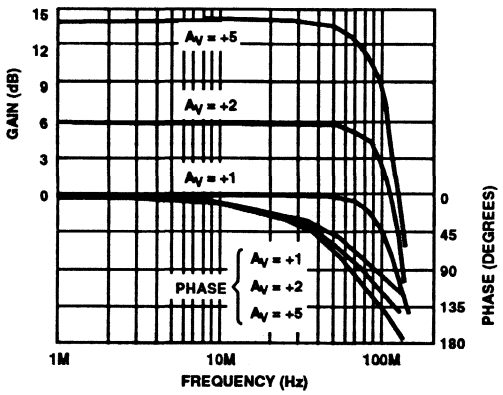


FIGURE 1. GAIN AND PHASE vs FREQUENCY

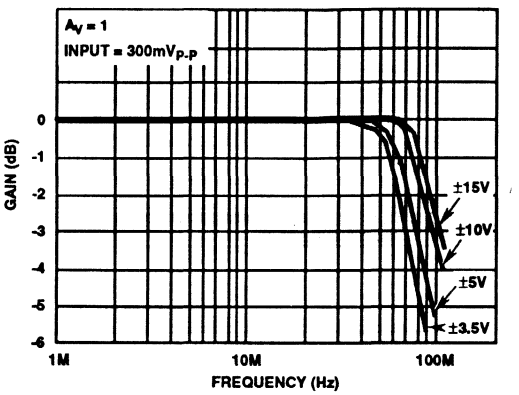


FIGURE 2. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

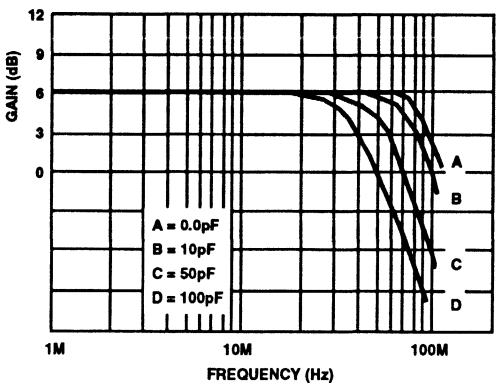


FIGURE 3. FREQUENCY RESPONSE vs C_L

V_{CC} = ±15V, A_V = +2, R_L = 1kΩ, Input = 10mV

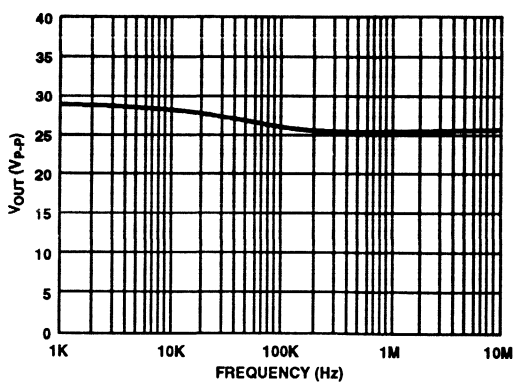


FIGURE 4. MAXIMUM UNDISTORTED SINEWAVE OUTPUT vs FREQUENCY

V_{CC} = ±15V, A_V = +1, Sinewave Input

Typical Performance Curves $V_{SUPPLY} = \pm 15V$, $T_A = +25^oC$, Unless Otherwise Specified. (Continued)

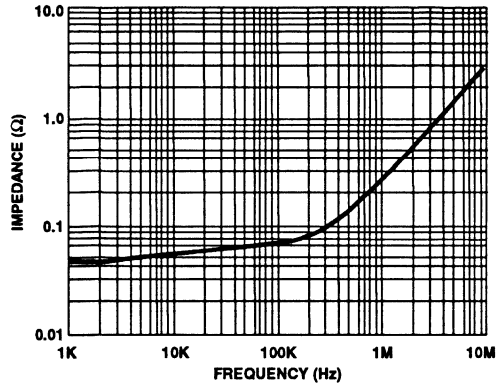


FIGURE 5. CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

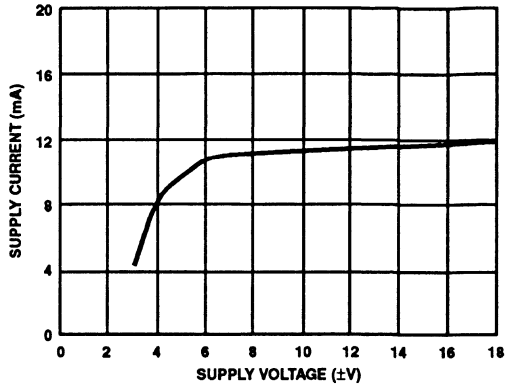


FIGURE 6. SUPPLY CURRENT vs SUPPLY VOLTAGE

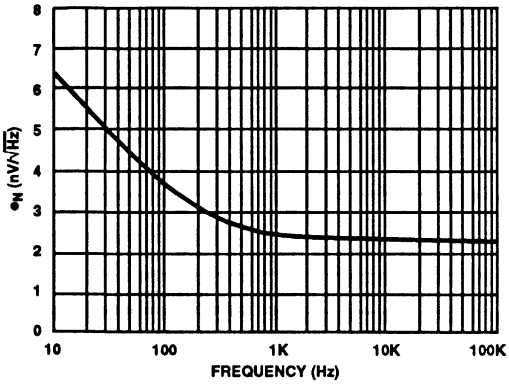


FIGURE 7. NOISE VOLTAGE vs FREQUENCY

$V_{CC} = \pm 15V$

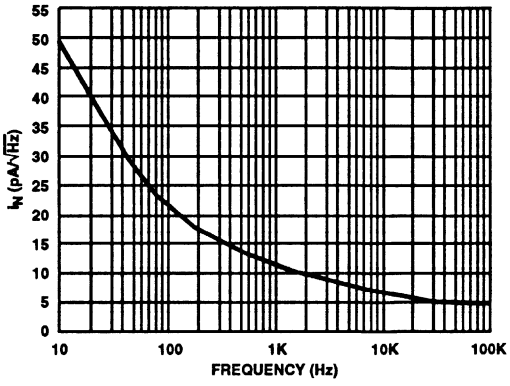
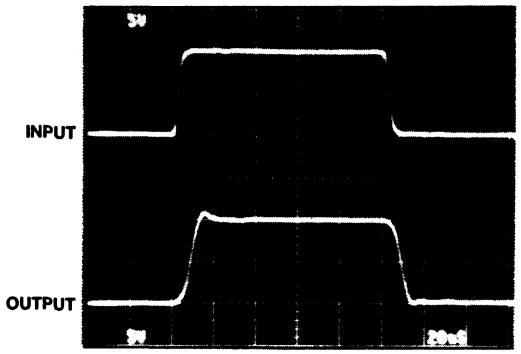


FIGURE 8. NOISE CURRENT vs FREQUENCY

$V_{CC} = \pm 15V$

Switching Waveforms

LARGE SIGNAL RESPONSE, $A_V = +1$
Vertical Scale: 5V/Div.
Horizontal Scale: 20ns/Div.



$A_V = +1$, $V_{SUPPLY} = \pm 15V$

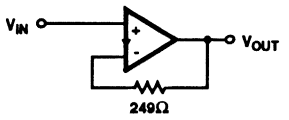
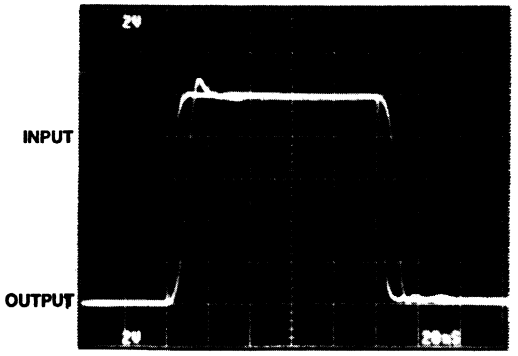


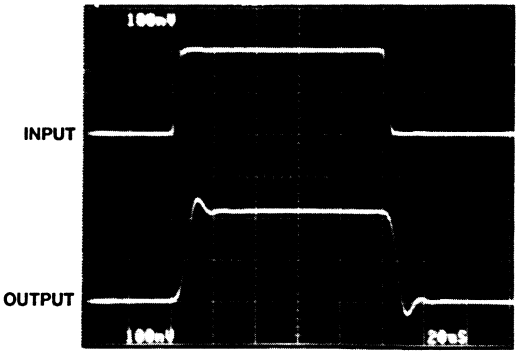
FIGURE 9. TEST CIRCUIT

PROPAGATION DELAY
Vertical Scale: 2V/Div.
Horizontal Scale: 20ns/Div.



$A_V = +1$, $V_{SUPPLY} = \pm 15V$

SMALL SIGNAL RESPONSE
Vertical Scale: 100mV/Div.
Horizontal Scale: 20ns/Div.



$A_V = +1$, $V_{SUPPLY} = \pm 15V$

Applications Information

Theory of Operation

The HA-5004 is a high performance amplifier that uses current feedback to achieve its outstanding performance. Although it is externally configured like an ordinary op amp in most applications, its internal operation is significantly different.

Inside the HA-5004, there is a unity gain buffer from the non-inverting (+) input to the inverting-input (as suggested by the circuit symbol), and the inverting terminal is a low impedance point. Error currents are sensed at the inverting input and amplified; a small change in input current produces a large change in output voltage. The ratio of output voltage delta due to input current delta is the transimpedance of the device.

Steady state current at the inverting input is very small because the transimpedance is large. The voltage across the input terminals is nearly zero due to the buffer amplifier. These two properties are similar to standard op amps and likewise simplify circuit analysis.

Resistor Selection

The HA-5004 is optimized for a feedback resistor of 250Ω, regardless of gain configuration. It is important to note that this resistor is required even for unity gain applications; higher gain settings use a second resistor like regular op amp circuits as shown in Figure 10 below.

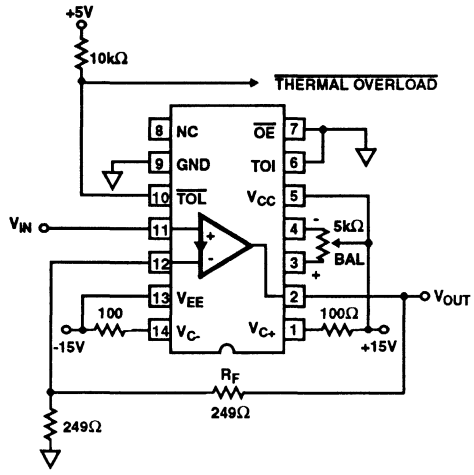


FIGURE 10. TYPICAL APPLICATION CIRCUIT, A_V = +2

Power Supplies

The HA-5004 will operate over a wide range of supply voltages with excellent performance. Supplies may be either single-ended or split, ranging from 6V (±3V) to 36V (±18V). Appropriate reduction in input and output signal excursion is necessary for operation at lower supply voltages. Bypass capacitors from each supply to ground are recommended, typically a 0.01μF ceramic in parallel with a 4.7μF electrolytic.

Current Limit

No internal current limiting is provided for the HA-5004 in order to maximize bandwidth and slew rate. However, power is supplied separately to the output stage via pins 1 (V_{C+}) and 14 (V_{C-}) so that external current limiting resistors may be used. If required, 100Ω resistors to each supply rail are recommended.

Enable/Disable and Thermal Overload Operation

The HA-5004 operates normally with a TTL low state on pin 7 ($\overline{OE}$) but it may be disabled manually by a TTL high state at this input. When disabled, the output and inverting-input go to a high impedance state and the circuit is electrically debiased, reducing supply current by about 5mA. It is important to keep the differential input voltage below the absolute maximum rating of 5V when the device is disabled.

If the power dissipation becomes excessive and chip temperature exceeds approximately 180°C, the HA-5004 will automatically disable itself. The thermal overload condition will be indicated by a low state at the $\overline{TOL}$ output on pin 10. ($\overline{TOL}$ is also low for manual shutdown via pin 7). Automatic thermal shutdown can be bypassed by a TTL high state on Thermal Overload Inhibit (TOI) pin 6. See the truth table for a summary of operation.

Offset Adjustment

Offset voltage may be nulled with a 5kΩ potentiometer between pins 3 and 4, center tapped to the positive supply. Setting the slider towards pin 3 (+BAL) increases output voltage; towards pin 4 (-BAL) decreases output voltage. Offset can be adjusted by about ±10mV with a 5K pot; this range is extended with a lower resistance potentiometer.

HARRIS SEMICONDUCTOR

HA-5020

100MHz Current Feedback Video Amplifier

March 1993

Features

- Wide Unity Gain Bandwidth 100MHz
- Slew Rate 800V/μs
- Output Current ..... ±30mA (Min)
- Drives 3.5V into 75Ω
- Differential Gain 0.025%
- Differential Phase ..... 0.025 Deg
- Low Input Voltage Noise ..... 4.5nV/$\sqrt{Hz}$
- Low Supply Current ..... 10mA (Max)
- Wide Supply Range ..... ±5V to ±15V
- Output Enable/Disable
- High Performance Replacement for EL2020

Applications

- Unity Gain Video/Wideband Buffer
- Video Gain Block
- Video Distribution Amp/Coax Cable Driver
- Flash A/D Driver
- Waveform Generator Output Driver
- Current to Voltage Converter; D/A Output Buffer
- Radar Systems
- Imaging Systems

Description

The HA-5020 is a wide bandwidth, high slew rate amplifier optimized for video applications and gains between 1 and 10. Manufactured on Harris' Reduced Feature Complementary Bipolar DI process, this amplifier uses current mode feedback to maintain higher bandwidth at a given gain than conventional voltage feedback amplifiers. Since it is a closed loop device, the HA-5020 offers better gain accuracy and lower distortion than open loop buffers.

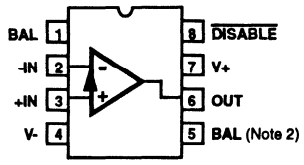
The HA-5020 features low differential gain and phase and will drive two double terminated 75Ω coax cables to video levels with low distortion. Adding a gain flatness performance of 0.1dB makes this amplifier ideal for demanding video applications. The bandwidth and slew rate of the HA-5020 are relatively independent of closed loop gain. The 100MHz unity gain bandwidth only decreases to 60MHz at a gain of 10. The HA-5020 used in place of a conventional op amp will yield a significant improvement in the speed power product. To further reduce power, the HA-5020 has a disable function which significantly reduces supply current, while forcing the output to a true high impedance state. This allows the outputs of multiple amplifiers to be wire-OR'd into multiplexer configurations. The device also includes output short circuit protection and output offset voltage adjustment.

The HA-5020 offers significant enhancements over competing amplifiers, such as the EL2020. Improvements include unity gain bandwidth, slew rate, video performance, lower supply current, and superior DC specifications.

The HA-5020 is available in commercial and industrial temperature ranges, and a choice of packages. See the "Ordering Information" section below for more information. For military grade product, please refer to the HA-5020/ 883 data sheet.

Pinout

HA-5020
(PDIP, CDIP, SOIC)
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA3-5020-5	0°C to +75°C	8 Lead Plastic DIP
HA7-5020-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P5020-5	0°C to +75°C	8 Lead SOIC
HA3-5020-9	-40°C to +85°C	8 Lead Plastic DIP
HA7-5020-9	-40°C to +85°C	8 Lead Ceramic DIP
HA0-5020-6	-40°C to +85°C	DIE

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2845.3**

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 36V
DC Input Voltage ..... $\pm V_{SUPPLY}$
Differential Input Voltage 10V
Output Current ..... Short Circuit Protected
Junction Temperature (Note 19) ..... +175°C
Junction Temperature (Plastic Package) (Note 19) ..... +150°C

Operating Temperature Range

HA-5020-5 ..... $0°C \le T_A \le +75°C$
HA-5020-9 ..... $-40°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JC}	θ_{JA}
Plastic DIP	34	96
Ceramic DIP	35	115
SOIC	43	158

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V+ = +15V$, $V- = -15V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \le 10pF$, Unless Otherwise Specified

PARAMETER	TEMP.	HA-5020-5, -9 MIN	HA-5020-5, -9 TYP	HA-5020-5, -9 MAX	UNITS
INPUT CHARACTERISTICS					
Input Offset Voltage (Notes 2, 20)	+25°C	-	2	8	mV
	Full	-	-	10	mV
Average Input Offset Voltage Drift	Full	-	10	-	µV/°C
V_{IO} Common Mode Rejection Ratio (Notes 3, 20)	+25°C	60	-	-	dB
	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio (Notes 4, 20)	+25°C	64	-	-	dB
	Full	60	-	-	dB
Non-Inverting Input (+IN) Current (Note 20)	+25°C	-	3	8	µA
	Full	-	-	20	µA
+IN Common Mode Rejection (Note 3)	+25°C	-	-	0.1	µA/V
	Full	-	-	0.5	µA/V
+IN Power Supply Rejection (Note 4)	+25°C	-	-	0.06	µA/V
	Full	-	-	0.2	µA/V
Inverting Input (-IN) Current (Note 20)	+25°C	-	12	20	µA
	Full	-	25	50	µA
-IN Common Mode Rejection (Note 3)	+25°C	-	-	0.4	µA/V
	Full	-	-	0.5	µA/V
-IN Power Supply Rejection (Note 4)	+25°C	-	-	0.2	µA/V
	Full	-	-	0.5	µA/V
TRANSFER CHARACTERISTICS					
Transimpedence (Note 20)	+25°C	3500	-	-	V/mA
	Full	1000	-	-	V/mA
Open Loop DC Voltage Gain (Note 12)	+25°C	70	-	-	dB
$R_L = 400\Omega$, $V_{OUT} = \pm 10V$	Full	65	-	-	dB
Open Loop DC Voltage Gain	+25°C	60	-	-	dB
$R_L = 100\Omega$, $V_{OUT} = \pm 2.5V$	Full	55	-	-	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 20)	+25°C to +85°C	±12	±12.7	-	V
	-40°C to 0°C	±11	±11.8	-	V

Electrical Specifications V+ = +15V, V- = -15V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, $C_L \leq$ 10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP.	HA-5020-5, -9			UNITS
		MIN	TYP	MAX	
Output Current	+25°C	±30	±31.7	-	mA
(Guaranteed by Output Voltage Test)	Full	±27.5	-	-	mA
POWER SUPPLY CHARACTERISTICS					
Quiescent Supply Current (Note 20)	Full	-	7.5	10	mA
Supply Current, Disabled (Notes 5, 20))	Full	-	5	7.5	mA
$\overline{\text{Disable}}$ Pin Input Current (Note 5)	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable (Note 6)	Full	350	-	-	µA
Maximum Pin 8 Current to Enable (Note 7)	Full	-	-	20	µA
AC CHARACTERISTICS (A_V = +1)					
Slew Rate (Note 8)	+25°C	600	800	-	V/µs
	Full	500	700	-	V/µs
Full Power Bandwidth (Note 9)	+25°C	9.6	12.7	-	MHz
(Guaranteed by Slew Rate Test)	Full	8.0	11.1	-	MHz
Rise Time (Note 10)	+25°C	-	5	-	ns
Fall Time (Note 10)	+25°C	-	5	-	ns
Propagation Delay (Notes 10, 20)	+25°C	-	6	-	ns
-3dB Bandwidth (Notes 11, 20)	+25°C	-	100	-	MHz
Settling Time to 1%, 10V Output Step	+25°C	-	45	-	ns
Settling Time to 0.25%, 10V Output Step	+25°C	-	100	-	ns
AC CHARACTERISTICS (A_V = +10, R_F = 383Ω)					
Slew Rate (Notes 8, 12)	+25°C	900	1100	-	V/µs
	Full	700	-	-	V/µs
Full Power Bandwidth (Note 9)	+25°C	14.3	17.5	-	MHz
(Guaranteed by Slew Rate Test)	Full	11.1	-	-	MHz
Rise Time (Note 10)	+25°C	-	8	-	ns
Fall Time (Note 10)	+25°C	-	8	-	ns
Propagation Delay (Notes 10, 20)	+25°C	-	9	-	ns
-3dB Bandwidth (Note 11)	+25°C	-	60	-	MHz
Settling Time to 1%, 10V Output Step	+25°C	-	55	-	ns
Settling Time to 0.1%, 10V Output Step	+25°C	-	90	-	ns
HARRIS VALUE ADDED SPECIFICATIONS					
Input Noise Voltage (f = 1kHz) (Note 20)	+25°C	-	4.5	-	nV/$\sqrt{\text{Hz}}$
+Input Noise Current (f = 1kHz) (Note 20)	+25°C	-	2.5	-	pA/$\sqrt{\text{Hz}}$
-Input Noise Current (f = 1kHz) (Note 20)	+25°C	-	25	-	pA/$\sqrt{\text{Hz}}$
Input Common Mode Range	Full	±10	±12	-	V
-Ibias Adjust Range (Note 2)	Full	±25	±40	-	µA
Overshoot (Note 20)	+25°C	-	7	-	%

Electrical Specifications $V+ = +15V$, $V- = -15V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP.	HA-5020-5, -9			UNITS
		MIN	TYP	MAX	
Output Current (Short Circuit, Notes 13, 20)	Full	±50	±65	-	mA
Output Current (Disabled, Notes 5, 14, 20)	Full	-	-	1	µA
Output Disable Time (Notes 15, 20)	+25°C	-	10	-	µs
Output Enable Time (Notes 16, 20)	+25°C	-	200	-	ns
Supply Voltage Range	+25°C	5	-	15	V
Output Capacitance (Disabled, Notes 5,17)	+25°C	-	15	-	pF
VIDEO CHARACTERISTICS					
Differential Gain (Notes 18, 20, 21)	+25°C	-	0.025	-	%
Differential Phase (Notes 18, 20, 21)	+25°C	-	0.025	-	Degrees
Gain Flatness to 5MHz	+25°C	-	0.1	-	dB
Chrominance to Luminance Gain (Note 18)	+25°C	-	0.02	-	dB
Chrominance to Luminance Delay (Note 18)	+25°C	-	0.3	-	ns

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Suggested V_{OS} Adjust Circuit: The inverting input current (-Ibias) can be adjusted with an external 10kΩ pot between pins 1 and 5, wiper connected to V+. Since -Ibias flows through the feedback resistor (R_F), the result is an adjustment in offset voltage. The amount of offset voltage adjustment is determined by the value of R_F ($\Delta V_{OS} = \Delta\text{-Ibias} * R_F$).
3. $V_{CM} = \pm 10V$.
4. $\pm 4.5V \leq V_S \leq \pm 18V$.
5. $\overline{\text{Disable}} = 0V$.
6. $R_L = 100\Omega$, $V_{IN} = 10V$. This is the minimum current which must be pulled out of the $\overline{\text{Disable}}$ pin in order to disable the output. The output is considered disabled when $-10mV \leq V_{OUT} \leq +10mV$.
7. $V_{IN} = 0V$. This is the maximum current that can be pulled out of the $\overline{\text{Disable}}$ pin with the HA-5020 remaining enabled. The HA-5020 is considered disabled when the supply current has decreased by at least 0.5mA.
8. V_{OUT} switches from -10V to +10V, or from +10V to -10V. Specification is from the 25% to 75% points.
9. $\text{FPBW} = \dfrac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $V_{PEAK} = 10V$.
10. $R_L = 100\Omega$, $V_{OUT} = 1V$. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
11. $R_L = 400\Omega$, $V_{OUT} = 100mV$.
12. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
13. $V_{IN} = \pm 10V$, $V_{OUT} = 0V$.
14. $V_{OUT} = \pm 10V$.
15. $V_{IN} = +10V$, $\overline{\text{Disable}} = +15V$ to 0V. Measured from the 50% point of $\overline{\text{Disable}}$ to $V_{OUT} = 0V$.
16. $V_{IN} = +10V$, $\overline{\text{Disable}} = 0V$ to +15V. Measured from the 50% point of $\overline{\text{Disable}}$ to $V_{OUT} = 10V$.
17. $V_{IN} = 0V$, Force V_{OUT} from 0V to ±10V, $t_R = t_F = 50ns$.
18. Measured with a VM700A video tester using a NTC-7 composite VITS.
19. Maximum power dissipation, including output load, must be designed to maintain junction temperature below +175°C for ceramic packages, and below +150°C for plastic packages.
20. See "Typical Performance Curves" for more information.
21. $R_L = 150\Omega$

Die Characteristics

DIE DIMENSIONS:
1640µm x 1520µm x 483µm ±25.4µm

METALLIZATION:
Type: Aluminum, 1% Copper
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
5.77×10^4 A/cm^2 at 30mA

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

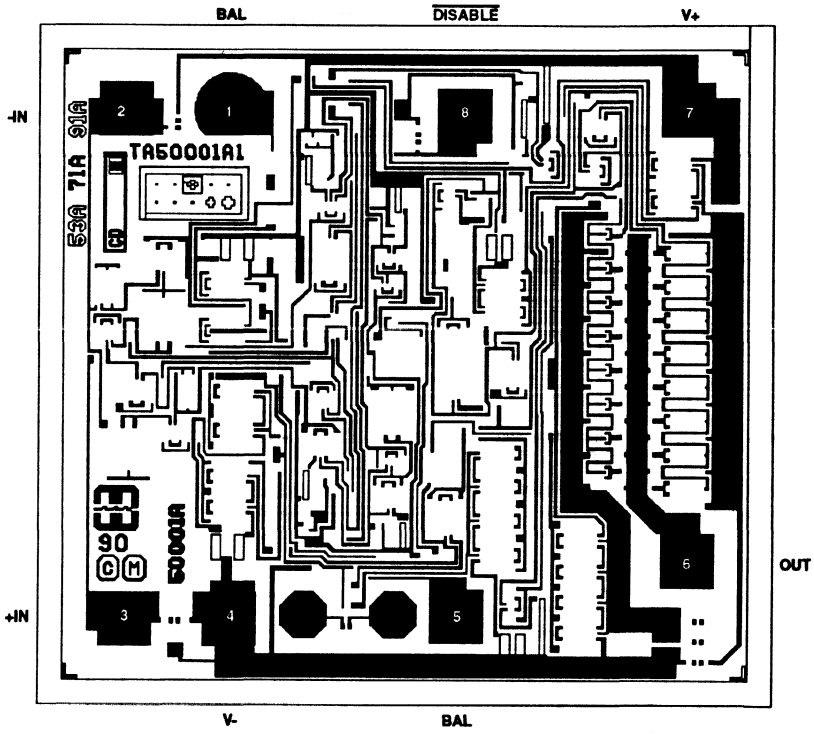
TRANSISTOR COUNT: 62

PROCESS: High Frequency Bipolar Dielectric Isolation

DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC
Gold Eutectic - Ceramic DIP

Metallization Mask Layout

HA-5020



Typical Performance Curves

$V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25°C$, Unless Otherwise Specified

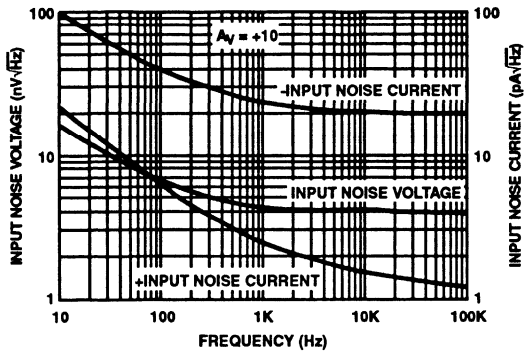


FIGURE 1. INPUT NOISE vs FREQUENCY
(Average of 18 Units from 3 Lots)

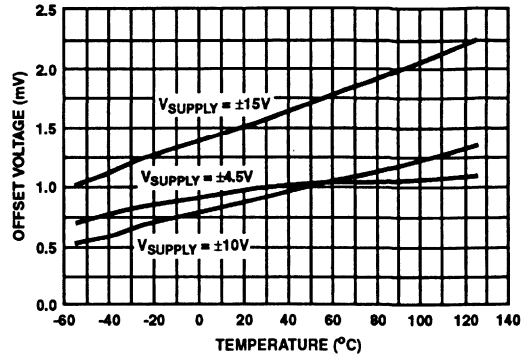


FIGURE 2. INPUT OFFSET VOLTAGE vs TEMPERATURE
(Absolute Value Average of 30 Units from 3 Lots)

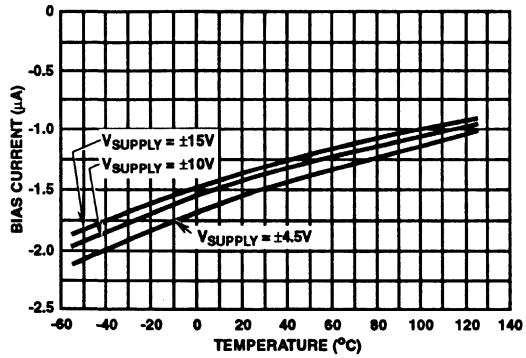


FIGURE 3. +INPUT BIAS CURRENT vs TEMPERATURE
Average of 30 Units from 3 Lots

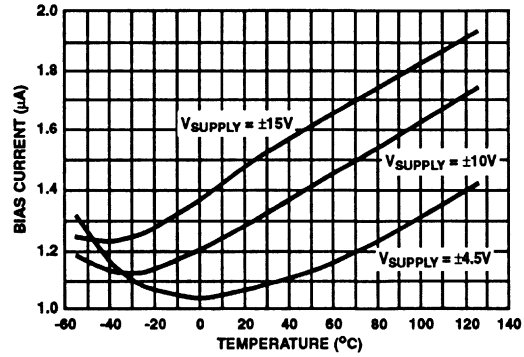


FIGURE 4. -INPUT BIAS CURRENT vs TEMPERATURE
Absolute Value Average of 30 Units from 3 Lots

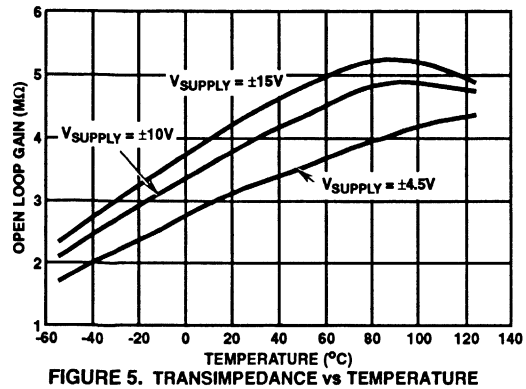


FIGURE 5. TRANSIMPEDANCE vs TEMPERATURE
Average of 30 Units from 3 Lots

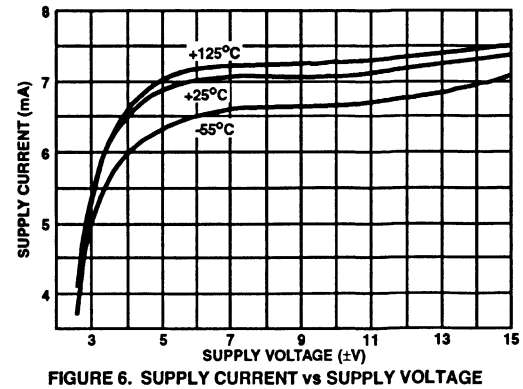


FIGURE 6. SUPPLY CURRENT vs SUPPLY VOLTAGE
Average of 30 Units from 3 Lots

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

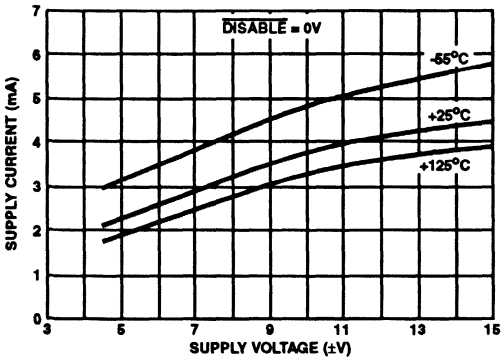


FIGURE 7. DISABLE SUPPLY CURRENT vs SUPPLY VOLTAGE
Average of 30 Units from 3 Lots

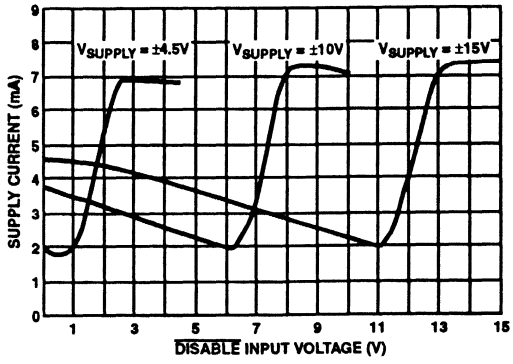


FIGURE 8. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

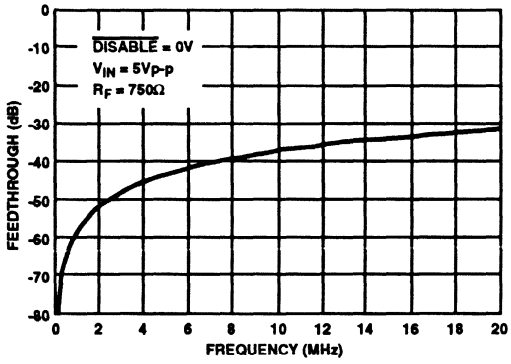


FIGURE 9. DISABLE MODE FEEDTHROUGH vs FREQUENCY

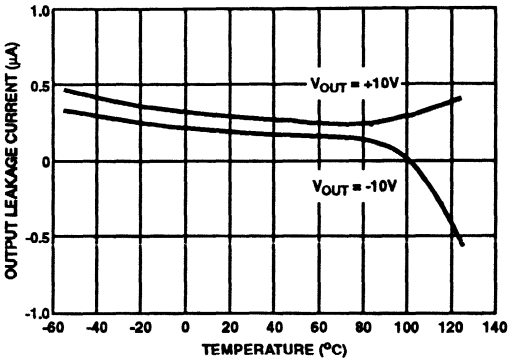


FIGURE 10. DISABLED OUTPUT LEAKAGE vs TEMPERATURE
Average of 30 Units from 3 Lots

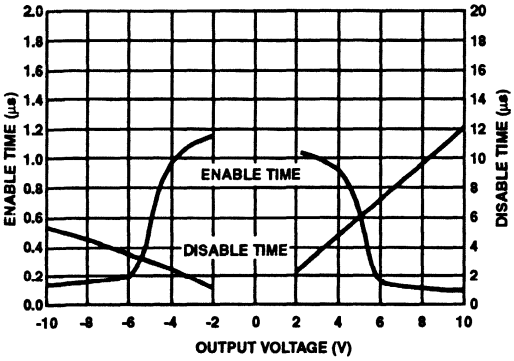


FIGURE 11. ENABLE/DISABLE TIME vs OUTPUT VOLTAGE
Average of 9 Units from 3 Lots

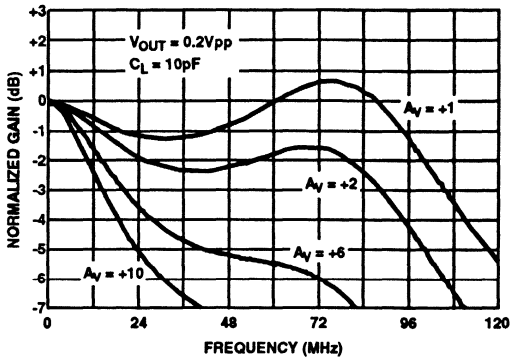


FIGURE 12. NON-INVERTING GAIN vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

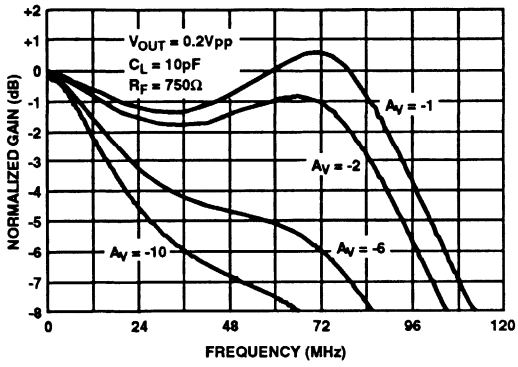


FIGURE 13. INVERTING FREQUENCY RESPONSE

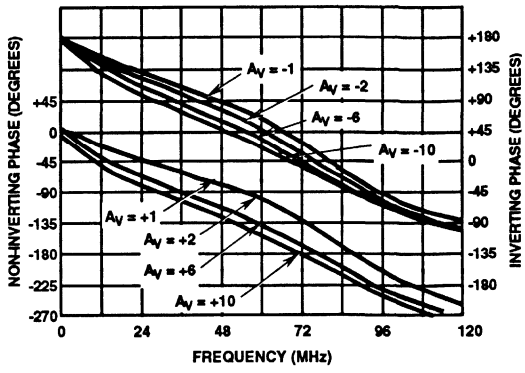


FIGURE 14. PHASE vs FREQUENCY

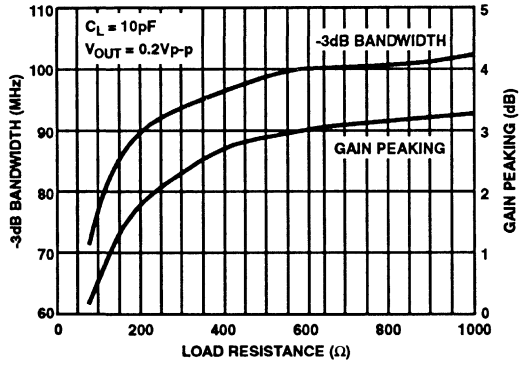


FIGURE 15. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

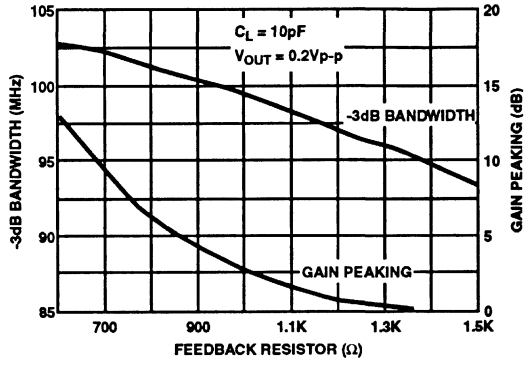


FIGURE 16. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

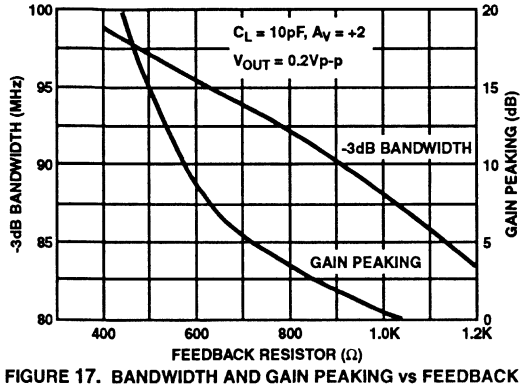


FIGURE 17. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

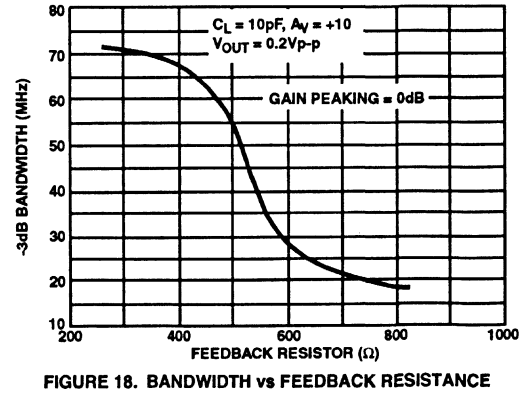


FIGURE 18. BANDWIDTH vs FEEDBACK RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

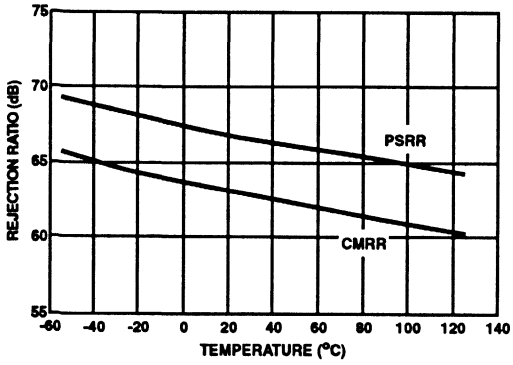


FIGURE 19. REJECTION RATIOS vs TEMPERATURE
Average of 30 Units from 3 Lots

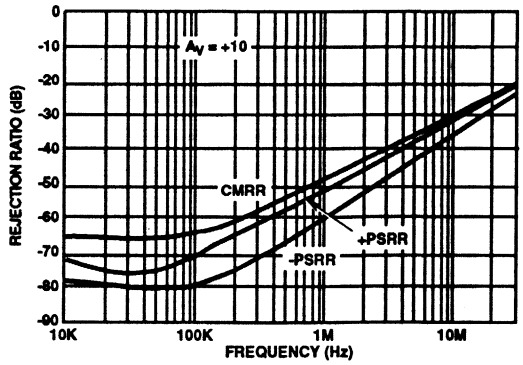


FIGURE 20. REJECTION RATIOS vs FREQUENCY

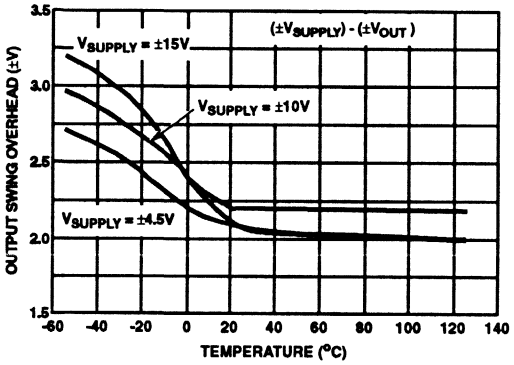


FIGURE 21. OUTPUT SWING OVERHEAD vs TEMPERATURE
Average of 30 Units from 3 Lots

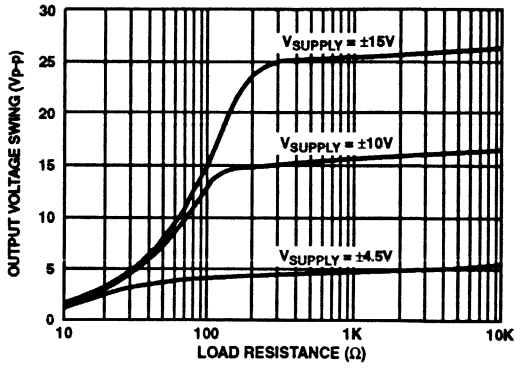


FIGURE 22. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

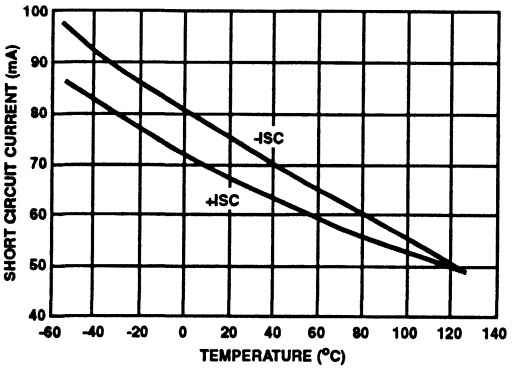


FIGURE 23. SHORT CIRCUIT CURRENT LIMIT vs TEMPERATURE

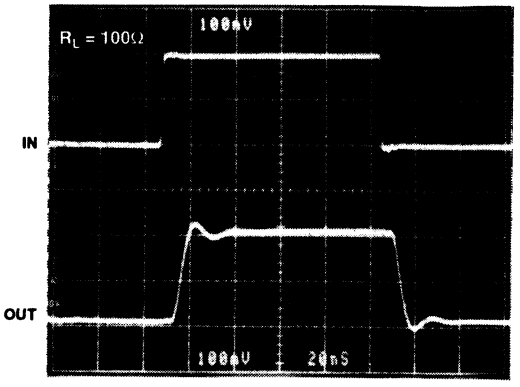


FIGURE 24. SMALL SIGNAL PULSE RESPONSE
Vertical Scale: V_{IN} = 100mV/Div.; V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

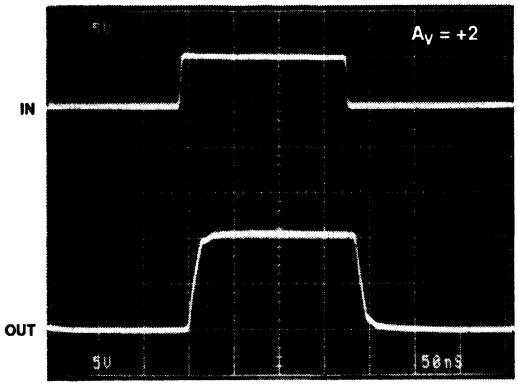


FIGURE 25. LARGE SIGNAL PULSE RESPONSE
Vertical Scale: V_{IN} = 5V/Div.; V_{OUT} = 5V/Div.
Horizontal Scale: 50ns/Div.

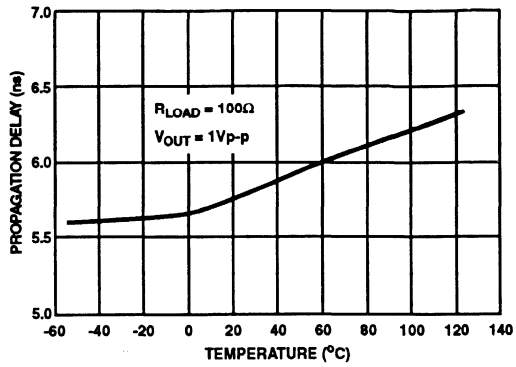


FIGURE 26. PROPAGATION DELAY vs TEMPERATURE
Average of 18 Units from 3 Lots

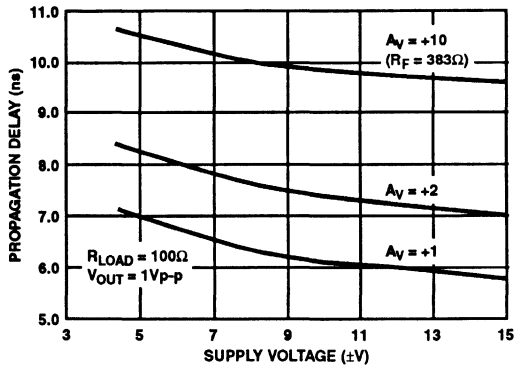


FIGURE 27. PROPAGATION DELAY vs SUPPLY VOLTAGE
Average of 18 Units From 3 Lots

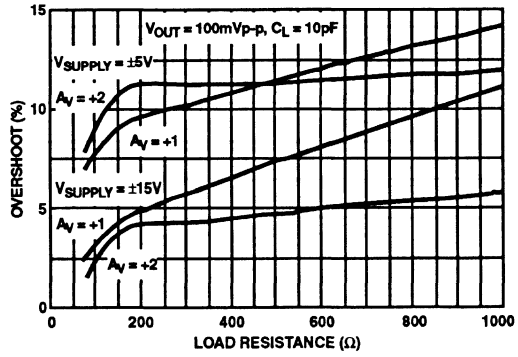


FIGURE 28. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

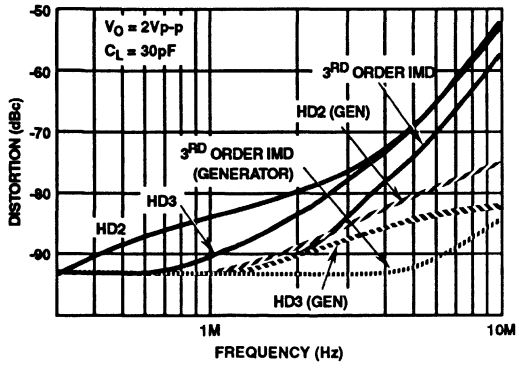


FIGURE 29. DISTORTION vs FREQUENCY

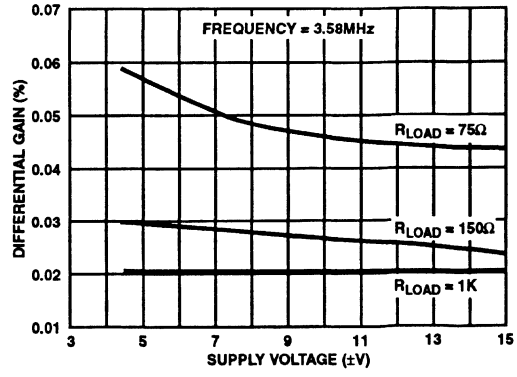


FIGURE 30. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE
Average of 18 Units from 3 Lots

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

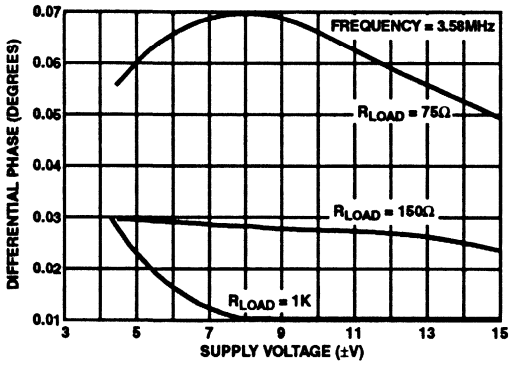


FIGURE 31. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE
Average of 18 Units from 3 Lots

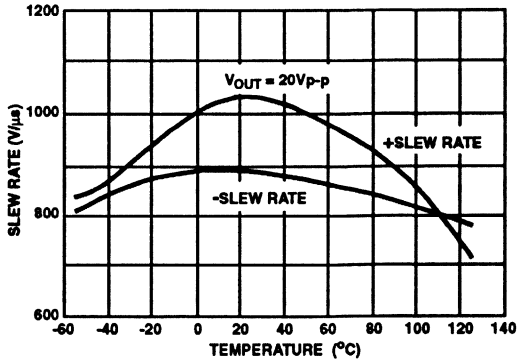


FIGURE 32. SLEW RATE vs TEMPERATURE
Average of 30 Units from 3 Lots

HARRIS SEMICONDUCTOR

HA5022, HA5024

ADVANCE INFORMATION

April 1993

Dual, Quad 100MHz Video Current Feedback Amplifier with Disable

Features

- Dual, Quad Versions of HA-5020
- Output Enable/Disable
- Wide Unity Gain Bandwidth 100MHz
- Slew Rate 800V/μs
- Output Current ..... ±30mA
- Differential Gain 0.025%
- Differential Phase ..... 0.025 Degrees
- Supply Current (per Amplifier) 7.5mA
- Supply Range ..... ±5V to ±15V
- Crosstalk Rejection at 10MHz ..... -60dB
- ESD Protection ..... >2000V
- Guaranteed Specifications at ±5V and ±15V Supplies

Applications

- Video Multiplexers; Video Switching and Routing
- Video Gain Block
- Video Distribution Amplifier/ RGB Amplifier
- Flash A/D Driver
- Current to Voltage Converter; DAC Buffer
- Medical Imaging
- Radar and Imaging Systems

Description

The HA5022 and HA5024 are dual and quad versions of the popular Harris HA-5020. They feature wide bandwidth and high slew rate, and are optimized for video applications and gains between 1 and 10. Both are current feedback amplifiers and thus yield less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make these amplifiers ideal for demanding video applications.

The HA5022 and HA5024 also feature a disable function that significantly reduces supply current while forcing the output to a true high impedance state. This functionality allows 2:1 and 4:1 video multiplexers to be implemented with a single IC.

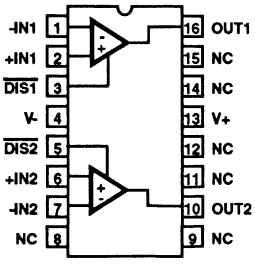
The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor. By reducing RF, the bandwidth can be increased to compensate for decreases at higher closed loop gains or heavy output loads.

Ordering Information

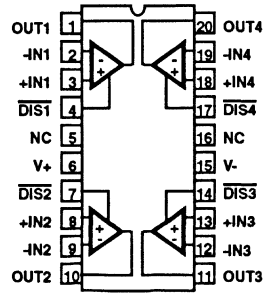
PART NUMBER	TEMPERATURE RANGE	PRODUCT DESCRIPTION
HA5022IP	-40°C to +85°C	16 Lead Plastic DIP
HA5022IJ	-40°C to +85°C	16 Lead Ceramic DIP
HA5022IB	-40°C to +85°C	16 Lead Narrow Body SOIC
HA5024IP	-40°C to +85°C	20 Lead Plastic DIP
HA5024IJ	-40°C to +85°C	20 Lead Ceramic DIP
HA5024IB	-40°C to +85°C	20 Lead SOIC

Pinouts

HA5022
(PDIP, CDIP, 150 MIL SOIC)
TOP VIEW



HA5024
(PDIP, CDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3392

HARRIS SEMICONDUCTOR

HA5023, HA5025

ADVANCE INFORMATION

April 1993

Dual, Quad 100MHz Video Current Feedback Amplifier

Features

- Wide Unity Gain Bandwidth 100MHz
- Slew Rate 800V/µs
- Output Current ..... ±30mA
- Differential Gain 0.025%
- Differential Phase ..... 0.025 Deg.
- Supply Current (per Amplifier) 7.5mA
- Supply Range ..... ±5V to ±15V
- Crosstalk Rejection at 10MHz ..... -60dB
- ESD Protection ..... >2000V
- Guaranteed Specifications at ±5V and ±15V Supplies

Applications

- Video Gain Block
- Video Distribution Amplifier/ RGB Amplifier
- Flash A/D Driver
- Current to Voltage Converter; DAC Buffer
- Medical Imaging
- Radar and Imaging Systems
- Video Switching and Routing

Description

The HA5023 and HA5025 are wide bandwidth high slew rate dual and quad amplifiers optimized for video applications and gains between 1 and 10. They are current feedback amplifiers and thus yield less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make these amplifiers ideal for demanding video applications.

The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor. By reducing R_F, the bandwidth can be increased to compensate for decreases at higher closed loop gains or heavy output loads.

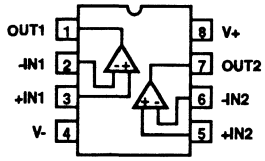
The performance of the HA5023 and HA5025 is very similar to the popular Harris HA-5020.

Ordering Information

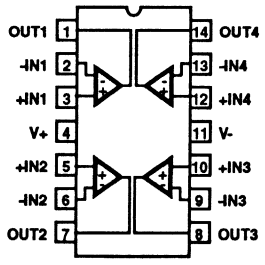
PART NUMBER	TEMPERATURE RANGE	PRODUCT DESCRIPTION
HA5023IP	-40°C to +85°C	8 Lead Plastic DIP
HA5023IJ	-40°C to +85°C	8 Lead Ceramic DIP
HA5023IB	-40°C to +85°C	8 Lead SOIC
HA5025IP	-40°C to +85°C	14 Lead Plastic DIP
HA5025IJ	-40°C to +85°C	14 Lead Ceramic DIP
HA5025IB	-40°C to +85°C	16 Lead Wide Body SOIC

Pinouts

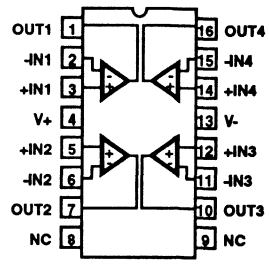
HA5023
(PDIP, CDIP, SOIC)
TOP VIEW



HA5025
(PDIP, CDIP)
TOP VIEW



HA5025
(300 MIL SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3393

HARRIS SEMICONDUCTOR

HA-5033

March 1993

Video Buffer

Features

- Differential Phase Error ..... 0.02 Degree
- Differential Gain Error 0.03%
- High Slew Rate 1100V/μs
- Wide Bandwidth (Small Signal) 250MHz
- Wide Power Bandwidth ..... DC to 17.5MHz
- Fast Rise Time 3ns
- High Output Drive ..... ±10V With 100Ω Load
- Wide Power Supply Range ..... ±5V to ±16V
- Replace Costly Hybrids

Applications

- Video Buffer
- High Frequency Buffer
- Isolation Buffer
- High Speed Line Driver
- Impedance Matching
- Current Boosters
- High Speed A/D Input Buffers
- For Further Application Ideas, See App. Note 548

Description

The HA-5033 is a unity gain monolithic I.C. designed for any application requiring a fast, wideband buffer. Featuring a bandwidth of 250MHz and outstanding differential phase/gain characteristics, this high performance voltage follower is an excellent choice for video circuit design. Other features, which include a minimum slew rate of 1000V/μs and high output drive capability, make the HA-5033 applicable for line driver and high speed data conversion circuits.

The high performance of this product is a result of the Harris Dielectric Isolation process. A major feature of this process is that it produces both PNP and NPN high frequency transistors which makes wide bandwidth designs, such as the HA-5033, practical. Alternative process methods typically produce a lower AC performance.

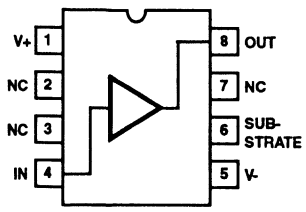
For the HA-5033 in 8 Lead SOIC with reduced thermal rating contact the factory.

Ordering Information

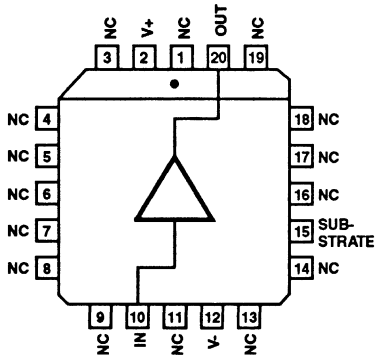
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-5033-2	-55°C to +125°C	12 Pin Can
HA2-5033-5	0°C to +75°C	12 Pin Can
HA3-5033-5	0°C to +75°C	8 Lead Plastic DIP
HA4-5033-5	0°C to +75°C	20 Lead PLCC

Pinouts

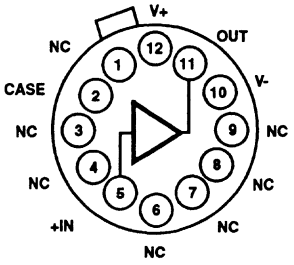
HA-5033 (PDIP)
TOP VIEW



HA-5033 (PLCC)
TOP VIEW



HA-5033 (TO-8 CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2924.1**

Absolute Maximum Ratings

Voltage Between V+ and V- Pins 40V
DC Input Voltage ..... V+ to V-
Output Current (Peak) (50ms On/1 Second Off) ..... ±200mA
Internal Power Dissipation (Note 2)
TO-8 (+25°C) 2.3W
Mini-DIP (+25°C) 1.3W
PLCC (+25°C) 1.7W
Maximum Junction Temperature ..... +175°C
Maximum Junction Temperature (Plastic Packages) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Ranges
HA-5033-2 ..... $-55°C \le T_A \le +125°C$
HA-5033-5 ..... $0°C \le T_A \le +75°C$
HA-5033-9 ..... $-40°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$
ESD Rating (Note 11) ..... >2000V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V_{SUPPLY} = \pm12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $C_L = 10pF$, Unless Otherwise Specified.

PARAMETER	TEMP	HA-5033-2 MIN	HA-5033-2 TYP	HA-5033-2 MAX	HA-5033-5 MIN	HA-5033-5 TYP	HA-5033-5 MAX	NOTE 10 HA-5033-9 MAX	UNITS
INPUT CHARACTERISTICS									
Offset Voltage	+25°C	-	5	15	-	5	15	15	mV
	Full	-	6	25	-	6	25	30	mV
Average Offset Voltage Drift	Full	-	33	-	-	33	-	-	µV/°C
Bias Current	+25°C	-	20	35	-	20	35	35	µA
	Full	-	30	50	-	30	50	50	µA
Input Resistance	+25°C	-	3	-	-	3	-	-	MΩ
Input Capacitance	+25°C	-	1.6	-	-	1.6	-	-	pF
Input Noise Voltage (Note 3)	+25°C	-	20	-	-	20	-	-	μV_{P-P}
TRANSFER CHARACTERISTICS									
Voltage Gain									
$R_L = 100\Omega$	+25°C	0.93	-	-	0.93	-	-	-	V/V
$R_L = 1k\Omega$	+25°C	0.93	0.99	-	0.93	0.99	-	-	V/V
$R_L = 100\Omega$	Full	0.92	-	-	0.92	-	-	-	V/V
-3dB Bandwidth	+25°C	-	250	-	-	250	-	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing									
$R_L = 100\Omega$	Full	±8	±10	-	±8	±10	-	-	V
$R_L = 1k\Omega$ (Note 4)	Full	±11	±12	-	±11	±12	-	-	V
Output Current	+25°C	±80	±100	-	±80	±100	-	-	mA
Output Resistance	+25°C	-	8	-	-	8	-	-	Ω
Full Power Bandwidth (Note 5)	+25°C	-	146	-	-	146	-	-	MHz
Full Power Bandwidth (Note 7)	+25°C	15.9	17.5	-	15.9	17.5	-	-	MHz
TRANSIENT RESPONSE									
Rise Time (Note 6)	+25°C	-	4.6	-	-	4.6	-	-	ns
Propagation Delay	+25°C	-	1	-	-	1	-	-	ns
Overshoot	+25°C	-	3	-	-	3	-	-	%
Slew Rate (Note 7)	+25°C	1	1.1	-	1	1.1	-	-	V/ns
Settling Time to 0.1%	+25°C	-	50	-	-	50	-	-	ns
Differential Phase Error (Note 8)	+25°C	-	0.02	-	-	0.02	-	-	Degree
Differential Gain Error (Note 8)	+25°C	-	0.03	-	-	0.03	-	-	%

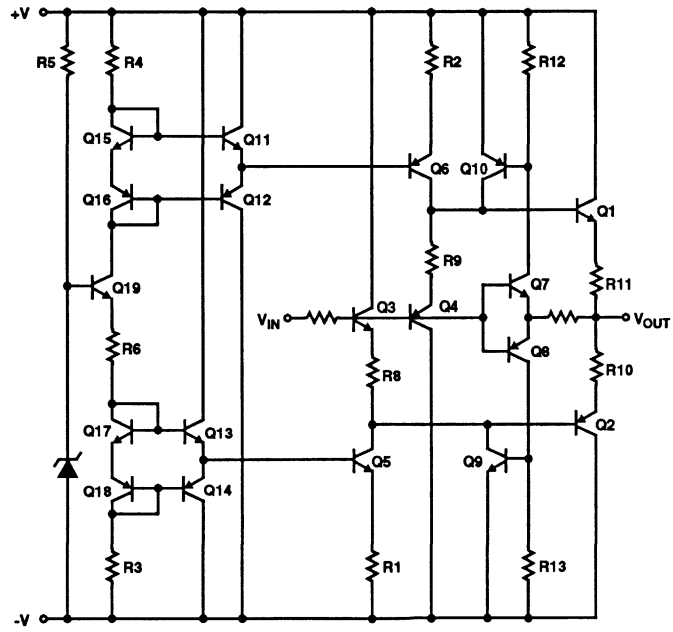
Electrical Specifications V_{SUPPLY} = ±12V, R_S = 50Ω, R_L = 100Ω, C_L = 10pF, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEMP	HA-5033-2			HA-5033-5			NOTE 10 HA-5033-9	UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MAX	
POWER SUPPLY CHARACTERISTICS									
Supply Current	+25°C	-	21	25	-	21	25	25	mA
	Full	-	21	30	-	21	30	30	mA
Power Supply Rejection Ratio	Full	54	-	-	54	-	-	-	dB
Harmonic Distortion (Note 9)	+25°C	-	<0.1	-	-	<0.1	-	-	%

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. See thermal constants in "Die Characteristics" section. Maximum power dissipation, including load conditions, must be designed to maintain the maximum junction temperature below +175°C for the can package, and below +150°C for the plastic packages.
2. See thermal constants in "Die Characteristics" section. Maximum power dissipation, including load conditions, must be designed to maintain the maximum junction temperature below +175°C for the can package, and below +150°C for the plastic packages.
3. 10Hz to 1MHz
4. $\pm V_{SUPPLY}$ = ±15V
5. V_{OUT} = $1V_{RMS}$, R_L = 1kΩ
6. V_{OUT} = 500mV
7. $\pm V_{SUPPLY}$ = ±15V, V_{OUT} = ±10V, R_L = 1kΩ.
8. Differential gain and phase error are nonlinear signal distortions found in video systems and are defined as follows: Differential gain error is defined as the change in amplitude at the color subcarrier frequency as the picture signal is varied from blanking to white level. Differential phase error is defined as the change in the phase of the color subcarrier as the picture signal is varied from blanking to white level. R_L = 300Ω.
9. V_{IN} = $1V_{RMS}$
10. Typical and minimum specification for the -9 version are the same as those for the -5 version.
11. Human Body Model.

Schematic Diagram



Die Characteristics

Transistor Count 20
Die Dimensions ..... 57 x 66 x 19 mils
Substrate Potential*
Process ..... High Frequency Bipolar-DI
Passivation ..... Nitride over Silox

* Connected to "Substrate" bond pad which is dielectrically isolated from V+ and V-.

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
HA2-5033 (Can)	65	34
HA3-5033 (Plastic DIP)	96	30
HA4-5033 (PLCC)	74	33

Test Circuits

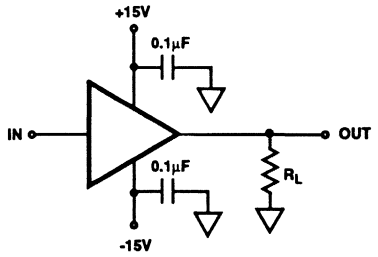


FIGURE 1. SLEW RATE AND SETTLING TIME

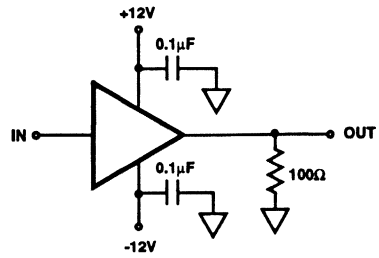


FIGURE 2. TRANSIENT RESPONSE

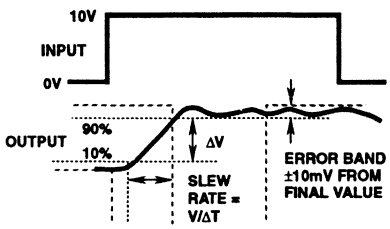
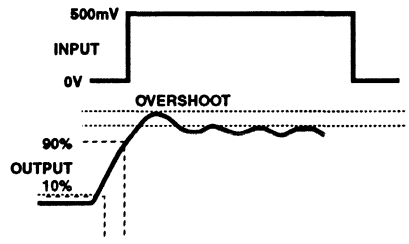


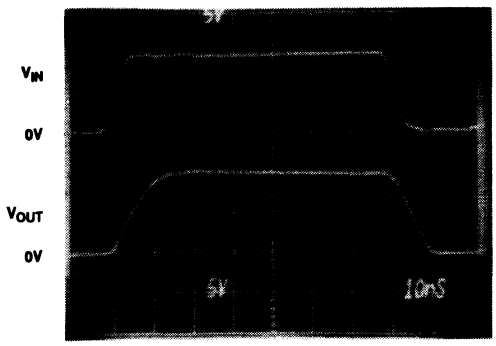
FIGURE 3. SETTLING TIME



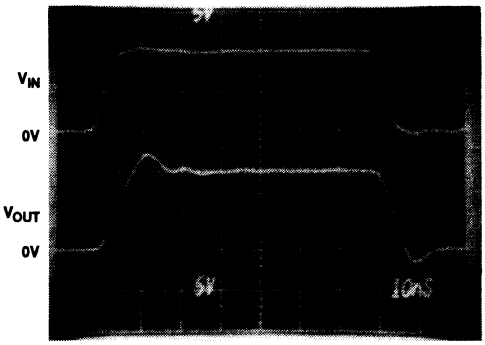
NOTE: Measured on both positive and negative transitions.

FIGURE 4. RISE TIME

+10V RESPONSE
T_A = +25°C, R_S = 50Ω, R_L = 100Ω

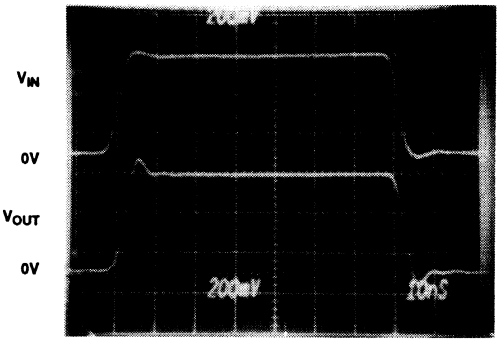


+10V RESPONSE
T_A = +25°C, R_S = 50Ω, R_L = 1kΩ



Test Circuits (Continued)

+0.5V PULSE RESPONSE
T_A = +25°C, R_S = 50Ω, R_L = 100Ω



Typical Performance Curves

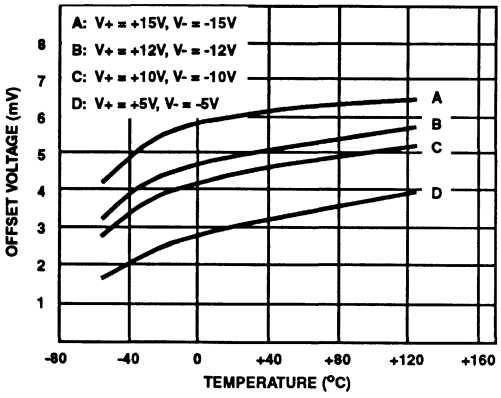


FIGURE 5. INPUT OFFSET VOLTAGE vs TEMPERATURE vs SUPPLY VOLTAGE

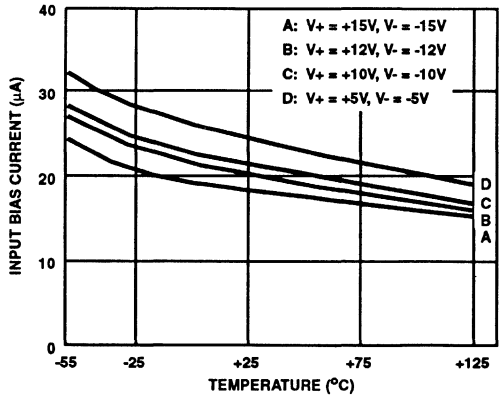


FIGURE 6. INPUT BIAS CURRENT vs TEMPERATURE vs SUPPLY VOLTAGE

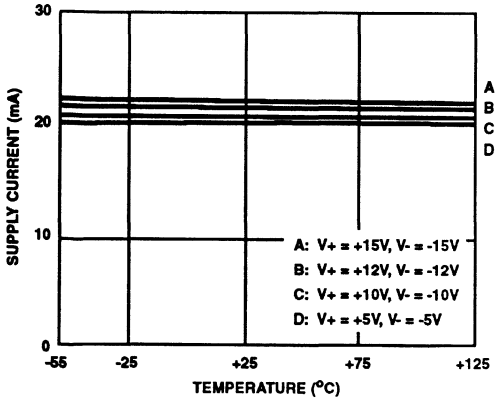


FIGURE 7. SUPPLY CURRENT vs TEMPERATURE vs SUPPLY VOLTAGE

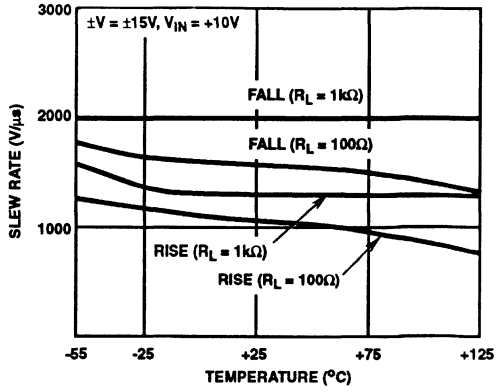


FIGURE 8. SLEW RATE vs TEMPERATURE

Typical Performance Curves (Continued)

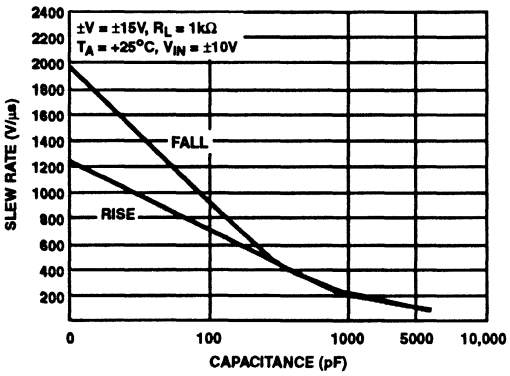


FIGURE 9. SLEW RATE vs LOAD CAPACITANCE (R_L = 1kΩ)

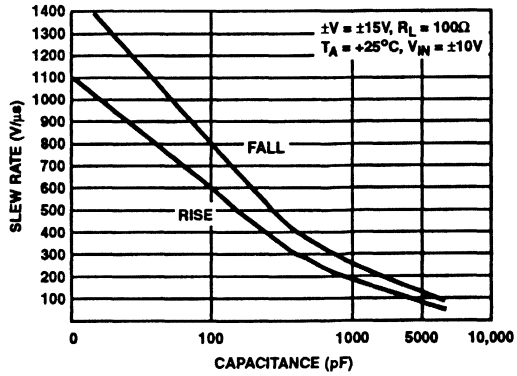


FIGURE 10. SLEW RATE vs LOAD CAPACITANCE (R_L = 100Ω)

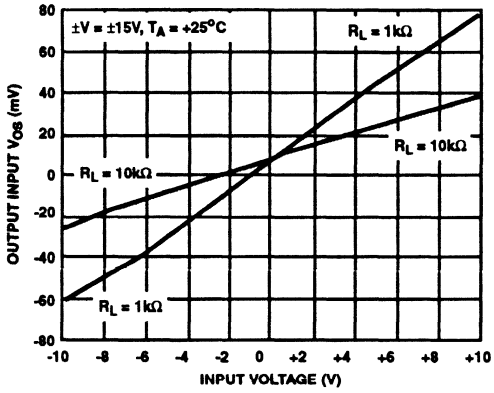


FIGURE 11. GAIN ERROR vs INPUT VOLTAGE

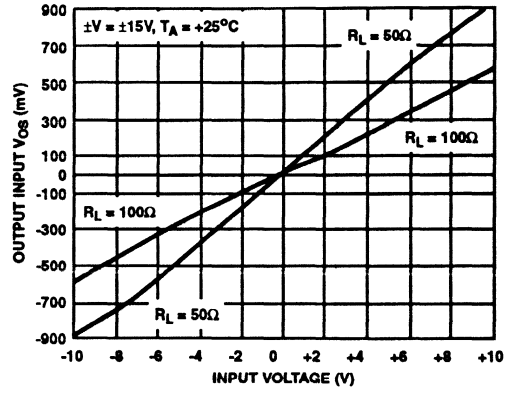


FIGURE 12. GAIN ERROR vs INPUT VOLTAGE

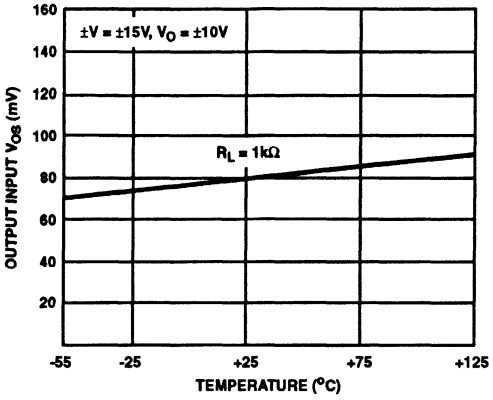


FIGURE 13. GAIN ERROR vs TEMPERATURE

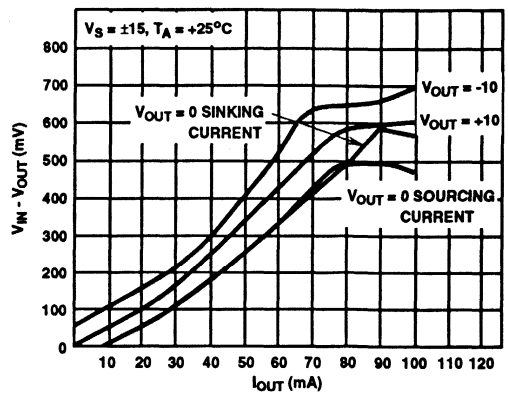


FIGURE 14. V_{IN} - V_{OUT} vs I_{OUT}

Typical Performance Curves (Continued)

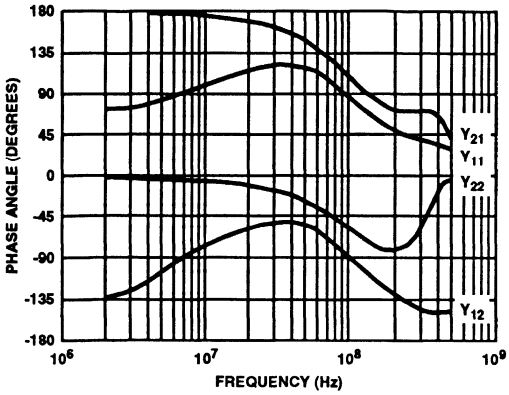
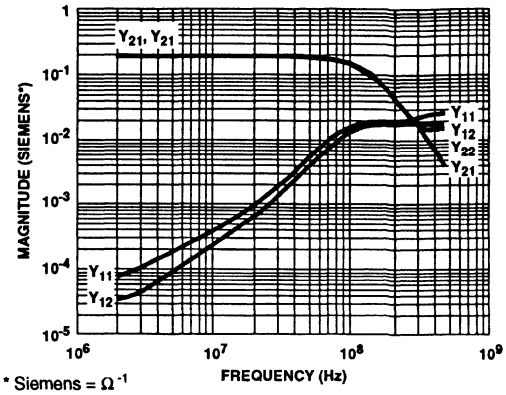


FIGURE 15. Y - PARAMETERS PHASE vs FREQUENCY



* Siemens = Ω^{-1}

FIGURE 16. Y - PARAMETER MAGNITUDE vs FREQUENCY

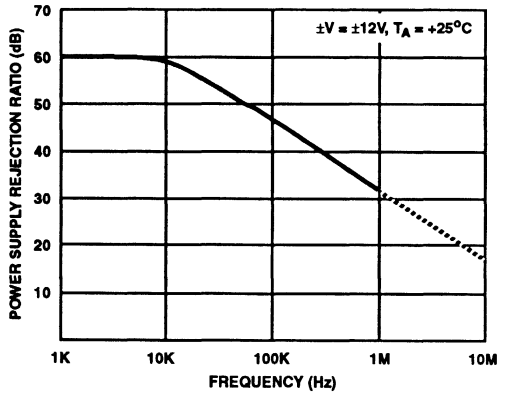


FIGURE 17. POWER SUPPLY REJECTION RATIO vs FREQUENCY

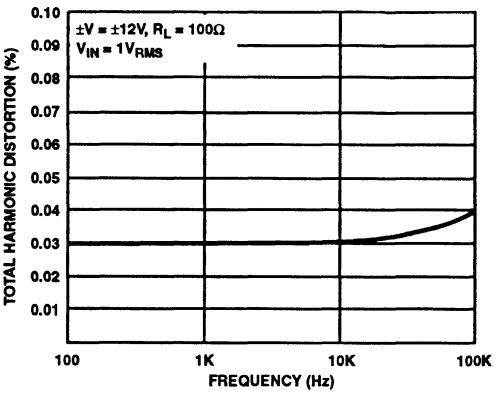


FIGURE 18. GAIN ERROR vs INPUT VOLTAGE

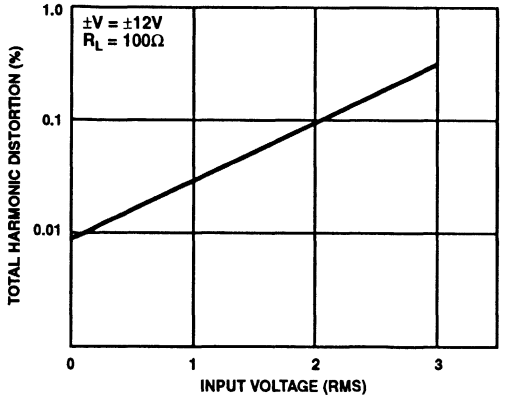


FIGURE 19. TOTAL HARMONIC DISTORTION vs RMS INPUT VOLTAGE

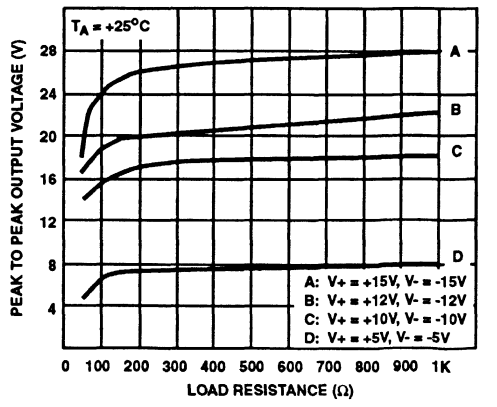


FIGURE 20. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

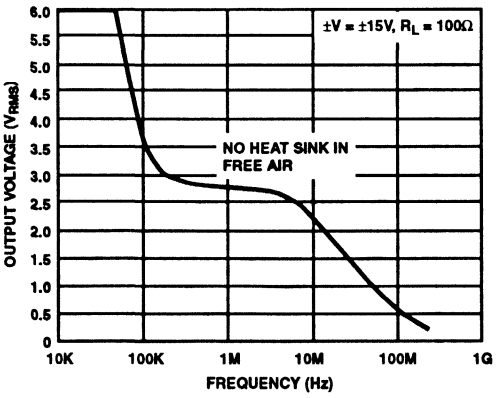


FIGURE 21. OUTPUT SWING vs FREQUENCY*

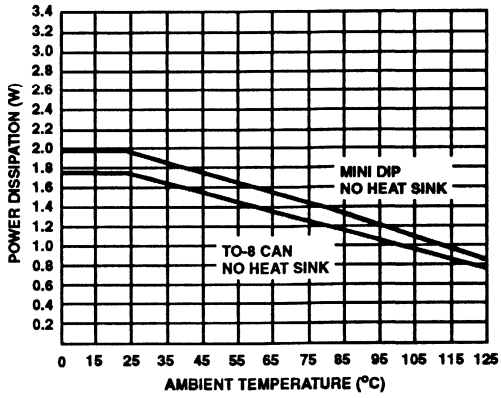


FIGURE 22. MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE

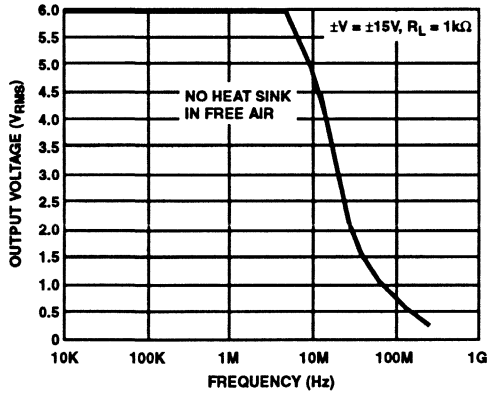


FIGURE 23. OUTPUT SWING vs FREQUENCY *

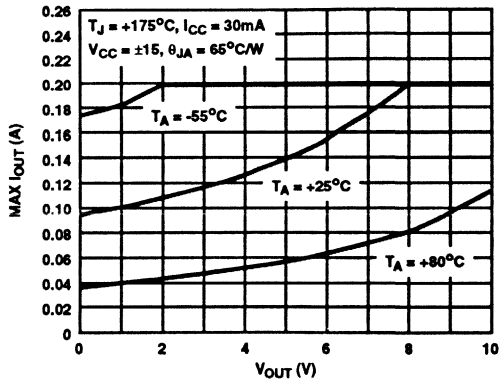


FIGURE 24. HA-5033 SOA, TO-8, NO SINK

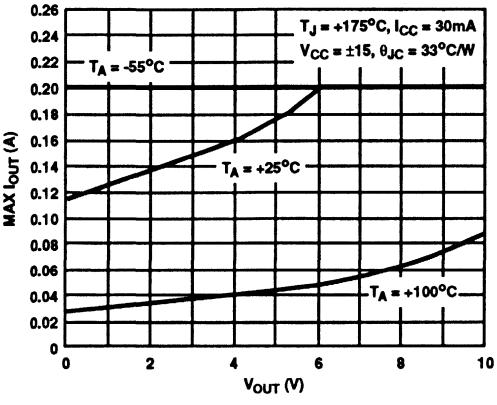


FIGURE 25. HA-5033, TO-8, AAVID 5792 θ_{SA} = 25°C/W

* This curve was obtained by noting the output voltage necessary to produce an observable distortion for a given frequency. If higher distortion is acceptable, then a higher output voltage for a given frequency can be obtained.

However, operating the HA-5033 with increased distortion (to the right of curve shown), will also be accompanied by an increase in supply current. The resulting increase in chip temperature must be considered and heat sinking will be necessary to prevent thermal runaway.

This characteristic is the result of the output transistor operation. If the signal amplitude or signal frequency or both are increased beyond the curve shown, the NPN, PNP output transistors will approach a condition of being simultaneously on. Under this condition, thermal runaway can occur.

Operating Instructions

Layout Considerations

The wide bandwidth of the HA-5033 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance. This ground plane shielding can also incorporate the metal case of the HA-5033 since pin #2 is internally tied to the package. This feature allows the user to make metal to metal contact between the ground plane and the package, which extends shielding, provides additional heat sinking and eliminates the use of a socket, IC sockets contribute inter-lead capacitance which limits device bandwidth and should be avoided.

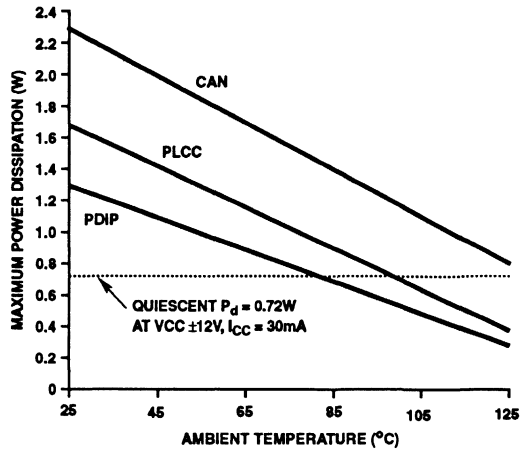
For the plastic Mini-DIP, pin 6 can be tied to either supply, grounded, or simply not used. But to optimize device performance and improve isolation, it is recommended that this pin be grounded.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

Power Supply Decoupling

For optimum device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1µF will minimize high frequency variations in supply voltage. Solid tantalum capacitors 1µF or larger will optimize low frequency performance.

It is also recommended that the bypass capacitors be connected close to the HA-5033 (preferably directly to the supply pins).



Graph is based on: $P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}}$

Where: T_{JMAX} = Maximum Junction Temperature of the Device

T_A = Ambient Temperature

θ_{JA} = Junction to Ambient Thermal Resistance

FIGURE 26. FREE AIR POWER DISSIPATION

Typical Applications (Also see Application Note 548)

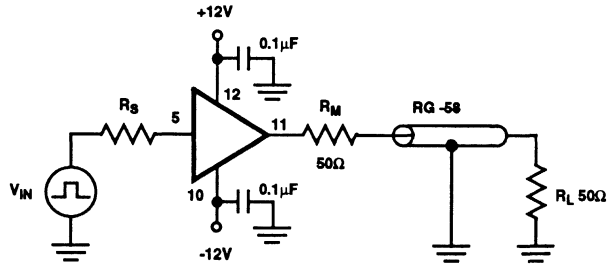


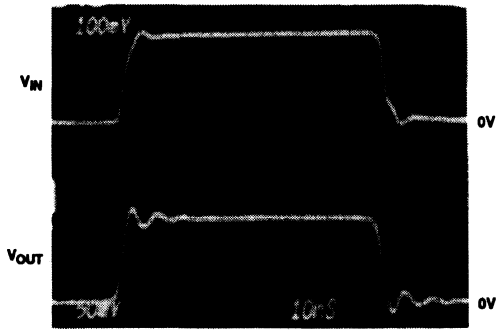
FIGURE 27. VIDEO COAXIAL LINE DRIVER 50Ω SYSTEM

Typical Applications (Also see Application Note 548)

POSITIVE PULSE RESPONSE

$T_A = +25°C$, $R_S = 50\Omega$, $R_M = R_L = 50\Omega$

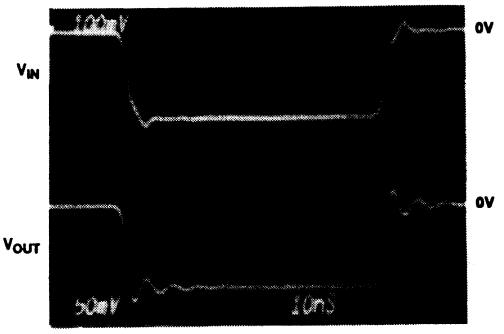
$$V_O = V_{IN}\left[\frac{R_L}{R_L + R_M}\right] = \left[\frac{1}{2}\right] V_{IN}$$



NEGATIVE PULSE RESPONSE

$T_A = +25°C$, $R_S = 50\Omega$, $R_M = R_L = 50\Omega$

$$V_O = V_{IN}\left[\frac{R_L}{R_L + R_M}\right] = \left[\frac{1}{2}\right] V_{IN}$$



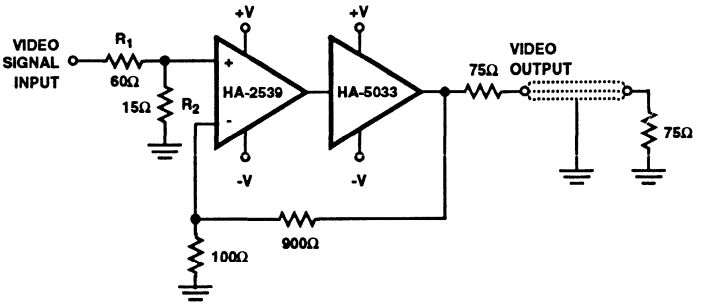


FIGURE 28. VIDEO GAIN BLOCK

HARRIS SEMICONDUCTOR

HA-5101, HA-5111

Low Noise, High Performance Operational Amplifiers

April 1993

Features

- Low Noise.....3.0nV/√Hz at 1kHz
- Wide Bandwidth.....10MHz (Compensated)
  100MHz (Uncompensated)
- High Slew Rate.....10V/μs (Compensated)
  50V/μs (Uncompensated)
- Low Offset Voltage Drift .....3μV/°C
- High Gain ..... 1 x 10^6V/V
- High CMRR/PSRR 100dB
- High Output Drive Capability 30mA

Applications

- High Quality Audio Preamplifiers
- High Q Active Filters
- Low Noise Function Generators
- Low Distortion Oscillators
- Low Noise Comparators
- For Further Design Ideas, See Application Note 554

Description

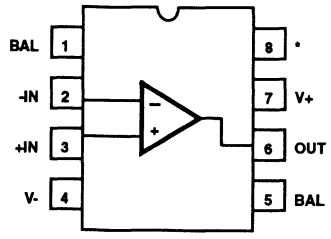
The HA-5101/5111 are dielectrically isolated operational amplifiers featuring low noise and high performance. Both amplifiers have an excellent noise voltage density of 3.0nV/√Hz at 1kHz. The uncompensated HA-5111 is stable at a minimum gain of 10 and has the same DC specifications as the unity gain stable HA-5101. The difference in compensation yields a 100MHz gain-bandwidth product and a 50V/μs slew rate for the HA-5111 versus a 10MHz unity gain bandwidth and a 10V/μs slew rate for the HA-5101.

DC characteristics of the HA-5101/5111 assure accurate performance. The 0.5mV offset voltage is externally adjustable and offset voltage drift is just 3μV/°C. An offset current of only 30nA reduces input current errors and an open loop voltage gain of 1 x 10^6V/V increases loop gain for low distortion amplification.

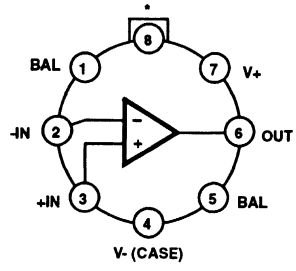
The HA-5101/5111 are ideal for audio applications, especially low-level signal amplifiers such as microphone, tape head and phono cartridge preamplifiers. Additionally, it is well suited for low distortion oscillators, low noise function generators and high Q filters.

Pinouts (See Ordering Information on Next Page)

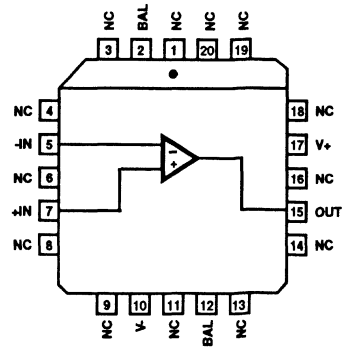
HA-5101, HA-5111
(PDIP, CDIP, SOIC)
TOP VIEW



HA-5101, HA-5111
(TO-99 METAL CAN)
TOP VIEW



HA-5101
(PLCC)
TOP VIEW



*HA-5101 No Connect
HA-5111 Compensation

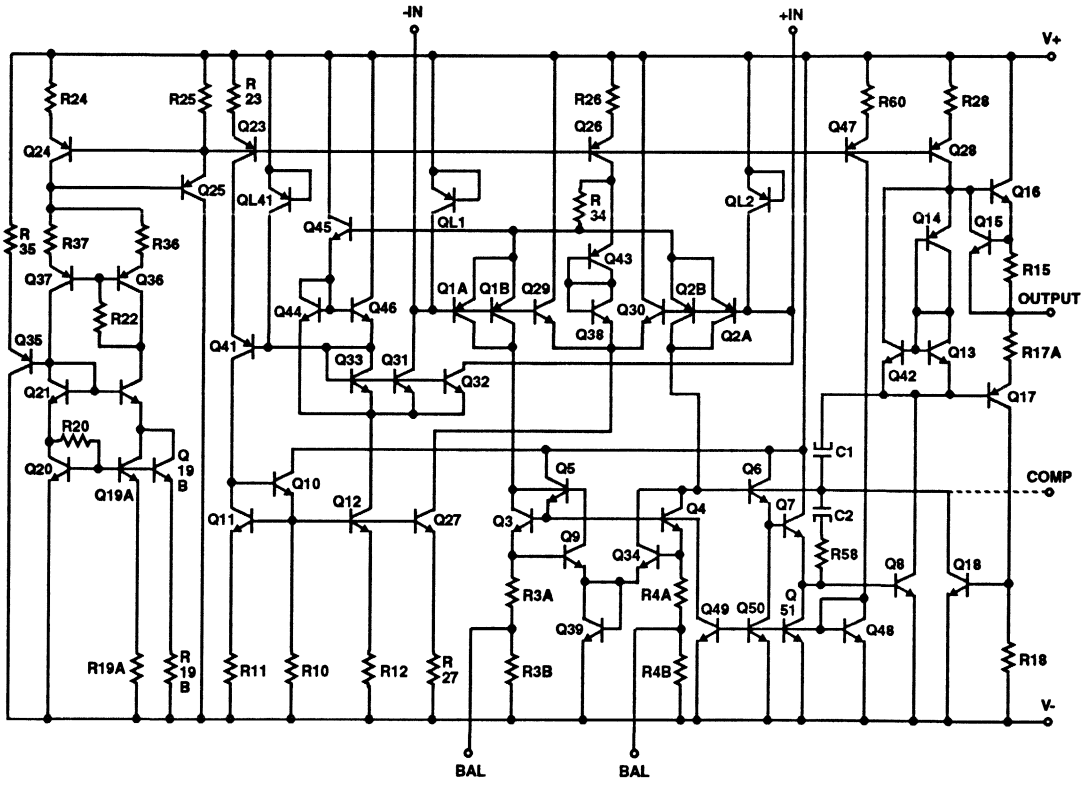
File Number **2905.1**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-5101-2	-55°C to +125°C	8 Pin Can
HA2-5101-5	0°C to +75°C	8 Pin Can
HA3-5101-5	0°C to +75°C	8 Lead Plastic DIP
HA4P5101-5	0°C to +75°C	20 Lead PLCC
HA7-5101-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5101-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P5101-5	0°C to +75°C	8 Lead SOIC
HA9P5101-9	-40°C to +85°C	8 Lead SOIC

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-5111-2	-55°C to +125°C	8 Pin Can
HA2-5111-5	0°C to +75°C	8 Pin Can
HA3-5111-5	0°C to +75°C	8 Lead Plastic DIP
HA7-5111-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5111-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P5111-5	0°C to +75°C	8 Lead SOIC
HA9P5111-9	-40°C to +85°C	8 Lead SOIC

Schematic



Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Specified

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage 7V
Voltage (at Any Lead) . . . . . $\pm V_{SUPPLY}$
Output Current . . . . . Full Short Circuit Protection
Junction Temperature (Note 8) . . . . . +175°C
Junction Temperature (Plastic Packages) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Operating Temperature Range
HA-5101/5111-2 . . . . . -55°C to +125°C
HA-5101/5111-5 . . . . . 0°C to +75°C
HA-5101/5111-9 . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = +15V, V- = -15V, R_S = 100Ω, R_L = 2kΩ, C_L = 50pF, Unless Otherwise Specified.

PARAMETER	TEMP	HA-5101-2, -5 HA-5111-2, -5			HA-5101-9 HA-5111-9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	0.5	3	-	0.5	3	mV
	Full	-	-	4	-	-	4	mV
Offset Voltage Drift	Full	-	3	-	-	3	-	µV/°C
Bias Current	+25°C	-	100	200	-	100	200	nA
	Full	-	-	325	-	-	325	nA
Offset Current	+25°C	-	30	75	-	30	75	nA
	Full	-	-	125	-	-	125	nA
Input Resistance	+25°C	-	500	-	-	500	-	kΩ
Common Mode Range	Full	±12	-	-	±12	-	-	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 2)	+25°C	-	1000	-	-	1000	-	kV/V
	Full	100	250	-	100	250	-	kV/V
Common Mode Rejection Ratio (Note 3)	Full	80	100	-	80	100	-	dB
Small Signal Bandwidth HA-5101 (A_V = 1)	+25°C	-	10	-	-	10	-	MHz
Minimum Stable Gain								
HA-5101	Full	1	-	-	1	-	-	V/V
HA-5111	Full	10	-	-	10	-	-	V/V
Gain Bandwidth Product HA-5111 (A_V = 10)	+25°C	-	100	-	-	100	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
R_L = 10kΩ	Full	±12	±13	-	±12	±13	-	V
R_L = 2kΩ	Full	±12	±13	-	±12	±13	-	V
(V_{PS} = ±18, R_L = 600)	+25°C	±15	-	-	±15	-	-	V
Output Current (Note 4)	+25°C	25	30	-	25	30	-	mA
Full Power Bandwidth (Note 5)								
HA-5101	+25°C	95	160	-	95	160	-	kHz
HA-5111	+25°C	630	790	-	630	790	-	kHz
Output Resistance	+25°C	-	110	-	-	110	-	Ω
Maximum Load Capacitance	+25°C	-	800	-	-	800	-	pF

Electrical Specifications $V+ = +15V$, $V- = -15V$, $R_S = 100\Omega$, $R_L = 2k\Omega$, $C_L = 50pF$, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEMP	HA-5101-2, -5 HA-5111-2, -5			HA-5101-9 HA-5111-9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 6)								
Rise Time								
HA-5101	+25°C	-	50	100	-	50	100	ns
HA-5111	+25°C	-	30	60	-	30	60	ns
Overshoot								
HA-5101	+25°C	-	20	35	-	20	35	%
HA-5111	+25°C	-	20	40	-	20	40	%
Slew Rate								
HA-5101	+25°C	6	10	-	6	10	-	V/µs
HA-5111	+25°C	40	50	-	40	50	-	V/µs
Settling Time (Note 7)								
HA-5101 0.01%	-	-	2.6	-	-	2.6	-	µs
HA-5111 0.01%	-	-	0.5	-	-	0.5	-	µs
NOISE CHARACTERISTICS (Note 10)								
Input Noise Voltage								
f = 10Hz	+25°C	-	5	7	-	5	7	$nV/\sqrt{Hz}$
f = 1kHz	+25°C	-	3.0	4.0	-	3.0	4.0	$nV/\sqrt{Hz}$
Input Noise Current								
f = 10Hz	+25°C	-	4.0	9	-	4.0	9	$pA/\sqrt{Hz}$
f = 1kHz		-	0.6	2.5	-	0.6	2.5	$pA/\sqrt{Hz}$
Broadband Noise Voltage f = DC to 30kHz	+25°C	-	0.870	-	-	0.870	-	µVrms
POWER SUPPLY CHARACTERISTICS								
Supply Current HA-5101/5111	Full	-	4	6	-	4	7	mA
Power Supply Rejection Ratio (Note 9)	Full	80	100	-	80	100	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $V_{OUT} = \pm 10V$, $R_L = 2K$.
3. $V_{CM} = \pm 10V$.
4. Output current is measured with $V_{OUT} = \pm 15V$ with $V_{SUPPLY} = \pm 18V$.
5. Full power bandwidth is guaranteed by equation: $\text{Full power bandwidth} = \frac{\text{Slew Rate}}{2\pi V_{Peak}}$, $V_{Peak} = 10V$
6. Refer to Test Circuits section of the data sheet.
7. Settling time is measured to 0.01% of final value for a 10V output step, and $A_V = -10$ for HA-5111 and 0.01% of final value for a 10V output step, $A_V = -1$ for HA-5101.
8. See Thermal Constants in "Die Characteristics" text. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below +175°C for hermetic packages, and below +150°C for the plastic packages.
9. Delta $V_{SUPPLY} = \pm 5V$.
10. The limits for these parameters are guaranteed based on lab characterization, and reflect lot-to-lot variation.

Die Characteristics

Transistor Count 54
Die Dimensions . . . . . 69 x 69 x 19 mils
(1800 x 1800 x 480µm)
Substrate Potential* . . . . . V- or Float
Process . . . . . Bipolar DI

* The Substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
HA2-5101/5111 (Can)	114	35
HA3-5101/5111 (PDIP)	94	32
HA4P5101 (PLCC)	74	33
HA7-5101/5111 (CDIP)	115	35
HA9P5101/5111 (SOIC)	157	43

Test Circuits

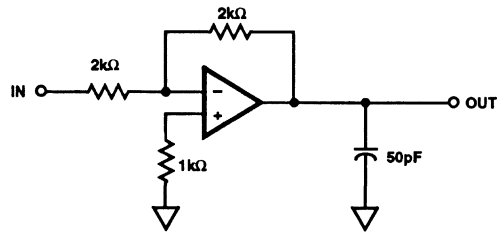


FIGURE 1. HA-5101 LARGE SIGNAL RESPONSE CIRCUIT

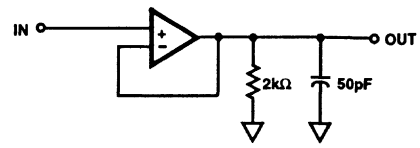
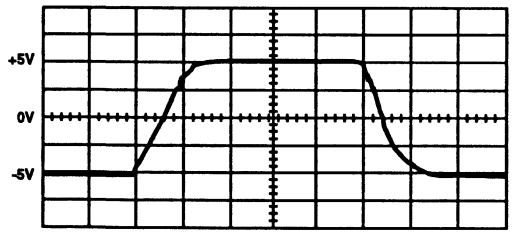
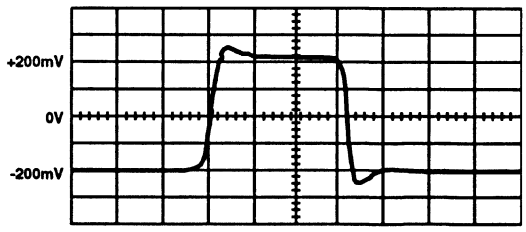


FIGURE 2. HA-5101 SMALL SIGNAL RESPONSE CIRCUIT



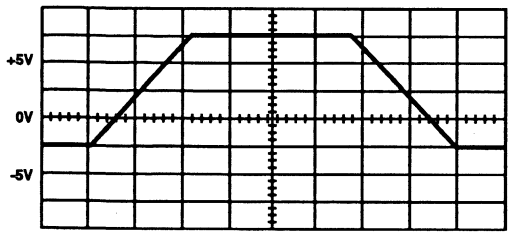
Ch. 1 = 2.5V/Div.
Timebase = 200ns/Div.

FIGURE 3. HA-5111 LARGE SIGNAL TRANSIENT RESPONSE



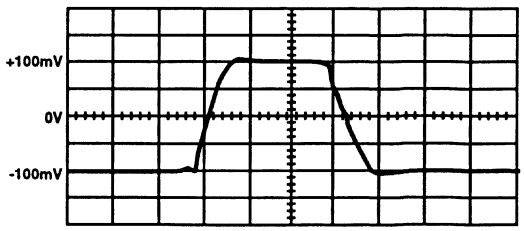
Ch. 1 = 100mV/Div.
Timebase = 100ns/Div.

FIGURE 4. HA-5111 SMALL SIGNAL TRANSIENT RESPONSE



Ch. 1 = 2.5V/Div.
Timebase = 1.00µs/Div.

FIGURE 5. HA-5101 LARGE SIGNAL TRANSIENT RESPONSE



Ch. 1 = 50mV/Div.
Timebase = 100ns/Div.

FIGURE 6. HA-5101 SMALL SIGNAL TRANSIENT RESPONSE

Test Circuits (Continued)

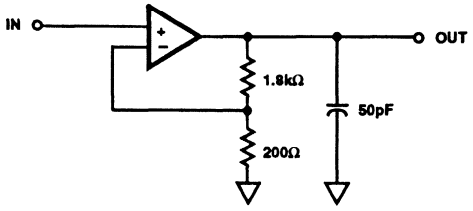


FIGURE 7. HA-5111 LARGE AND SMALL SIGNAL RESPONSE CIRCUIT

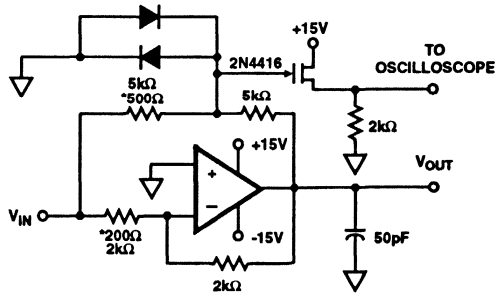


FIGURE 8. SETTLING TIME CIRCUIT

- A_V = -1 (HA-5101), *A_V = -10 (HA-5111)
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional, HP5082-2810 recommended.

Typical Performance Curves

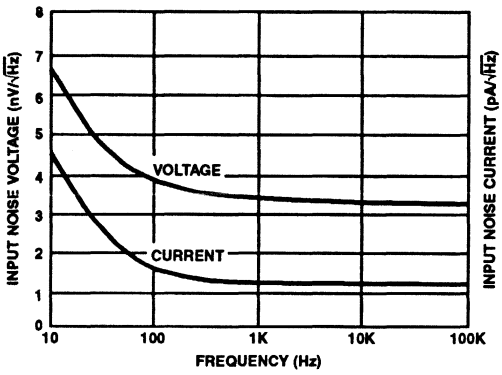


FIGURE 9. HA-5101/11 NOISE SPECTRUM

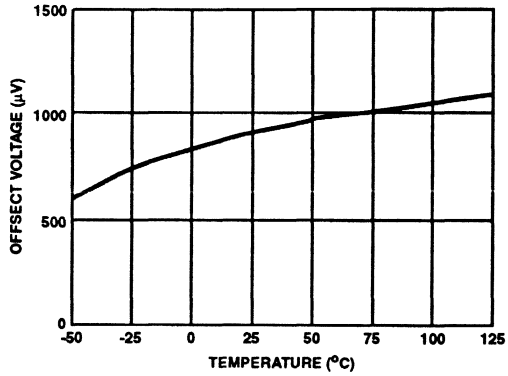
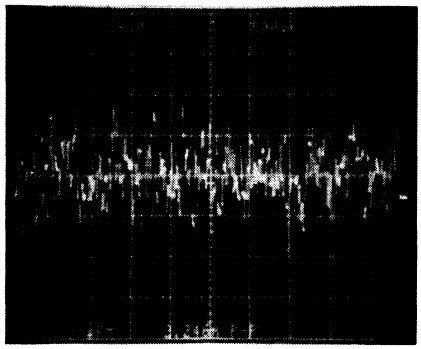
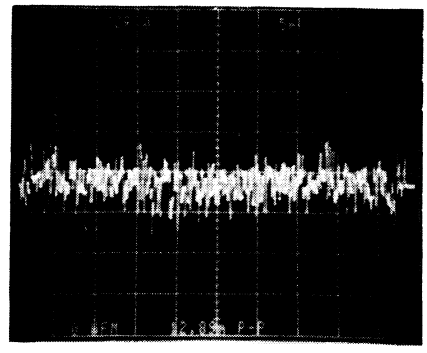


FIGURE 10. OFFSET VOLTAGE vs TEMPERATURE

PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz
A_V = 25000 V_{CC} = ±15V (2.25µVp-p RTO)



PEAK-TO-PEAK TOTAL NOISE 0.1Hz TO 1MHz
A_V = 25000, V_{CC} = ±15V (12.89mVp-p RTO)



Typical Performance Curves (Continued)

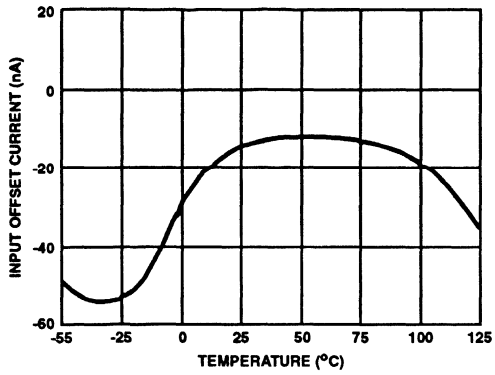


FIGURE 11. INPUT OFFSET CURRENT vs TEMPERATURE

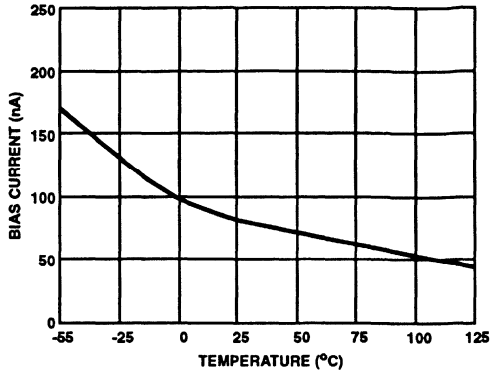


FIGURE 12. INPUT BIAS CURRENT vs TEMPERATURE

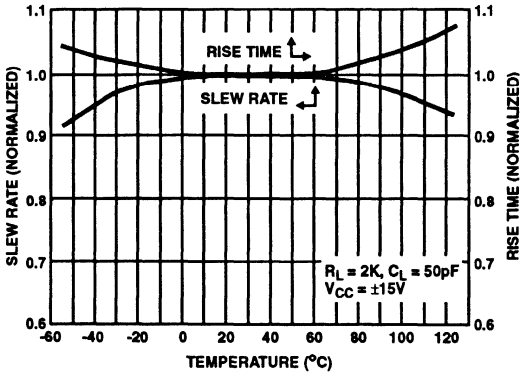


FIGURE 13. SLEW RATE/RISE TIME vs TEMPERATURE

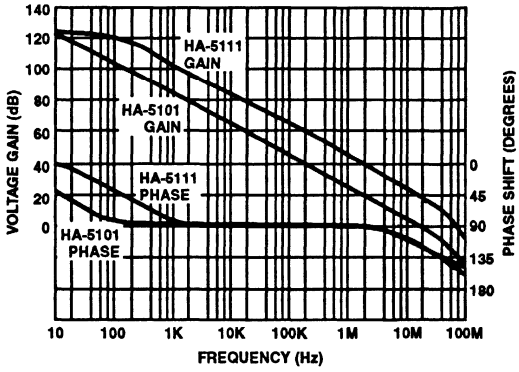


FIGURE 14. OPEN-LOOP GAIN/PHASE vs FREQUENCY

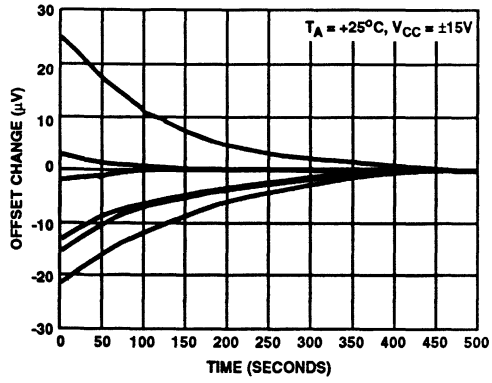


FIGURE 15. INPUT OFFSET WARMUP DRIFT vs TIME (Normalizd To Zero Final Value) (Six Representative Units)

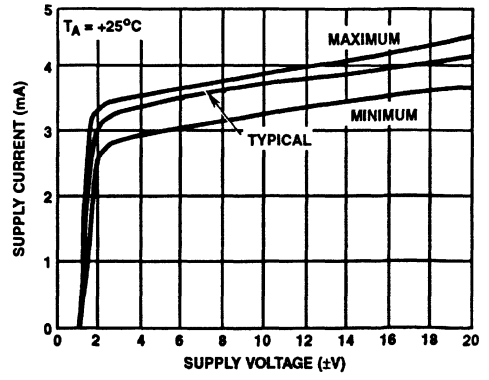


FIGURE 16. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

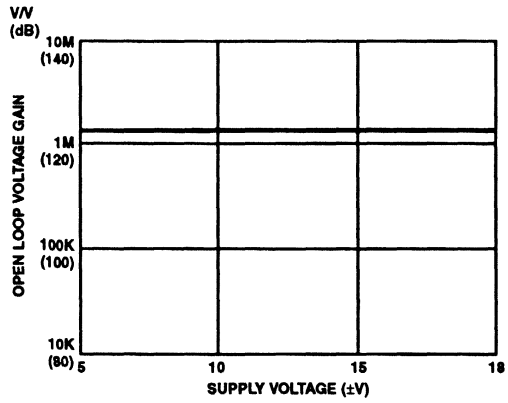


FIGURE 17. DC OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE

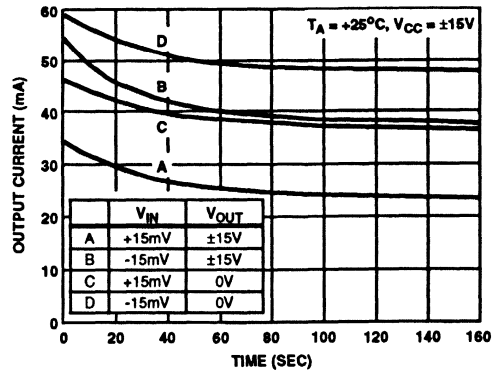


FIGURE 18. SHORT CIRCUIT CURRENT vs TIME

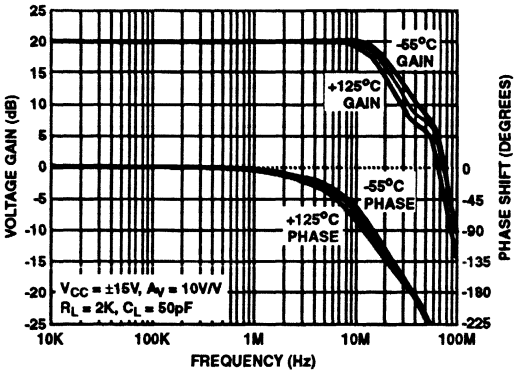


FIGURE 19. HA-5111 CLOSED-LOOP GAIN AND PHASE AT HIGH AND LOW TEMPERATURE (Typical Response of One Amplifier)

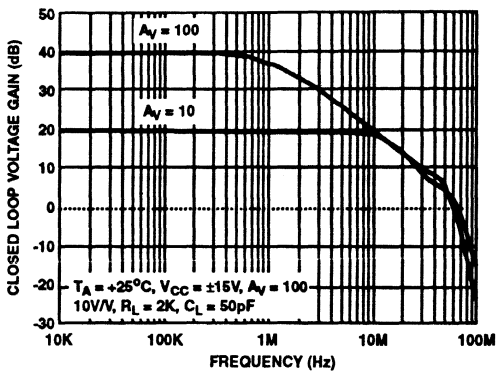


FIGURE 20. HA-5111 CLOSED-LOOP VOLTAGE GAIN vs FREQUENCY AT DIFFERENT CLOSED-LOOP GAINS

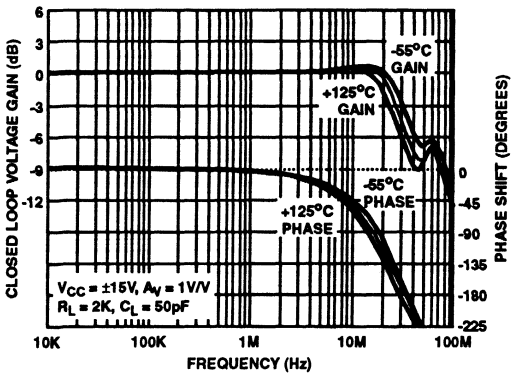


FIGURE 21. HA-5101 CLOSED-LOOP GAIN AND PHASE AT HIGH AND LOW TEMPERATURE (Typical Response Of One Amplifier)

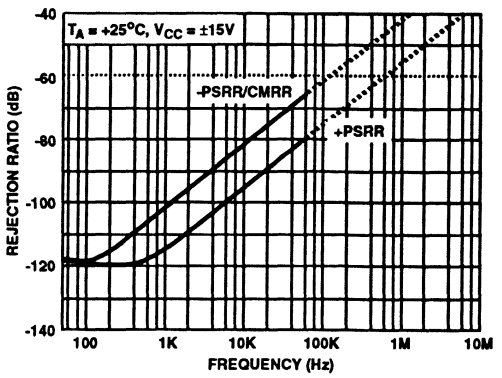


FIGURE 22. HA-5111 REJECTION RATIOS vs FREQUENCY

Typical Performance Curves (Continued)

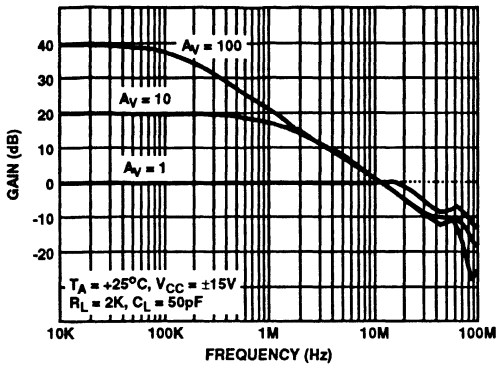


FIGURE 23. HA-5101 CLOSED-LOOP VOLTAGE GAIN vs FREQUENCY AT DIFFERENT CLOSED-LOOP GAINS

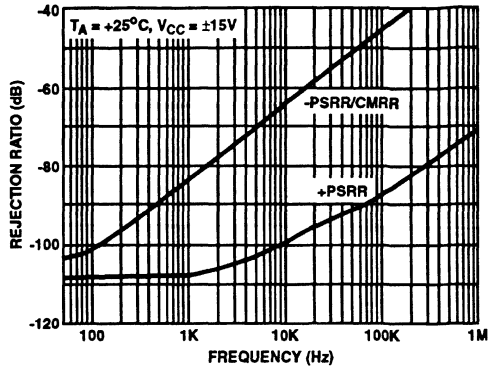


FIGURE 24. HA-5101 REJECTION RATIOS vs FREQUENCY

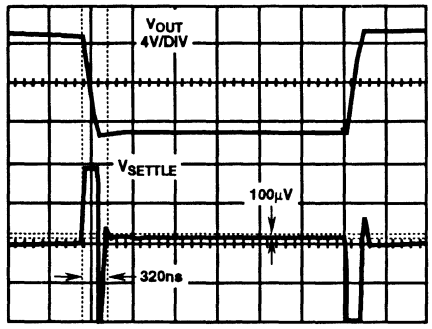


FIGURE 25. HA-5111 SETTLING WAVEFORM 500ns/DIV.

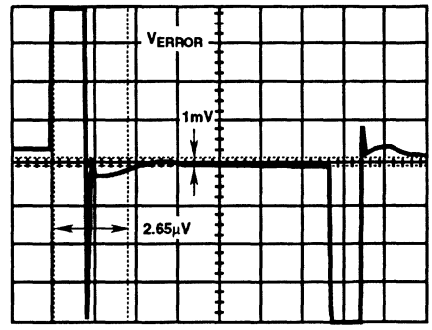


FIGURE 26. HA-5101 SETTLING WAVEFORM 1.5µs/DIV

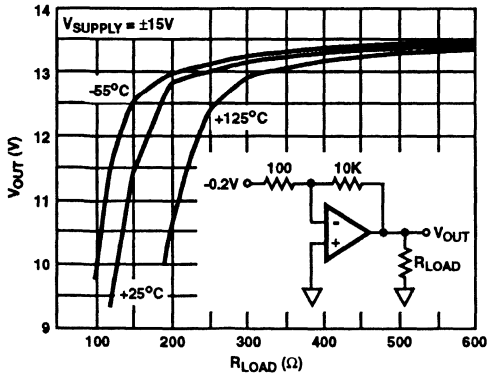


FIGURE 27. HA-5101 V_{OUT} vs R_L

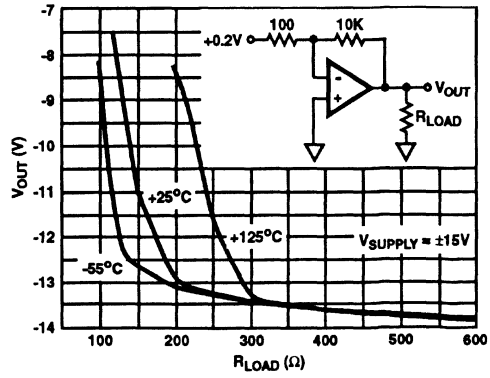


FIGURE 28. HA-5101 V_{OUT} vs R_L

Applications Information

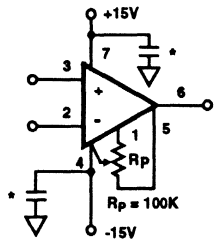
Operation At ±5V Supply

The HA-5101/11 performs well at V_{CC} = ±5V exhibiting typical characteristics as listed below:

I_{CC}	3.7	mA
V_{IO}	0.5	mV
I_{BIAS}	56	nA
A_{VOL} (V_O = ±3V)	106	kV/V
V_{OUT}	3.7	V
I_{OUT}	13	mA
CMRR (ΔV_{CM} = ±2.5V)	90	dB
PSRR (ΔV_{CC} = 0.5V)	90	dB
Unity Bandwidth (5101)	10	MHz
GBW (5111)	100	MHz
Slew Rate (5101)	7	V/µs
Slew Rate (5111)	40	V/µs

Offset Adjustment

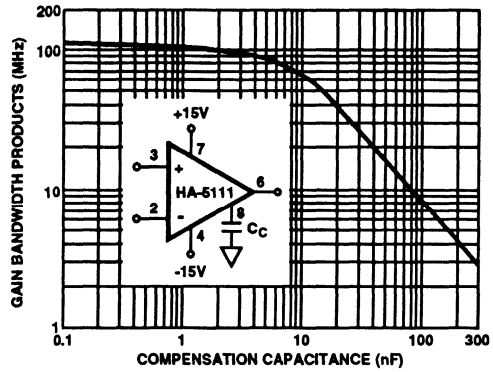
* The following is the recommended V_{IO} adjust configuration:



* Proper decoupling is always recommended, 0.1µF high quality capacitor should be at or very near the device's supply pins.

Compensation

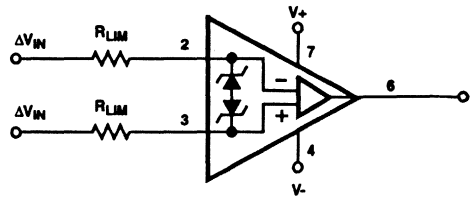
An external compensation capacitor can be used with the HA-5111 connected between pin 8 and ground (or V-, V+ not Recommended). A plot of gain bandwidth product vs compensation capacitor has been included as a design aid. The capacitor should be a high frequency type mounted near the device leads to minimize parasitics.



Input Protection

The HA-5101/11 has built-in back-to-back protection diodes which will limit the differential input voltage to approximately 7V. If the 5101/11 will be used in conditions where that voltage may be exceeded, then current limiting resistors must be used. No more than 25mA should be allowed to flow in the HA-5101/11's input.

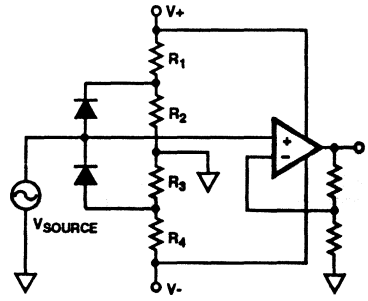
Comparator Circuit



Choose R_{LIM} Such That: $\frac{(\Delta V_{INMAX} - 7V)}{25mA} \leq 2R_{LIM}$

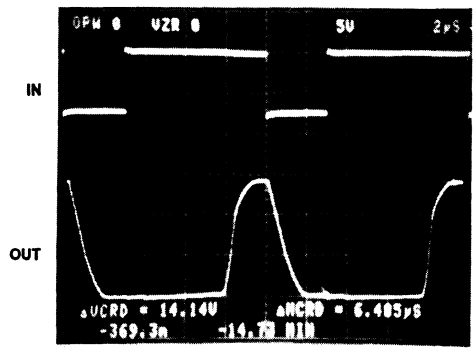
Output Saturation

When an op amp is overdriven, output devices can saturate and sometimes take a long time to recover. Saturation can be avoided (sometimes) by using circuits such as:



If saturation cannot be avoided the HA-5101/11 recovers from a 25% overdrive in about 6.5µs (see photos).

Top: Input
Bottom: Output, 5V/Div., 2µs/Div.



Output is overdriven negative and recovers in 6µs.

HARRIS SEMICONDUCTOR

HA-5102, HA-5104 HA-5112, HA-5114

Low Noise, High Performance Operational Amplifiers

April 1993

Features

- Low Noise . . . . . 4.3nV/√Hz
- Wide Bandwidth . . . . 8MHz (Compensated) 60MHz (Uncompensated)
- High Slew Rate . . . . . 3V/µs (Compensated) 20V/µs (Uncompensated)
- Low Offset Voltage 0.5mV
- Available in Duals or Quads

Applications

- High Q, Active Filters
- Audio Amplifiers
- Instrumentation Amplifiers
- Integrators
- Signal Generators
- For Further Design Ideas, See Application Note 554

Description

Low noise and high performance are key words describing HA-5102/04/12/14. These general purpose amplifiers offer an array of dynamic specifications ranging from a 3V/µs slew rate and 8MHz bandwidth (5102/04) to 20V/µs slew rate and 60MHz gain-bandwidth-product (HA-5112/14). Complementing these outstanding parameters is a very low noise specification of 4.3nV/√Hz at 1kHz.

Fabricated using the Harris high frequency DI process, these operational amplifiers also offer excellent input specifications such as a 0.5mV offset voltage and 30nA offset current. Complementing these specifications are 108dB open loop gain and 60dB channel separation. Consuming a very modest amount of power (90mW/ package for duals and 150mW/package for quads), HA-5102/04/12/14 also provide 15mA of output current.

This impressive combination of features make this series of amplifiers ideally suited for designs ranging from audio amplifiers and active filters to the most demanding signal conditioning and instrumentation circuits.

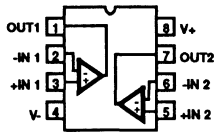
These operational amplifiers are available in dual or quad form with industry standard pinouts allowing for immediate inter-changeability with most other dual and quad operational amplifiers.

HA-5102	Dual, Comp.	HA-5104	Quad, Comp.
HA-5112	Dual, Uncomp.	HA-5114	Quad, Uncomp.

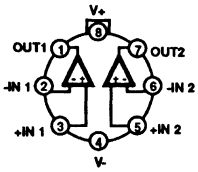
Refer to the /883 data sheet for military product.

Pinouts (See Ordering Information on Next Page)

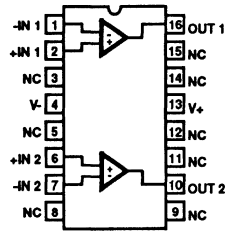
HA-5102/5112 (PDIP, CDIP) TOP VIEW



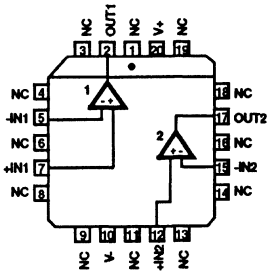
HA-5102/5112 (TO-99 METAL CAN) TOP VIEW



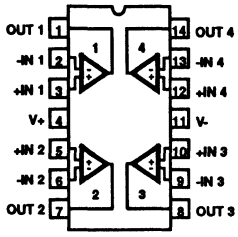
HA-5102/5112 (300 MIL SOIC) TOP VIEW



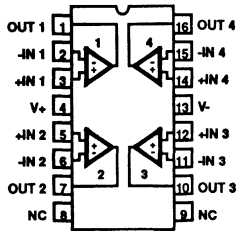
HA-5102 (PLCC) TOP VIEW



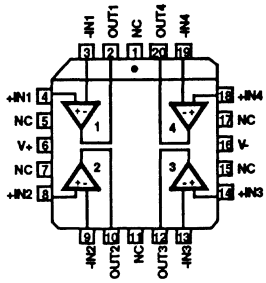
HA-5104/5114 (PDIP, CDIP) TOP VIEW



HA-5104/5114 (300 MIL SOIC) TOP VIEW



HA-5104/5114 (PLCC) TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

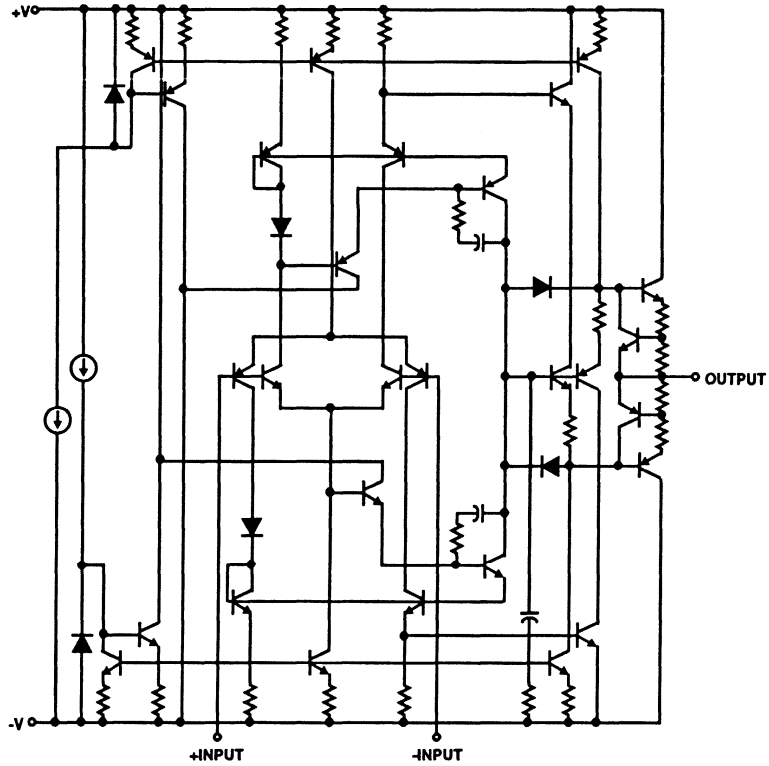
File Number **2925.1**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-5102-2	-55°C to +125°C	8 Pin Can
HA2-5102-5	0°C to +75°C	8 Pin Can
HA3-5102-5	0°C to +75°C	8 Lead Plastic DIP
HA4P5102-5	0°C to +75°C	20 Lead PLCC
HA7-5102-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5102-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P5102-5	0°C to +75°C	16 Lead Widebody SOIC
HA9P5102-9	-40°C to +85°C	16 Lead Widebody SOIC
HA1-5104-2	-55°C to +125°C	14 Lead Ceramic DIP
HA1-5104-5	0°C to +75°C	14 Lead Ceramic DIP
HA3-5104-5	0°C to +75°C	14 Lead Plastic DIP
HA4P5104-5	0°C to +75°C	20 Lead PLCC
HA9P5104-5	0°C to +75°C	16 Lead Widebody SOIC
HA9P5104-9	-40°C to +85°C	16 Lead Widebody SOIC

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-5112-2	-55°C to +125°C	8 Pin Can
HA2-5112-5	0°C to +75°C	8 Pin Can
HA3-5112-5	0°C to +75°C	8 Lead Plastic DIP
HA7-5112-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5112-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P5112-5	0°C to +75°C	16 Lead Widebody SOIC
HA9P5112-9	-40°C to +85°C	16 Lead Widebody SOIC
HA1-5114-2	-55°C to +125°C	14 Lead Ceramic DIP
HA1-5114-5	0°C to +75°C	14 Lead Ceramic DIP
HA3-5114-5	0°C to +75°C	14 Lead Plastic DIP
HA4P5114-5	0°C to +75°C	20 Lead PLCC
HA9P5114-5	0°C to +75°C	16 Lead Widebody SOIC
HA9P5114-9	-40°C to +85°C	16 Lead Widebody SOIC

Simplified Schematic



Absolute Maximum Ratings (Note 1)

T_A = +25°C, Unless Otherwise Stated

Supply Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage 7V
Input Voltage (Note 2) ..... ±15V
Output Short Circuit Duration (Note 3) ..... Indefinite
Junction Temperature (Note 4) ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Ranges
HA-5102/5104/5112/5114-2 ..... -55°C ≤ T_A ≤ +125°C
HA-5102/5104/5112/5114-5 ..... 0°C ≤ T_A ≤ +75°C
HA-5102/5104/5112/5114-9 ..... -40°C ≤ T_A ≤ +85°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = 15V D.C., V- = -15V D.C., Unless Otherwise Specified

PARAMETER	TEMP	HA-5102-2, -5 HA-5112-2, -5			HA-5104-2, -5 HA-5114-2, -5			HA-5102-9 HA-5112-9			HA-5104-9 HA-5114-9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS														
Offset Voltage	+25°C	-	0.5	2.0	-	0.5	2.5	-	0.5	2.0	-	0.5	2.5	mV
	Full	-	-	2.5	-	-	3.0	-	-	2.5	-	-	3.0	mV
Offset Voltage Average Drift	Full	-	3	-	-	3	-	-	3	-	-	3	-	µV/°C
Bias Current	+25°C	-	130	200	-	130	200	-	130	200	-	130	200	nA
	Full	-	-	325	-	-	325	-	-	500	-	-	500	nA
Offset Current	+25°C	-	30	75	-	30	75	-	30	75	-	30	75	nA
	Full	-	-	125	-	-	125	-	-	125	-	-	125	nA
Input Resistance	+25°C	-	500	-	-	500	-	-	500	-	-	500	-	kΩ
Common Mode Range	Full	±12	-	-	±12	-	-	±12	-	-	±12	-	-	V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 5)	+25°C	100	250	-	100	250	-	80	250	-	80	250	-	kV/V
	Full	100	-	-	100	-	-	80	-	-	80	-	-	kV/V
Common Mode Rejection Ratio (Note 6)	Full	86	95	-	86	95	-	80	95	-	80	95	-	dB
Small Signal Bandwidth HA-5102/5104 (A_V = 1)	+25°C	-	8	-	-	8	-	-	8	-	-	8	-	MHz
Gain Bandwidth Product HA-5112/5114 (A_V = 10)	+25°C	-	60	-	-	60	-	-	60	-	-	60	-	MHz
Channel Separation (Note 7)	+25°C	-	60	-	-	60	-	-	60	-	-	60	-	dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (R_L = 10kΩ)	Full	±12	±13	-	±12	±13	-	±12	±13	-	±12	±13	-	V
(R_L = 2kΩ)	Full	±10	±12	-	±10	±12	-	±10	±12	-	±10	±12	-	V
Output Current (Note 8)	Full	±10	±15	-	±10	±15	-	±7	±15	-	±7	±15	-	mA
Full Power Bandwidth (Note 9) HA-5102/5104	+25°C	16	47	-	16	47	-	16	47	-	16	47	-	kHz
HA-5112/5114	+25°C	191	318	-	191	318	-	191	318	-	191	318	-	kHz
Output Resistance	+25°C	-	110	-	-	110	-	-	110	-	-	110	-	Ω
STABILITY														
Minimum Stable Closed Loop Gain HA-5102/5104	Full	1	-	-	1	-	-	1	-	-	1	-	-	V/V
HA-5112/5114	Full	10	-	-	10	-	-	10	-	-	10	-	-	V/V

Electrical Specifications V+ = 15V D.C., V- = -15V D.C., Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	HA-5102-2, -5 HA-5112-2, -5			HA-5104-2, -5 HA-5114-2, -5			HA-5102-9 HA-5112-9			HA-5104-9 HA-5114-9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 10)														
Rise Time														
HA-5102/5104	+25°C	-	108	200	-	108	200	-	108	200	-	108	200	ns
HA-5112/5114	+25°C	-	48	100	-	48	100	-	48	100	-	48	100	ns
Overshoot														
HA-5102/5104	+25°C	-	20	35	-	20	35	-	20	35	-	20	35	%
HA-5112/5114	+25°C	-	30	40	-	30	40	-	30	40	-	30	40	%
Slew Rate														
HA-5102/5104	+25°C	1	3	-	1	3	-	1	3	-	1	3	-	V/µs
HA-5112/5114	+25°C	12	20	-	12	20	-	12	20	-	12	20	-	V/µs
Settling Time (Note 11)														
HA-5102/5104	+25°C	-	4.5	-	-	4.5	-	-	4.5	-	-	4.5	-	µs
HA-5112/5114	+25°C	-	0.6	-	-	0.6	-	-	0.6	-	-	0.6	-	µs
NOISE CHARACTERISTICS (Note 12)														
Input Noise Voltage														
f = 10Hz	+25°C	-	9	25	-	9	25	-	9	25	-	9	25	$nV/\sqrt{Hz}$
f = 1kHz	+25°C	-	4.3	6.0	-	4.3	6.0	-	4.3	6.0	-	4.3	6.0	$nV/\sqrt{Hz}$
Input Noise Current														
f = 10Hz	+25°C	-	5.1	15	-	5.1	15	-	5.1	15	-	5.1	15	$pA/\sqrt{Hz}$
f = 1kHz	+25°C	-	0.57	3	-	0.57	3	-	0.57	3	-	0.57	3	$pA/\sqrt{Hz}$
Broadband Noise Voltage														
f = DC to 30kHz	+25°C	-	870	-	-	870	-	-	870	-	-	870	-	nV_{RMS}
POWER SUPPLY CHARACTERISTICS														
Supply Current	+25°C	-	3.0	5.0	-	5.0	6.5	-	3.0	5.0	-	5.0	6.5	mA
Power Supply Rejection Ratio (Note 6)	Full	86	100	-	86	100	-	80	100	-	80	100	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages < ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. See thermal constants in "Die Characteristics" section. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below +175°C for hermetic packages, and below +150°C for plastic packages.
5. V_{OUT} = ±10V, R_L = 2kΩ.
6. V_{CM} = ±5.0V .
7. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 100mV peak; R_S = 1kΩ. (Refer to Channel Separation vs. Frequency Curve for test circuits.).
8. Output current is measured with V_{OUT} = ±5V.
9. Full power bandwidth is guaranteed by equation: Full power bandwidth $= \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
10. Refer to Test Circuits section of the data sheet.
11. Settling time is measured to 0.1% of final value for a 1 volt input step, and A_V = -10 for HA-5112/5114, and a 10V input step, A_V = -1 for HA-5102/5104.
12. The limits for these parameters are guaranteed based on lab characterization, and reflect lot-to-lot variation.

Die Characteristics

Transistor Count
- HA-5102/5112 93
- HA-5104/5114 175

Die Dimensions
- HA-5102/5112 . . . . . 98.4 x 67.3 x 19 mils (2500 x 1710 x 480µm)
- HA-5104/5114 . . . . . 99.6 x 95.3 x 19 mils (2530 x 2420 x 480µm)

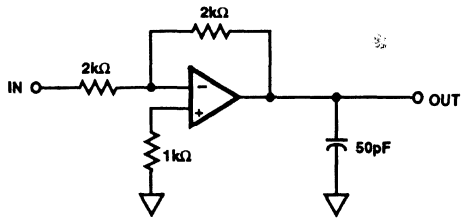
Substrate Potential* . . . . . V-
Process . . . . . Bipolar-DI
Passivation . . . . . Nitride

* The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
HA2-5102/5112 (CAN)	108	33
HA3-5102/5112 (PDIP)	92	30
HA4P5102 (PLCC)	74	33
HA7-5102/5112 (CDIP)	114	34
HA9P5102/5112 (SOIC)	112	35
HA1-5104/5114 (CDIP)	71	13
HA3-5104/5114 (PDIP)	86	25
HA4P5104/5114 (PLCC)	74	32
HA9P5104/5114 (SOIC)	96	26

Test Circuits

HA-5102, HA5104



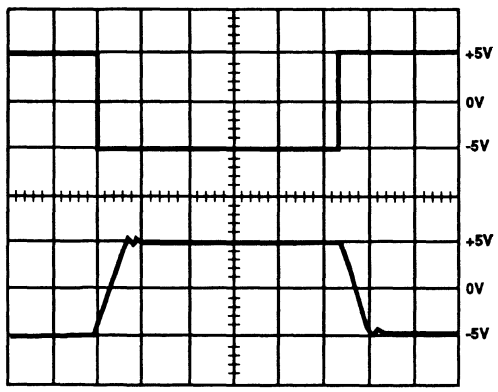
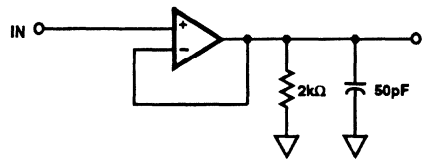


FIGURE 1. LARGE SIGNAL RESPONSE CIRCUIT
Volts: 5V/Div., Time: 5µs/Div. (A_V = -1)



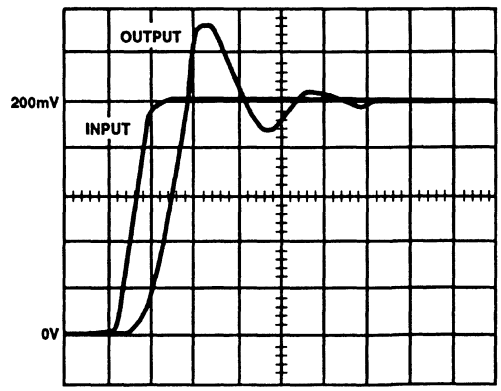
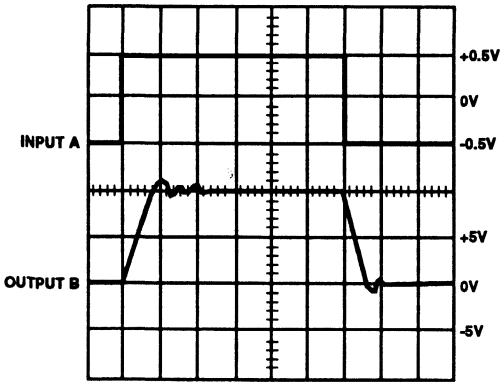


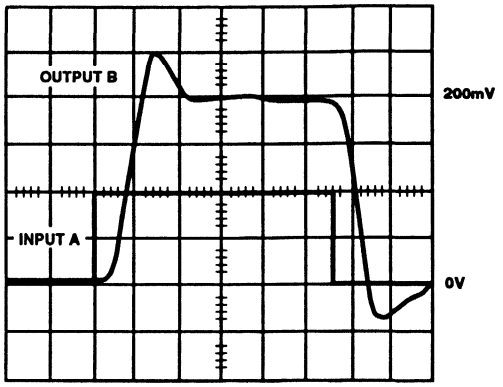
FIGURE 2. SMALL SIGNAL RESPONSE CIRCUIT
Volts: 40mV/Div., Time: 50ns/Div. (A_V = +1)

Test Circuits (Continued)

HA-5112, HA5114



Volts: Input A: 0.5V/Div., Output B: 5V/Div. Time: 50ns/Div.



Volts: Input A: 0.01V/Div., Output B: 50mV/Div. Time: 50ns/Div.

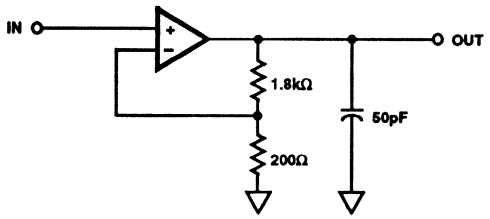
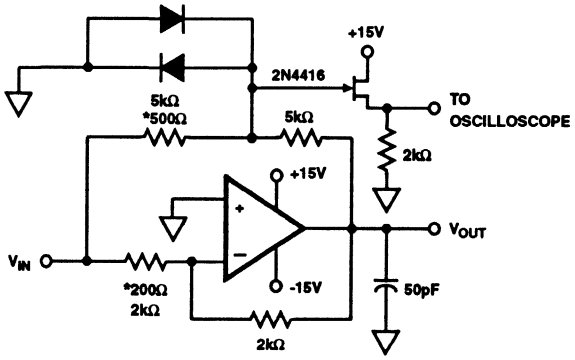


FIGURE 3. LARGE AND SMALL SIGNAL RESPONSE CIRCUIT
(A_V = +10)



- A_V = -1 (HA-5102/5104), *A_V = -10 (HA-5112/5114)
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional, HP5082-2810 recommended.

FIGURE 4. SETTLING TIME CIRCUIT

Typical Performance Curves

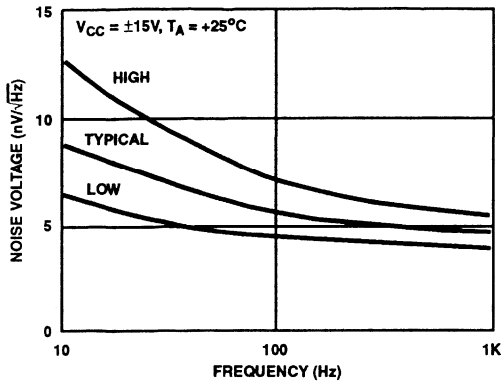


FIGURE 5. INPUT NOISE VOLTAGE DENSITY

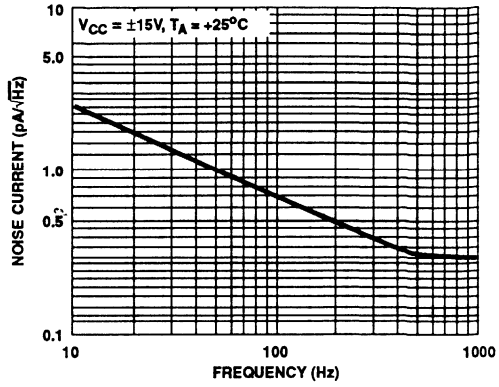


FIGURE 6. INPUT NOISE CURRENT DENSITY

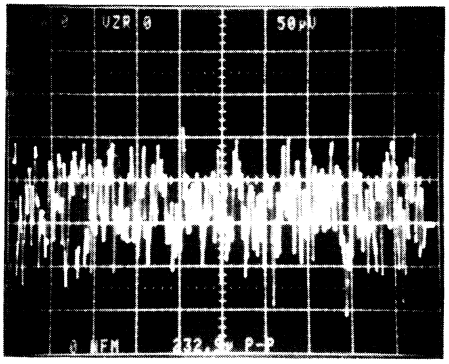


FIGURE 7. 0.1Hz TO 10Hz NOISE
V_{CC} = ±15V, T_A = +25°C, 50µV/Div., 1s/Div., A_V = 1000V/V
Input Noise = 0.232μV_{P-P}

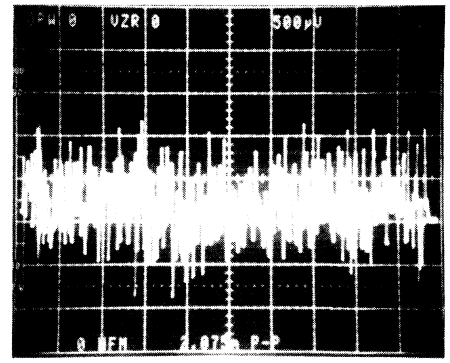


FIGURE 8. 0.1Hz TO 1MHz NOISE
V_{CC} = ±15V, T_A = +25°C, 500µV/Div., 1s/Div., A_V = 1000V/V
Total Output Noise = 2.075μV_{P-P}

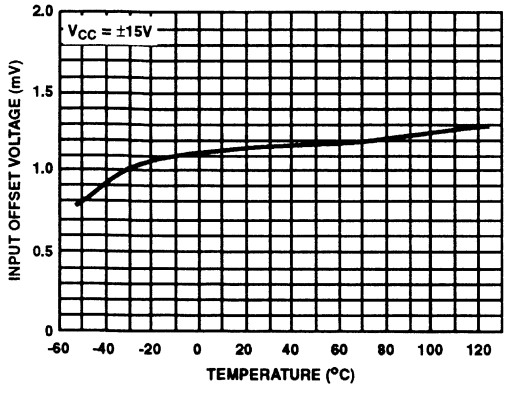


FIGURE 9. V_{IO} vs TEMPERATURE

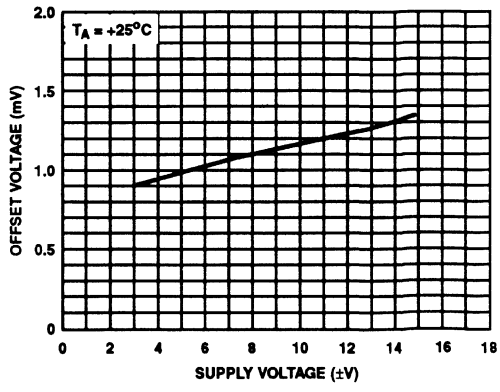


FIGURE 10. V_{IO} vs V_{CC}

Typical Performance Curves (Continued)

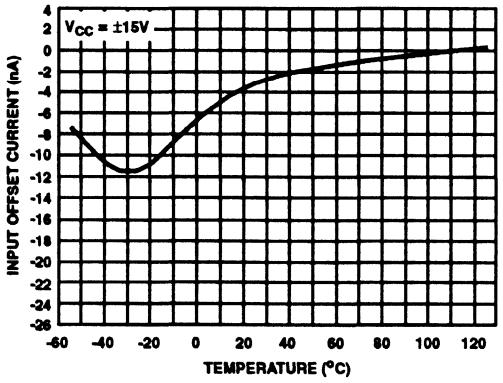


FIGURE 11. I_{IO} vs TEMPERATURE

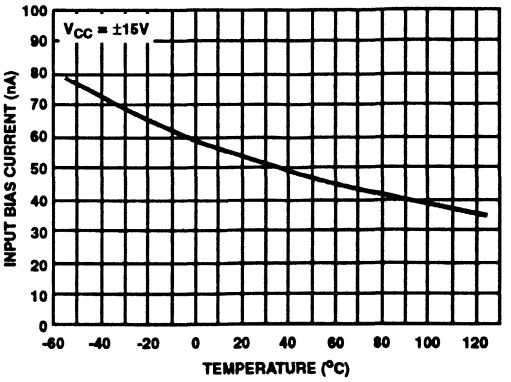


FIGURE 12. I_{BIAS} vs TEMPERATURE

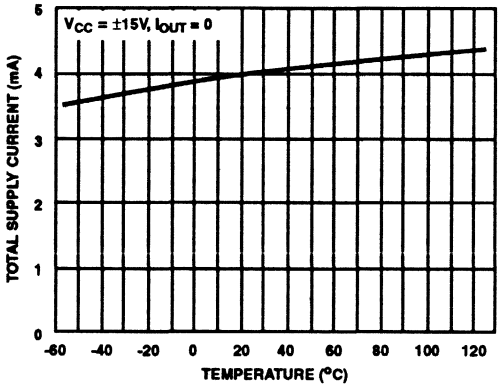


FIGURE 13. I_{CC} vs TEMPERATURE (HA-5104/14)

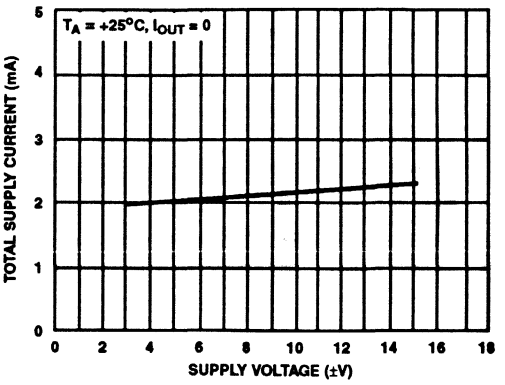


FIGURE 14. I_{CC} vs V_{CC} (HA-5102/12)

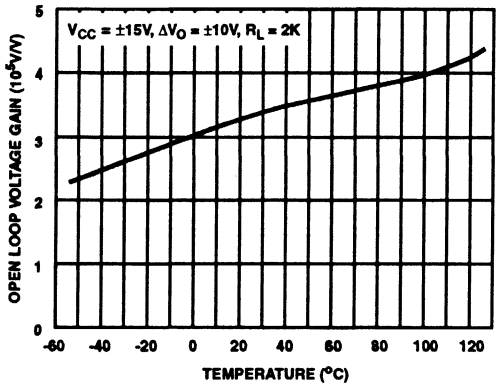


FIGURE 15. A_{VOL} vs TEMPERATURE

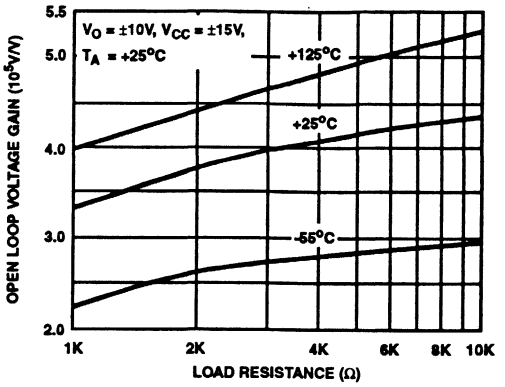


FIGURE 16. A_{VOL} vs LOAD RESISTANCE

Typical Performance Curves (Continued)

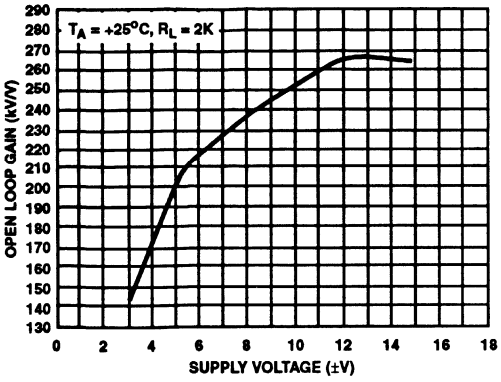


FIGURE 17. A_{VOL} vs V_{CC}

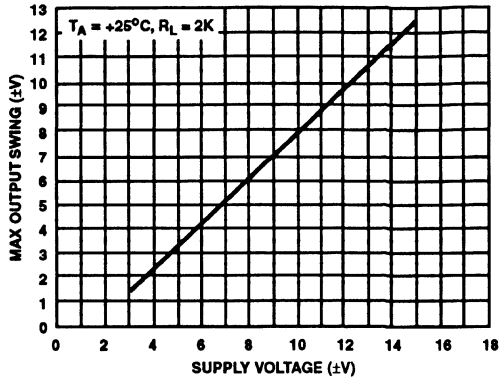


FIGURE 18. V_{OUT} vs V_{CC}

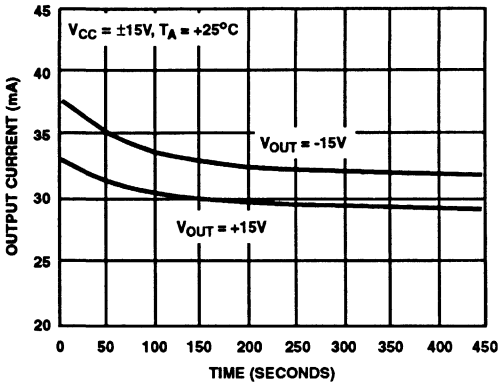


FIGURE 19. OUTPUT SHORT CIRCUIT CURRENT vs TIME

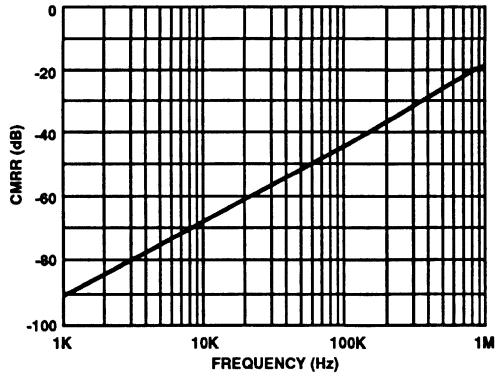


FIGURE 20. CMRR vs FREQUENCY

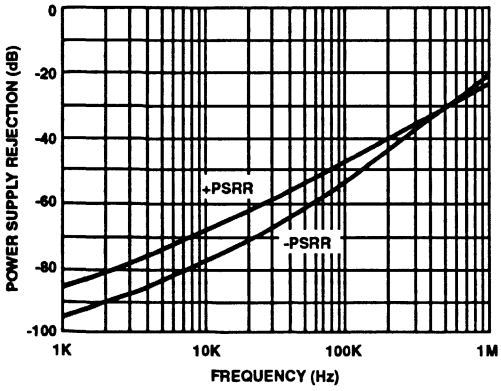


FIGURE 21. PSRR vs FREQUENCY

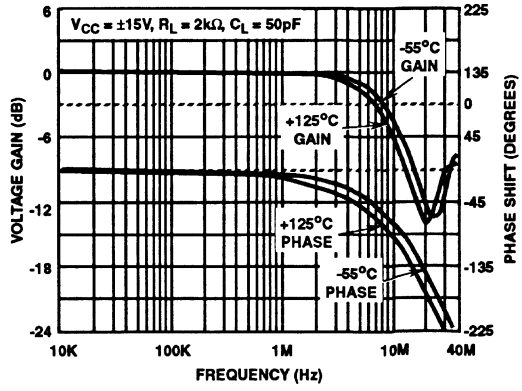


FIGURE 22. HA-5104/02 UNITY GAIN FREQUENCY RESPONSE

Typical Performance Curves (Continued)

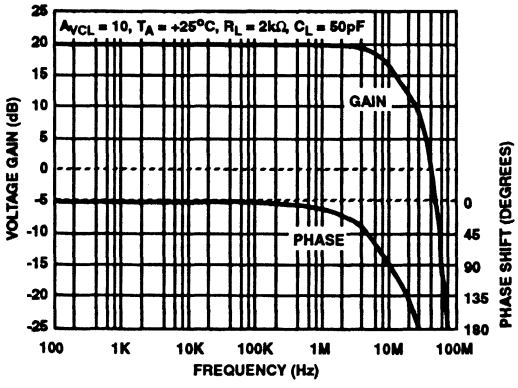


FIGURE 23. HA-5112/14 FREQUENCY RESPONSE

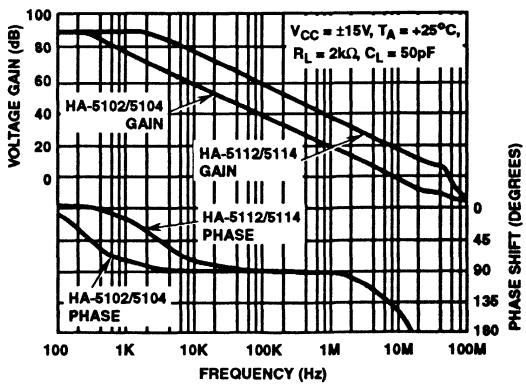


FIGURE 24. OPEN LOOP GAIN vs FREQUENCY

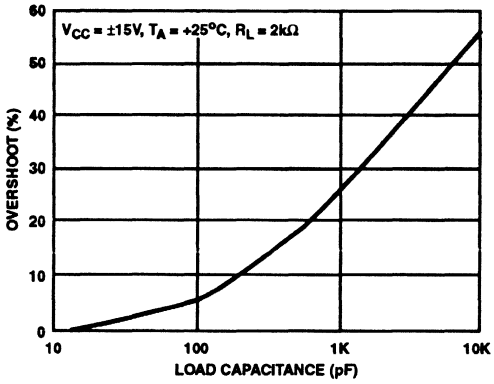


FIGURE 25. SMALL SIGNAL OVERSHOOT vs C_{LOAD}

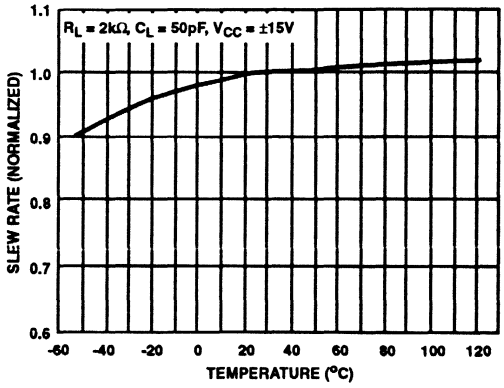


FIGURE 26. SLEW RATE vs TEMPERATURE

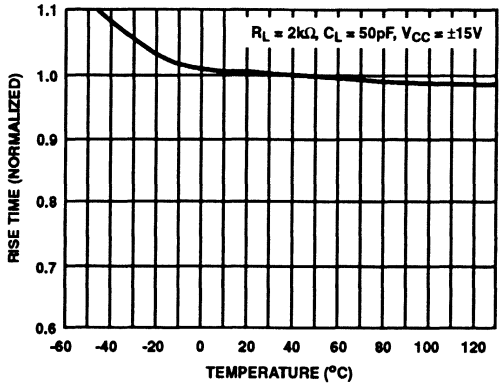


FIGURE 27. RISE TIME vs TEMPERATURE

HARRIS SEMICONDUCTOR

HA-5127

Ultra-Low Noise Precision Operational Amplifier

March 1993

Features

- High Speed 10V/μs
- Wide Unity Gain Bandwidth 8.5MHz
- Low Noise ..... 3nV/√Hz at 1kHz
- Low V_{OS} 10μV
- High CMRR 126dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-5127-2	-55°C to +125°C	8 Pin CAN
HA2-5127-5	0°C to +75°C	8 Pin CAN
HA2-5127A-2	-55°C to +125°C	8 Pin CAN
HA2-5127A-5	0°C to +75°C	8 Pin CAN
HA3-5127A-5	0°C to +75°C	8 Lead Plastic DIP
HA7-5127-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5127-5	0°C to +75°C	8 Lead Ceramic DIP
HA7-5127A-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5127A-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P5127-5	0°C to +75°C	8 Lead SOIC

Description

The HA-5127 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3nV/√Hz) precision instrumentation performance with high speed (10V/μs) wideband capability.

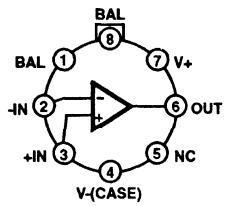
This amplifier's impressive list of features include low V_{OS} (10μV), wide unity gain-bandwidth (8.5MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140mW of power.

Using the HA-5127 allows designers to minimize errors while maximizing speed and bandwidth.

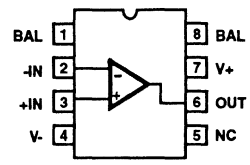
This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5127's qualities include instrumentation amplifiers, pulse amplifiers, audio preamplifiers, and signal conditioning circuits. This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37. For the military grade product, refer to the HA-5127/883 data sheet.

Pinouts

HA-5127
(TO-99 METAL CAN)
TOP VIEW



HA-5127
(PDIP, CDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2906.1**

Specifications HA-5127, HA-5127A

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated
Supply Voltage Between V+ and V- Terminals 44V
Differential Input Voltage (Note 2) 0.7V
Output Current ..... Full Short Circuit Protection
Junction Temperature (Note 13) ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-5127/27A-2 ..... -55°C ≤ T_A ≤ +125°C
HA5127/27A-5 ..... 0°C ≤ T_A ≤ +75°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = 15V, V- = -15V, C_L < 50pF, R_S < 100Ω

PARAMETER	TEMP	HA-5127A			HA-5127			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	10	25	-	30	100	µV
	Full	-	30	60	-	70	300	µV
Average Offset Voltage Drift	Full	-	0.2	0.6	-	0.4	1.8	µV/°C
Bias Current	+25°C	-	±10	±40	-	±15	±80	nA
	Full	-	±20	±60	-	±35	±150	nA
Offset Current	+25°C	-	7	35	-	12	75	nA
	Full	-	15	50	-	30	135	nA
Common Mode Range	Full	±10.3	±11.5	-	±10.3	±11.5	-	V
Differential Input Resistance (Note 3)	+25°C	1.5	6	-	0.8	4	-	MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 4)	+25°C	-	0.08	0.18	-	0.09	0.25	μV_{P-P}
Input Noise Voltage Density (Note 5)								
f = 10Hz	+25°C	-	3.5	5.5	-	3.8	8.0	$nV/\sqrt{Hz}$
f = 100Hz		-	3.1	4.5	-	3.3	5.6	$nV/\sqrt{Hz}$
f = 1000Hz		-	3.0	3.8	-	3.2	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 5)								
f = 10Hz	+25°C	-	1.7	4.0	-	1.7	-	$pA/\sqrt{Hz}$
f = 100Hz		-	1.0	2.3	-	1.0	-	$pA/\sqrt{Hz}$
f = 1000Hz		-	0.4	0.6	-	0.4	0.6	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 6)	+25°C	1000	1800	-	700	1500	-	V/mV
	Full	600	1200	-	300	800	-	V/mV
Common Mode Rejection Ratio (Note 7)	Full	114	126	-	100	120	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	V/V
Unity-Gain-Bandwidth	+25°C	5	8.5	-	5	8.5	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
R_L = 600Ω	+25°C	±10.0	±11.5	-	±10.0	±11.5	-	V
R_L = 2kΩ	Full	±11.7	±13.8	-	±11.5	±13.5	-	V

Electrical Specifications $V+ = 15V$, $V- = -15V$, $C_L < 50pF$, $R_S < 100\Omega$ **(Continued)**

PARAMETER	TEMP	HA-5127A			HA-5127			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Full Power Bandwidth (Note 8)	+25°C	111	160	-	111	160	-	kHz
Output Resistance, Open Loop	+25°C	-	70	-	-	70	-	Ω
Output Current	+25°C	16.5	25	-	16.5	25	-	mA
TRANSIENT RESPONSE (Note 9)								
Rise Time	+25°C	-	-	150	-	-	150	ns
Slew Rate (Note 11)	+25°C	7	10	-	7	10	-	V/µs
Settling Time (Note 10)	+25°C	-	1.5	-	-	1.5	-	µs
Overshoot	+25°C	-	20	40	-	20	40	%
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	3.5	-	-	3.5	-	mA
	Full	-	-	4.0	-	-	4.0	mA
Power Supply Rejection Ratio (Note 12)	Full	-	2	4	-	16	51	µV/V

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. The limits for this parameter are guaranteed based on lab characterization, and reflect lot-to-lot variation.
6. $V_{OUT} = \pm 10V$, $R_L = 2k\Omega$
7. $V_{CM} = \pm 10V$
8. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
9. Refer to Test Circuits section of the data sheet.
10. Settling time is specified to 0.1% of final value for a 10V output step and $A_V = -1$.
11. V_{OUT} = 10V Step
12. $V_S = \pm 4.5V$ to $\pm 18V$
13. See Thermal Constants in "Die Characteristics" section.

Die Characteristics

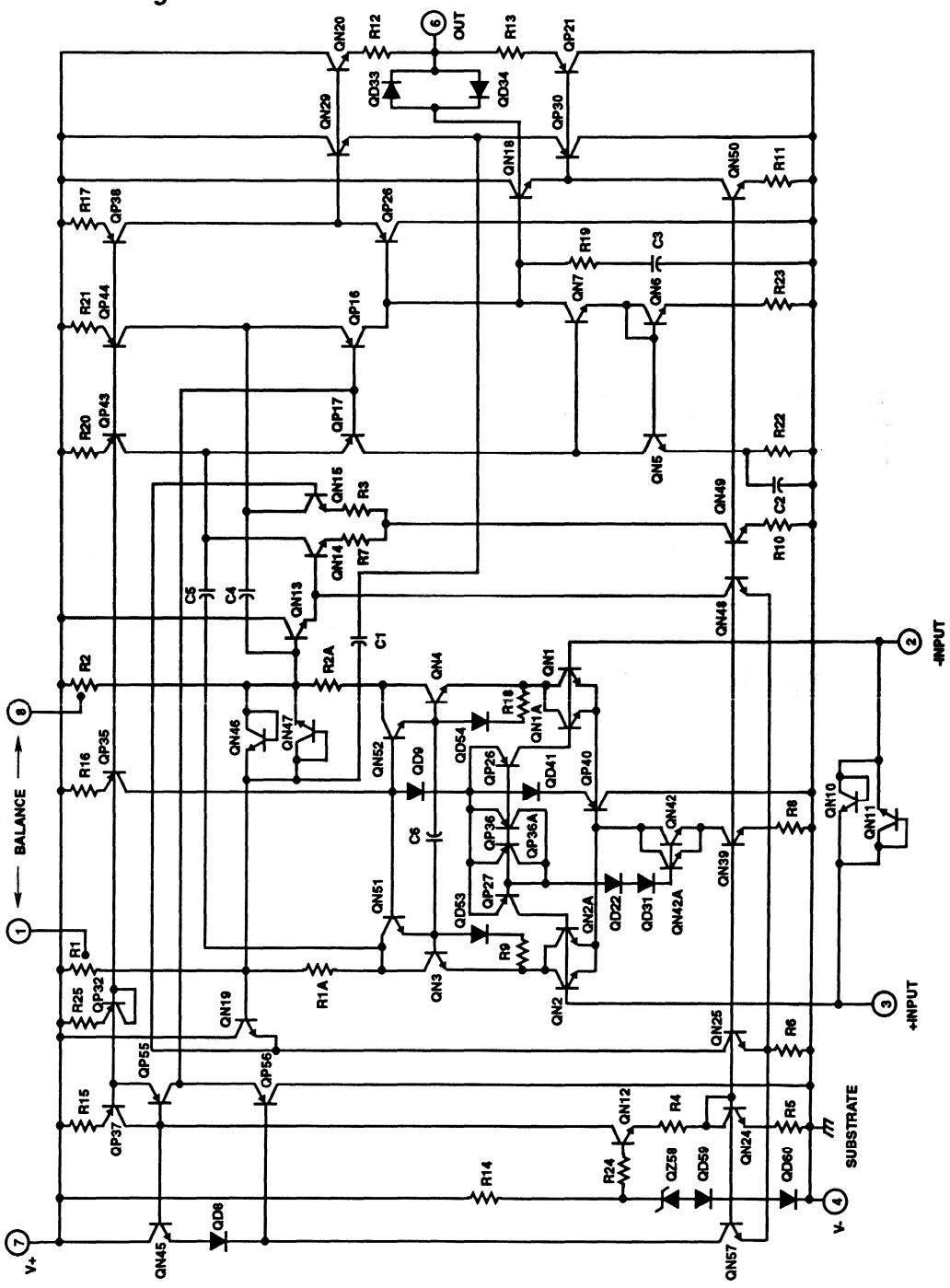
Transistor Count 63
Die Dimensions ..... 65 x 104.3 x 19 mils
(1700µm x 2600µm x 480µm)

Substrate Potential* ..... V-
Process ..... Bipolar-DI

* The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic Mini-DIP	114	34
TO-99 Metal Can	108	33
Plastic DIP	92	30
SOIC	157	43

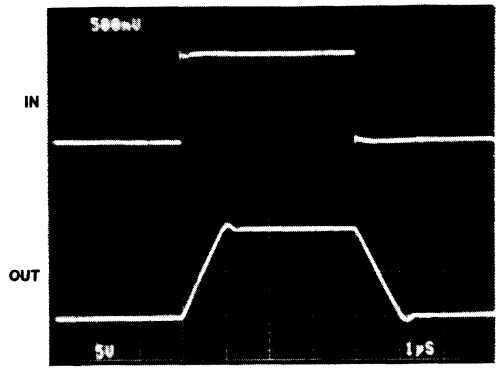
Schematic Diagram



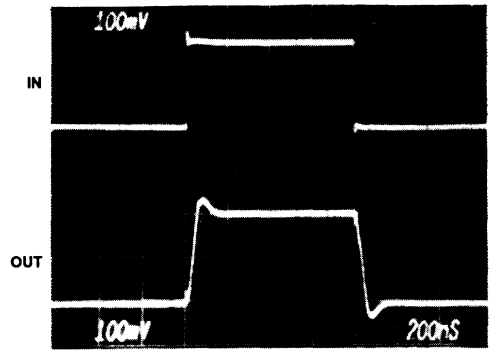
Test Circuits

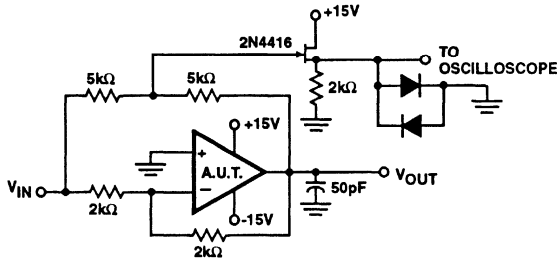
FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUITS

LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 0.5V/Div.)
(Output = 5V/Div.)
Horizontal Scale: (Time = 1µs/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: 100mV/Div.)
Horizontal Scale: (200ns/Div.)





- $A_V = -1$
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V

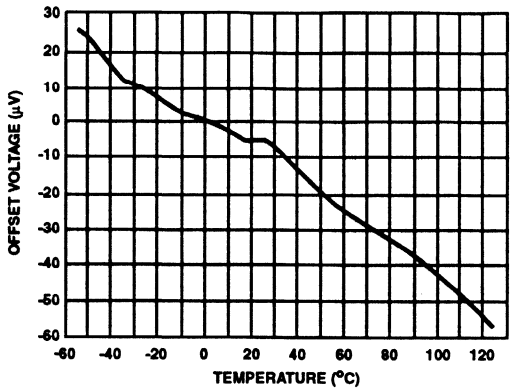


FIGURE 3. TYPICAL OFFSET VOLTAGE DRIFT vs TEMPERATURE

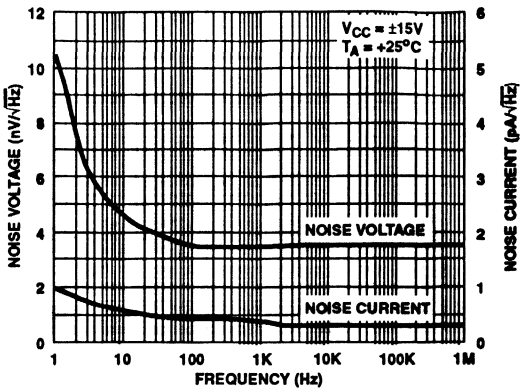


FIGURE 4. NOISE CHARACTERISTICS

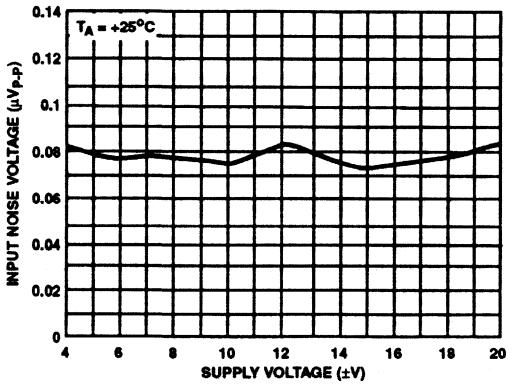


FIGURE 5. NOISE vs SUPPLY VOLTAGE

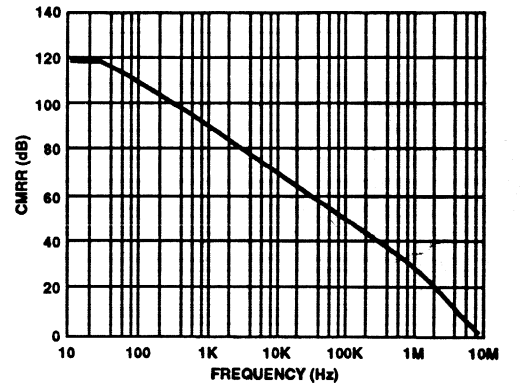


FIGURE 6. CMRR vs FREQUENCY

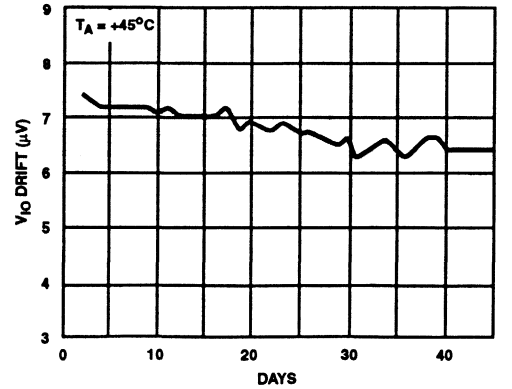


FIGURE 7. OFFSET VOLTAGE DRIFT vs TIME

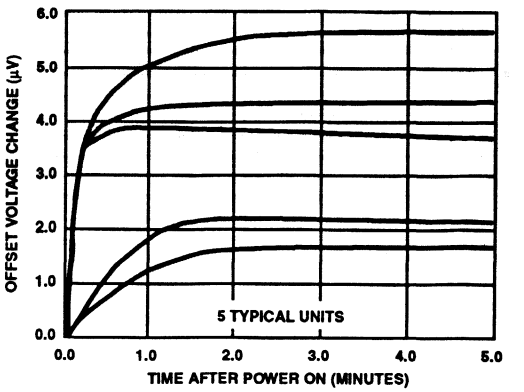


FIGURE 8. OFFSET VOLTAGE WARM UP DRIFT

Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V (Continued)

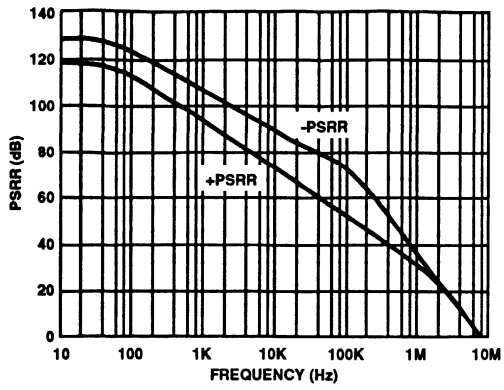


FIGURE 9. PSRR vs FREQUENCY

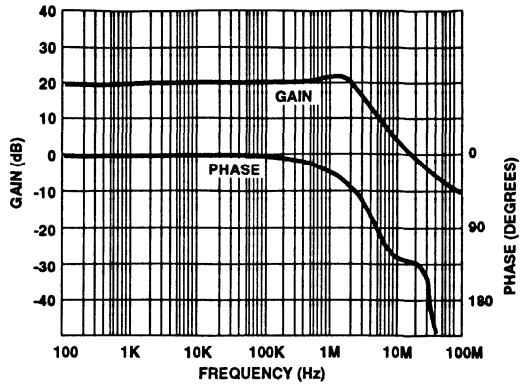


FIGURE 10. CLOSED LOOP GAIN AND PHASE vs FREQUENCY

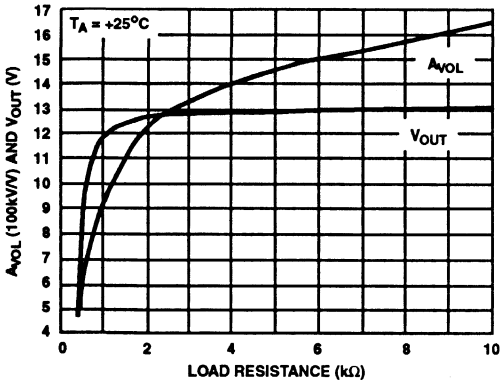


FIGURE 11. A_{VOL} AND V_{OUT} vs LOAD RESISTANCE

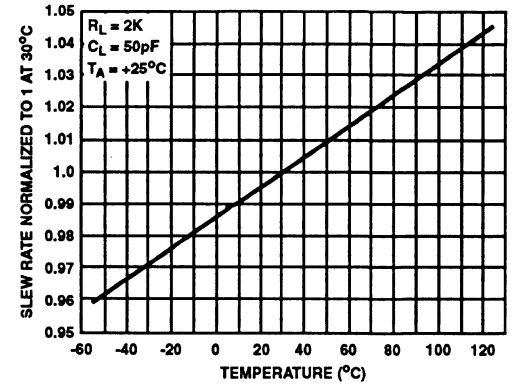


FIGURE 12. NORMALIZED SLEW RATE vs TEMPERATURE

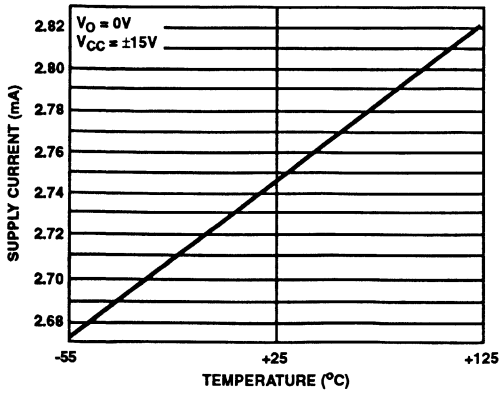


FIGURE 13. SUPPLY CURRENT vs TEMPERATURE

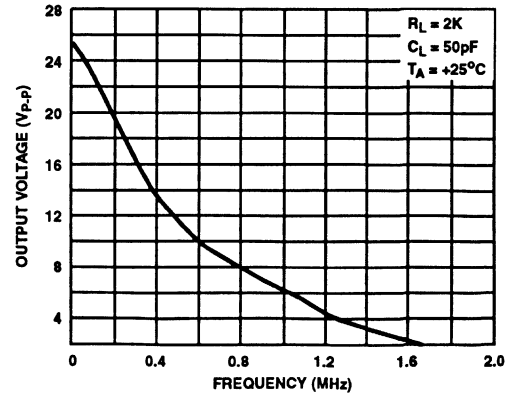


FIGURE 14. MAX UNDISTORTED SINEWAVE OUTPUT vs FREQUENCY

Typical Performance Curves Unless Otherwise Specified: $T_A = +25°C$, $V_{SUPPLY} = \pm 15V$ (Continued)

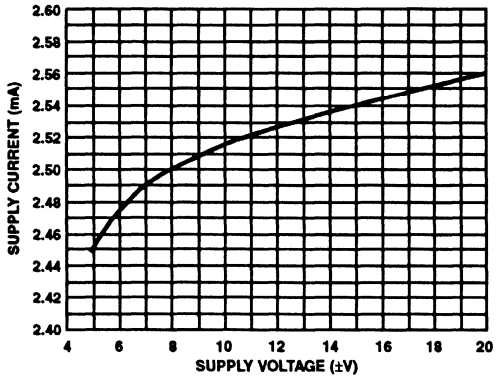


FIGURE 15. SUPPLY CURRENT vs SUPPLY VOLTAGE

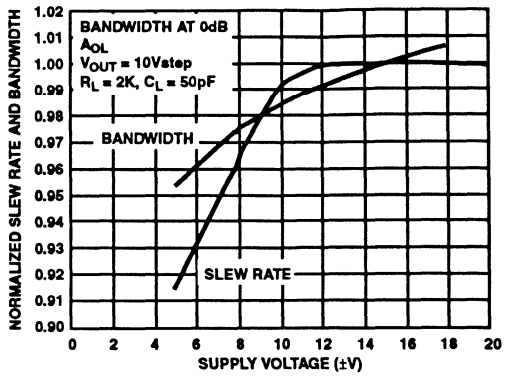


FIGURE 16. BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE

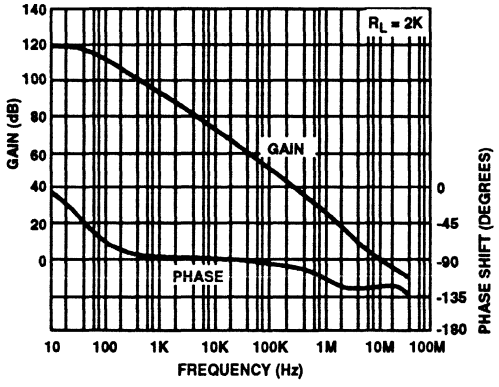


FIGURE 17. OPEN LOOP GAIN AND PHASE vs FREQUENCY

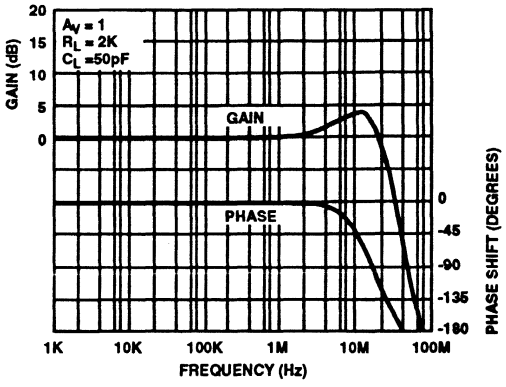


FIGURE 18. CLOSED LOOP GAIN AND PHASE vs FREQUENCY

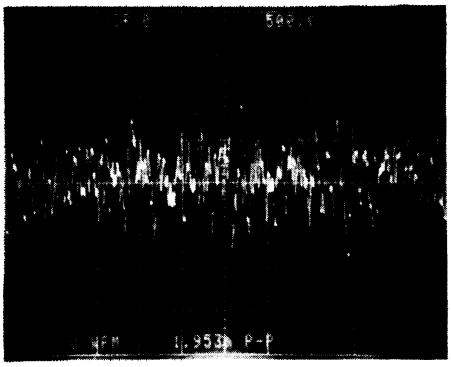
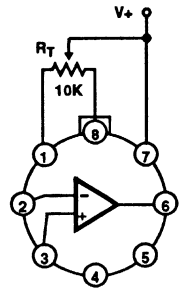


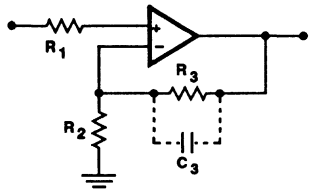
FIGURE 19. PEAK-TO-PEAK NOISE VOLTAGE (0.1Hz TO 10Hz)
Horizontal Scale = 1sec/Div.
Vertical Scale = 0.002μV/Div.
A_{CL} = 25,000V/V, E_N = 0.08μV_{P-P} RTI

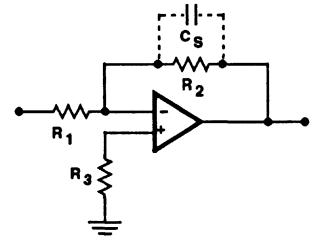
Application Information



Tested Offset Adjustment Range is $|V_{OS}| + 1mV|$ minimum referred to output. Typical range is ±4mV with R_T = 10kΩ.

FIGURE 20. SUGGESTED OFFSET VOLTAGE ADJUSTMENT





Low resistances are preferred for low noise applications as a 1kΩ resistor has 4nV/√Hz of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

FIGURE 21. SUGGESTED STABILITY CIRCUITS

HARRIS SEMICONDUCTOR HA-5130, HA-5135

April 1993

Precision Operational Amplifiers

Features

- Low Offset Voltage.....25μV Max
- Low Offset Voltage Drift .....0.4μV/°C
- Low Noise.....9nV/√Hz
- Open Loop Gain.....140dB
- Unity Gain Bandwidth 2.5MHz
- All Bipolar Construction

Applications

- High Gain Instrumentation
- Precision Data Acquisition
- Precision Integrators
- Biomedical Amplifiers
- Precision Threshold Detectors

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HA2-5130-2	-55°C to +125°C	8 Pin Can
HA2-5130-5	0°C to +75°C	8 Pin Can
HA2-5135-2	-55°C to +125°C	8 Pin Can
HA2-5135-5	0°C to +75°C	8 Pin Can
HA7-5130-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5130-5	0°C to +75°C	8 Lead Ceramic DIP
HA7-5135-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5135-5	0°C to +75°C	8 Lead Ceramic DIP

Description

The Harris HA-5130/5135 are precision operational amplifiers manufactured using a combination of key technological advancements to provide outstanding input characteristics.

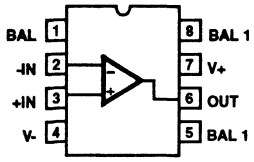
A Super Beta input stage is combined with laser trimming, dielectric isolation and matching techniques to produce 25μV (Maximum) input offset voltage and 0.4μV/°C input offset voltage average drift. Other features enhanced by this process include 9nV/√Hz (Typ.) Input Noise Voltage, 1nA Input Bias Current and 140dB Open Loop Gain.

These features coupled with 120dB CMRR and PSRR make HA-5130/5135 an ideal device for precision DC instrumentation amplifiers. Excellent input characteristics in conjunction with 2.5MHz bandwidth and 0.8V/μs slew rate, make this amplifier extremely useful for precision integrator and biomedical amplifier designs. These amplifiers are also well suited for precision data acquisition and for accurate threshold detector applications.

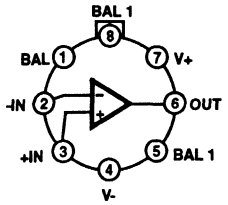
HA-5130/5135 offers added features over the industry standard OP-07 in regards to bandwidth and slew rate specifications. For the military grade product, refer to the HA-5135/883 data sheet.

Pinouts

HA-5130/5135 (CDIP)
TOP VIEW

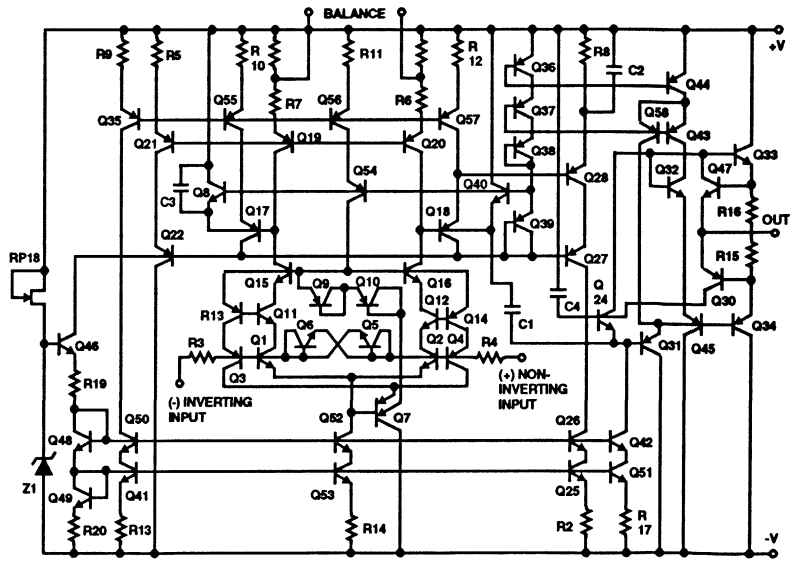


HA-5130/5135 (TO-99 CAN)
TOP VIEW



(Both BAL 1 pins are connected together internally)

Schematic Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2907.1**

Absolute Maximum Ratings

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage 7V
Output Short Circuit Duration . . . . . Indefinite
Junction Temperature (Note 1) . . . . . +175°C
Lead Temperature (Soldering 10 Sec.) . . . . . 300°C

Operating Conditions

Operating Temperature Ranges
HA-5130/5135-2 . . . . . -55°C ≤ T_A ≤ +125°C
HA-5130/5135-5 . . . . . 0°C ≤ T_A ≤ +75°C
Storage Temperature Range . . . . . -65°C ≤ T_A ≤ +150°C

Thermal Resistance (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP Package	113	34
TO-99 Metal Can	108	33

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = +15V, V- = -15V

PARAMETER	TEMP	HA-5130-2/-5			HA-5135-2/-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	10	25	-	10	75	µV
	Full	-	50	60	-	50	130	µV
Average Offset Voltage Drift	Full	-	0.4	0.6	-	0.4	1.3	µV/°C
Bias Current	+25°C	-	±1	±2	-	±1	±4	nA
	Full	-	-	±4	-	-	±6	nA
Bias Current Average Drift	Full	-	0.02	0.04	-	0.02	0.04	nA/°C
Offset Current	+25°C	-	-	2	-	-	4	nA
	Full	-	-	4	-	-	5.5	nA
Offset Current Average Drift	Full	-	0.02	0.04	-	0.02	0.04	nA/°C
Common Mode Range	Full	±12	-	-	±12	-	-	V
Differential Input Resistance	+25°C	20	30	-	20	30	-	MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 2)	+25°C	-	-	0.6	-	-	0.6	μV_{P-P}
Input Noise Voltage Density (Note 2)								
f = 10Hz	+25°C	-	13.0	18.0	-	13.0	18.0	$nV/\sqrt{Hz}$
f = 100Hz		-	10.0	13.0	-	10.0	13.0	$nV/\sqrt{Hz}$
f = 1000Hz		-	9.0	11.0	-	9.0	11.0	$nV/\sqrt{Hz}$
Input Noise Current 0.1Hz to 10Hz (Note 2)	+25°C	-	15	30	-	15	30	pA_{P-P}
Input Noise Current Density (Note 2)								
f = 10Hz	+25°C	-	0.4	0.8	-	0.4	0.8	$pA/\sqrt{Hz}$
f = 100Hz		-	0.17	0.23	-	0.17	0.23	$pA/\sqrt{Hz}$
f = 1000Hz		-	0.14	0.17	-	0.14	0.17	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	120	140	-	120	140	-	dB
	Full	120	-	-	120	-	-	dB
Common Mode Rejection Ratio (Note 4)	Full	110	120	-	106	120	-	dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	0.6	2.5	-	0.6	2.5	-	MHz

Electrical Specifications V+ = +15V, V- = -15V **(Continued)**

PARAMETER	TEMP	HA-5130-2/-5			HA-5135-2/-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 5)	+25°C	±10	±12	-	±10	±12	-	V
	Full	±10	-	-	±10	-	-	V
Full Power Bandwidth (Note 6)	+25°C	8	10	-	8	10	-	kHz
Output Current (Note 7)	+25°C	±15	±20	-	±15	±20	-	mA
Output Resistance (Note 8)	+25°C	-	45	-	-	45	-	Ω
TRANSIENT RESPONSE (Note 9)								
Rise Time	+25°C	-	340	-	-	340	-	ns
Slew Rate	+25°C	0.5	0.8	-	0.5	0.8	-	V/µs
Settling Time (Note 10)	+25°C	-	11	-	-	11	-	µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	1.0	1.7	-	1.0	1.7	mA
Power Supply Rejection Ratio (Note 11)	Full	100	130	-	94	130	-	dB

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below +175°C.
2. Not tested. 90% of units meet or exceed these specifications.
3. V_{OUT} = ±10V; R_L = 2K. Gain dB = 20 $\log_{10} A_V$.
   ∴120dB = 1MV/V
   140dB = 10MV/V
4. V_{CM} = ±10V DC
5. R_L = 600Ω.
6. R_L = 2K; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
7. V_{OUT} = 10V
8. Output resistance measured under open loop conditions (f = 100Hz).
9. Refer to test circuits section of the data sheet.
10. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
11. V_{SUPPLY} = ±5V DC to ±20V DC.

Test Circuits

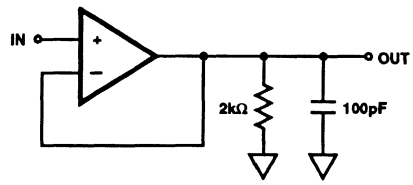
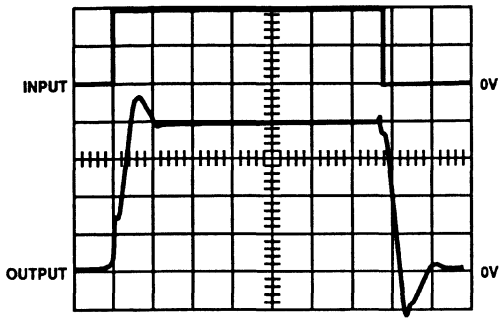


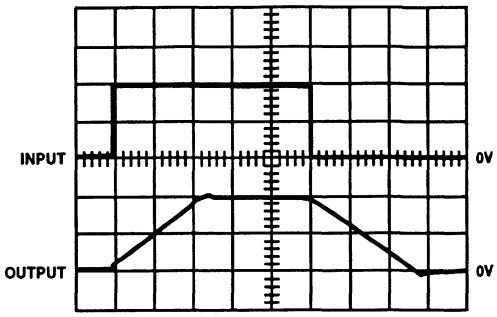
FIGURE 1. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT

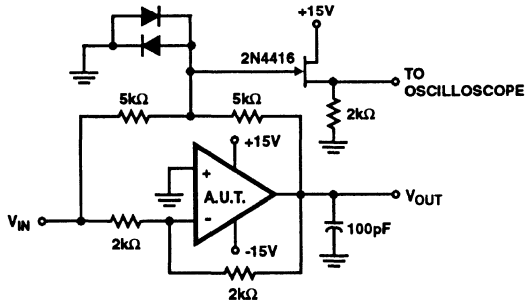
Test Circuits (Continued)

SMALL SIGNAL RESPONSE
Vertical Scale: Volts: 50mV/Div. Output
Volts: 100mV/Div. Input
Horizontal Scale: Time: 1µs/Div.



LARGE SIGNAL RESPONSE
Vertical Scale: Volts: 5V/Div.
Horizontal Scale: Time: 5µs/Div.





$A_V = -1$

Feedback and summing resistors should be 0.1% matched.

Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLING TIME CIRCUIT

Typical Performance Curves

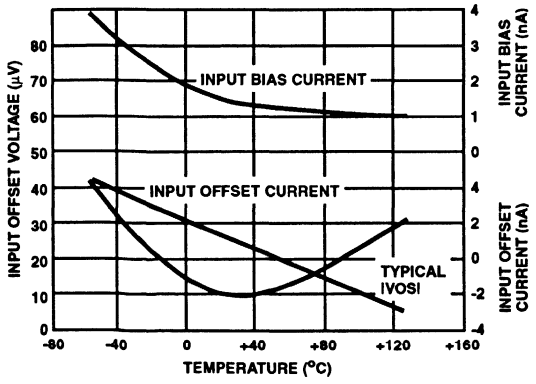


FIGURE 3. INPUT OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

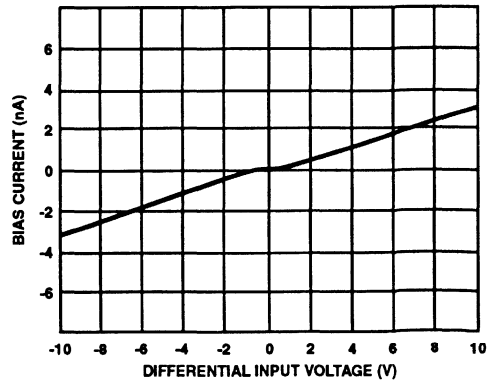


FIGURE 4. INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

Typical Performance Curves (Continued)

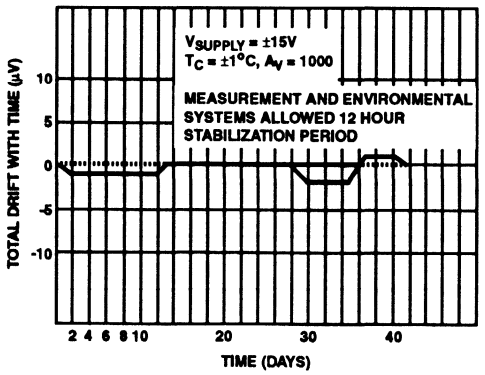


FIGURE 5. HA-5130 OFFSET VOLTAGE STABILITY vs TIME

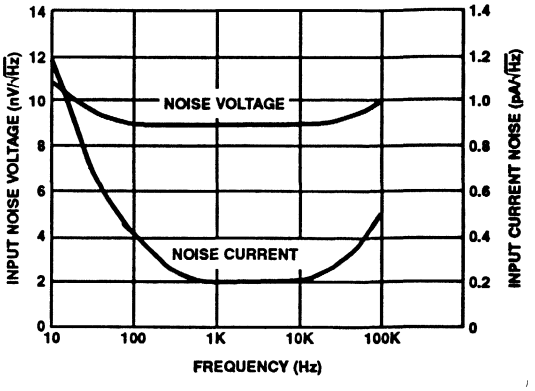


FIGURE 6. INPUT NOISE vs FREQUENCY

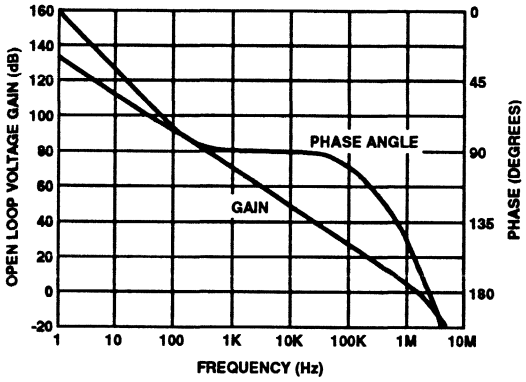


FIGURE 7. OPEN LOOP FREQUENCY RESPONSE

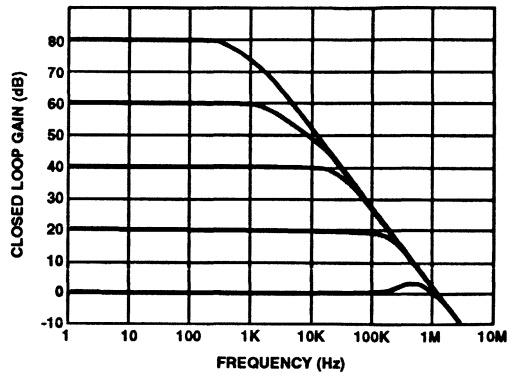


FIGURE 8. CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS

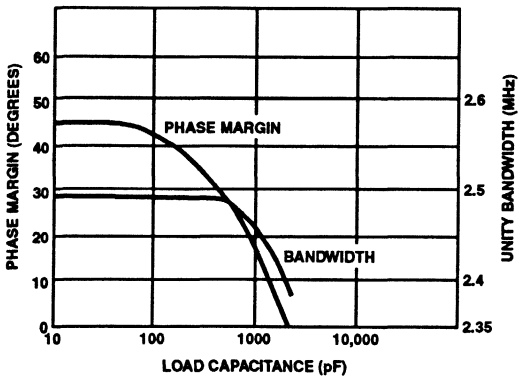


FIGURE 9. SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE

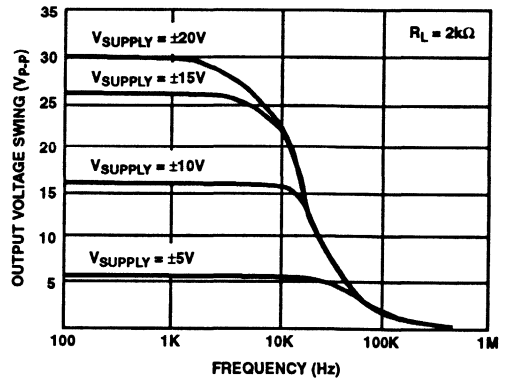


FIGURE 10. OUTPUT VOLTAGE SWING vs FREQUENCY AND SUPPLY VOLTAGE

Typical Performance Curves (Continued)

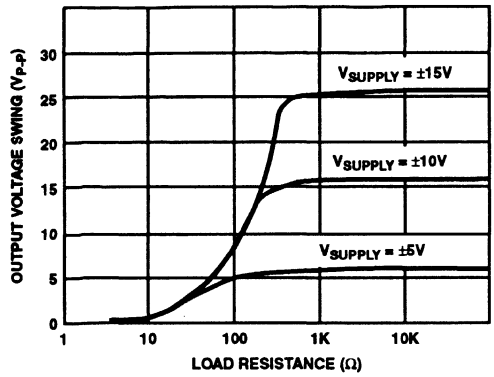


FIGURE 11. MAXIMUM OUTPUT VOLTAGE SWING vs LOAD RESISTANCE AND SUPPLY VOLTAGE

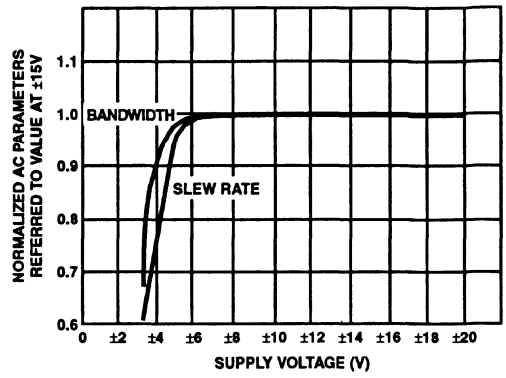


FIGURE 12. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

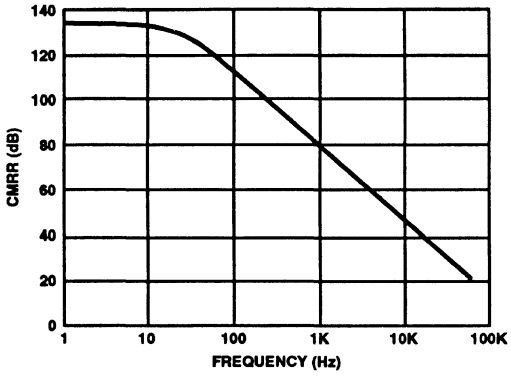


FIGURE 13. CMRR vs FREQUENCY

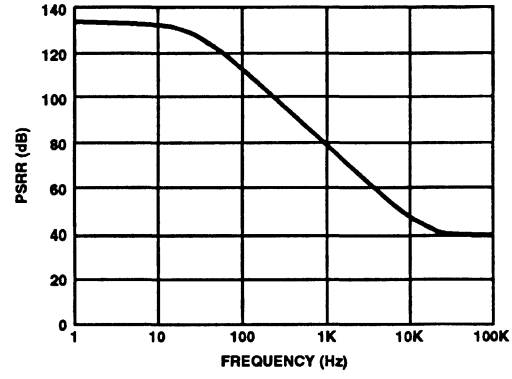


FIGURE 14. PSRR vs FREQUENCY

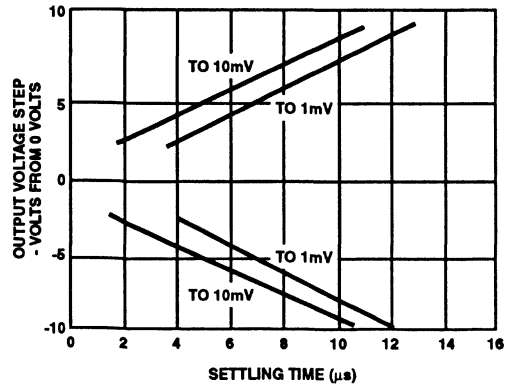


FIGURE 15. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

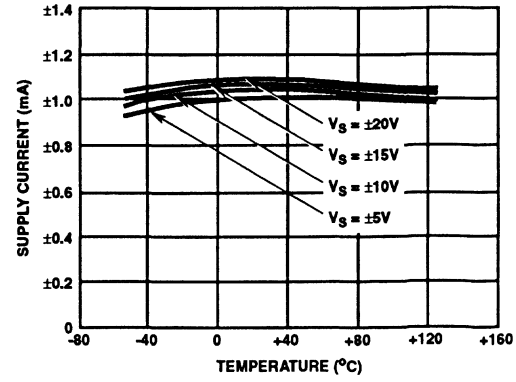
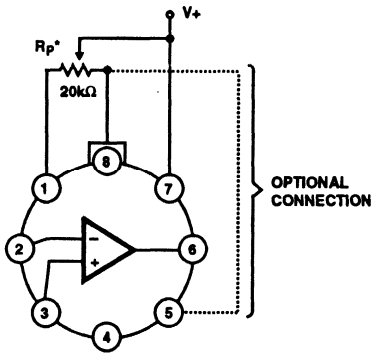


FIGURE 16. POWER SUPPLY CURRENT vs TEMPERATURE AND SUPPLY VOLTAGE

Applying the HA-5130, HA-5135 Operational Amplifiers

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. CONSIDERATIONS FOR PROTOTYPING: The following list of recommendations are suggested for prototyping.
   - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces and implementation of moisture barriers when required is suggested.
   - Error voltages generated by thermocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuity from heat generating components is recommended.
   - Shielded cable input leads, guard rings and shield drivers are recommended for the most critical applications.
3. When driving large capacitive loads (> 500pF), a small value resistor (≈50Ω) should be connected in series with the output and inside the feedback loop.
4. OFFSET VOLTAGE ADJUSTMENT: A 20kΩ balance potentiometer is recommended if offset nulling is required. However, other potentiometer values such as 10kΩ, 50kΩ and 100kΩ may be used. The minimum adjustment range for given values is ±2mV.
5. SATURATION RECOVERY: Input and output saturation recovery time is negligible in most applications. However, care should be exercised to avoid exceeding the absolute maximum ratings of the device.
6. DIFFERENTIAL INPUT VOLTAGES: Inputs are shunted with back-to-back diodes for overvoltage protection. In applications where differential input voltages in excess of 1V are applied between the inputs, the use of limiting resistors at the inputs is recommended.

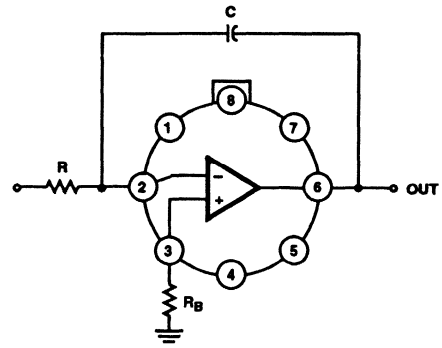
Applications



* Although R_P is shown equal to 20kΩ, other values such as 50kΩ, 100kΩ and 1kΩ may be used. Range of adjustment is approximately ±2.5mV. V_{OS} TC of the amplifier is optimized at minimal V_{OS}.

Tested Offset Adjustment is $|V_{OS}|$ + 1mV| minimum referred to output.

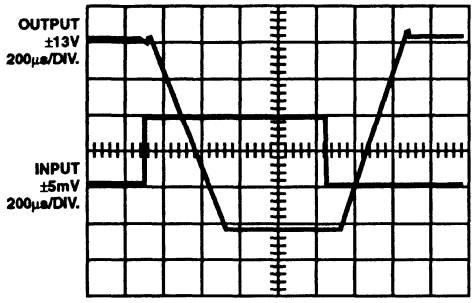
FIGURE 17. OFFSET NULLING CONNECTIONS

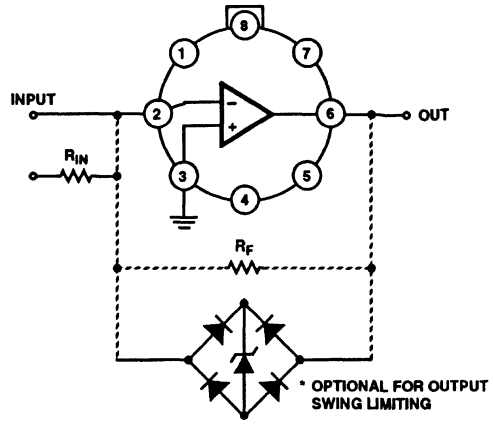


The excellent input and gain characteristics of HA-5130 are well suited for precision integrator applications. Accurate integration over seven decades of frequency using HA-5130, virtually nullifies the need for more expensive chopper-type amplifiers.

FIGURE 18. PRECISION INTEGRATOR

Applications (Continued)





Low V_{OS} coupled with high open loop Gain, high CMRR and high PSRR make HA-5130 ideally suited for precision detector applications.

FIGURE 19. ZERO CROSSING DETECTOR

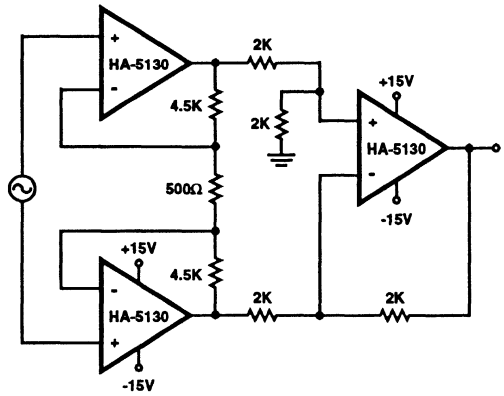


FIGURE 20. PRECISION INSTRUMENTATION AMPLIFIER (A_V = 100)

HARRIS SEMICONDUCTOR

HA-5134

April 1993

Precision Quad Operational Amplifier

Features

- Low Offset Voltage.....Max 200μV
- Low Offset Voltage Drift .....Max 2μV/°C
- Offset Voltage Match (5134A).... Full Temp. Max 250μV
- High Channel Separation 120dB
- Low Noise.....7nV/√Hz
- Wide Unity Gain Bandwidth 4MHz
- High CMRR/PSRR (Typ).....120dB
- Dielectric Isolation

Applications

- Instrumentation Amplifiers
- State-Variable Filters
- Precision Integrators
- Threshold Detectors
- Precision Data Acquisition Systems
- Low-Level Transducer Amplifiers

Description

The HA-5134 is a precision quad operational amplifier that is pin compatible with the OP-400, LT1014, OP11, RM4156, and LM148 as well as the HA-4741. Each amplifier features guaranteed maximum values for offset voltage of 200μV, offset voltage drift of 2μV/°C, and offset current of 75nA over the full military temperature range while CMRR/PSRR is guaranteed greater than 94dB and A_{VOL} is guaranteed above 500kV/V from -55°C to +125°C.

Precision performance of the HA-5134 is enhanced by a noise voltage density of 7nV/√Hz at 1kHz, noise current density of 1pA/√Hz at 1kHz and channel separation of 120dB. Each unity-gain stable quad amplifier is fabricated using the dielectric isolation process to assure performance in the most demanding applications.

The HA-5134 is ideal for compact circuits such as instrumentation amplifiers, state-variable filters, and low-level transducer amplifiers. Other applications include precision data acquisition, precision integrators, and accurate threshold detectors in designs where board space is a limitation.

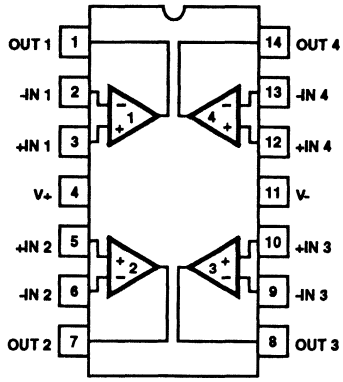
For military grade product, refer to the HA-5134/883 datasheet.

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HA1-5134-2	-55°C to +125°C	14 Lead Ceramic DIP
HA1-5134-5	0°C to +75°C	14 Lead Ceramic DIP
HA1-5134A-2	-55°C to +125°C	14 Lead Ceramic DIP
HA1-5134A-5	0°C to +75°C	14 Lead Ceramic DIP

Pinout

HA-5134 (CDIP)
TOP VIEW



2 OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2926.1**

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated
Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage (Note 2) 6V
Output Current ..... Full Short Circuit Protection
Voltage at any Op Amp Terminal ..... V+, V-
Junction Temperature (Note 3) ..... +175°C
Lead Temperature (Soldering 10 Sec.) ..... 300°C

Operating Conditions

Operating Temperature Ranges
HA-5134A/5134-2 ..... -55°C < T_A < +125°C
HA-5134A/5134-5 ..... 0°C < T_A < +75°C
Storage Temperature Range ..... -65°C < T_A < +150°C

Thermal Resistance (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP Package	71	13

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{CC} = ±15V, R_{LOAD} = 2K, C_{LOAD} = 50pF, $R_S \leq 100\Omega$, Unless Otherwise Specified

PARAMETER	TEMP	HA-5134A-2/-5			HA-5134-2/-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	50	100	-	50	200	µV
	Full	-	75	250	-	75	350	µV
Average Offset Voltage Drift	Full	-	0.3	1.2	-	0.3	2	µV/°C
Offset Voltage Match	Full	-	-	250	-	-	-	µV
Bias Current	+25°C	-	±10	±25	-	±10	±50	nA
	Full	-	±20	±50	-	±20	±75	nA
Offset Current	+25°C	-	10	25	-	10	50	nA
	Full	-	15	50	-	15	75	nA
Average Offset Current Drift	Full	-	0.05	-	-	0.05	-	nA/°C
Common Mode Range	Full	±10	-	-	±10	-	-	V
Differential Input Resistance	+25°C	-	30	-	-	30	-	MΩ
Input Noise Voltage (0.1Hz to 10Hz)	+25°C	-	0.2	-	-	0.2	-	µVp-p
Input Noise Voltage Density								
f = 10Hz	+25°C	-	10	-	-	10	-	nV/√Hz
f = 100Hz		-	7.5	-	-	7.5	-	nV/√Hz
f = 1kHz		-	7	-	-	7	-	nV/√Hz
Input Noise Current Density								
f = 10Hz	+25°C	-	3	-	-	3	-	pA/√Hz
f = 100Hz		-	1.5	-	-	1.5	-	pA/√Hz
f = 1kHz		-	1	-	-	1	-	pA/√Hz
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (V_{OUT} = ±10V)	+25°C	800	1200	-	800	1200	-	kV/V
	Full	500	750	-	500	750	-	kV/V
Common Mode Rejection Ratio (V_{CM} = ±10V)	+25°C	115	120	-	100	120	-	dB
	Full	110	115	-	94	115	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	V/V
Unity-Gain Bandwidth	+25°C	-	4	-	-	4	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	12	13.5	-	12	13.5	-	V
Output Current	+25°C	-	20	-	-	20	-	mA
Full Power Bandwidth (Note 4)	+25°C	12	16	-	12	16	-	kHz
Channel Separation (V_{OUT} = ±10V)	+25°C	120	136	-	120	136	-	dB

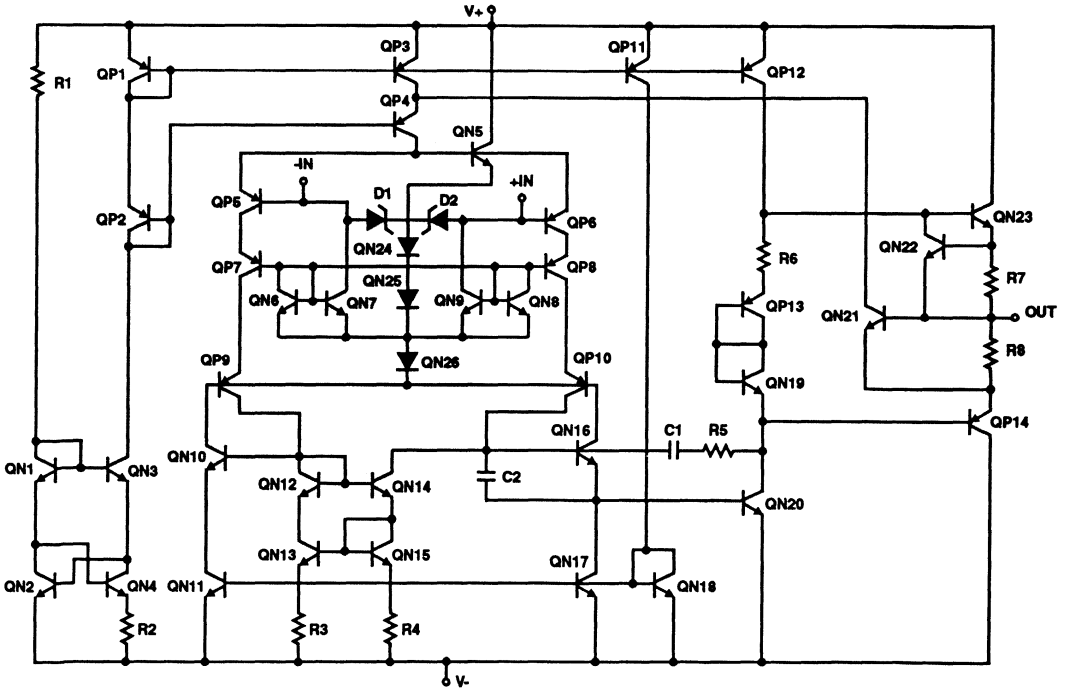
Electrical Specifications V_{CC} = ±15V, R_{LOAD} = 2K, C_{LOAD} = 50pF, $R_S \leq 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	HA-5134A-2/-5			HA-5134-2/-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 5)								
Rise Time (Note 6)	+25°C	-	200	400	-	200	400	ns
Slew Rate	+25°C	0.75	1.0	-	0.75	1.0	-	V/µs
Overshoot	+25°C	-	20	40	-	20	40	%
Settling Time (Note 7)	+25°C	-	13	-	-	13	-	µs
POWER SUPPLY CHARACTERISTICS								
Supply Current (All Amps)	Full	-	6.5	8	-	6.5	8	mA
Power Supply Rejection Ratio (Note 8)	+25°C	110	120	-	100	120	-	dB
	Full	100	115	-	94	115	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 6V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below +175°C.
4. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; V_{peak} = 10V
5. Refer to Test Circuits section of the data sheet.
6. Time from 10% to 90% of 200mV output step, A_V = 1.
7. Specified to 0.01% of a 10V step, A_V = -1.
8. V_S = ±5V to ±18V.

Schematic Diagram (Each Amplifier)



Test Circuits

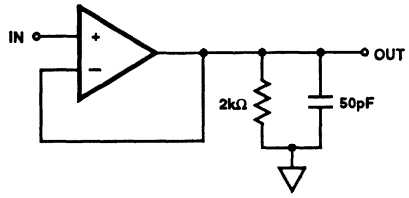
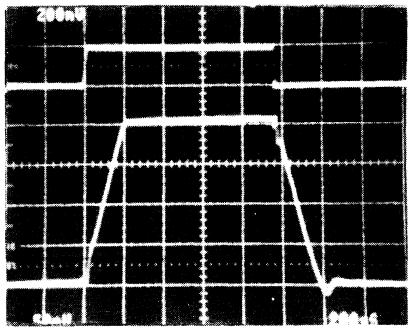
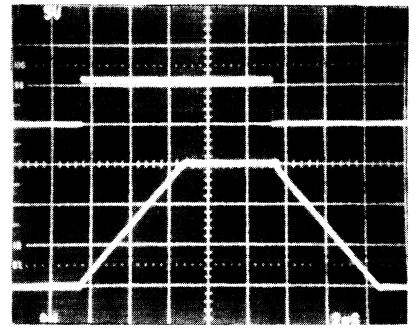


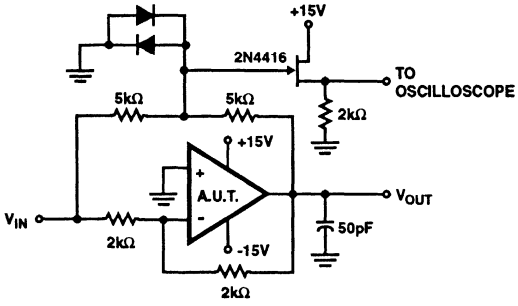
FIGURE 1. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT

SMALL SIGNAL RESPONSE
Vertical: 50mV/Div. Horizontal: 200ns/Div.
T_A = +25°C, V_{CC} = ±15V, A_V = +1, R_L = 2kΩ, C_L = 50pF



LARGE SIGNAL RESPONSE
Vertical: 2V/Div. Horizontal : 2µs/Div.
T_A = +25°C, V_{CC} = ±15V, A_V = +1, R_L = 2kΩ, C_L = 50pF

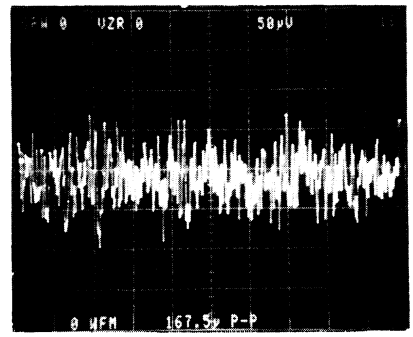




A_V = -1
Feedback and summing resistors should be 0.1% matched.
Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLING TIME CIRCUIT

PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz
T_A = +25°C, V_{CC} = ±15V, A_V = 1000



en_{P-P} = 0.167µV_{P-P}
0.05µV/Div., 1s/Div.

Performance Curves

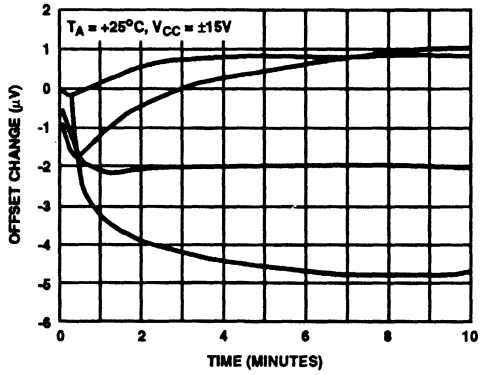


FIGURE 3. V_{IO} WARM-UP DRIFT

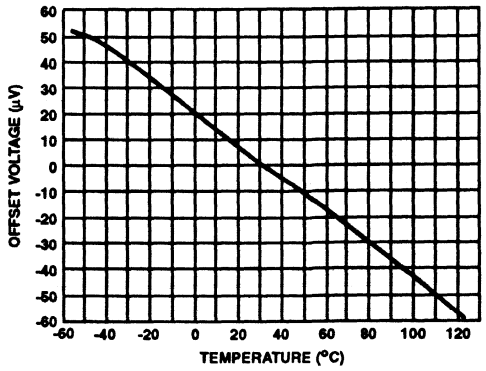


FIGURE 4. INPUT OFFSET VOLTAGE vs TEMPERATURE

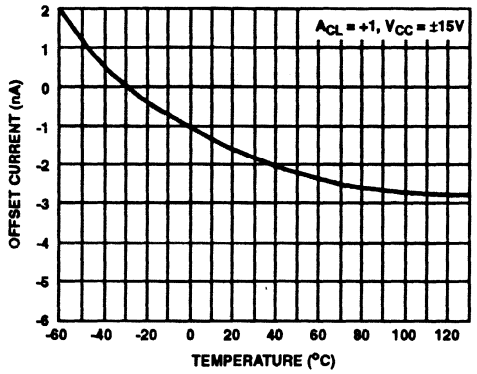


FIGURE 5. OFFSET CURRENT vs TEMPERATURE

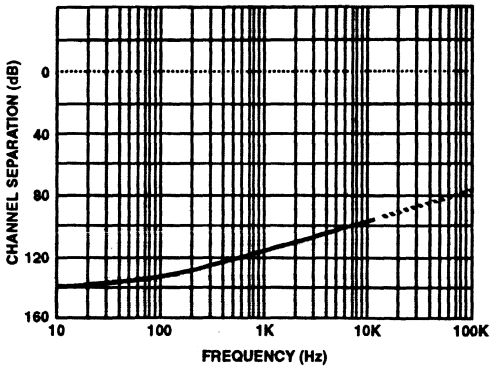


FIGURE 6. CHANNEL SEPARATION vs FREQUENCY

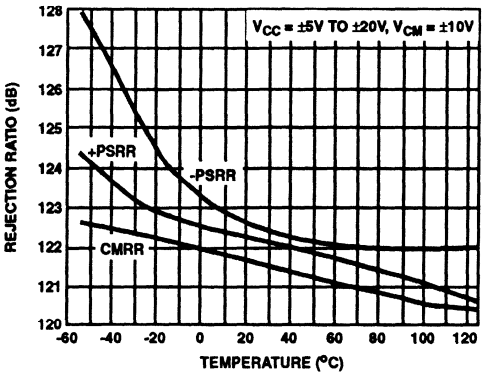


FIGURE 7. REJECTION RATIOS vs TEMPERATURE

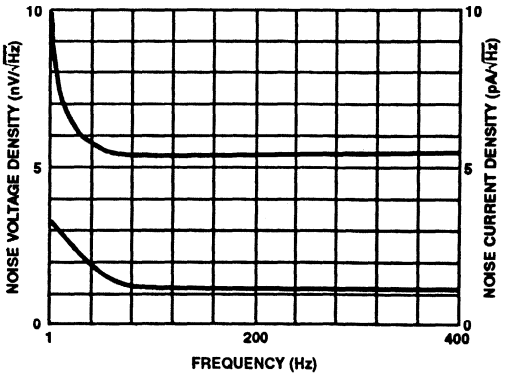


FIGURE 8. NOISE VOLTAGE DENSITY vs FREQUENCY

Performance Curves (Continued)

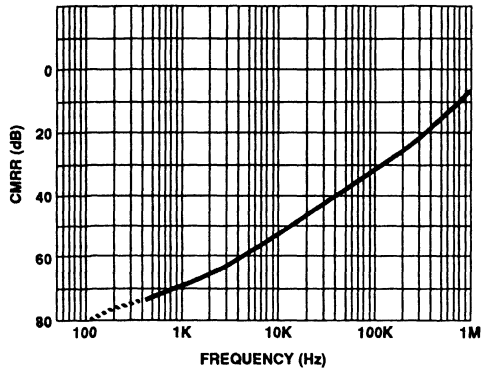


FIGURE 9. CMRR vs FREQUENCY

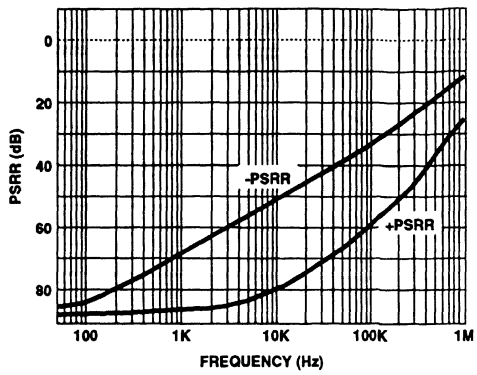


FIGURE 10. PSRR vs FREQUENCY

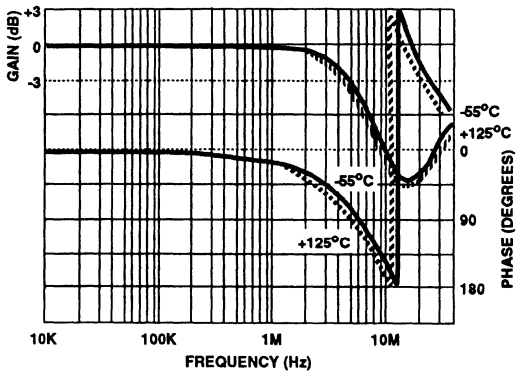


FIGURE 11. CLOSED LOOP FREQUENCY RESPONSE vs TEMPERATURE

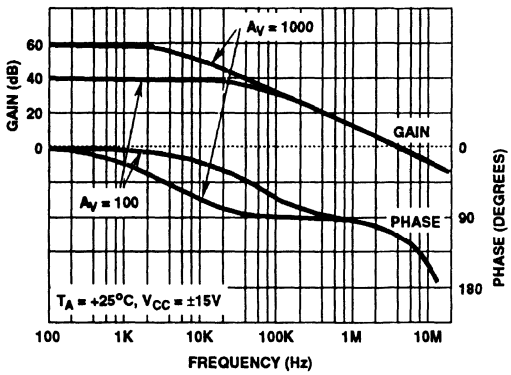


FIGURE 12. CLOSED LOOP GAIN/PHASE vs FREQUENCY

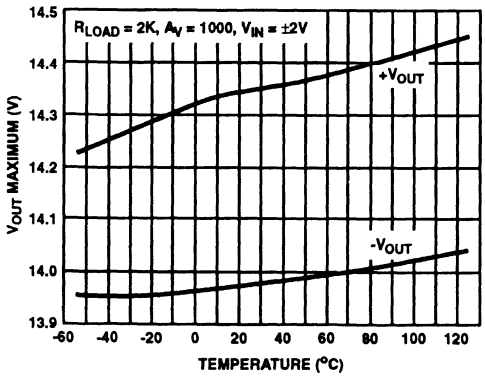


FIGURE 13. MAXIMUM OUTPUT VOLTAGE vs TEMPERATURE

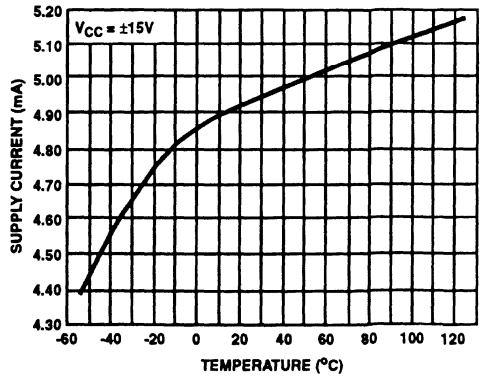


FIGURE 14. SUPPLY CURRENT vs TEMPERATURE

Performance Curves (Continued)

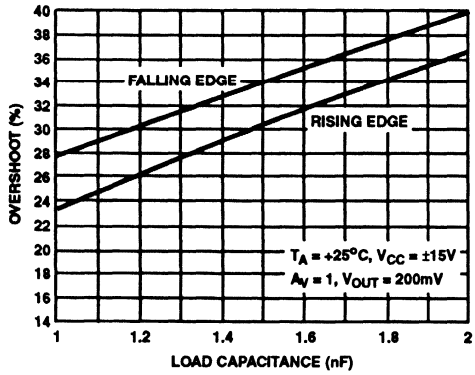


FIGURE 15. OVERSHOOT vs C_{LOAD}

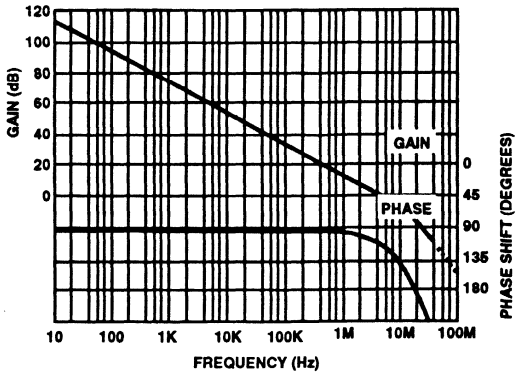
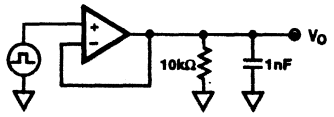
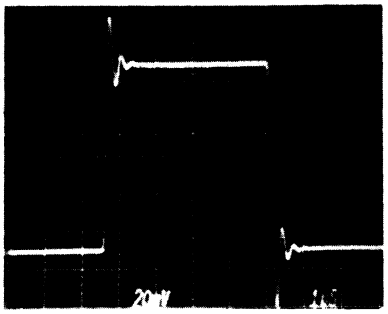


FIGURE 16. OPEN LOOP GAIN & PHASE vs FREQUENCY

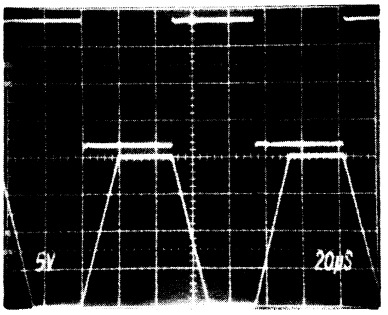
Applications Information





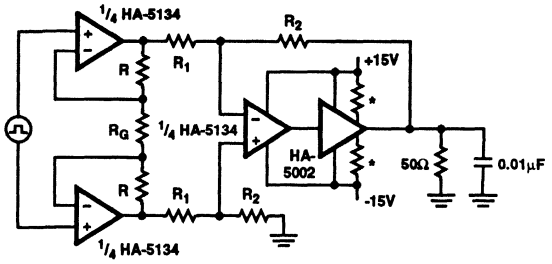
T_A = +25°C, V_{CC} = ±15V, A_V = 1, R_L = 10kΩ
20mV/Div, 1µs/Div.

TRANSIENT RESPONSE OF APPLICATION CIRCUIT #1



V_{OUT} = ±10V, R_{LOAD} = 50Ω C_{LOAD} = 0.01µF, A_V = 3, V_{CC} = ±15V
Top: Input, 2V/Div., 20µs/Div. Bottom: Output, 5V/Div, 20µs/Div.

FIGURE 17. SMALL SIGNAL TRANSIENT RESPONSE (C_{LOAD} = 1nF)



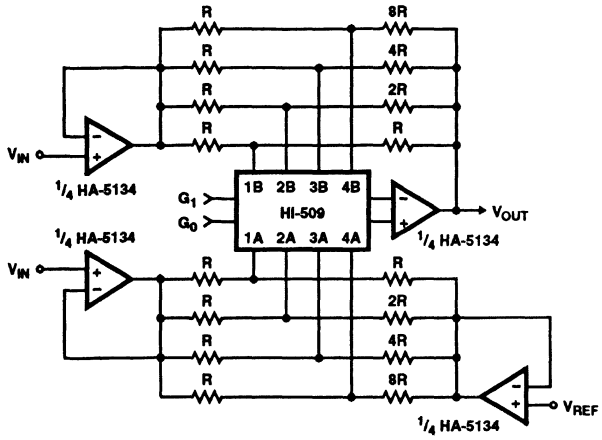
$$A_V = \left(1 + \frac{2R}{R_G}\right)\left(\frac{R_2}{R_1}\right)$$

* 10Ω - 100Ω recommended for short circuit limiting.

NOTE: When driving heavy loads the HA-5002 may contribute to thermal errors. Proper thermal shielding is recommended.

FIGURE 18. APPLICATION CIRCUIT #1: INSTRUMENTATION AMPLIFIER WITH POWER OUTPUT

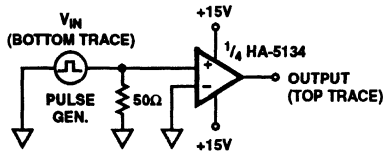
Applications Information (Continued)

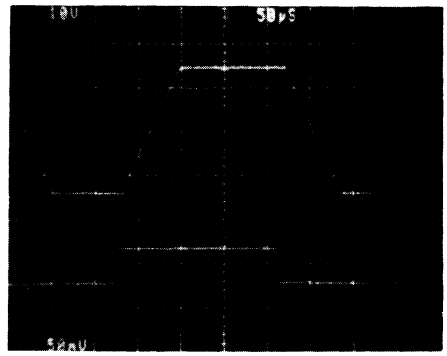


G_1	G_0	A_V
0	0	-1
0	1	-2
1	0	-4
1	1	-8

High A_{VOL} of HA-5134 reduces gain error.
Gain Error ≅ 0.004% at A_V = 8.

FIGURE 19. APPLICATION CIRCUIT #2: PROGRAMMABLE GAIN AMPLIFIER





Horizontal: 50µs/Div.
V_{IN} = ±25mV, V_{OUT} = ±14V

NOTE: If differential input voltages greater than 6V are present, input current must be limited to less than 25mA.

FIGURE 20. APPLICATION CIRCUIT #3: PRECISION COMPARATOR

General Considerations

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01µF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. CONSIDERATIONS FOR PROTOTYPING: The following list of recommendations are suggested for prototyping.

   - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces and implementation of moisture barriers when required is suggested.
   - Error voltages generated by thermocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuitry from heat generating components is recommended.
   - Shielded cable input leads, guard rings and shield drivers are recommended for the most critical applications.

HARRIS SEMICONDUCTOR

HA-5137

Ultra-Low Noise Precision Wideband Operational Amplifier

March 1993

Features

- High Speed 20V/μs
- Wide Gain Bandwidth ($A_V \geq 5$) 63MHz
- Low Noise ..... 3nV/$\sqrt{Hz}$ at 1kHz
- Low V_{OS} 10μV
- High CMRR 126dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers
- For Further Design Ideas See Application Note 553

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-5137-2	-55°C to +125°C	8 Pin Can
HA2-5137-5	0°C to +75°C	8 Pin Can
HA2-5137A-2	-55°C to +125°C	8 Pin Can
HA2-5137A-5	0°C to +75°C	8 Pin Can
HA3-5137-5	0°C to +75°C	8 Lead Plastic DIP
HA3-5137A-5	0°C to +75°C	8 Lead Plastic DIP
HA7-5137-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5137-5	0°C to +75°C	8 Lead Ceramic DIP
HA7-5137A-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5137A-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P5137-5	0°C to +75°C	8 Lead SOIC

Description

The HA-5137 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris Dielectric Isolation technology and advanced processing techniques, this unique design unites low noise (3nV/$\sqrt{Hz}$) precision instrumentation performance with high speed (20V/μs) wideband capability.

This amplifier's impressive list of features include low V_{OS} (10μV), wide gain bandwidth (63MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140mW of power.

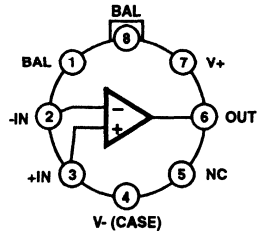
Using the HA-5137 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than five.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5137's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

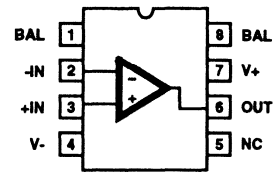
This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than five. For the military grade product, refer to the HA-5137/883 data sheet.

Pinouts

HA-5137 (TO-99 METAL CAN)
TOP VIEW



HA-5137 (PDIP, CDIP, SOIC)
TOP VIEW



File Number **2908.1**

Absolute Maximum Ratings

T_A = +25°C Unless Otherwise Specified
Voltage Between V+ and V- Terminals 44V
Differential Input Voltage (Note 1) 0.7V
Output Current ..... Full Short Circuit Protection
Junction Temperature (Note 12) ..... +175°C
Junction Temperature (Plastic Packages) ..... +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Operating Temperature Ranges

HA-5137/37A-2 ..... -55°C ≤ T_A ≤ +125°C
HA-5137/37A-5 ..... 0°C ≤ T_A ≤ +75°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +15V, V- = -15V, C_L ≤ 50pF, R_S ≤ 100Ω

PARAMETER		TEMP	HA-5137A MIN	HA-5137A TYP	HA-5137A MAX	HA-5137 MIN	HA-5137 TYP	HA-5137 MAX	UNITS
INPUT CHARACTERISTICS									
Offset Voltage		+25°C	-	10	25	-	30	100	µV
		Full	-	30	60	-	70	300	µV
Average Offset Voltage Drift		Full	-	0.2	0.6	-	0.4	1.8	µV/°C
Bias Current		+25°C	-	10	40	-	15	80	nA
		Full	-	20	60	-	35	150	nA
Offset Current		+25°C	-	7	35	-	12	75	nA
		Full	-	15	50	-	30	135	nA
Common Mode Range		Full	±10.3	±11.5	-	±10.3	±11.5	-	V
Differential Input Resistance (Note 2)		+25°C	1.5	6	-	0.8	4	-	MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 3)		+25°C	-	0.08	0.18	-	0.09	0.25	μV_{P-P}
Input Noise Voltage Density (Note 4)	f = 10Hz	+25°C	-	3.5	5.5	-	3.8	8.0	$nV/\sqrt{Hz}$
	f = 100Hz	+25°C	-	3.1	4.5	-	3.3	5.6	$nV/\sqrt{Hz}$
	f = 1000Hz	+25°C	-	3.0	3.8	-	3.2	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 4)	f = 10Hz	+25°C	-	1.7	4.0	-	1.7	-	$pA/\sqrt{Hz}$
	f = 100Hz	+25°C	-	1.0	2.3	-	1.0	-	$pA/\sqrt{Hz}$
	f = 1000Hz	+25°C	-	0.4	0.6	-	0.4	0.6	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain (Note 5)		+25°C	1000	1800	-	700	1500	-	V/mV
		Full	600	1200	-	300	800	-	V/mV
Common Mode Rejection Ratio (Note 6)		Full	114	126	-	100	120	-	dB
Minimum Stable Gain		+25°C	5	-	-	5	-	-	V/V
Gain-Bandwidth-Product	f = 10kHz	+25°C	60	80	-	60	80	-	MHz
	f = 1MHz	+25°C	-	63	-	-	63	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 600Ω	+25°C	±10.0	±11.5	-	±10.0	±11.5	-	V
	R_L = 2kΩ	Full	±11.7	±13.8	-	±11.4	±13.5	-	V
Full Power Bandwidth (Note 7)		+25°C	220	320	-	220	320	-	kHz
Output Resistance, Open Loop		+25°C	-	70	-	-	70	-	Ω
Output Current		+25°C	16.5	25	-	16.5	25	-	mA

Electrical Specifications $V+ = +15V$, $V- = -15V$, $C_L \leq 50pF$, $R_S \leq 100\Omega$ **(Continued)**

PARAMETER	TEMP	HA-5137A			HA-5137			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C	-	-	100	-	-	100	ns
Slew Rate (Note 10)	+25°C	14	20	-	14	20	-	V/µs
Settling Time (Note 9)	+25°C	-	1.0	-	-	1.0	-	µs
Overshoot	+25°C	-	20	40	-	20	40	%
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	3.5	-	-	3.5	-	mA
	Full	-	-	4.0	-	-	4.0	mA
Power Supply Rejection Ratio (Note 11)	Full	-	2	4	-	16	51	µV/V

NOTES:

1. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
2. This parameter value is based upon design calculations.
3. Refer to Typical Performance section of the data sheet.
4. The limits for this parameter are based on lab characterization, and reflect lot-to-lot variation.
5. $V_{OUT} = \pm 10V$, $R_L = 2k\Omega$
6. $V_{CM} = \pm 10V$
7. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Refer to Test Circuits section of the data sheet.
9. Settling time is specified to 0.1% of final value for a 10V output step and $A_V = -5$.
10. $V_{OUT} = \pm 3V$ (6V Step).
11. $V_S = \pm 4V$ to $\pm 18V$
12. See Thermal Constants in "Die Characteristics" text.

Die Characteristics

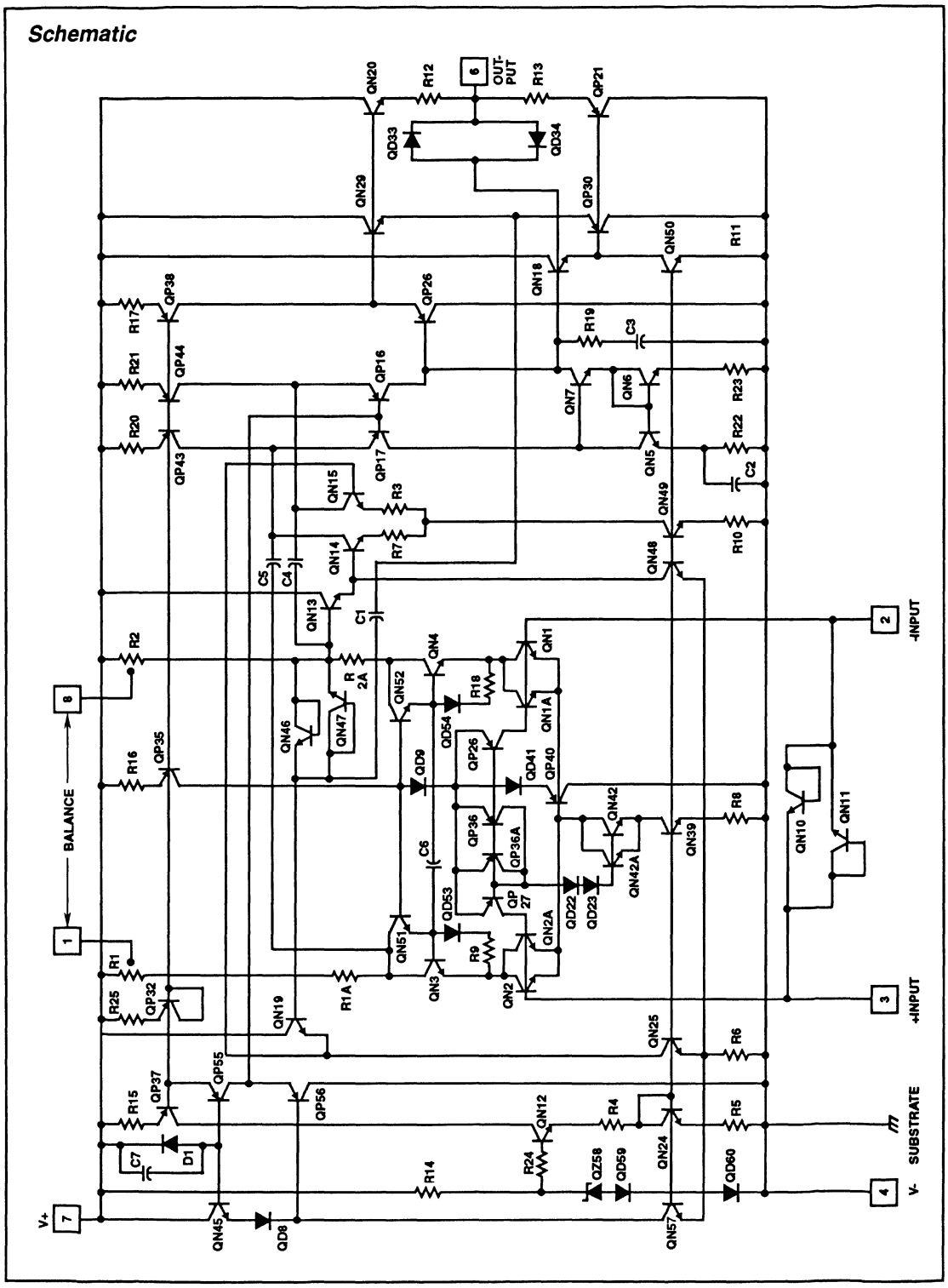
Transistor Count 63
Die Dimensions ..... 65 x 104.3 x 19 mils
(1700µm x 2600µm x 480µm)

Substrate Potential* ..... V-
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic Mini-DIP	114	34
TO-99 Metal Can	108	33
Plastic DIP	92	30
SOIC	157	43

* The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Schematic



Test Circuits

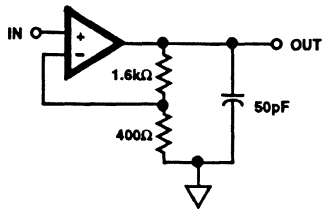
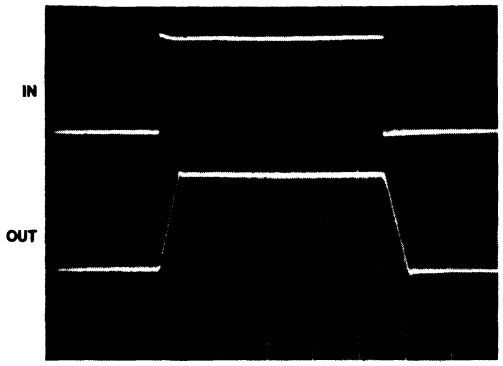


FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

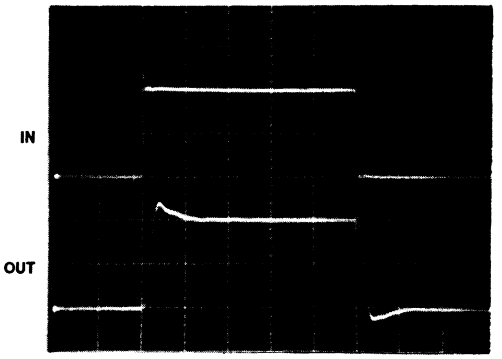
LARGE SIGNAL RESPONSE

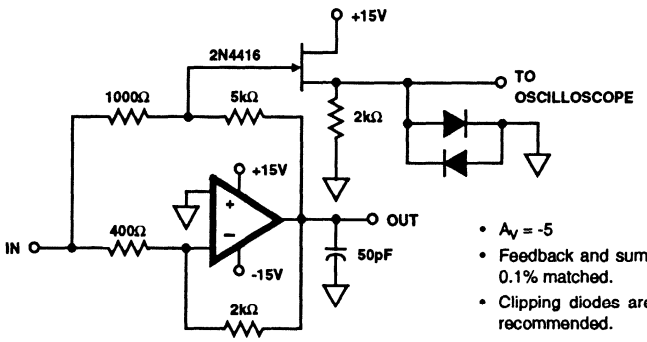
Vertical Scale: (Volts: Input = 1V/Div.)
(Volts: Output = 5V/Div.)
Horizontal Scale: (Time = 1μs/Div.)



SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: Input = 20mV/Div.)
(Volts: Output = 100mV/Div.)
Horizontal Scale: (Time = 100ns/Div.)





- A_V = -5
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V

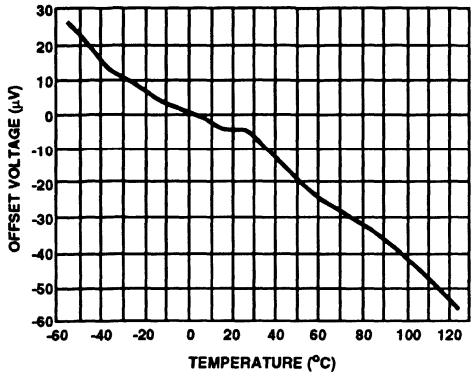


FIGURE 3. TYPICAL OFFSET VOLTAGE DRIFT vs TEMPERATURE

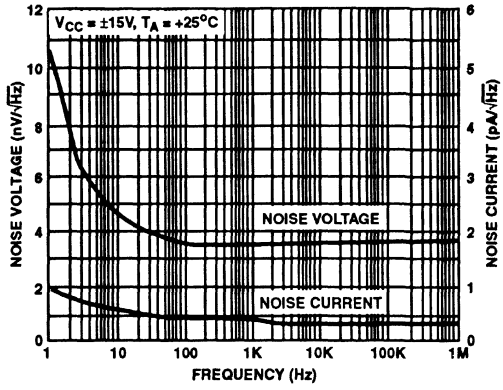


FIGURE 4. NOISE CHARACTERISTICS

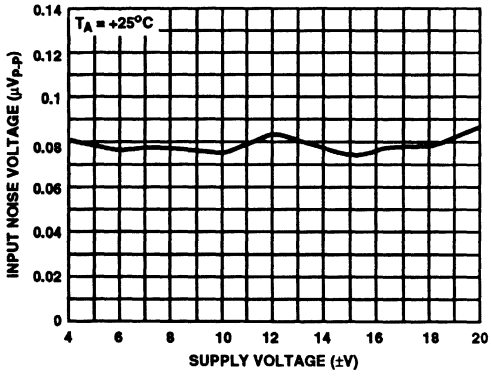


FIGURE 5. NOISE vs SUPPLY VOLTAGE

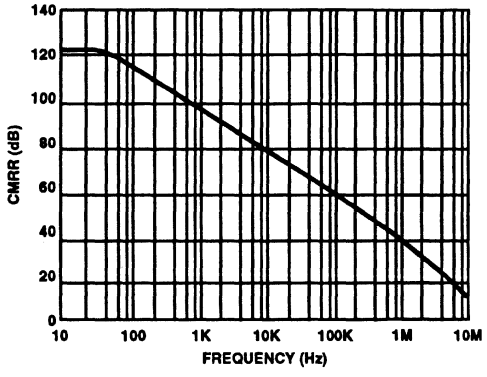


FIGURE 6. CMRR vs FREQUENCY

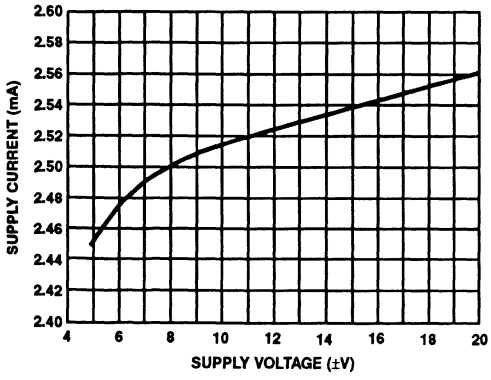


FIGURE 7. SUPPLY CURRENT vs SUPPLY VOLTAGE

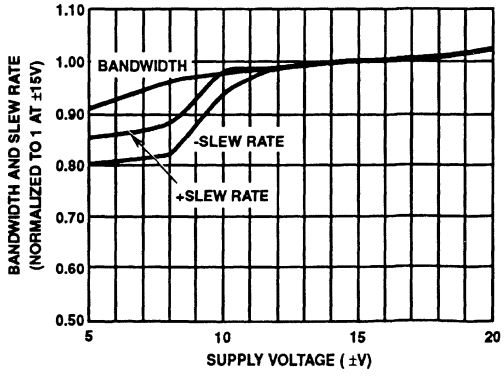


FIGURE 8. BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE

Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V (Continued)

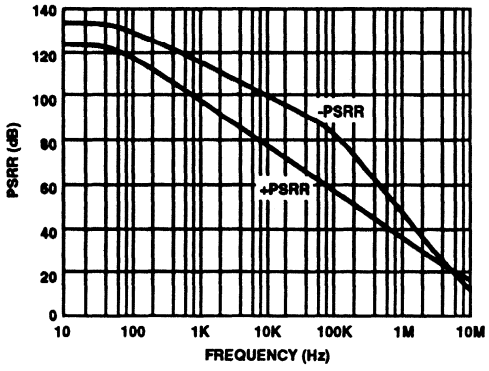


FIGURE 9. PSRR vs FREQUENCY

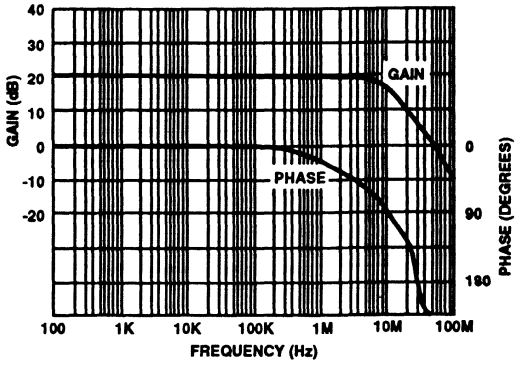


FIGURE 10. CLOSED LOOP GAIN AND PHASE vs FREQUENCY

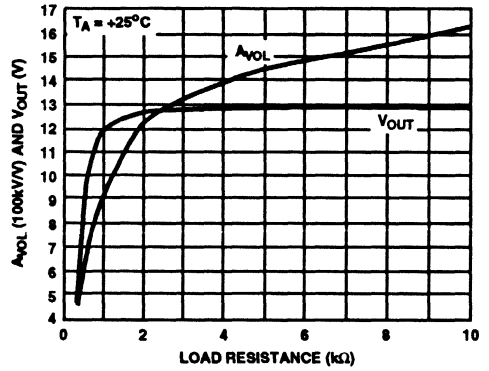


FIGURE 11. A_{VOL} AND V_{OUT} vs LOAD RESISTANCE

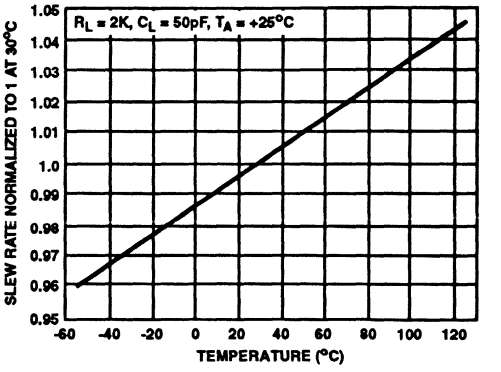


FIGURE 12. NORMALIZED SLEW RATE vs TEMPERATURE

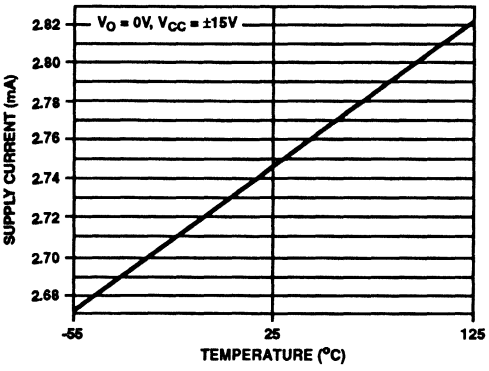


FIGURE 13. SUPPLY CURRENT vs TEMPERATURE

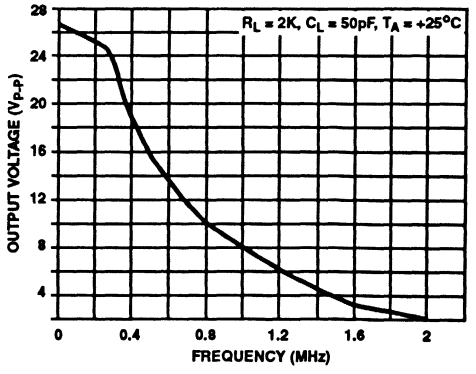


FIGURE 14. V_{OUT} MAX (UNDISTORTED SINEWAVE OUTPUT) vs FREQUENCY

Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V (Continued)

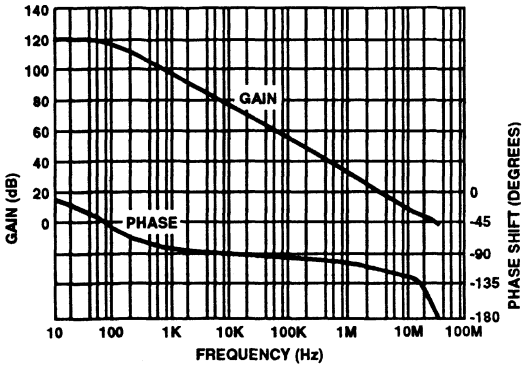


FIGURE 15. OPEN LOOP GAIN AND PHASE vs. FREQUENCY

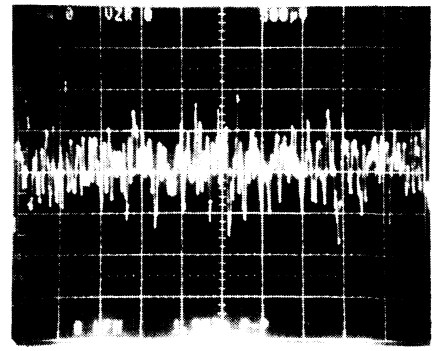


FIGURE 16. PEAK-TO-PEAK NOISE VOLTAGE (0.1Hz TO 10Hz)
A_{CL} = 25,000V/V
Horizontal Scale = 1sec/Div.
Vertical Scale = 0.002μV/Div.
E_N = 0.08μV_{P-P} RTI

Application Information

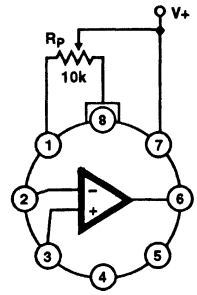
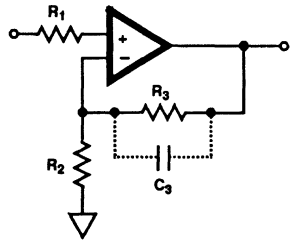
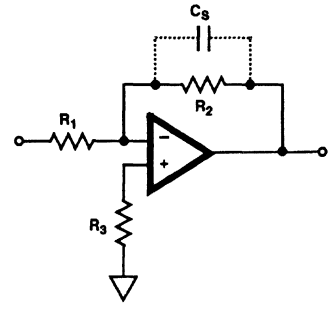


FIGURE 17. SUGGESTED OFFSET VOLTAGE ADJUSTMENT

Test Offset Adjustment Range is $|V_{OS}$ + 1mV| minimum referred to output. Typical range is ±4mV with R_P = 10kΩ.





Low resistances are preferred for low noise applications as a 1kΩ resistor has 4nV/$\sqrt{Hz}$ of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

FIGURE 18. SUGGESTED STABILITY CIRCUITS

HA-5142, HA-5144

Dual/Quad Ultra-Low Power Operational Amplifiers

April 1993

Features

- Low Supply Current 45μA/Amp
- Wide Supply Voltage Range Single . . . . . 3V to 30V or Dual . . . . . ±1.5V to ±15V
- High Slew Rate 1.5V/μs
- High Gain 100kV/V
- Unity Gain Stable
- Available in Duals and Quads

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Instrumentation
- For Further Design Ideas See Application Note 544

Description

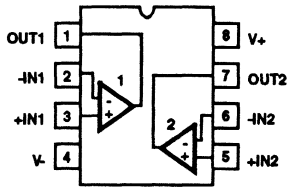
The HA-5142/44 ultra-low power operational amplifiers provide AC and DC performance characteristics similar to or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. In applications which require low power dissipation and good AC electrical characteristics, this family offers the industry's best speed/power ratio.

The HA-5142/44 provides accurate signal processing by virtue of their low input offset voltage (2mV), low input bias current (45nA), high open loop gain (100kV/V) and low noise (20nV/√Hz), for low power operational amplifiers. These characteristics coupled with a 1.5V/μs slew rate and a 400kHz bandwidth make the HA-5142/44 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (3V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment. These parts are also tested and guaranteed at both ±15V and single ended +5V supplies.

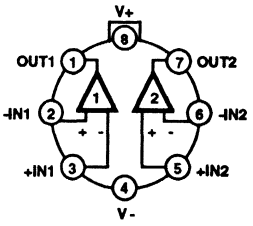
These amplifiers are available with industry standard pinouts which allow the HA-5142/5144's to be interchangeable with most other operational amplifiers. For military grade product refer to the 5142, 5144/883 data sheet.

Pinouts (See Ordering Information on Next Page)

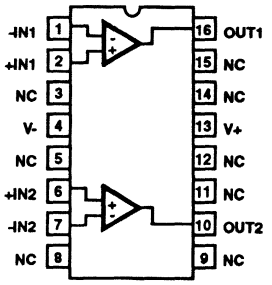
HA-5142 (PDIP, CDIP)
TOP VIEW



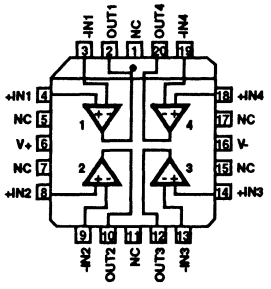
HA-5142 (TO-99 METAL CAN)
TOP VIEW



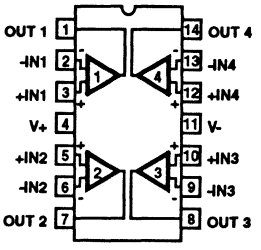
HA-5142 (300 mil SOIC)
TOP VIEW



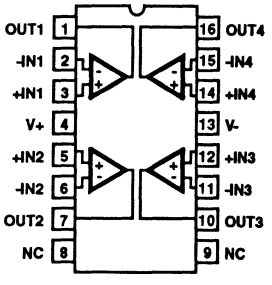
HA-5144 (PLCC)
TOP VIEW



HA-5144 (PDIP, CDIP)
TOP VIEW



HA-5144 (300 mil SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

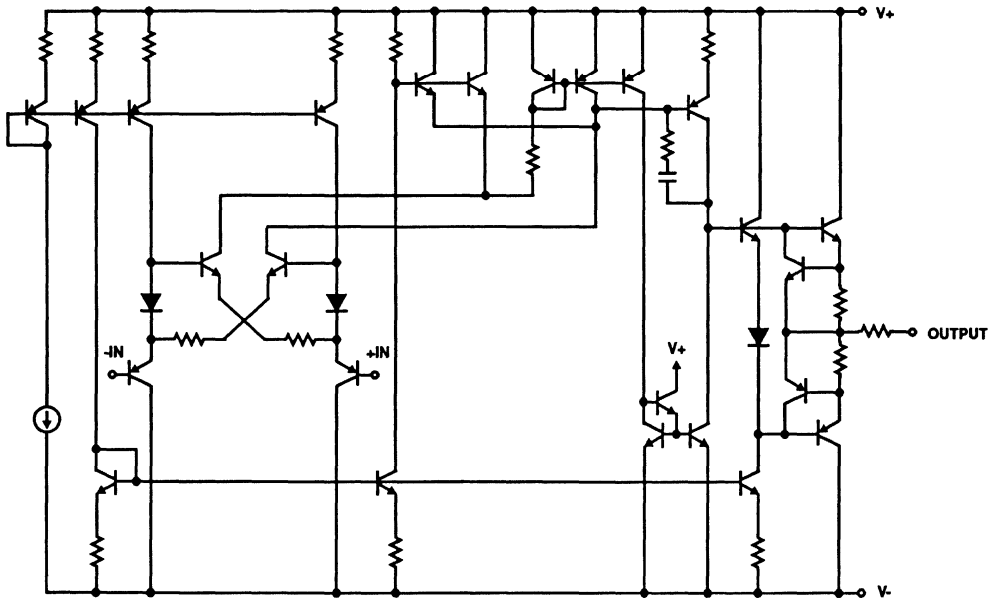
File Number **2909.1**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-5142-2	-55°C to +125°C	8 Pin Can
HA2-5142-5	0°C to +75°C	8 Pin Can
HA3-5142-5	0°C to +75°C	8 Lead Plastic DIP
HA7-5142-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5142-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P5142-5	0°C to +75°C	16 Lead Wide Body SOIC
HA9P5142-9	-40°C to +85°C	16 Lead Wide Body SOIC

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-5144-2	-55°C to +125°C	14 Lead Ceramic DIP
HA1-5144-5	0°C to +75°C	14 Lead Ceramic DIP
HA3-5144-5	0°C to +75°C	14 Lead Plastic DIP
HA4P5144-5	0°C to +75°C	20 Lead PLCC
HA9P5144-5	0°C to +75°C	16 Lead Wide Body SOIC
HA9P5144-9	-40°C to +85°C	16 Lead Wide Body SOIC

Schematic Diagram



Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 7V
Output Current ..... Short Circuit Protected
Junction Temperature (Note 12) ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-5142/44-5 ..... $0°C \le T_A \le +75°C$
HA-5142/44-2 ..... $-55°C \le T_A \le +125°C$
HA-5142/44-9 ..... $-40°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$R_S = 100\Omega$, $C_L \le 10pF$, Unless Otherwise Specified

PARAMETER	TEMP	-2, -5, -9 V+ = +5V, V- = 0V			-2, -5, -9 V+ = +15V, V- = -15V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage (Note 11)	+25°C	-	2	6	-	2	6	mV
	Full	-	-	8	-	-	8	mV
Average Offset Voltage Drift	Full	-	3	-	-	3	-	µV/°C
Bias Current (Note 11)	+25°C	-	45	100	-	45	100	nA
	Full	-	-	125	-	-	125	nA
Offset Current (Note 11)	+25°C	-	0.3	10	-	0.3	10	nA
	Full	-	-	20	-	-	20	nA
Common Mode Range	Full	0 to 3	-	-	±10	-	-	V
Differential Input Resistance	+25°C	-	0.6	-	-	0.6	-	MΩ
Input Noise Voltage (f = 1kHz)	+25°C	-	20	-	-	20	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C	-	0.25	-	-	0.25	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 2, 4)	+25°C	20	100	-	20	100	-	kV/V
	Full -2, -5	15	-	-	15	-	-	kV/V
	Full -9	12	-	-	12	-	-	kV/V
Common Mode Rejection Ratio (Note 7)	Full -2, -5	77	105	-	77	105	-	dB
	Full -9	70	105	-	70	105	-	dB
Bandwidth (Notes 2, 3)	+25°C	-	0.4	-	-	0.4	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Notes 2, 10)	+25°C	1.0 to 3.8	0.7 to 4.2	-	±10	±13	-	V
	Full	1.2 to 3.5	0.9 to 4.0	-	±10	±13	-	V
Full Power Bandwidth (Notes 2, 4, 8)	+25°C	-	240	-	-	24	-	kHz

Electrical Specifications $R_S = 100\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	-2, -5, -9 V+ = +5V, V- = 0V			-2, -5, -9 V+ = +15V, V- = -15V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Notes 2, 3)								
Rise Time	+25°C	-	600	-	-	600	-	ns
Slew Rate (Note 6)	+25°C	0.8	1.5	-	0.8	1.5	-	V/µs
Settling Time (Note 5)	+25°C	-	10	-	-	10	-	µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	45	80	-	100	150	µA/Amp
	Full	-	-	100	-	-	200	µA/Amp
Power Supply Rejection Ratio (Note 9)	Full -2, -5	77	105	-	77	105	-	dB
	Full -9	70	105	-	70	105	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $R_L = 50k\Omega$
3. $C_L = 50pF$
4. $V_O = 1.4$ to 2.5V for $V_{CC} = +5, 0V$; $V_O = \pm 10V$ for $V_{CC} = \pm 15V$.
5. Settling Time is specified to 0.1% of final value for a 3V output step and $A_V = -1$ for $V_{CC} = +5V, 0V$. Output step = 10V for $V_{CC} = \pm 15V$.
6. Maximum input slew rate = 10V/µs.
7. $V_{CM} = 0$ to 3V for $V_{CC} = +5, 0V$; $V_{CM} = \pm 10V$ for $V_{CC} = \pm 15V$.
8. Full Power Bandwidth is guaranteed by equation: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
9. $\Delta V_S = +10V$ for $V_{CC} = +5, 0V$; $\Delta V_S = \pm 5V$ for $V_{CC} = \pm 15V$.
10. For $V_{CC} = +5, 0V$ terminate R_L at +2.5V. Typical output current is ±3mA.
11. $V_O = 1.4V$ for $V_{CC} = +5V, 0V$.
12. See Thermal Constants in "Die Characteristics" section.

Die Characteristics

Transistor Count
- HA-5142 66
- HA-5144 132

Substrate Potential* ..... V-

Process ..... Bipolar-DI

* The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
HA1-5144 (CDIP)	71	13
HA2-5142 (CAN)	111	34
HA3-5142 (Plastic Mini DIP)	92	30
HA3-5144 (PDIP)	108	38
HA4P5144 (PLCC)	74	32
HA7-5142 (Ceramic Mini DIP)	114	35
HA9P5142 (SOIC)	113	35
HA9P5144 (SOIC)	96	26

Test Circuits

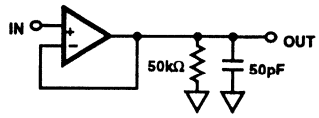
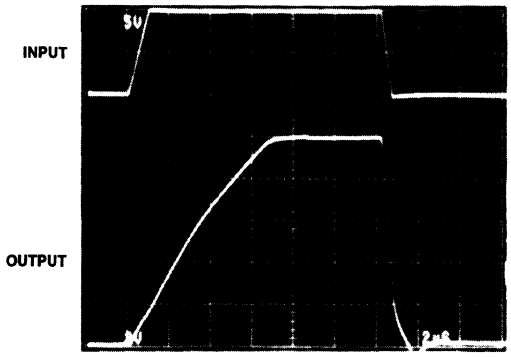


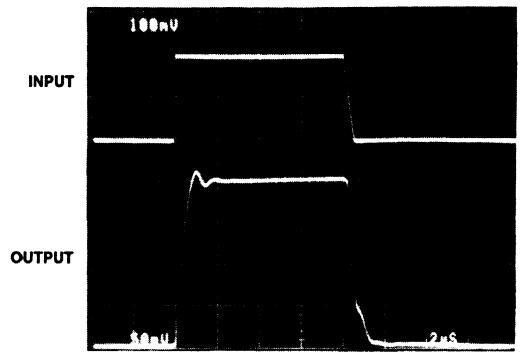
FIGURE 1. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT

LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 5V/Div.; Output = 2V/Div.)
Horizontal Scale: (Time: 2µs/Div.)



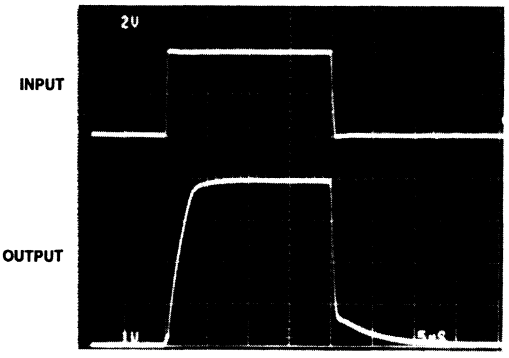
$+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V

SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 2µs/Div.)



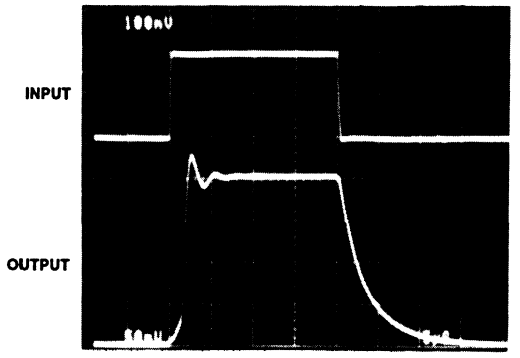
$+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V

LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 2V/Div.; Output = 1V/Div.)
Horizontal Scale: (Time: 5µs/Div.)



$+V_{SUPPLY}$ = +5V, $-V_{SUPPLY}$ = 0V

SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 5µs/Div.)



$+V_{SUPPLY}$ = +5V, $-V_{SUPPLY}$ = 0V

Typical Performance Curves $V_S = \pm 2.5V$, $T_A = +25°C$, Unless Otherwise Specified

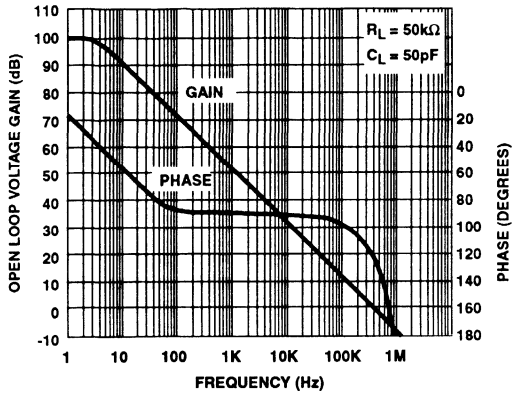


FIGURE 2. OPEN LOOP FREQUENCY RESPONSE

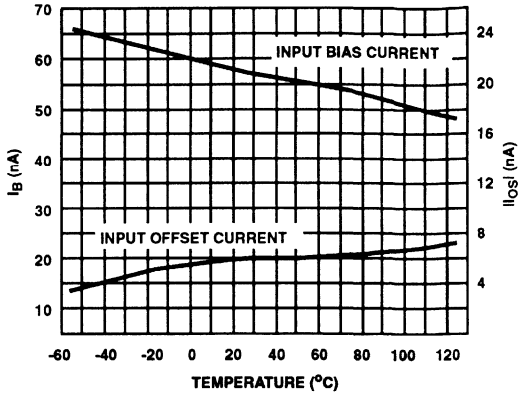


FIGURE 3. INPUT OFFSET CURRENT AND BIAS CURRENT vs TEMPERATURE

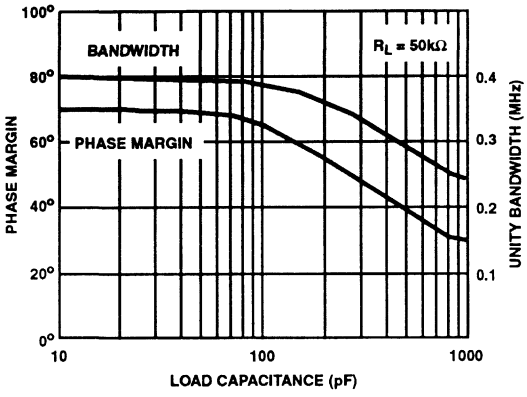


FIGURE 4. BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE

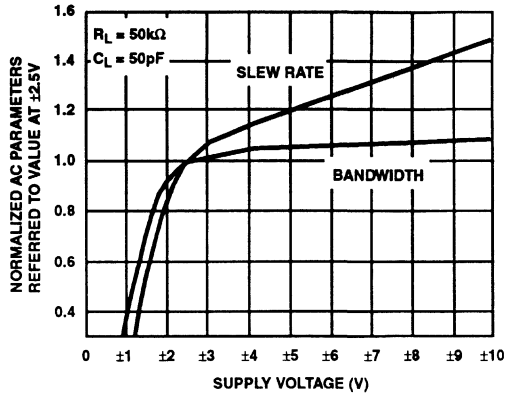


FIGURE 5. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

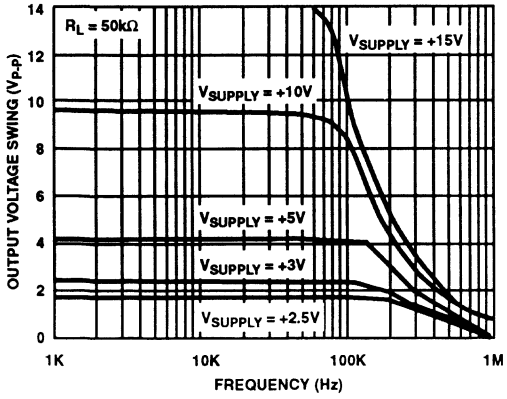


FIGURE 6. OUTPUT VOLTAGE SWING vs FREQUENCY AND SINGLE SUPPLY VOLTAGE

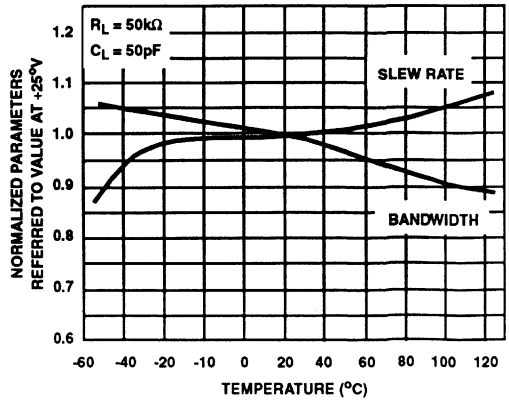


FIGURE 7. NORMALIZED AC PARAMETERS vs TEMPERATURE

Typical Performance Curves $V_S = \pm 2.5V$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

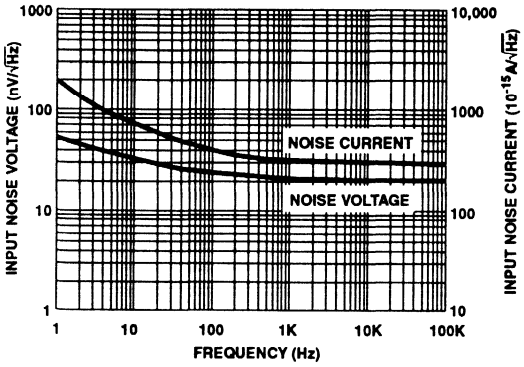


FIGURE 8. INPUT NOISE vs FREQUENCY

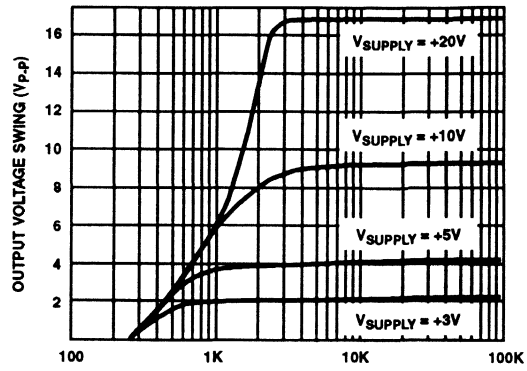


FIGURE 9. MAXIMUM OUTPUT VOLTAGE SWING vs LOAD RESISTANCE AND SINGLE SUPPLY VOLTAGE

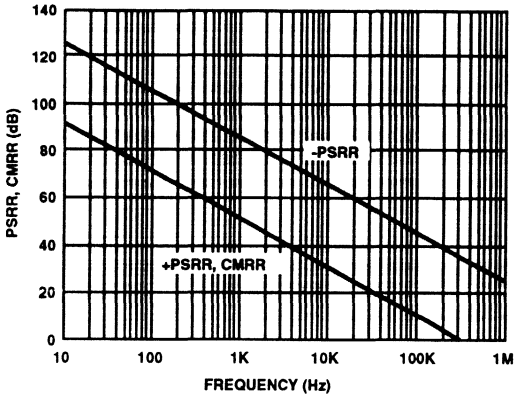


FIGURE 10. PSRR AND CMRR vs FREQUENCY

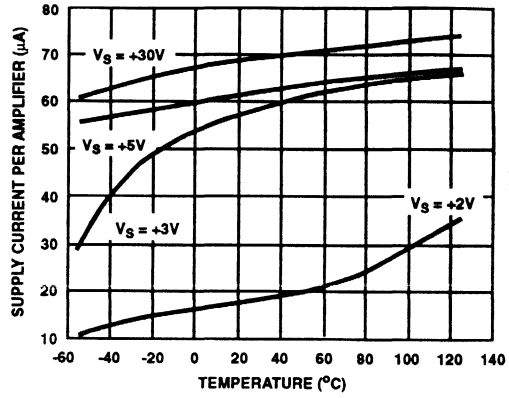


FIGURE 11. POWER SUPPLY CURRENT vs TEMPERATURE AND SINGLE SUPPLY VOLTAGE

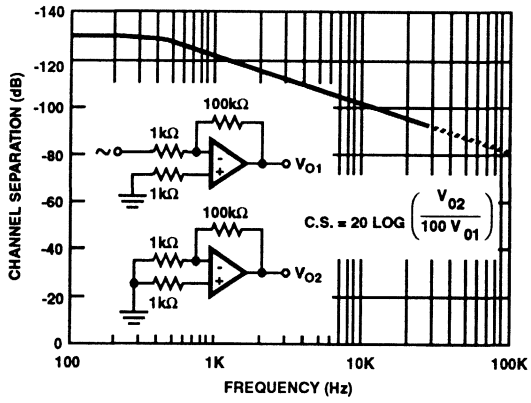


FIGURE 12. CHANNEL SEPARATION vs FREQUENCY

HARRIS SEMICONDUCTOR

HA-5147

Ultra-Low Noise Precision High Slew Rate Wideband Operational Amplifier

March 1993

Features

- High Speed 35V/μs
- Wide Gain Bandwidth ($A_V \geq 10$) 120MHz
- Low Noise ..... 3nV/√Hz at 1kHz
- Low V_{OS} 10μV
- High CMRR 126dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HA2-5147-2	-55°C to +125°C	8 Pin Can
HA2-5147-5	0°C to +75°C	8 Pin Can
HA2-5147A-2	-55°C to +125°C	8 Pin Can
HA2-5147A-5	0°C to +75°C	8 Pin Can
HA3-5147-5	0°C to +75°C	8 Lead Plastic DIP
HA7-5147-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5147-5	0°C to +75°C	8 Lead Ceramic DIP
HA7-5147A-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5147A-5	0°C to +75°C	8 Lead Ceramic DIP

Description

The HA-5147 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3nV/√Hz) precision instrumentation performance with high speed (35V/μs) wideband capability.

This amplifier's impressive list of features include low V_{OS} (10μV), wide gain bandwidth (120MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140mW of power.

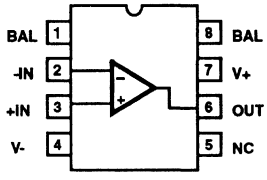
Using the HA-5147 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than ten.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5147's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits. Further application ideas are given in Application Note 553.

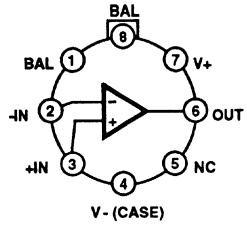
This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than ten. For military grade product, refer to the HA-5147/883 data sheet.

Pinouts

HA-5147
(PDIP, CDIP)
TOP VIEW



HA-5147
(TO-99 METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2910.1**

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated
Voltage Between V+ and V- Terminals ..... ±44V
Differential Input Voltage (Note 2) 0.7V
Output Current ..... Full Short Circuit Protection
Junction Temperature (Note 13) ..... +175°C
Junction Temperature (Plastic Packages) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Ranges
HA-5147/47A-2 ..... -55°C ≤ T_A ≤ +125°C
HA-5147/47A-5 ..... 0°C ≤ T_A ≤ +75°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = 15V, V- = -15V, C_L ≤ 50pF, R_S ≤ 100Ω

PARAMETERS	TEMP	HA-5147A			HA-5147			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	10	25	-	30	100	µV
	Full	-	30	60	-	70	300	µV
Average Offset Voltage Drift	Full	-	0.2	0.6	-	0.4	1.8	µV/°C
Bias Current	+25°C	-	10	40	-	15	80	nA
	Full	-	20	60	-	35	150	nA
Offset Current	+25°C	-	7	35	-	12	75	nA
	Full	-	15	50	-	30	135	nA
Common Mode Range	Full	±10.3	±11.5	-	±10.3	±11.5	-	V
Differential Input Resistance (Note 3)	+25°C	1.5	6	-	0.8	4	-	MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 4)	+25°C	-	0.08	0.18	-	0.09	0.25	μV_{P-P}
Input Noise Voltage Density (Note 5)								
f = 10Hz	+25°C	-	3.5	5.5	-	3.8	8.0	$nV/\sqrt{Hz}$
f = 100Hz		-	3.1	4.5	-	3.3	5.6	$nV/\sqrt{Hz}$
f = 1000Hz		-	3.0	3.8	-	3.2	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 5)								
f = 10Hz	+25°C	-	1.7	4.0	-	1.7	-	$pA/\sqrt{Hz}$
f = 100Hz		-	1.0	2.3	-	1.0	-	$pA/\sqrt{Hz}$
f = 1000Hz		-	0.4	0.6	-	0.4	0.6	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Minimum Stable Gain	+25°C	10	-	-	10	-	-	V/V
Large Signal Voltage Gain (Note 6)	+25°C	1000	1800	-	700	1500	-	V/mV
	Full	600	1200	-	300	800	-	V/mV
Common Mode Rejection Ratio (Note 7)	Full	114	126	-	100	120	-	dB
Gain-Bandwidth-Product								
f = 10kHz	+25°C	120	140	-	120	140	-	MHz
f = 1MHz		-	120	-	-	120	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
R_L = 600Ω	+25°C	±10.0	±11.5	-	±10.0	±11.5	-	V
R_L = 2kΩ	Full	±11.7	±13.8	-	±11.4	±13.5	-	V
Full Power Bandwidth (Note 8)	+25°C	445	500	-	445	500	-	kHz
Output Resistance, Open Loop	+25°C	-	70	-	-	70	-	Ω
Output Current	+25°C	16.5	25	-	16.5	25	-	mA

Electrical Specifications V+ = 15V, V- = -15V, $C_L \leq 50pF$, $R_S \leq 100\Omega$

PARAMETERS	TEMP	HA-5147A			HA-5147			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 9)								
Rise Time	+25°C	-	22	50	-	22	50	ns
Slew Rate (Note 11)	+25°C	28	35	-	28	35	-	V/µs
Settling Time (Note 10)	+25°C	-	400	-	-	400	-	ns
Overshoot	+25°C	-	20	40	-	20	40	%
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	3.5	-	-	3.5	-	mA
	Full	-	-	4.0	-	-	4.0	mA
Power Supply Rejection Ratio (Note 12)	Full	-	2	4	-	16	51	µV/V

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. The limits for this parameter are guaranteed based on lab characterization, and reflect lot-to-lot variation.
6. $V_{OUT} = \pm 10V$, $R_L = 2k\Omega$
7. $V_{CM} = \pm 10V$
8. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
9. Refer to Test Circuits section of the data sheet.
10. Settling time is specified to 0.1% of final value for a 10V output step and $A_V = -10$.
11. $V_{OUT} = \pm 3V$ (6V Step).
12. $V_S = \pm 4V$ to $\pm 18V$
13. See thermal constants in "Die Characteristics" section.

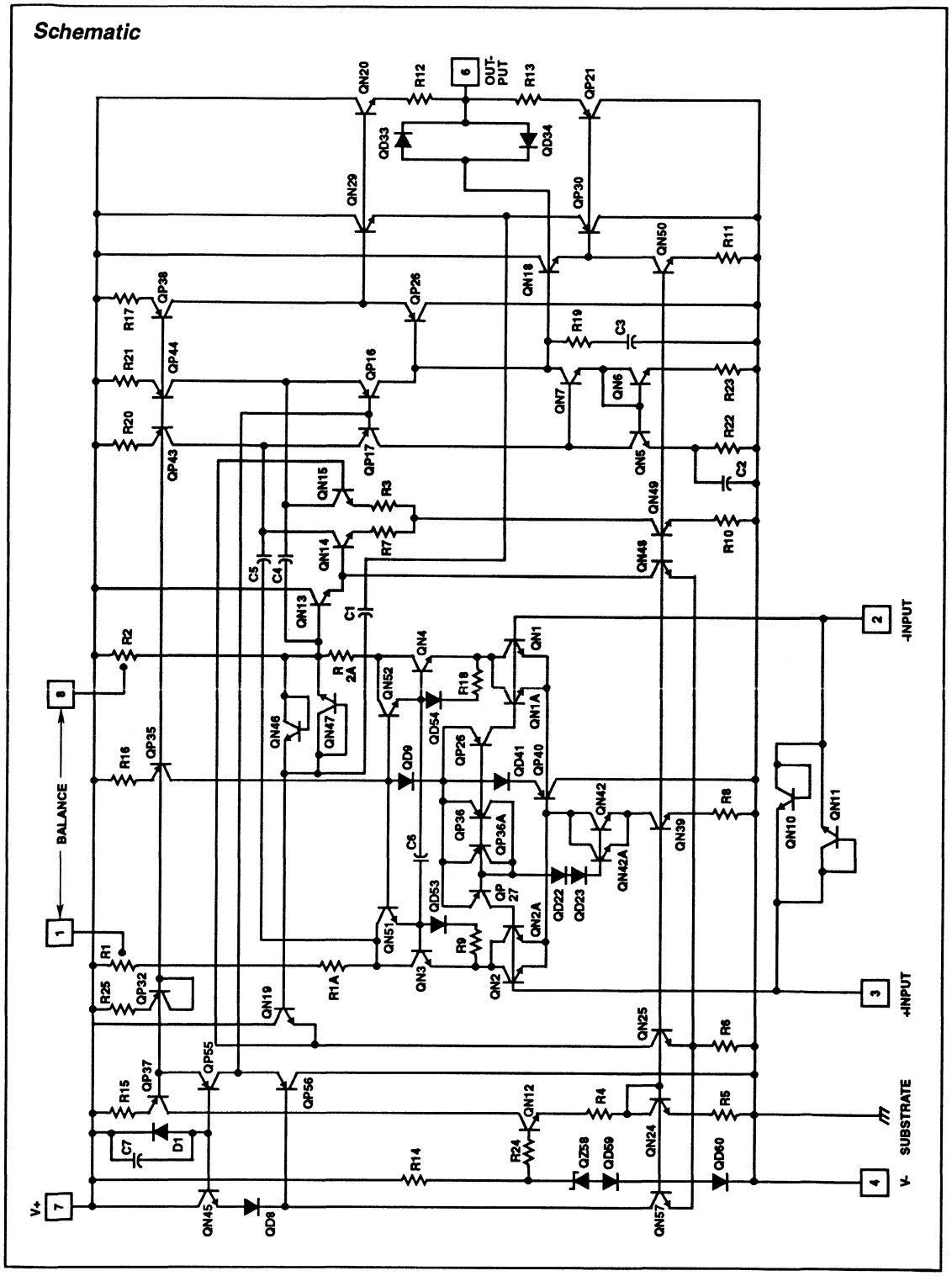
Die Characteristics

Transistor Count 63
Die Dimensions ..... 65 x 104.3 x 19 mils
Substrate Potential* ..... V-
Process ..... Bipolar -DI

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic Mini-DIP	114	34
TO-99 Metal Can	108	33
Plastic DIP	92	30

* The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Schematic


QN20
R12
6
OUT-PUT
R13
QP21
QD33
QD34
QN29
QP30
QN50
R11
QN18
QP38
QP26
R17
R19
C3
QP44
QP16
QN7
QN6
R23
R21
R22
QP43
QP17
QN5
C2
R20
QN15
R3
QN49
R7
R10
QN14
QN48
C5
C4
QN13
C1
2
-INPUT
R2
QN4
QN1
R 2A
QN52
R18
8
QN46
QN47
QN1A
QP35
QD54
QP26
R16
QD9
QD41
QP40
QN42
R8
QP36
QP36A
QN10
QN11
C6
QN39
QN42A
QD22
QD23
QP 27
QD53
QN2A
QN51
1
R1
R9
QN3
QN2
R25
QP32
R1A
3
+INPUT
QN19
QN25
R6
QP55
QP37
R15
QP56
QN12
R4
R5
SUBSTRATE
C7
D1
R24
QZ58
QD59
QN24
QD60
R14
4
V-
7
V+
QN45
QD8
QN57

Test Circuits

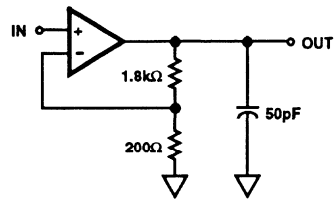
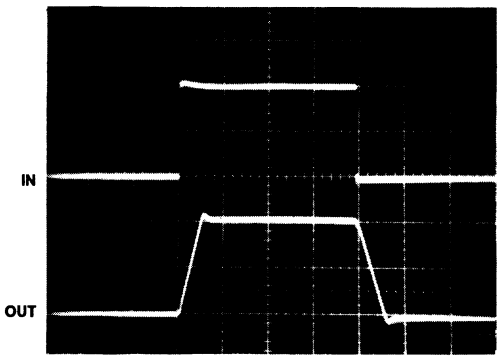
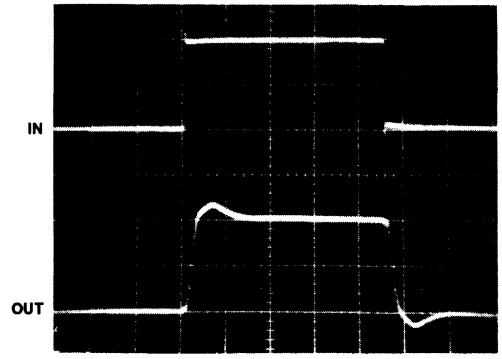


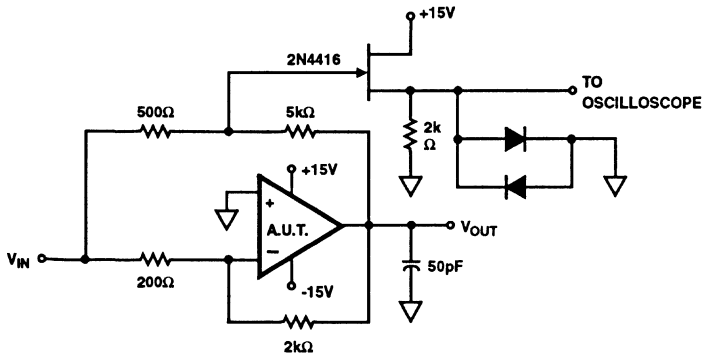
FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 0.5V/Div.)
(Volts: Output = 5V/Div.)
Horizontal Scale: (Time: 500ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 10mV/Div)
(Volts: Output = 100mV/Div)
Horizontal Scale: (Time: 100ns/Div)





$A_V = -10$

Feedback and summing resistors should be 0.1% matched.

Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Typical Performance Curves T_A = +25°C, V_{SUPPLY} = ±15V, Unless Otherwise Specified

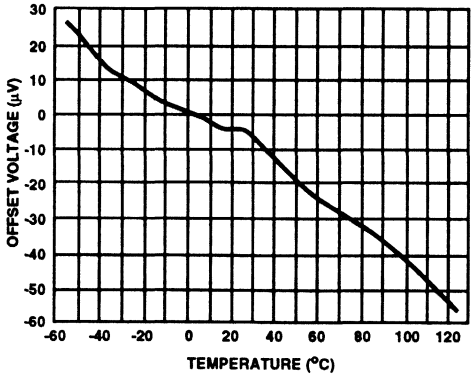


FIGURE 3. TYPICAL OFFSET VOLTAGE DRIFT vs. TEMPERATURE

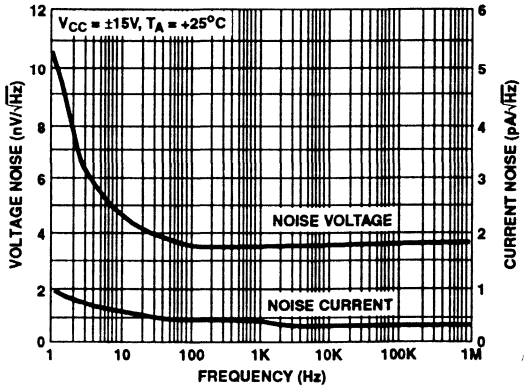


FIGURE 4. NOISE CHARACTERISTICS

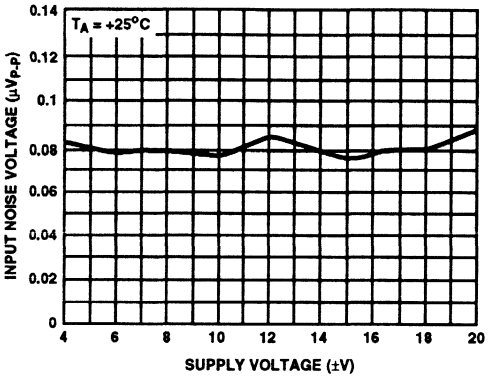


FIGURE 5. NOISE vs. SUPPLY VOLTAGE

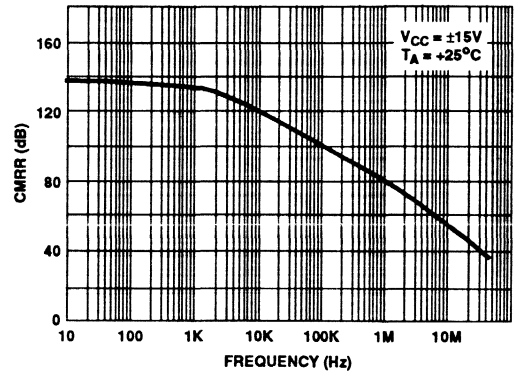


FIGURE 6. CMRR vs. FREQUENCY

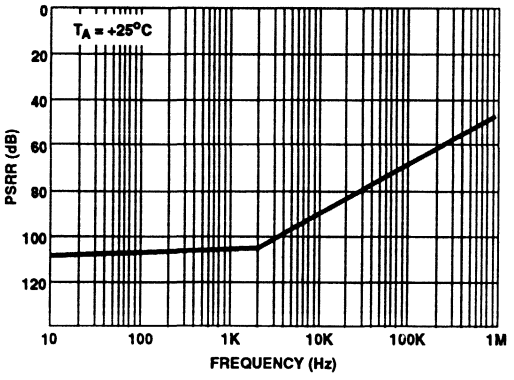


FIGURE 7. PSRR vs. FREQUENCY

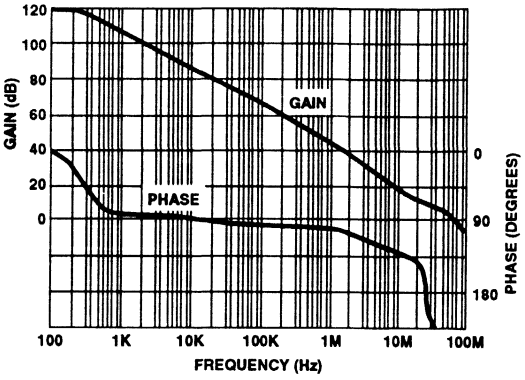


FIGURE 8. OPEN LOOP GAIN AND PHASE vs. FREQUENCY

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified (Continued)

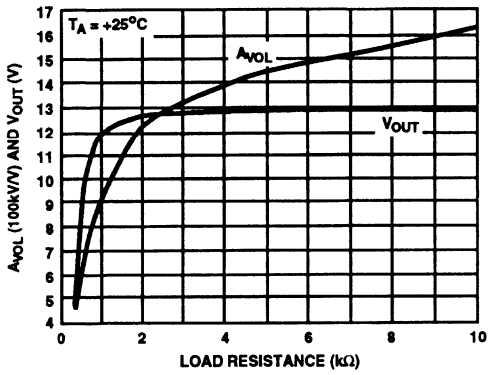


FIGURE 9. A_{VOL} AND V_{OUT} vs. LOAD RESISTANCE

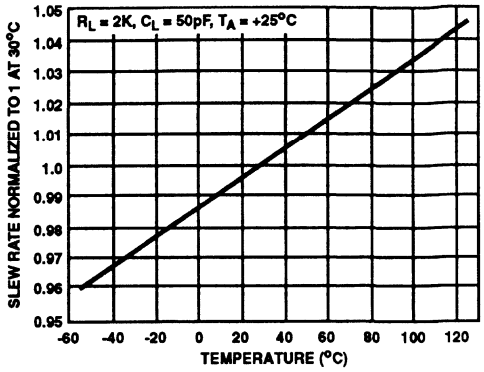


FIGURE 10. NORMALIZED SLEW RATE vs. TEMPERATURE

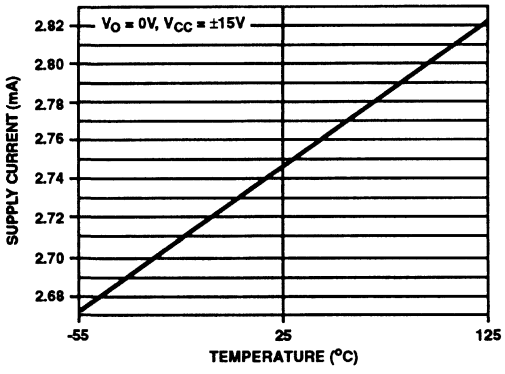


FIGURE 11. SUPPLY CURRENT vs. TEMPERATURE

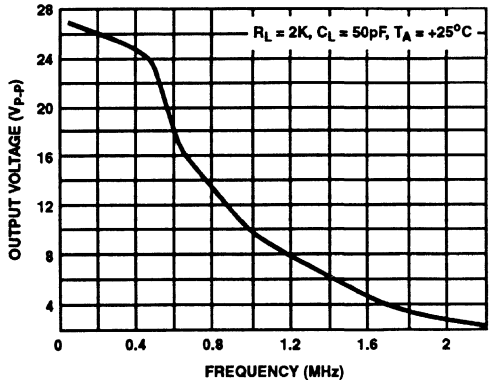


FIGURE 12. V_{OUT} MAX (UNDISTORTED SINEWAVE OUTPUT) vs. FREQUENCY

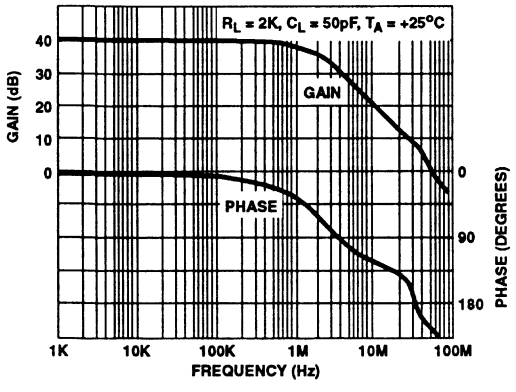


FIGURE 13. CLOSED LOOP GAIN AND PHASE vs FREQUENCY

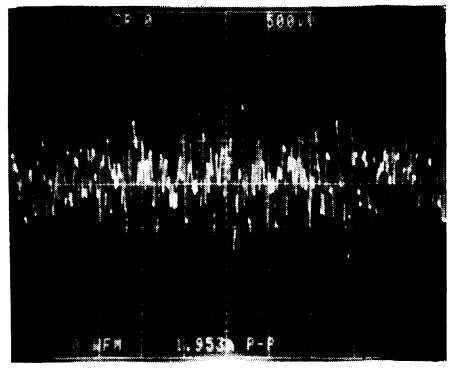
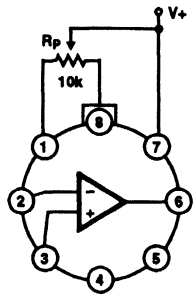


FIGURE 14. PEAK-TO-PEAK NOISE VOLTAGE (0.1Hz TO 10Hz)

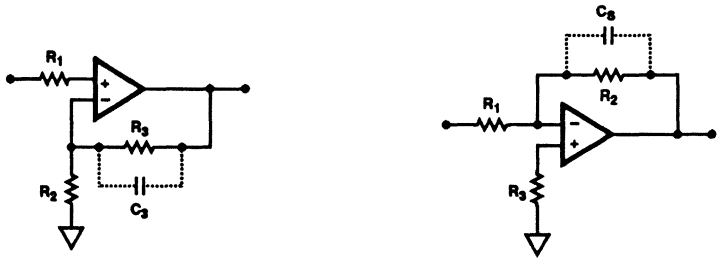
A_{CL} = 25,000V/V
Horizontal Scale = 1sec/Div. Vertical Scale = 0.002μV/Div.
$E_N = 0.08\mu V_{P-P}$ RTI

Application Information



Tested Offset Adjustment Range is $|V_{OS}$ +1mV| minimum referred to output. Typical range is ±4mV with R_T = 10kΩ.

FIGURE 15. SUGGESTED OFFSET VOLTAGE ADJUSTMENT



Low resistances are preferred for low noise applications as a 1kΩ resistor has 4nV/$\sqrt{Hz}$ of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

FIGURE 16. SUGGESTED STABILITY CIRCUITS

HARRIS SEMICONDUCTOR

HA-5160, HA-5162

Wideband, JFET Input High Slew Rate, Uncompensated, Operational Amplifiers

March 1993

Features

- Wide Gain Bandwidth ($A_V \geq 10$) 100MHz
- High Slew Rate 120V/μs
- Settling Time 280ns
- Power Bandwidth 1.9MHz
- Offset Voltage 1.0mV
- Bias Current 20pA

Applications

- Video and RF Amplifiers
- Data Acquisition
- Pulse Amplifiers
- Precision Signal Generation

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-5160-2	-55°C to +125°C	8 Pin Can
HA2-5160-5	0°C to +75°C	8 Pin Can
HA2-5162-5	0°C to +75°C	8 Pin Can

Description

The HA-5160 is a wideband, uncompensated, operational amplifier with FET/Bipolar technologies and Dielectric Isolation. This monolithic amplifier features superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. This device has excellent phase margin at a closed loop gain of 10 without external compensation.

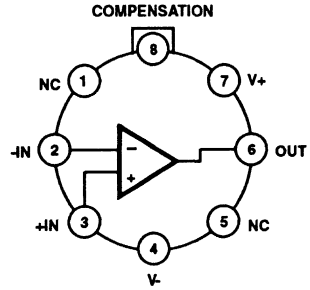
The HA-5160/5162 offers a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics, the Harris devices have nearly constant slew rate, bandwidth, and settling characteristics over the operating temperature range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. Note also that Harris specified all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

Complementing the HA-5160/5162's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and a very high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications. The HA-5160 provides excellent performance for applications which require both precision and high speed performance. The HA-5162 meets or exceeds the performance specifications of National's hybrid op amp, the LH0062.

Military version (/883) data sheets are available upon request.

Pinout

HA-5160/5162
(TO-99 METAL CAN)
TOP VIEW



Case connected to V-

Specifications HA-5160, HA-5162

Absolute Maximum Ratings

Voltage Between V+ and V- 40V
Differential Input Voltage..... 40V
Peak Output Current..... Full Short Circuit Protection
Junction Temperature (Note 2)..... +175°C
Lead Temperature (Soldering 10 Sec.)..... +300°C

Operating Conditions

Operating Temperature Ranges
HA-5160-2.....$-55°C \leq T_A \leq +125°C$
HA-5160-5.....$0°C \leq T_A \leq +75°C$
HA-5162-5.....$0°C \leq T_A \leq +75°C$
Storage Temperature Range.....$-65°C \leq T_A \leq +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +15V, V- = -15V, Unless Otherwise Specified.

PARAMETER	TEMP	HA-5160-2 -55°C to +125°C			HA-5160-5 0°C to +75°C			HA-5162-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	-	1	3	-	1	3	-	3	15	mV
	Full	-	3	5	-	3	5	-	5	20	mV
Offset Voltage Average Drift	Full	-	10	-	-	20	-	-	20	35	µV/°C
Bias Current	+25°C	-	20	50	-	20	50	-	20	65	pA
	Full	-	5	10	-	5	10	-	5	10	nA
Offset Current	+25°C	-	2	10	-	2	10	-	2	10	pA
	Full	-	2	5	-	2	5	-	2	5	nA
Input Capacitance	+25°C	-	5	-	-	5	-	-	5	-	pF
Input Resistance	+25°C	-	10^{12}	-	-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Range	Full	±10	±11	-	±10	±11	-	±10	±11	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	75	150	-	75	150	-	25	100	-	kV/V
	Full	60	100	-	60	100	-	25	75	-	kV/V
Common Mode Rejection Ratio (Note 4)	Full	74	80	-	74	80	-	70	80	-	dB
Minimum Stable Gain	+25°C	10	-	-	10	-	-	10	-	-	V/V
Gain Bandwidth Product ($A_V \geq 10$)	Full	-	100	-	-	100	-	-	100	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 5)	+25°C	±10	±11	-	±10	±11	-	±10	±11	-	V
	Full	±10	±11	-	±10	±11	-	±10	±11	-	V
Output Current (Note 6)	+25°C	±10	±20	-	±10	±20	-	±10	±20	-	mA
Output Short Circuit Current	+25°C	-	±35	-	-	±35	-	-	±35	-	mA
Full Power Bandwidth (Note 3, 7)	+25°C	1.6	1.9	-	1.6	1.9	-	0.8	1.1	-	MHz
Output Resistance (Note 8)	+25°C	-	50	-	-	50	-	-	50	-	Ω

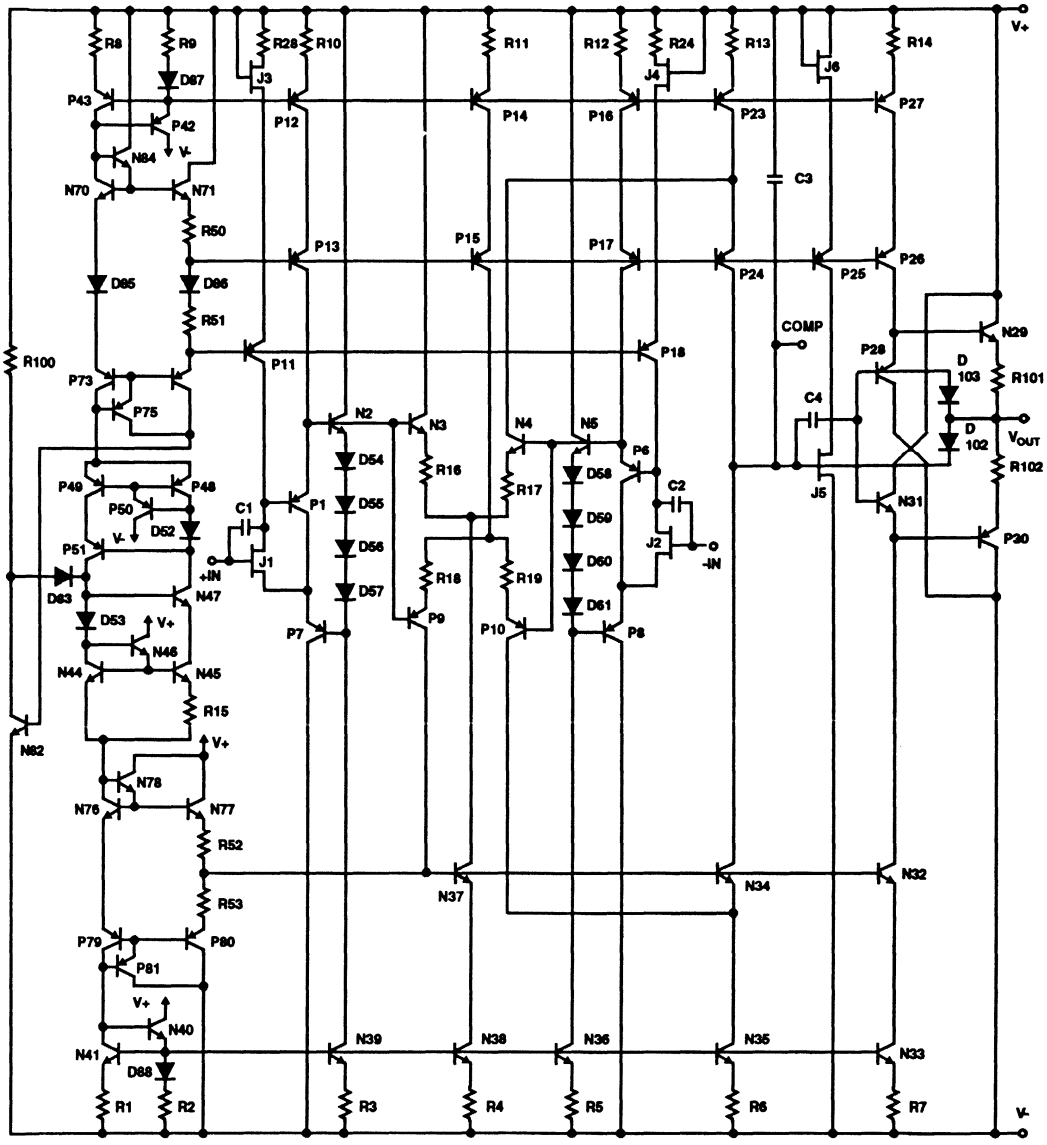
Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEMP	HA-5160-2 -55°C to +125°C			HA-5160-5 0°C to +75°C			HA-5162-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 9)											
Rise Time	+25°C	-	20	-	-	20	-	-	20	-	ns
Slew Rate	+25°C	100	120	-	100	120	-	50	70	-	V/µs
Settling Time (Note 10)	+25°C	-	280	-	-	280	-	-	400	-	ns
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full	-	8	10	-	8	10	-	8	12	mA
Power Supply Rejection Ratio (Note 11)	+25°C	74	86	-	74	86	-	70	86	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. See thermal constant in "Die Characteristics" section.
3. $V_{OUT} = \pm 10V$, $R_L = 2k\Omega$
4. $V_{CM} = \pm 10VDC$
5. $R_L = 2k\Omega$
6. $V_{OUT} = \pm 10V$
7. Full Power Bandwidth guaranteed, based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Output resistance measured under open loop conditions.
9. Refer to Test circuits section of the data sheet, where $A_V = +10$.
10. Settling Time is measured to 0.2% of final value for a 10V output step and $A_V = 10$.
11. $V_{SUPPLY} = \pm 10VDC$ to $\pm 20VDC$

Schematic Diagram



Die Characteristics

Transistor Count 82
Die Dimensions ..... 131 x 72 x 19 mils
(3330µm x 1830µm x 483µm)
Substrate Potential (Powered Up) ..... None

Process ..... Bipolar/JFET DI

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
HA2-5160/5162 (-2, -5, -7)	100	31

Test Circuits

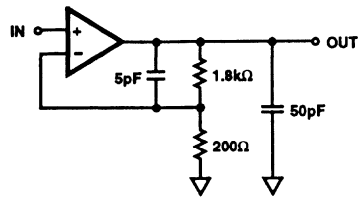
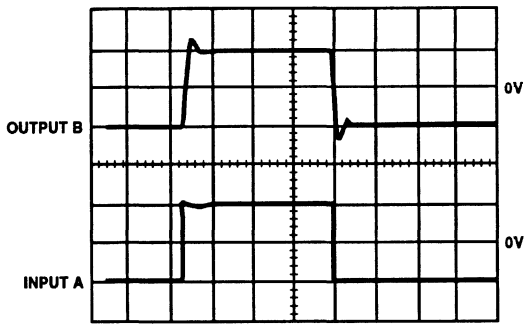
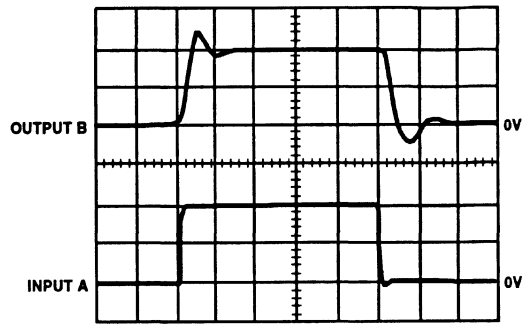


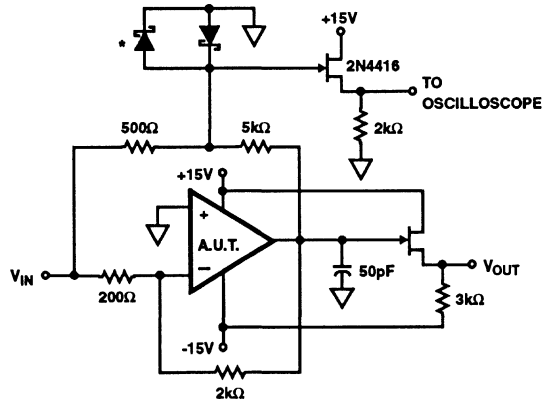
FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

LARGE SIGNAL RESPONSE
Vertical Scale: A = 0.5V/Div., B = 5V/Div.
Horizontal Scale: Time = 500ns/Div.



SMALL SIGNAL RESPONSE
Vertical Scale: A = 10mV/Div., B = 100mV/Div.
Horizontal Scale: Time = 100ns/Div.





A_V = -10

Feedback and summing resistors should be 0.1% matched.

* Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Typical Performance Curves

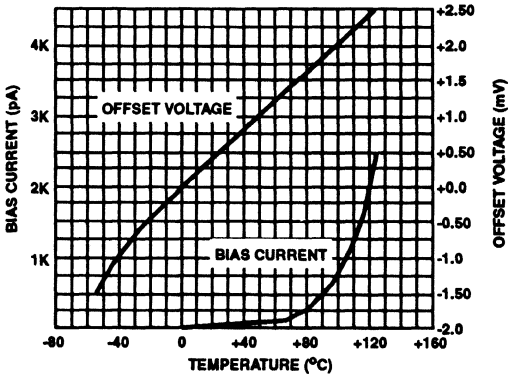


FIGURE 3. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE

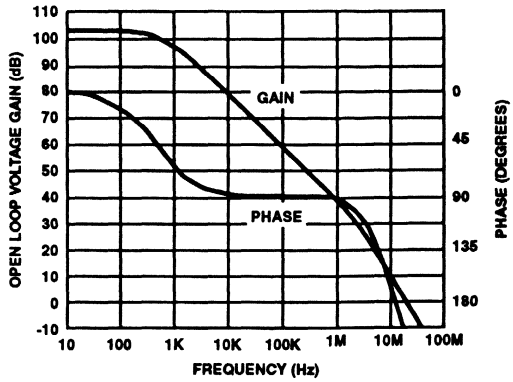


FIGURE 4. OPEN LOOP FREQUENCY RESPONSE

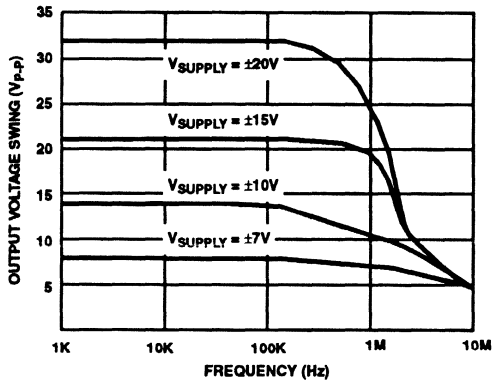


FIGURE 5. OUTPUT VOLTAGE SWING vs. FREQUENCY

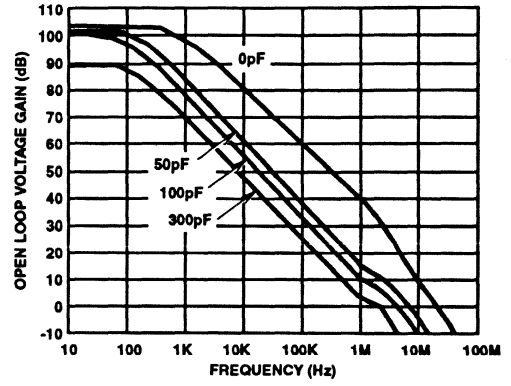


FIGURE 6. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS COMPENSATION CAPACITANCES

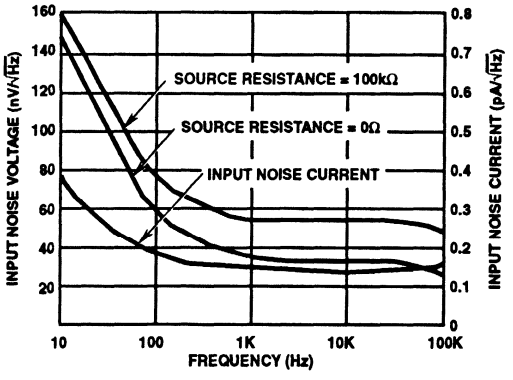


FIGURE 7. INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY

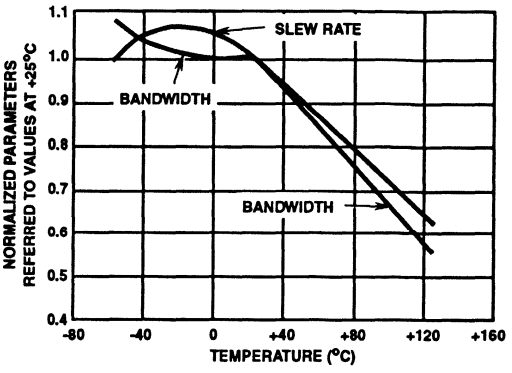


FIGURE 8. NORMALIZED AC PARAMETERS vs. TEMPERATURE

Typical Performance Curves (Continued)

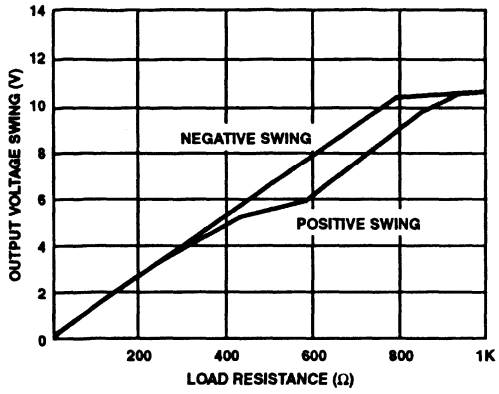


FIGURE 9. OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE

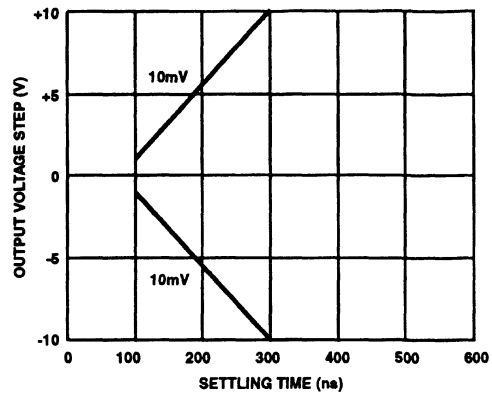


FIGURE 10. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

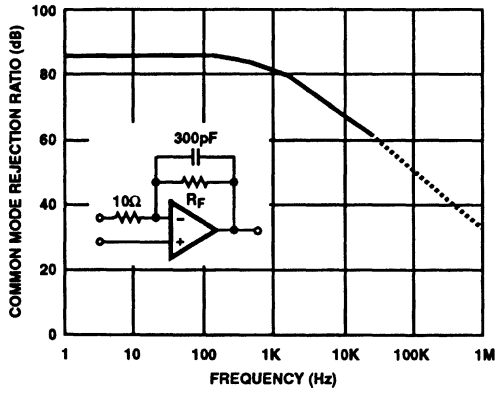


FIGURE 11. COMMON MODE REJECTION RATIO vs FREQUENCY

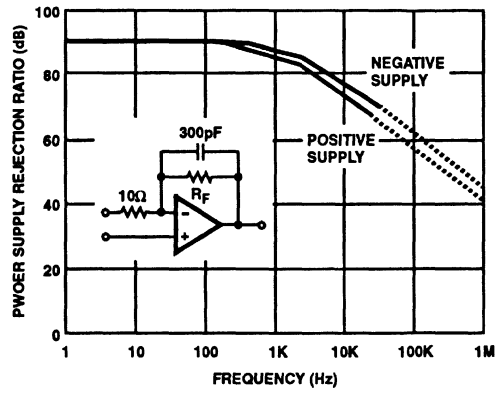


FIGURE 12. POWER SUPPLY REJECTION RATIO vs FREQUENCY

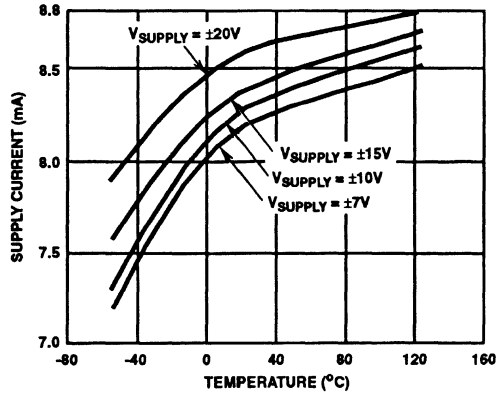


FIGURE 13. POWER SUPPLY CURRENT vs TEMPERATURE

Applying the HA-5160/5162

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. STABILITY: The phase margin of the HA-5160/5162 will be improved by connecting a small capacitor (>10pF) between the output and the inverting input of the device This small capacitor compensates for the input capacitance of the FET.
3. CAPACITIVE LOADS: When driving large capacitive loads (>100pF), it is suggested that a small resistor (≈100Ω) be connected in series with the output of the device and inside the feedback loop.
4. POWER SUPPLY MINIMUM: The absolute supply minimum is ±6V and the safe level is ±7V.

Applications

SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY*

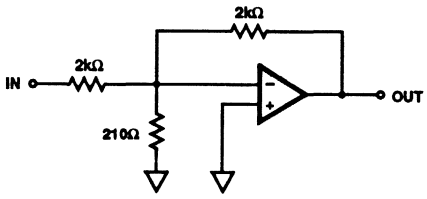
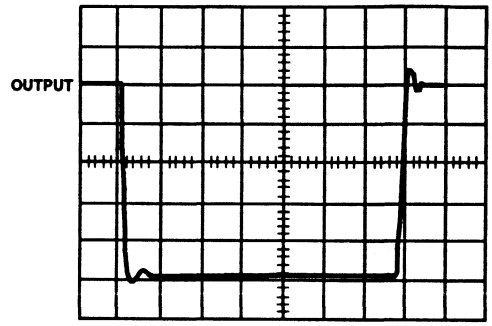


FIGURE 14. INVERTING UNITY GAIN CIRCUIT

INVERTING UNITY GAIN PULSE RESPONSE
Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 500ns/Div.)



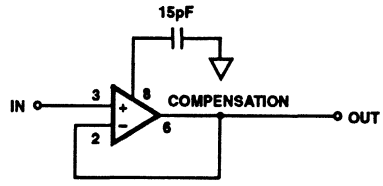
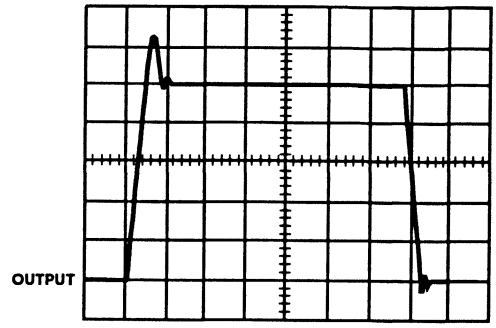


FIGURE 15. NONINVERTING UNITY GAIN CIRCUIT

NONINVERTING UNITY GAIN PULSE RESPONSE
Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 500ns/Div.)



* Values were determined experimentally for optimum speed and settling time.

HARRIS SEMICONDUCTOR

HA-5170

Precision JFET Input Operational Amplifier

March 1993

Features

- Low Offset Voltage.....100μV
- Low Offset Voltage Drift .....2μV/°C
- Low Noise.....10nV/$\sqrt{Hz}$
- High Open Loop Gain 600kV/V
- Wide Bandwidth.....8MHz
- Unity Gain Stable
- Applications
- High Gain Instrumentation Amplifiers
- Precision Data Acquisition
- Precision Integrators
- Precision Threshold Detectors
- For Further Design Ideas, Refer to App. Note 540

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-5170-2	-55°C to +125°C	8 Pin Can
HA2-5170-5	0°C to +75°C	8 Pin Can
HA7-5170-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5170-5	0°C to +75°C	8 Lead Ceramic DIP

Description

The Harris HA-5170 is a precision, JFET input, operational amplifier which features low noise, low offset voltage and low offset voltage drift. Constructed using FET/Bipolar technology, the Harris Dielectric Isolation (DI) process, and laser trimming this amplifier offers low input bias and offset currents. This operational amplifier design also completely eliminates the troublesome errors due to warm-up drift.

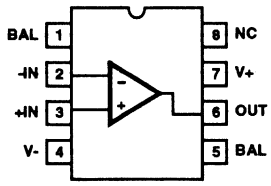
Complementing these excellent input characteristics are dynamic performance characteristics never before available from precision operational amplifiers. An 8V/μs slew rate and 8MHz bandwidth allow the designer to extend precision instrumentation applications in both speed and bandwidth. These characteristics make the HA-5170 well suited for precision integrator amplifier designs.

The superior input characteristics also make the HA-5170 ideally suited for transducer signal amplifiers, precision voltage followers and precision data acquisition systems. For application assistance, please refer to Application Note 540 addressing specifically this device.

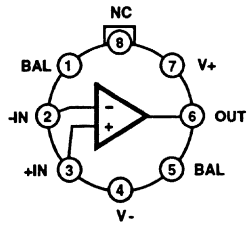
Military version (-8) product and data sheets available upon request.

Pinouts

HA-5170
(CDIP)
TOP VIEW



HA-5170
(TO-99 METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2912.1**

Absolute Maximum Ratings (Note 1)

T_A = +25°C, Unless Otherwise Specified

Voltage Between V+ and V- Terminals 44.0V
Differential Input Voltage 30.0V
Output Short Circuit Duration ..... Indefinite
Junction Temperature (Note 2) ..... +175°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-5170-2 ..... -55°C ≤ T_A ≤ +125°C
HA-5170-5 ..... 0°C ≤ T_A ≤ +75°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	113	34
Can	105	32

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified

PARAMETER	TEMP	HA-5170-2 -55°C to +125°C			HA-5170-5 0°C to + 75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	0.1	0.3	-	0.1	0.3	mV
	Full	-	-	0.5	-	-	0.5	mV
Average Offset Voltage Drift (Note 3)	Full	-	2	5	-	2	5	µV/°C
Bias Current	+25°C	-	20	100	-	20	100	pA
	Full	-	3	30	-	0.1	2	nA
Bias Current Average Drift	Full	-	3	-	-	3	-	pA/°C
Offset Current	+25°C	-	3	30	-	3	60	pA
	Full	-	-	5	-	-	0.1	nA
Offset Current Average Drift (Note 3)	Full	-	0.3	1	-	0.3	1	pA/°C
Common Mode Range	Full	±10	+15.1	-	±10	+15.1	-	V
	Full		-12	-	-	-12	-	V
Differential Input Capacitance	+25°C	-	80	100	-	80	100	pF
Differential Input Resistance (Note 3)	+25°C	$1x10^{10}$	$6x10^{10}$	-	$1x10^{10}$	$6x10^{10}$	-	Ω
Input Capacitance (Single Ended)	+25°C	-	12	-	-	12	-	pF
Input Noise Voltage 0.1Hz to10Hz (Note 3)	+25°C	-	0.5	5	-	0.5	5	μV_{P-P}
Input Noise Voltage Density (Note 3)								
f_O = 10Hz	+25°C	-	20	150	-	20	150	nV/$\sqrt{Hz}$
f_O = 100Hz	+25°C	-	12	50	-	12	50	nV/$\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	10	25	-	10	25	nV/$\sqrt{Hz}$
Input Noise Current Density (Note 3)								
f_O = 10Hz	+25°C	-	0.05	-	-	0.05	-	pA/$\sqrt{Hz}$
f_O = 100Hz	+25°C	-	0.01	-	-	0.01	-	pA/$\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	0.01	0.1	-	0.01	0.1	pA/$\sqrt{Hz}$

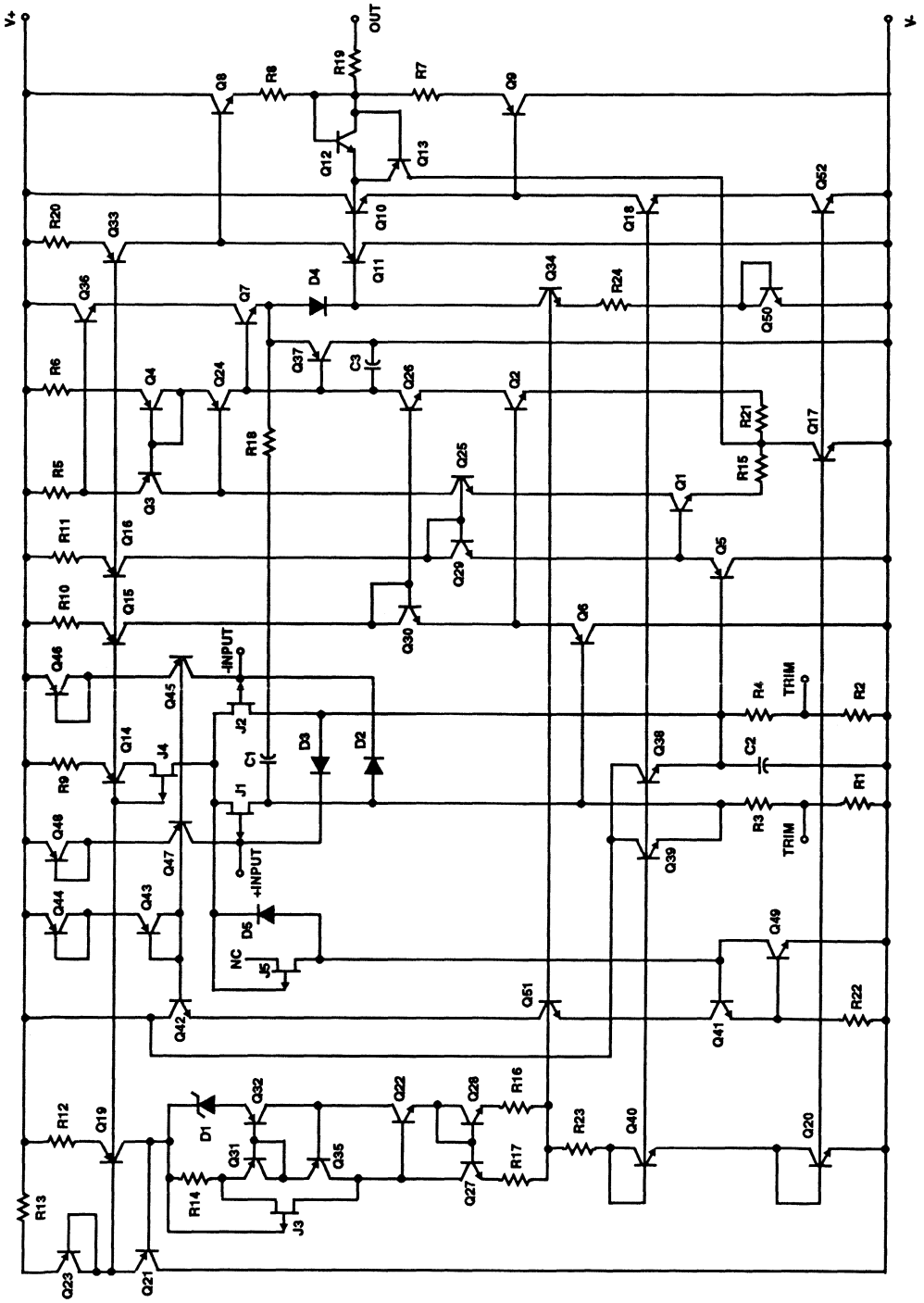
Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified

PARAMETER	TEMP	HA-5170-2 -55°C to +125°C			HA-5170-5 0°C to + 75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 4)	+25°C	300	600	-	300	600	-	kV/V
	Full	200	-	-	250	-	-	kV/V
Common Mode Rejection Ratio (Note 5)	Full	85	100	-	90	100	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	V/V
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	4	8	-	4	8	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12	-	±10	±12	-	V
Full Power Bandwidth (Note 7)	+25°C	80	120	-	80	120	-	kHz
Output Current (Note 8)	+25°C	±10	±15	-	±10	±15	-	mA
Output Resistance (Note 3 & 9)	+25°C	-	45	100	-	45	100	Ω
TRANSIENT RESPONSE								
Rise Time	+25°C	-	45	100	-	45	100	ns
Slew Rate	+25°C	5	8	-	5	8	-	V/µs
Settling Time (Notes 3 & 10)	+25°C	-	1	5	-	1	5	µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	1.9	2.5	-	1.9	2.5	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105	-	90	105	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceable of the circuit may be impaired. Functional operable under any of these conditions is not necessarily implied.
2. Maximum power dissipation must be designed to maintain junction temperature below +175°C.
3. Parameter is not 100% tested. 90% of all units meet or exceed these specifications.
4. V_{OUT} = ±10V, R_L = 2kΩ.
5. ΔV_{CM} = ±10VDC.
6. R_L = 2kΩ.
7. R_L = 2kΩ; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SlewRate}{2\pi V_{PEAK}}$
8. V_{OUT} = ±10V. I_{SC} turns on at ≅ 23mA.
9. Output resistance measured under open loop conditions (f = 100Hz).
10. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
11. V+ = +15V, V- = -10V to -20V and V- = -15V, V+ = +10V to +20V.

Schematic


V+
V-
OUT
-INPUT
+INPUT
TRIM
TRIM
NC
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
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Q43
Q44
Q45
Q46
Q47
Q48
Q49
Q50
Q51
Q52
D1
D2
D3
D4
D5
J1
J2
J3
J4
J5
C1
C2
C3
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24

Test Circuits

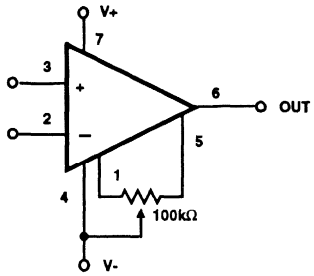


FIGURE 1. V_{OS} ADJUSTMENT

Tested Offset Adjustment Range is $|V_{OS}$ + 1mV| minimum referred to output. Typical range is ±5mV with R_T = 1kΩ and ±15mV with R_T = 100kΩ.

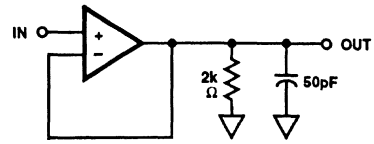
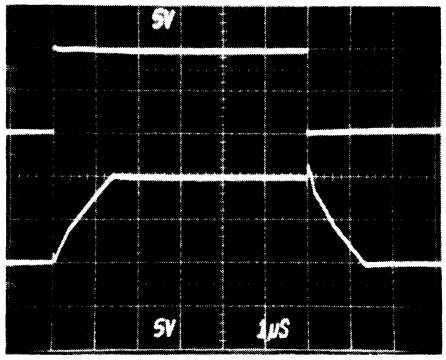


FIGURE 2. LARGE AND SMALL SIGNAL RESPONSE CIRCUIT

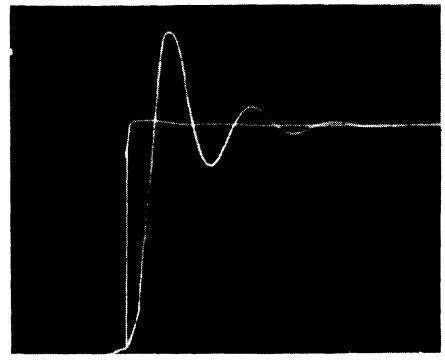
LARGE SIGNAL RESPONSE

Vertical Scale: 5V/Div.
Horizontal Scale: 1μs/Div.



SMALL SIGNAL RESPONSE

Vertical Scale: 10mV/Div.
Horizontal Scale: 100ns/Div.



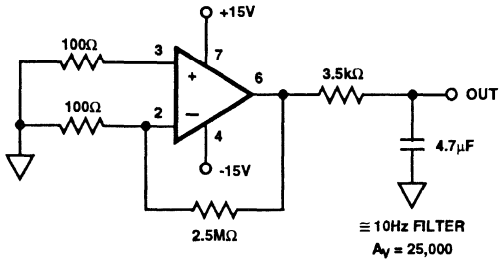
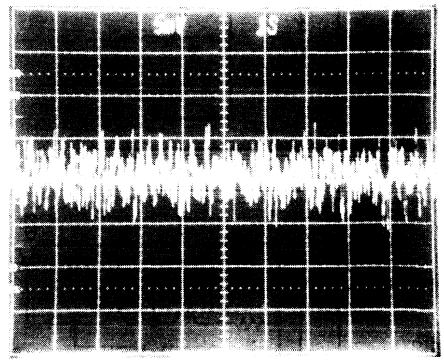


FIGURE 3. LOW FREQUENCY NOISE TEST CIRCUIT

HA-5170 LOW FREQUENCY NOISE (0.1Hz TO 10Hz)

Vertical Scale: 200nV/Div. (Noise Referred to Input)
5mV/Div. at Output, A_{VCL} = 25,000.
Horizontal Scale: 1s./Div.



Typical Performance Curves

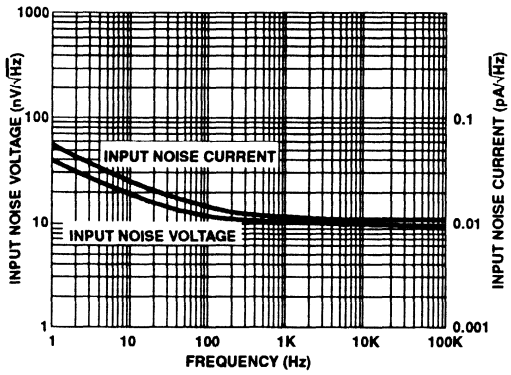


FIGURE 4. INPUT NOISE vs FREQUENCY

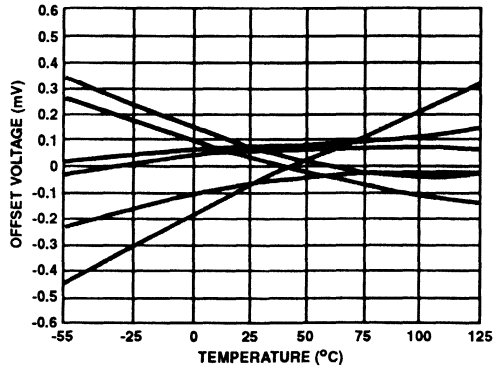


FIGURE 5. OFFSET VOLTAGE DRIFT vs TEMPERATURE OF REPRESENTATIVE UNITS

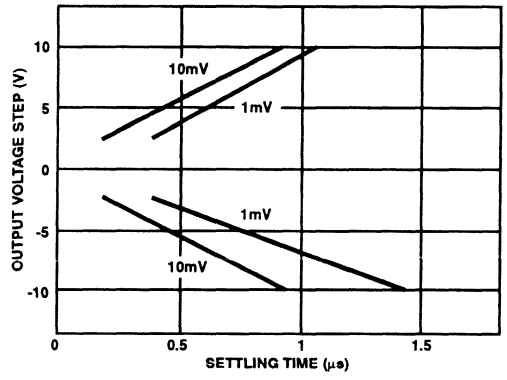


FIGURE 6. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

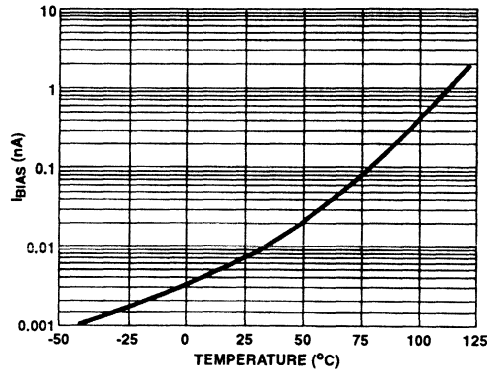


FIGURE 7. BIAS CURRENT vs TEMPERATURE

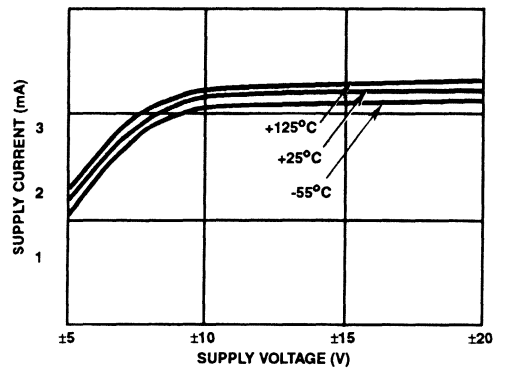


FIGURE 8. POWER SUPPLY CURRENT vs SUPPLY VOLTAGE AND TEMPERATURE

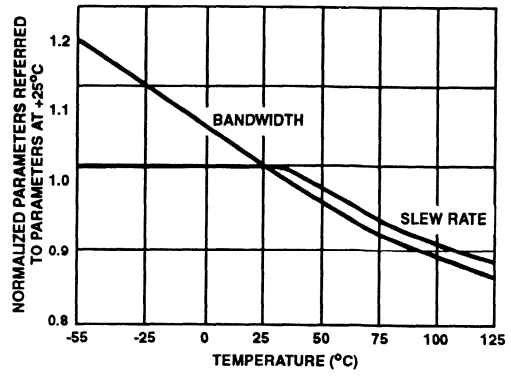


FIGURE 9. NORMALIZED AC PARAMETERS vs TEMPERATURE

Typical Performance Curves (Continued)

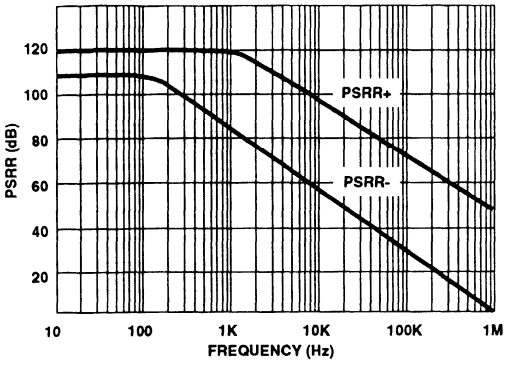


FIGURE 10. POWER SUPPLY REJECTION RATIO vs FREQUENCY

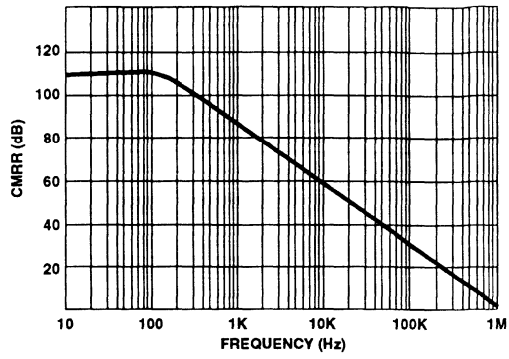


FIGURE 11. COMMON MODE REJECTION RATIO vs FREQUENCY

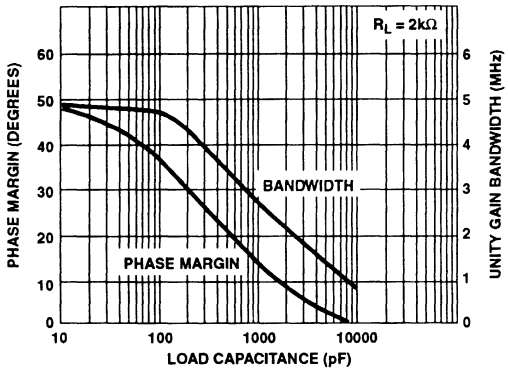


FIGURE 12. SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE

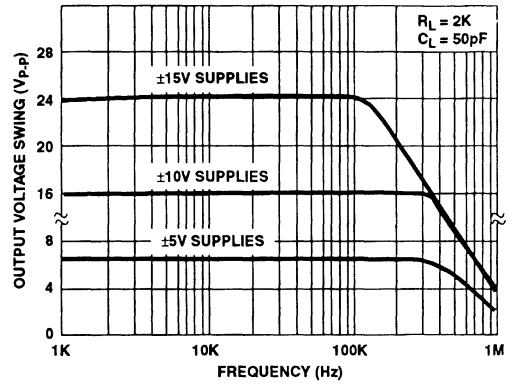


FIGURE 13. OUTPUT VOLTAGE SWING vs FREQUENCY AND SUPPLY VOLTAGE

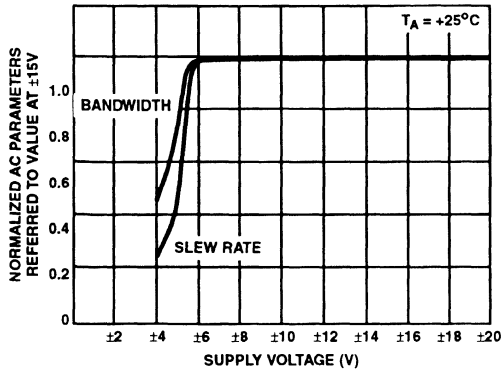


FIGURE 14. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

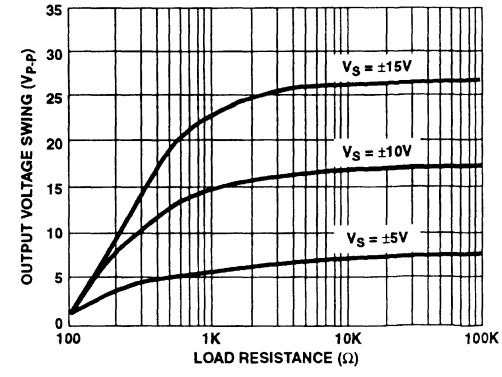


FIGURE 15. MAXIMUM OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

Typical Performance Curves (Continued)

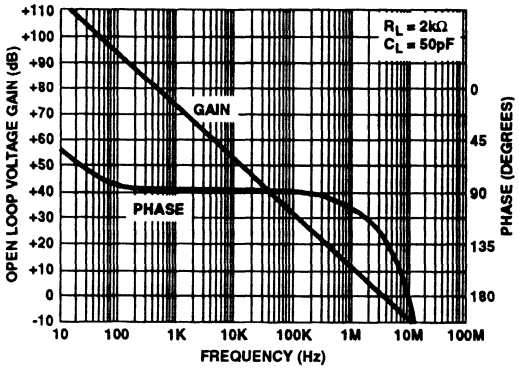


FIGURE 16. OPEN LOOP FREQUENCY RESPONSE

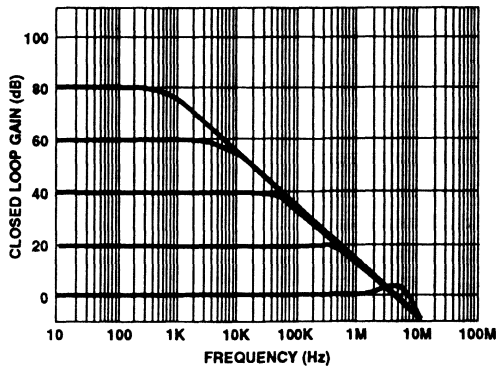


FIGURE 17. CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS

HARRIS SEMICONDUCTOR

HA-5177

Ultra-Low Offset Voltage Operational Amplifier

March 1993

Features

- Low Offset Voltage 20μV
- Low Offset Voltage Drift ..... 0.2μV/°C
- High Voltage Gain 150dB
- High CMRR 140dB
- High PSRR 135dB
- Low Noise ..... 9.0nV/√Hz
- Low Power Consumption ..... 51mW Max.

Applications

- High Gain Instrumentation Amplifiers
- Precision Control Systems
- Precision Integrators
- High Resolution Data Converters
- Precision Threshold Detectors
- Low Level Transducer Amplifiers

Description

The HA-5177 is a monolithic, all bipolar, precision operational amplifier, utilizing Harris dielectric isolation and advance processing techniques. This design features a combination of precision input characteristics, wide bandwidth (2MHz) and high speed (0.8V/μs).

The HA-5177 uses advanced matching techniques and laser trimming to produce low offset voltage (20μV) and low offset voltage drift (0.2μV/°C). This design also features low voltage noise (9.0nV/√Hz), low current noise (1.2pA/√Hz), nanoamp input currents, and 120dB minimum gain.

These outstanding features along with high CMRR (140dB) and high PSRR (135dB) make this unity gain stable amplifier ideal for high resolution data acquisition systems, precision integrators, and low level transducer amplifiers.

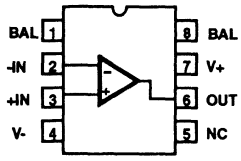
The HA-5177 can be used as a direct replacement for the OP05, OP07, and OP77 while offering higher bandwidth and slew rate. See the HA-5177/883 data sheet for military grade parts and LCC package.

Ordering Information

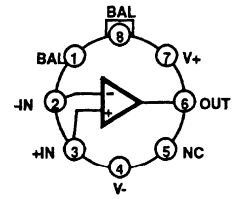
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-5177-2	-55°C to +125°C	8 Pin CAN
HA2-5177-5	0°C to +75°C	8 Pin CAN
HA3-5177-5	0°C to +75°C	8 Lead Plastic DIP
HA7-5177-2	-55°C to +125°C	8 Lead Ceramic DIP
HA7-5177-5	0°C to +75°C	8 Lead Ceramic DIP
HA9P5177-5	0°C to +75°C	8 Lead SOIC

Pinouts

HA-5177
(PDIP, CDIP, SOIC)
TOP VIEW



HA-5177
(TO-99 METAL CAN)
TOP VIEW



File Number 2913.1

Absolute Maximum Ratings (Note 1)

Supply Voltage Between V+ and V- Terminals 44V
Differential Input Voltage 7V
Output Current . . . . . Short Circuit Protected
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Operating Temperature Range
HA-5177-2 . . . . . $-55°C \le T_A \le +125°C$
HA-5177-5 . . . . . $0°C \le T_A \le +75°C$
Storage Temperature Range . . . . . $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified

PARAMETER	TEMP	HA-5177 MIN	HA-5177 TYP	HA-5177 MAX	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	+25°C	-	20	60	µV
	Full	-	40	100	µV
Average Offset Voltage Drift	Full	-	0.2	0.6	µV/°C
Bias Current	+25°C	-	1.2	6	nA
	Full	-	2.4	8	nA
Bias Current Average Drift	Full	-	15	35	pA/°C
Offset Current	+25°C	-	0.6	6	nA
	Full	-	1.0	8	nA
Offset Current Average Drift	Full	-	1.5	50	pA/°C
Common Mode Range	Full	±12	-	-	V
Differential Input Resistance	+25°C	-	47	-	MΩ
Input Noise Voltage 0.1Hz to 10Hz	+25°C	-	0.35	0.6	μV_{P-P}
Input Noise Voltage Density					
f_O = 10Hz	+25°C	-	13	18	$nV/\sqrt{Hz}$
f_O = 100Hz	+25°C	-	10	13	$nV/\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	9	11	$nV/\sqrt{Hz}$
Input Noise Current 0.1Hz to 10Hz	+25°C	-	14	45	pA_{P-P}
Input Noise Current Density					
f_O = 10Hz	+25°C	-	7.1	10	$pA/\sqrt{Hz}$
f_O = 100Hz	+25°C	-	3.3	5	$pA/\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	1.2	2	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Note 2)	+25°C	126	150	-	dB
	Full	120	140	-	dB
Common Mode Rejection Ratio (Note 3)	Full	110	140	-	dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	0.6	2	-	MHz

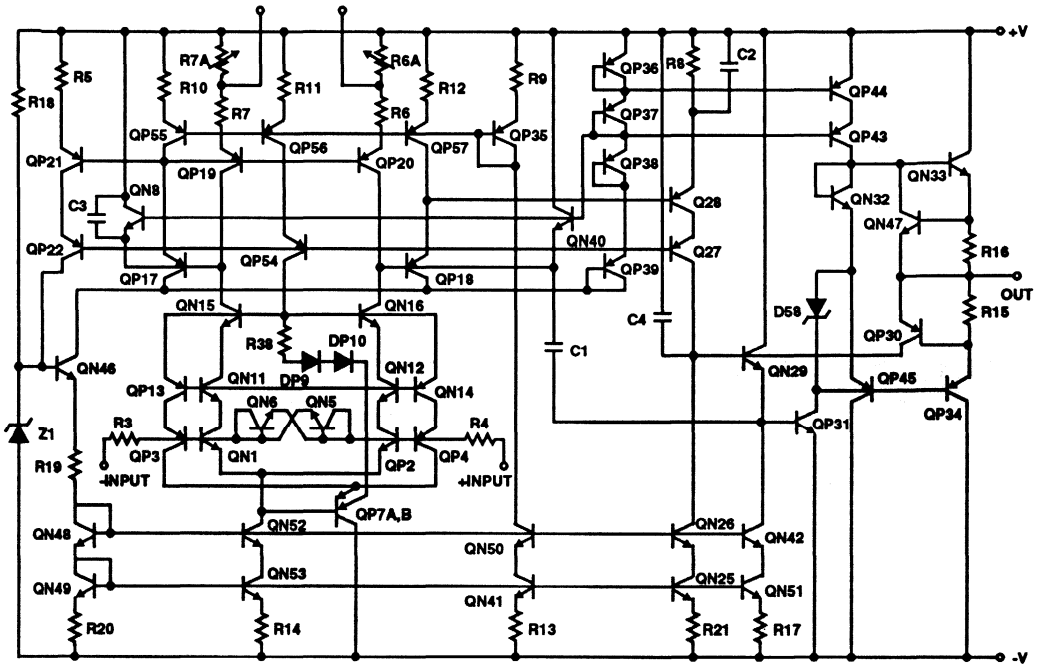
Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	HA-5177			UNITS
		MIN	TYP	MAX	
OUTPUT CHARACTERISTICS					
Output Voltage Swing					
R_L = 600Ω	+25°C	±10	±12.5	-	V
R_L = 2kΩ	+25°C	±12	±13	-	V
R_L = 2kΩ	Full	±12	±12.5	-	V
Full Power Bandwidth (Note 5)	+25°C	8	10	-	kHz
Output Current (Note 6)	+25°C	15	20	-	mA
Output Resistance	+25°C	-	60	-	Ω
TRANSIENT RESPONSE					
Rise Time (Note 10)	+25°C	-	310	420	ns
Slew Rate (Note 11)	+25°C	0.5	0.8	-	V/µs
Settling Time (Notes 7, 8)	+25°C	-	14	-	µs
Overshoot (Note 10)	+25°C	-	10	40	%
POWER SUPPLY CHARACTERISTICS					
Supply Current	Full	-	1.2	1.7	mA
Power Supply Rejection Ratio (Note 9)	Full	110	135	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, R_L = 2kΩ.
3. ΔV_{CM} = ±10V D.C.
4. R_L = 2kΩ.
5. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$, V_{PEAK} = 10V
6. V_{OUT} = ±10V.
7. Refer to test circuits section of the data sheet.
8. Settling time is measured to 0.1% of final value for a 10V output step and A_V = +1.
9. ΔV_{SUPPLY} = ±10V D.C. to ±20V D.C.
10. A_V = 1, R_L = 2kΩ, V_{OUT} = ±200mV.
11. A_V = 1, R_L = 2kΩ, V_{OUT} = 0 to ±3V.

Schematic Diagram



Die Characteristics

Transistor Count 71
Die Dimensions ..... 102 x 71.7 x 19 mils
(2590 x 1820 x 485µm)

Substrate Potential* ..... V-
Process ..... High Frequency Bipolar DI
Passivation ..... Silox

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic Mini-DIP	113	34
TO-99 Metal Can	124	38
Plastic Mini DIP	92	30
SOIC	157	42

* The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Test Circuits

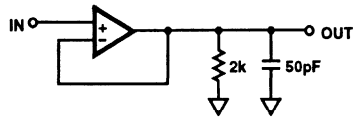


FIGURE 1. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT

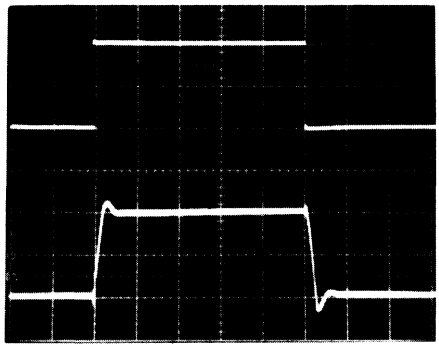


FIGURE 2. SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: 100mV/Div.)
Horizontal Scale: (Time: 2μs/Div.)

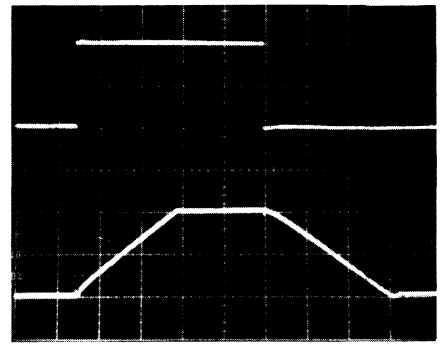
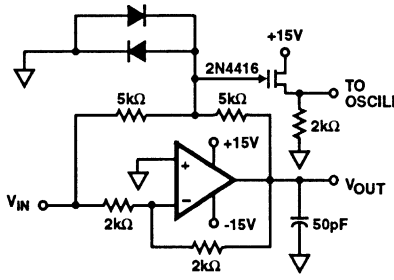


FIGURE 3. LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: 5V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



- $A_V = -1$
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 4. SETTLING TIME CIRCUIT

Typical Performance Curves $V_S = \pm 15V$, $T_A = +25°C$

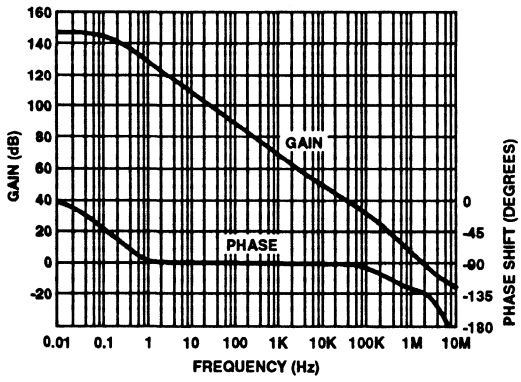


FIGURE 5. OPEN LOOP GAIN AND PHASE vs FREQUENCY

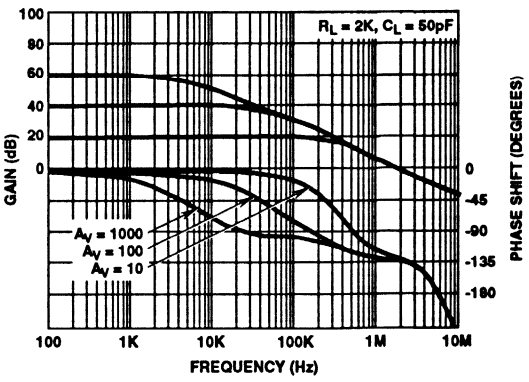


FIGURE 6. VARIOUS CLOSED LOOP GAINS vs FREQUENCY

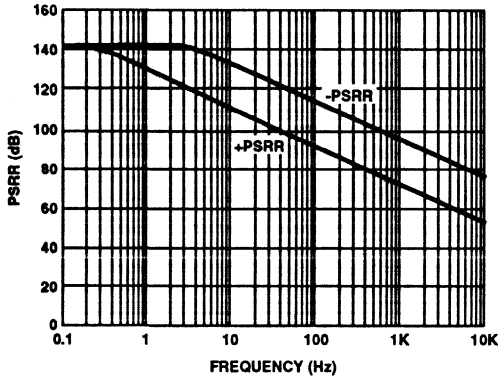


FIGURE 7. PSRR vs FREQUENCY

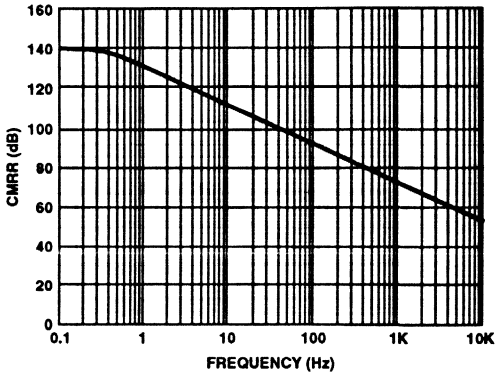


FIGURE 8. CMRR vs. FREQUENCY

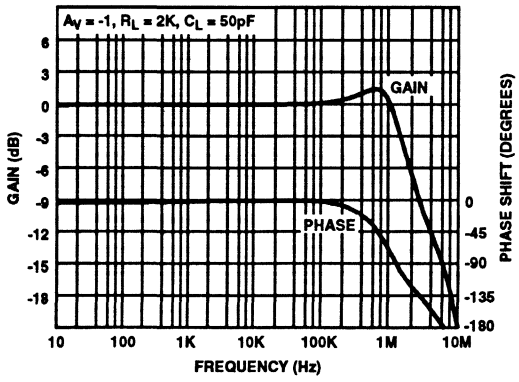


FIGURE 9. CLOSED LOOP GAIN AND PHASE vs. FREQUENCY

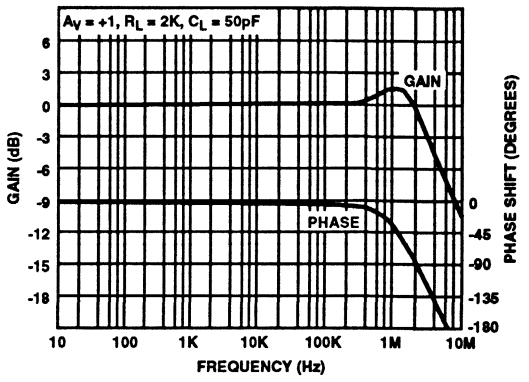


FIGURE 10. CLOSED LOOP GAIN AND PHASE vs. FREQUENCY

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$ (Continued)

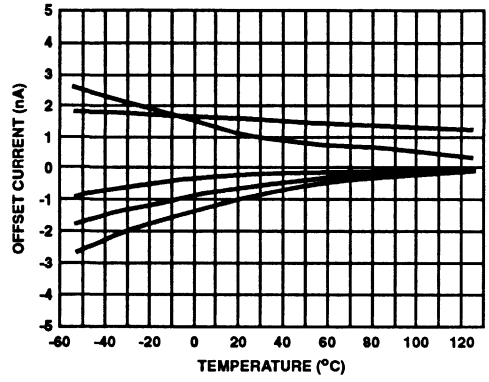


FIGURE 11. OFFSET CURRENT vs TEMPERATURE
Five Representative Units

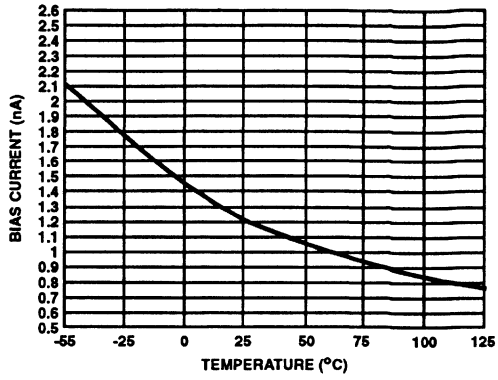


FIGURE 12. BIAS CURRENT vs TEMPERATURE

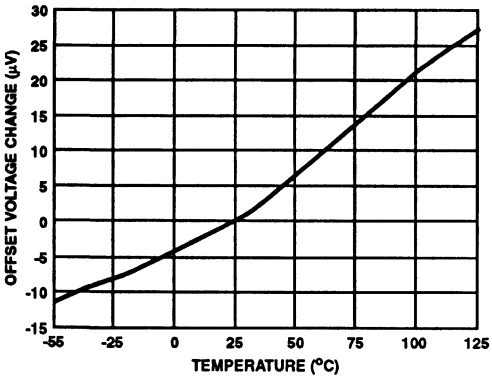


FIGURE 13. OFFSET VOLTAGE vs TEMPERATURE

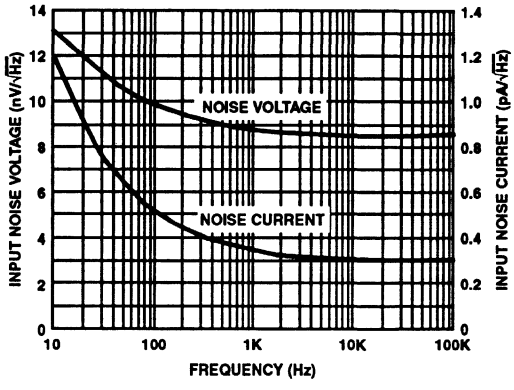


FIGURE 14. INPUT NOISE vs FREQUENCY

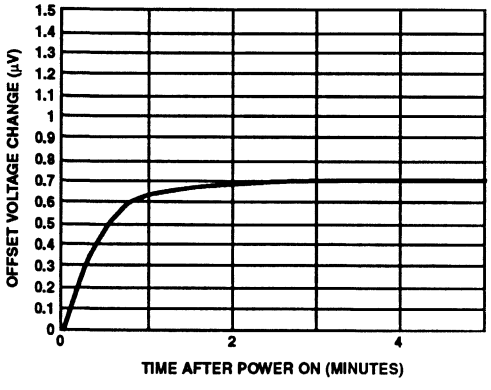


FIGURE 15. OFFSET VOLTAGE WARM-UP DRIFT

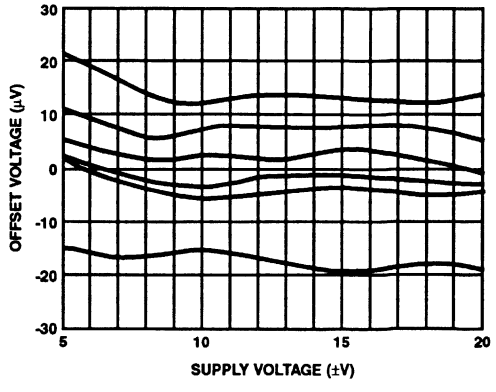


FIGURE 16. OFFSET VOLTAGE vs SUPPLY VOLTAGE
Six Representative Units

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$ (Continued)

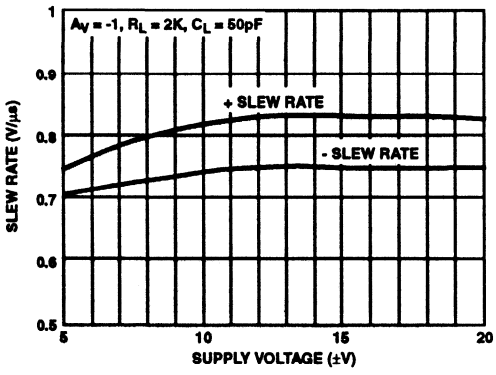


FIGURE 17. SLEW RATE vs. SUPPLY VOLTAGE

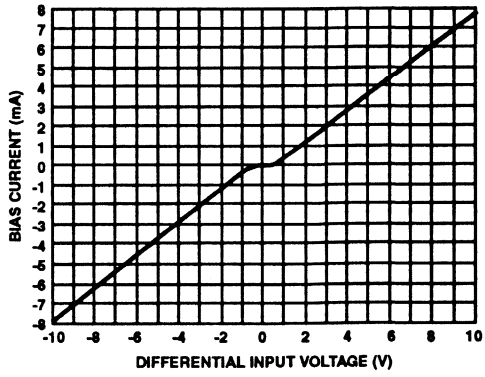


FIGURE 18. BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

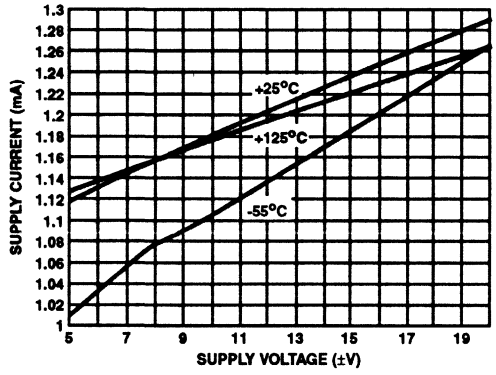


FIGURE 19. SUPPLY CURRENT vs SUPPLY VOLTAGE

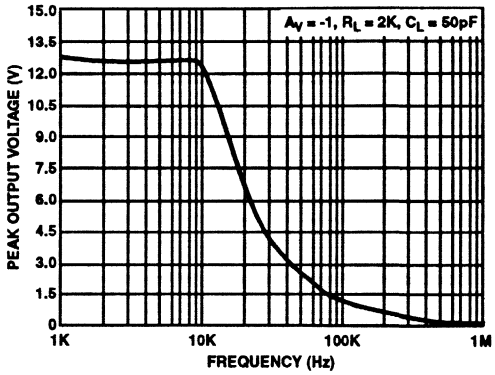


FIGURE 20. OUTPUT VOLTAGE vs FREQUENCY

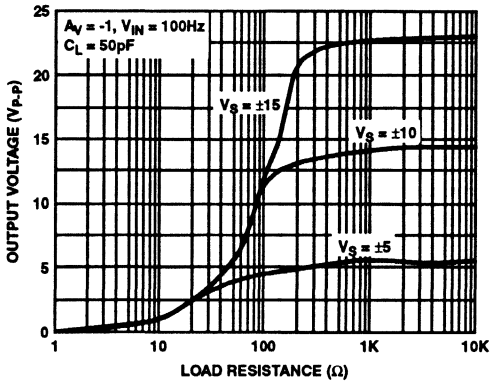


FIGURE 21. OUTPUT VOLTAGE vs LOAD RESISTANCE

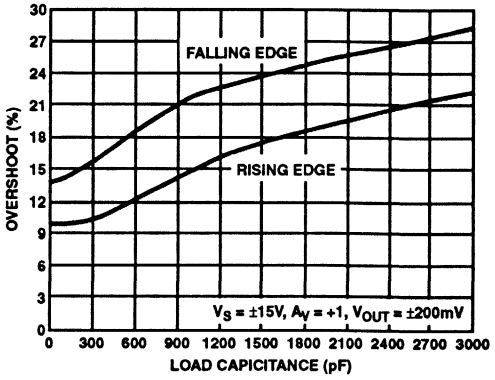


FIGURE 22. OVERSHOOT vs LOAD CAPACITANCE

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$ (Continued)

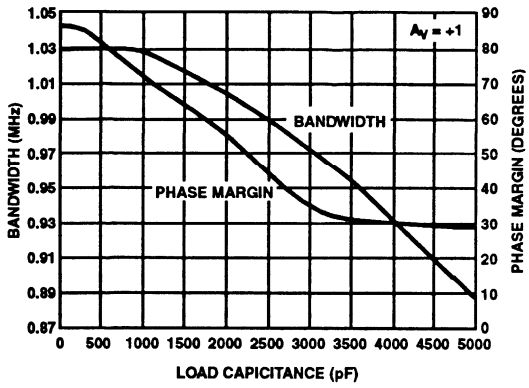


FIGURE 23. SMALL SIGNAL BANDWIDTH AND PHASE MARGIN

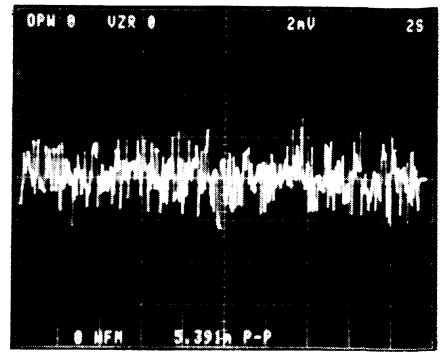


FIGURE 24. PEAK-TO-PEAK NOISE (0.1Hz TO 10Hz)
A_V = 25,000, E_N = 0.22μV_{P-P} RTI

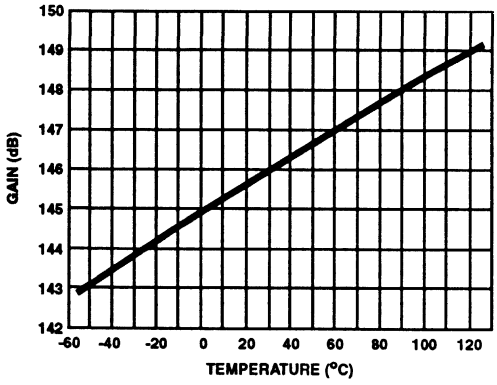


FIGURE 25. OPEN LOOP GAIN vs TEMPERATURE

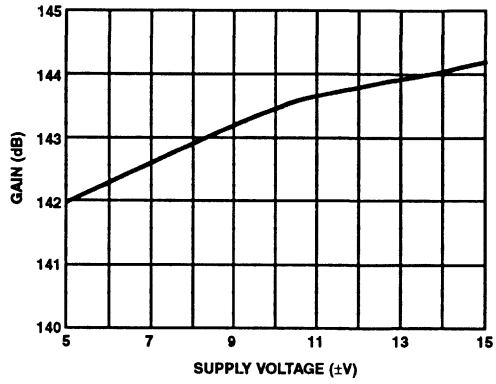


FIGURE 26. OPEN LOOP GAIN vs SUPPLY VOLTAGE

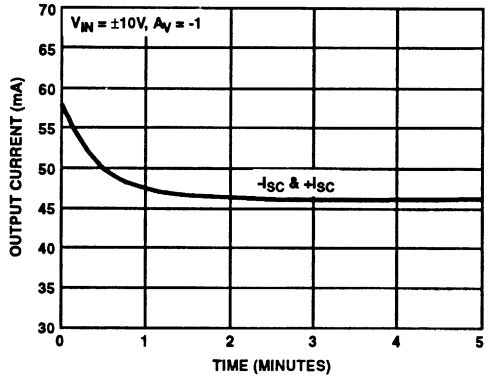


FIGURE 27. OUTPUT SHORT CIRCUIT CURRENT vs TIME

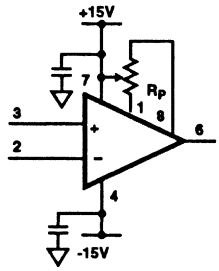
Applications Information

Operation Below 15V Supply

The HA-5177 performs well down to ±5V supplies. At ±5V supplies there is a slight degradation of slew rate and open loop gain. There is very little change in bias currents and offset voltage.

Offset Adjustment

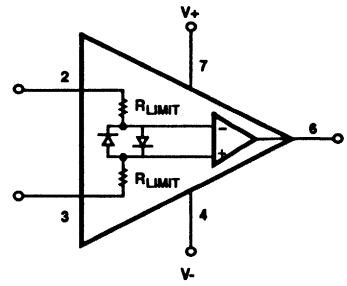
The following is the recommended V_{IO} adjust configuration:



Setting R_P = 20K will give an adjustment range of ±2.6mV.

Input Protection

The HA-5177 input stage has built in back-to-back protection diodes with series current limiting resistors.



The Bias currents will increase when a differential voltage of 0.7 volts is exceeded.

The internal current limiting resistors sufficiently limit current therefore, no external resistors are required.

Refer to the "Bias Current vs Differential Input Voltage" curve in the Typical Performance Curves section

HA-5190, HA-5195

Wideband, Fast Settling Operational Amplifiers

March 1993

Features

- Fast Settling Time (0.1%) 70ns
- Very High Slew Rate 200V/μs
- Wide Gain-Bandwidth ($A_V \geq 5$) 150MHz
- Power Bandwidth 6.5MHz
- Low Offset Voltage 3mV
- Input Noise Voltage ..... 6nV/$\sqrt{Hz}$
- Bipolar D.I. Construction

Applications

- Fast, Precise D/A Converters
- High Speed Sample-Hold Circuits
- Pulse and Video Amplifiers
- Wideband Amplifiers

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-5190-2	-55°C to +125°C	14 Lead Ceramic DIP
HA1-5195-5	0°C to +75°C	14 Lead Ceramic DIP
HA2-5190-2	-55°C to +125°C	12 Pin Can
HA2-5195-5	0°C to +75°C	12 Pin Can
HA9P5195-5	0°C to +75°C	14 Lead SOIC
HA9P5195-9	-40°C to +85°C	14 Lead SOIC

Description

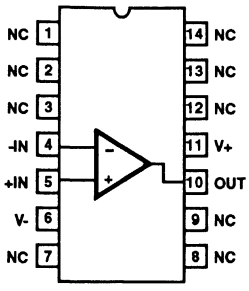
HA-5190/5195 are monolithic operational amplifiers featuring a combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with Dielectric Isolation, these devices are capable of delivering 200V/μs slew rate with a settling time of 70ns (0.1%, 5V output step). These truly differential amplifiers are designed to operate at gains ≥ 5 without the need for external compensation. Other outstanding HA-5190/5195 features are 150MHz gain bandwidth product and 6.5MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 3mV offset voltage and 6.0nV/$\sqrt{Hz}$ input voltage noise at 1kHz.

With 200V/μs slew rate and 70ns settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample/hold circuits. The 5190/5195 are also ideally suited for a variety of pulse and wideband video amplifiers. Please refer to Application Notes 525 and 526 for some of these application designs.

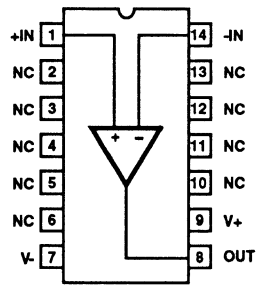
At temperatures above +75°C a heat sink is required for the HA-5190 (see Note 2 and Application Note 556). For military versions, please request the HA-5190/883 data sheet.

Pinouts

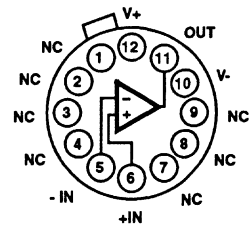
HA-5190/5195 (CDIP)
TOP VIEW



HA-5195 (SOIC)
TOP VIEW



HA-5190/5195 (TO-8 METAL CAN)
TOP VIEW



Case Tied To V-

File Number **2914.1**

Absolute Maximum Ratings

Voltage Between V+ and V- 35V
Differential Input Voltage 6V
Output Current ..... 50mA (Peak)
Junction Temperature (Note 1) ..... +175°C
Junction Temperature (Plastic Packages) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Ranges
HA-5190-2 ..... $-55°C \le T_A \le +125°C$
HA-5195-5 ..... $0°C \le T_A \le +75°C$
HA-5195-9 ..... $-40°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V_{SUPPLY} = \pm 15V$, $R_L = 200\Omega$, Unless Otherwise Specified

PARAMETERS	TEMP	HA-5190-2			HA-5195-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	3	5	-	3	6	mV
	Full	-	-	10	-	-	10	mV
Average Offset Voltage Drift	Full	-	20	-	-	20	-	µV/°C
Bias Current	+25°C	-	5	15	-	5	15	µA
	Full	-	-	20	-	-	20	µA
Offset Current	+25°C	-	1	4	-	1	4	µA
	Full	-	-	6	-	-	6	µA
Input Resistance	+25°C	-	10	-	-	10	-	kΩ
Input Capacitance	+25°C	-	1	-	-	1	-	pF
Common Mode Range	Full	±5	-	-	±5	-	-	V
Input Noise Current (f = 1kHz, Rg = 0Ω)	+25°C	-	5	-	-	5	-	$pA/\sqrt{Hz}$
Input Noise Voltage (f = 1kHz, Rg = 0Ω)	+25°C	-	6	-	-	6	-	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 2)	+25°C	15	30	-	10	30	-	kV/V
	Full	5	-	-	5	-	-	kV/V
Common Mode Rejection Ratio (Note 3)	Full	74	95	-	74	95	-	dB
Minimum Stable Gain	+25°C	5	-	-	5	-	-	V/V
Gain-Bandwidth-Product (Note 4)	+25°C	-	150	-	150	-	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 2)	Full	±5	±8	-	±5	±8	-	V
Output Current (Note 2)	+25°C	±25	±30	-	±25	±30	-	mA
Output Resistance	+25°C	-	30	-	-	30	-	Ω
Full Power Bandwidth (Notes 2, 5)	+25°C	5	6.5	-	5	6.5	-	MHz
TRANSIENT RESPONSE (Note 6)								
Rise Time	+25°C	-	13	18	-	13	18	ns
Overshoot	+25°C	-	8	-	-	8	-	%
Slew Rate	+25°C	160	200	-	160	200	-	V/µs
Settling Time (Note 6)								
5V Step to 0.1%	+25°C	-	70	-	-	70	-	ns
5V Step to 0.01%	+25°C	-	100	-	-	100	-	ns
2.5V Step to 0.1%	+25°C	-	50	-	-	50	-	ns
2.5V Step to 0.01%	+25°C	-	80	-	-	80	-	ns

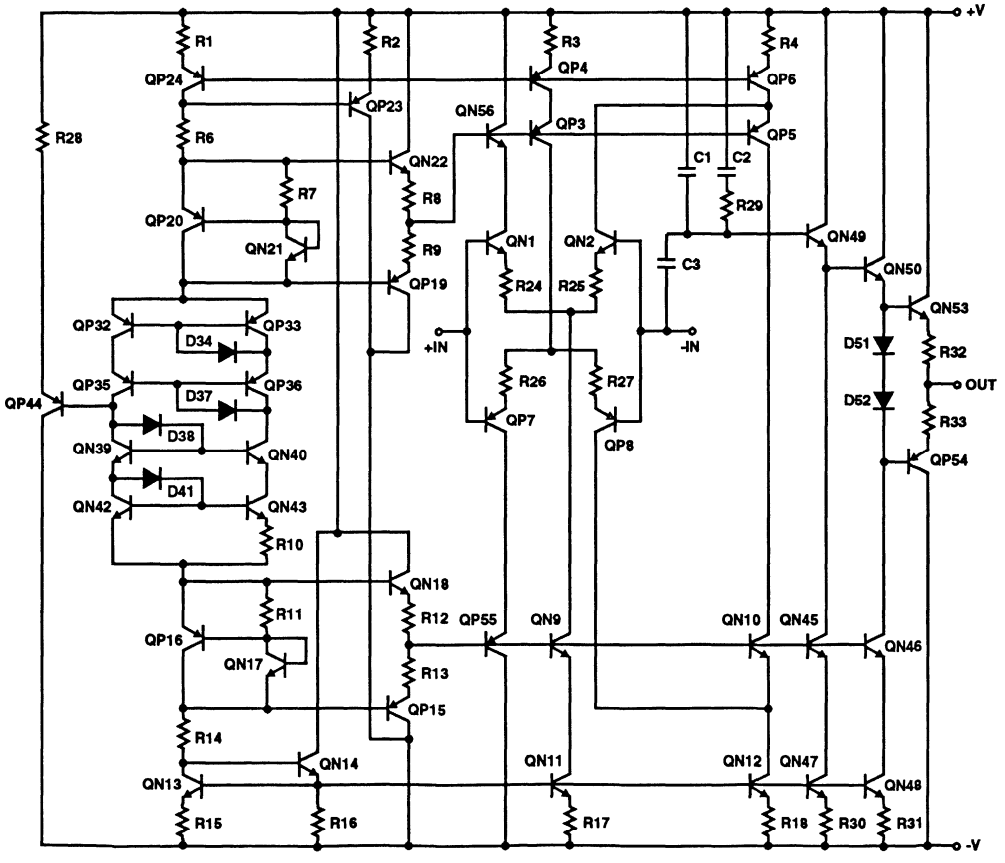
Electrical Specifications V_{SUPPLY} = ±15V, R_L = 200Ω, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEMP	HA-5190-2			HA-5195-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	19	28	-	19	28	mA
Power Supply Rejection Ratio (Note 7)	Full	70	90	-	70	90	-	dB

NOTES:

1. Recommended heat sinks: For TO-8 Metal Can, Thermalloy #2240A (θ_{SA} = 27°C/W) or #2268B (θ_{SA} = 24°C/W). For 14 lead Ceramic DIP: AAVID #5602B (θ_{SA} = 16°C/W). See Die Characteristics section for θ_{JA}/θ_{JC} values.
2. R_L = 200Ω, C_L < 10pF, V_{OUT} = ±5V.
3. ΔV_{CM} = ±5V.
4. V_{OUT} = 90mV, A_V = 10.
5. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
6. Refer to Test Circuits section of the data sheet.
7. ΔV_{SUPPLY} = ±10VDC to ±20VDC.

Schematic Diagram



Die Characteristics

Transistor Count 49
Die Dimensions . . . . . 0.087 x 0.052 x 0.019 inches (2210 x 1320 x 483 mm)
Substrate Potential (Powered Up)* . . . . . V-
Process . . . . . High Frequency Bipolar Dielectric Isolation
Passivation . . . . . Nitride

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	71	14
Metal Can	63	30
SOIC	119	36

* The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Test Circuits

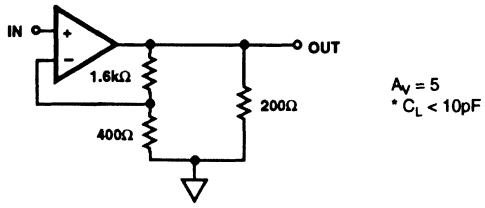
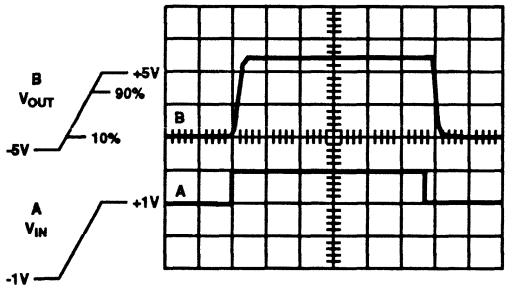
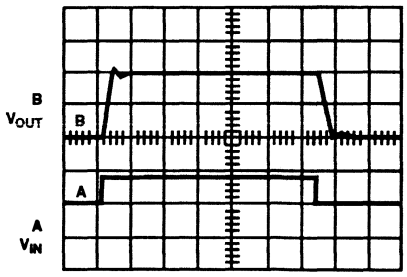


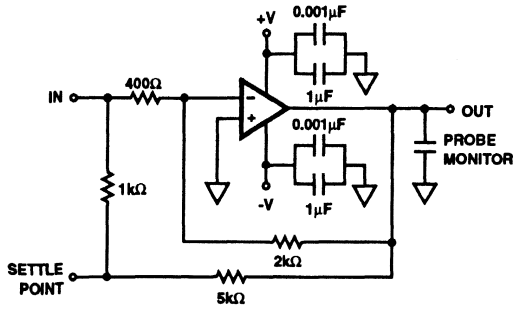
FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT*

LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: A = 2.0V/Div., B = 4.0/Div.)
Horizontal Scale: (Time: 100ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: A = 50mV/Div., B = 100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)





- A_V = -5
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- Settle Point (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Typical Performance Curves

V+ = +15V, V- = -15V, T_A = +25°C, Unless Otherwise Specified.

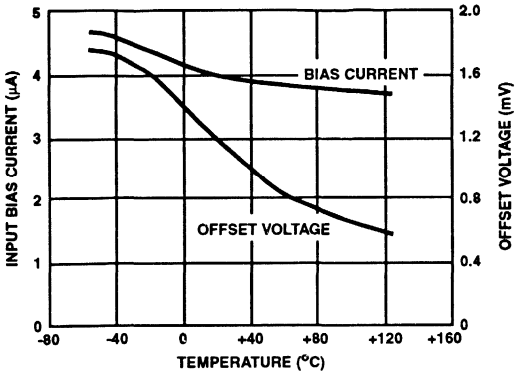


FIGURE 3. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs TEMPERATURE

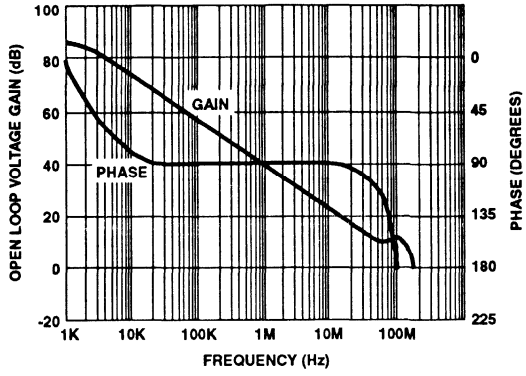


FIGURE 4. OPEN LOOP FREQUENCY RESPONSE

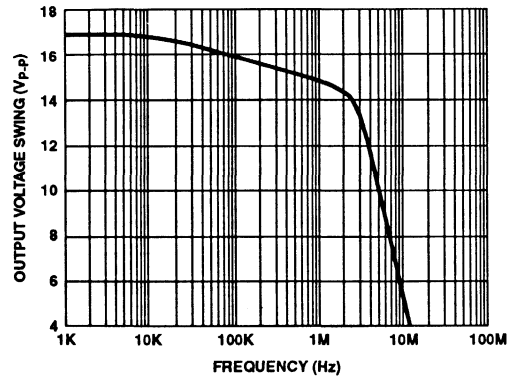


FIGURE 5. OUTPUT VOLTAGE SWING vs FREQUENCY

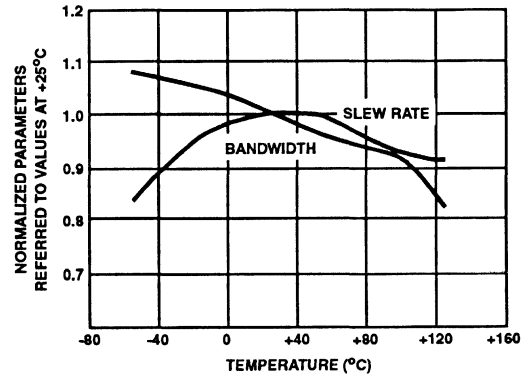


FIGURE 6. NORMALIZED AC PARAMETERS vs TEMPERATURE

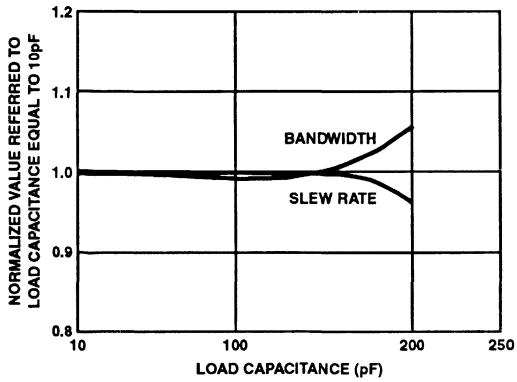


FIGURE 7. NORMALIZED AC PARAMETERS vs LOAD CAPACITANCE

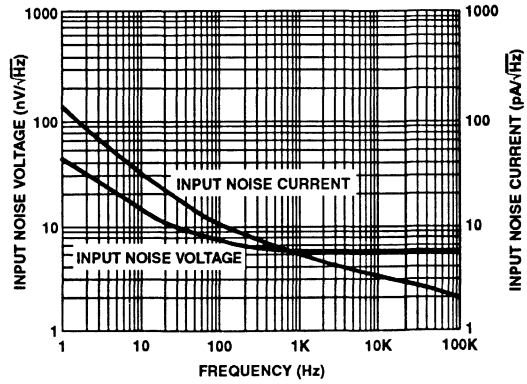


FIGURE 8. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY

Typical Performance Curves V+ = +15V, V- = -15V, T_A = +25°C, Unless Otherwise Specified. (Continued)

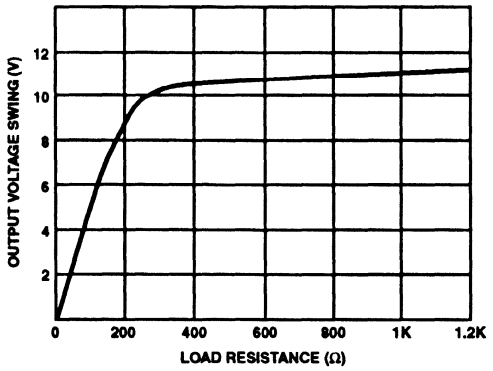


FIGURE 9. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

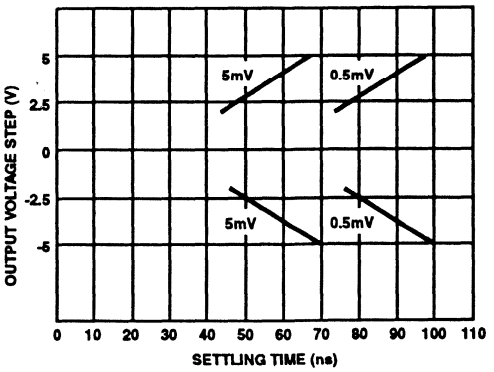


FIGURE 10. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

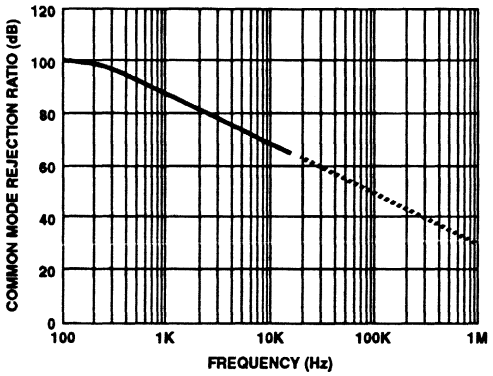


FIGURE 11. COMMON MODE REJECTION RATIO vs FREQUENCY

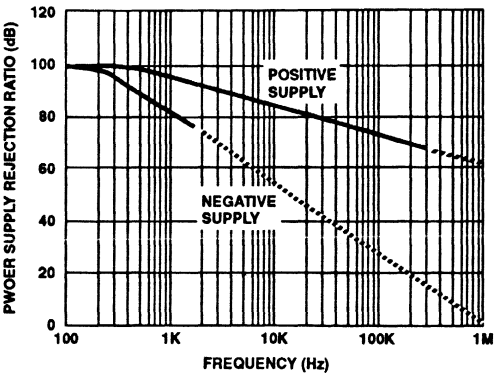


FIGURE 12. POWER SUPPLY REJECTION RATIO vs FREQUENCY

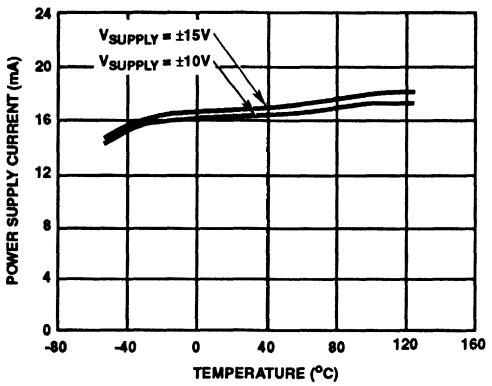
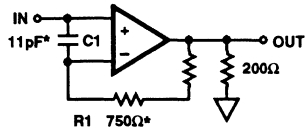


FIGURE 13. POWER SUPPLY CURRENT vs TEMPERATURE

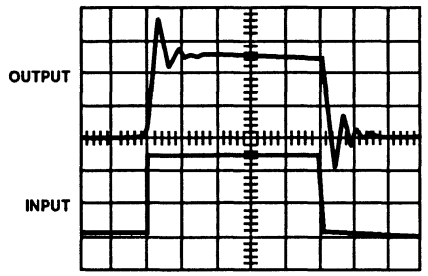
Applying the HA-5190/5195

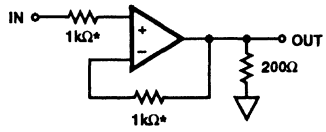
1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. STABILITY CONSIDERATIONS: HA-5190/5195 is stable at gains > 5. Gains < 5 are covered below. Feedback resistors should be of carbon composition located as near to the input terminals as possible.
3. WIRING CONSIDERATIONS: Video pulse circuits should be built on a ground plane. Minimum point to point connections directly to the amplifier terminals should be used. When ground planes cannot be used, good single point grounding techniques should be applied.
4. OUTPUT SHORT CIRCUIT: HA-5190/5195 does not have output short circuit protection. Short circuits to ground can be tolerated for approximately 10 seconds. Short circuits to either supply will result in immediate destruction of the device.
5. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads (> 100pF) a small resistor (100Ω) should be connected in series with the output and inside the feedback loop.

Typical Applications (Also see Application Notes 525 and 526)

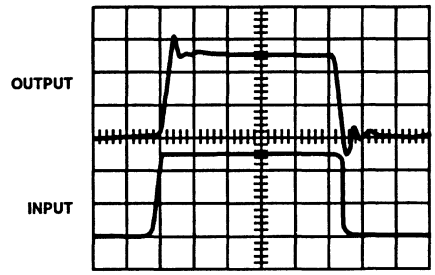


Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 100ns/Div.)



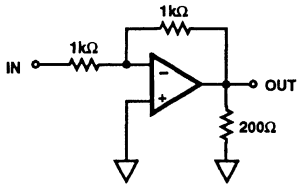


Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 100ns/Div.)



* Values were determined experimentally for optimum speed and settling time. R1 and C1 should be optimized for each particular application to ensure best overall frequency response.

FIGURE 14. SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY: NONINVERTING



Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (50ns/Div.)

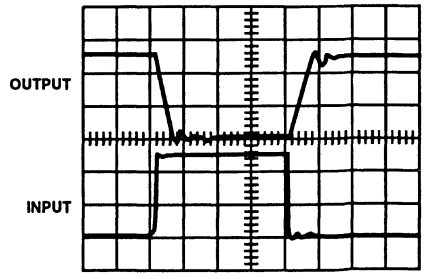


FIGURE 15. SUGGESTED COMPENSATION FOR INVERTING UNITY GAIN

Typical Applications (Also see Application Notes 525 and 526) (Continued)

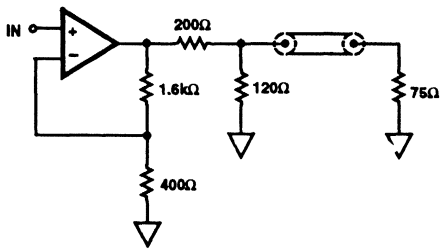


FIGURE 16. VIDEO PULSE AMPLIFIER/75Ω COAXIAL DRIVER

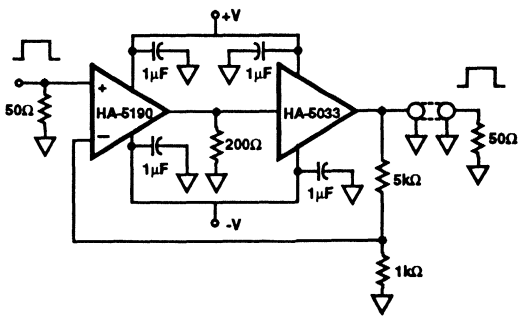


FIGURE 17. VIDEO PULSE AMPLIFIER COAXIAL LINE DRIVER

HARRIS SEMICONDUCTOR

HA-5221, HA-5222

Low Noise, Wideband Precision Operational Amplifiers

March 1993

Features

- Gain Bandwidth Product 100MHz
- Unity Gain Bandwidth 35MHz
- High Slew Rate 35V/μs
- Low Offset Voltage 0.3mV
- High Open Loop Gain 128dB
- Channel Separation at 10kHz 110dB
- Low Noise Voltage at 1kHz ..... 3.4nV/√Hz
- High Output Current 56mA
- Low Supply Current per Amplifier 8mA

Applications

- Precision Test Systems
- Active Filtering
- Small Signal Video
- Accurate Signal Processing
- RF Signal Conditioning

Description

The HA-5221/5222 are single and dual high performance dielectrically isolated, monolithic op amps, featuring precision DC characteristics while providing excellent AC characteristics. Designed for audio, video, and other demanding applications, noise (3.4nV/√Hz at 1kHz), total harmonic distortion (< 0.005%), and DC errors are kept to a minimum.

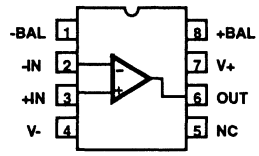
The precision performance is shown by low offset voltage (0.3mV), low bias currents (40nA), low offset currents (15nA), and high open loop gain (128dB). The combination of these excellent DC characteristics with the fast settling time (0.4μs) make the HA-5221/5222 ideally suited for precision signal conditioning.

The unique design of the HA-5221/5222 gives them outstanding AC characteristics not normally associated with precision op amps, high unity gain bandwidth (35MHz) and high slew rate (35V/μs). Other key specifications include high CMRR (95dB) and high PSRR (100dB). The combination of these specifications will allow the HA-5221/5222 to be used in RF signal conditioning as well as video amplifiers.

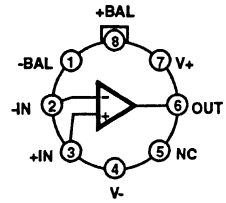
For MIL-STD-883C compliant product and Ceramic LCC packaging, consult the HA-5221/5222/883C data sheet.

Pinouts (See Ordering Information on Next Page)

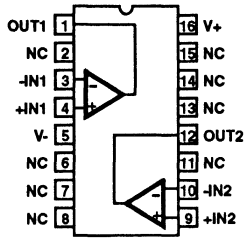
HA-5221 (PDIP, CDIP, SOIC)
TOP VIEW



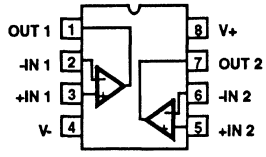
HA-5221 (TO-99 METAL CAN)
TOP VIEW



HA-5222 (PDIP, 300 mil SOIC)
TOP VIEW



HA-5222 (CDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2915.1**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-5221-5	0°C to +75°C	8 Lead CAN
HA2-5221-9	-40°C to +85°C	8 Lead CAN
HA3-5221-5	0°C to +75°C	8 Lead Plastic DIP
HA7-5221-5	0°C to +75°C	8 Lead Ceramic DIP
HA7-5221-9	-40°C to +85°C	8 Lead Ceramic DIP
HA9P5221-5	0°C to +75°C	8 Lead SOIC

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA3-5222-5	0°C to +75°C	16 Lead Plastic DIP
HA3-5222-9	-40°C to +85°C	16 Lead Plastic DIP
HA7-5222-5	0°C to +75°C	8 Lead Ceramic DIP
HA7-5222-9	-40°C to +85°C	8 Lead Ceramic DIP
HA9P5222-5	0°C to +75°C	16 Lead Wide Body SOIC
HA9P5222-9	-40°C to +85°C	16 Lead Wide Body SOIC

Absolute Maximum Ratings (Note 1)

Supply Voltage Between V+ and V- Terminals 35V
Differential Input Voltage (Note 14) 5V
Output Current Short Circuit Duration ..... Indefinite
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-5221/5222-9 ..... $-40°C \leq T_A \leq +85°C$
HA-5221/5222-5 ..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = 15V, V- = -15V, Unless Otherwise Specified

PARAMETER	TEMP	HA-5221-9 & HA-5222-9			HA-5221-5 & HA-5222-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Offset Voltage	+25°C	-	0.30	0.75	-	0.30	0.75	mV
	Full	-	0.35	1.5	-	0.35	1.5	mV
Average Offset Voltage Drift	Full	-	0.5	-	-	0.5	-	µV/°C
Input Bias Current	+25°C	-	40	80	-	40	100	nA
	Full	-	70	200	-	70	200	nA
Input Offset Current	+25°C	-	15	50	-	15	100	nA
	Full	-	30	150	-	30	150	nA
Input Offset Voltage Match	+25°C	-	400	750	-	400	750	µV
	Full	-	-	1500	-	-	1500	µV
Common Mode Range	+25°C	±12	-	-	±12	-	-	V
Differential Input Resistance	+25°C	-	70	-	-	70	-	kΩ
Input Noise Voltage f_O = 0.1Hz to 10Hz	+25°C	-	0.25	-	-	0.25	-	µVp-p
Input Noise Voltage f_O = 10Hz	+25°C	-	6.2	10	-	6.2	10	$nV/\sqrt{Hz}$
Density (Note 2, 15) f_O = 100Hz	+25°C	-	3.6	6	-	3.6	6	$nV/\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	3.4	4.0	-	3.4	4.0	$nV/\sqrt{Hz}$
Input Noise Current f_O = 10Hz	+25°C	-	4.7	8.0	-	4.7	8.0	$pA/\sqrt{Hz}$
Density (Note 2, 15) f_O = 100Hz	+25°C	-	1.8	2.8	-	1.8	2.8	$pA/\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	0.97	1.8	-	0.97	1.8	$pA/\sqrt{Hz}$
THD+N (Note 3)	+25°C	-	<0.005	-	-	<0.005	-	%
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	106	128	-	106	128	-	dB
	Full	100	120	-	100	120	-	dB
Common Mode Rejection Ratio (Note 5)	Full	86	95	-	86	95	-	dB
Unity Gain Bandwidth (-3dB)	+25°C	-	35	-	-	35	-	MHz

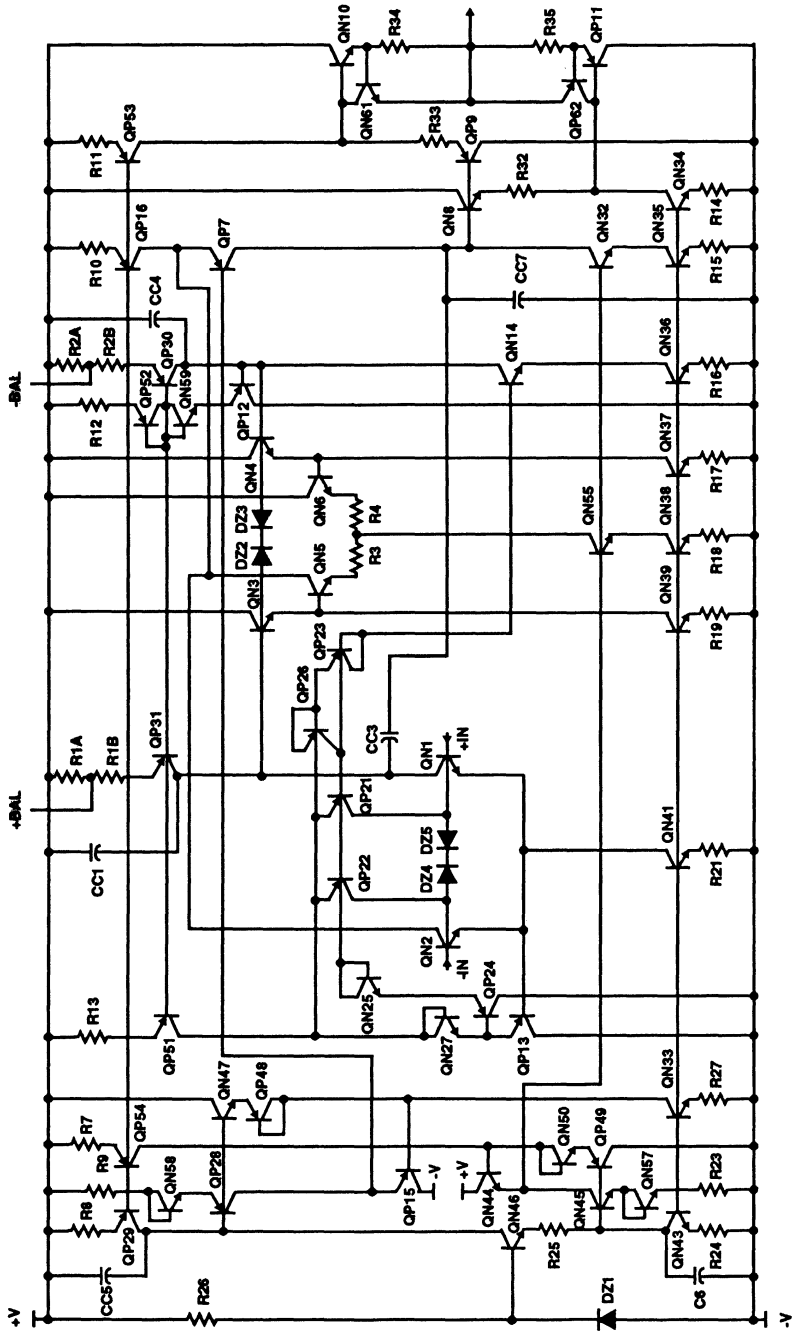
Electrical Specifications V+ = 15V, V- = -15V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	HA-5221-9 & HA-5222-9			HA-5221-5 & HA-5222-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Gain Bandwidth Product (1kHz to 400kHz)	+25°C	-	100	-	-	100	-	MHz
Minimum Stable Gain	Full	1	-	-	1	-	-	V/V
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
R_L = 333Ω	Full	±10	-	-	±10	-	-	V
R_L = 1kΩ	+25°C	±12	±12.5	-	±12	±12.5	-	V
R_L = 1kΩ	Full	±11.5	±12.1	-	±11.5	±12.1	-	V
Output Current (Note 6)	Full	±30	±56	-	±30	±56	-	mA
Output Resistance	+25°C	-	10	-	-	10	-	Ω
Full Power Bandwidth (Note 7)	+25°C	398	557	-	398	557	-	kHz
Channel Separation (Note 8)	+25°C	-	110	-	-	110	-	dB
TRANSIENT RESPONSE (Note 13)								
Slew Rate (Note 9, 15)	Full	25	35	-	25	35	-	V/µs
Rise Time (Note 10, 15)	Full	-	13	20	-	13	20	ns
Overshoot (Note 10, 15)	Full	-	28	50	-	28	50	%
Settling Time (Note 11)								
0.1%	+25°C	-	0.4	-	-	0.4	-	µs
0.01%	+25°C	-	1.5	-	-	1.5	-	µs
POWER SUPPLY								
PSRR (Note 12)	Full	86	100	-	86	100	-	dB
Supply Current	Full	-	8	11	-	8	11	mA/Op Amp

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Refer to typical performance curve in data sheet.
3. A_{VCL} = 10, f_O = 1kHz, V_O = 5Vrms, R_L = 600Ω, 10Hz to 100kHz, Minimum resolution of test equipment is 0.005%.
4. V_{OUT} = 0 to ±10V, R_L = 1K, C_L = 50pF.
5. V_{CM} = ±10V.
6. V_{OUT} = ±10V.
7. Full Power Bandwidth is calculated by: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{Peak}}$, V_{Peak} = 10V
8. HA-5222 only, f_O = 10kHz, R_L = 1K, C_L = 50pF.
9. V_{OUT} = ±2.5V, R_L = 1K, C_L = 50pF.
10. V_{OUT} = ±100mV, R_L = 1K, C_L = 50pF.
11. Settling time is specified for a 10V step and A_V = -1.
12. V_S = ±10V to ±20V.
13. See Test Circuits.
14. Input is protected by back-to-back zener diodes. See applications section.
15. Guaranteed by characterization.

Schematic Diagram



Die Characteristics

Transistor Count
- HA-5221 64
- HA-5222 128

Die Dimensions
- HA-5221 . . . . . 94 x 72 x 19mils (2400 x 1840 x 480µm)
- HA-5222 . . . . . 185 x 78 x 19mils (4690 x 1980 x 480µm)

Substrate Potential* . . . . . V-
Process . . . . . High Frequency, Bipolar, DI
Passivation . . . . . Silox

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
HA2-5221 (Can)	111	35
HA7-5221 (Ceramic DIP)	114	34
HA7-5222 (Ceramic DIP)	112	32
HA3-5221 (Plastic DIP)	92	30
HA9P5221 (SOIC)	157	42
HA3-5222 (Plastic DIP)	85	23
HA9P5222 (SOIC)	95	26

* The substrate may be left floating (Insulating Die Mount) or it may be on a conductor at V- potential.

Test Circuits

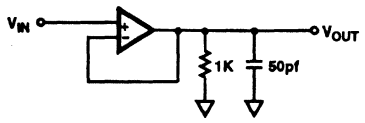


FIGURE 1. TRANSIENT RESPONSE TEST CIRCUIT

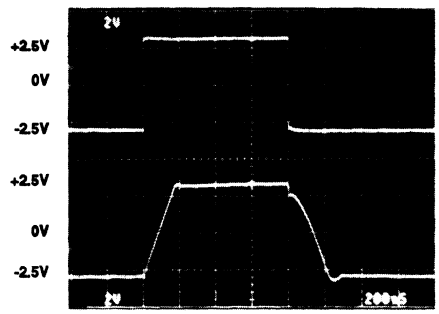


FIGURE 2. LARGE SIGNAL RESPONSE
V_{OUT} = ±2.5V
Vertical Scale: 2V/div., Horizontal Scale: 200ns/div.

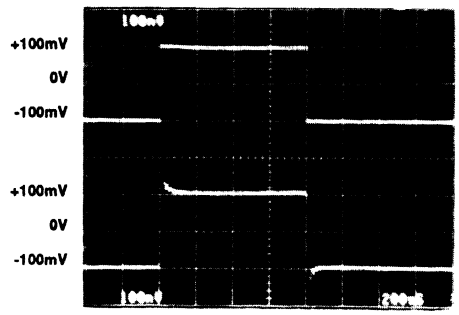
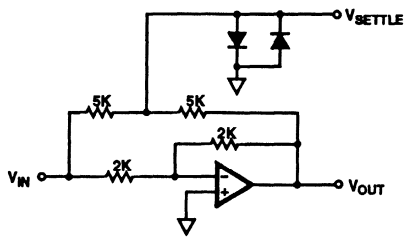


FIGURE 3. SMALL SIGNAL RESPONSE
V_{OUT} = ±100mV
Vertical Scale: 100mV/div., Horizontal Scale: 200ns/div.



- AV = -1
- Feedback and summing resistors must be matched (0.1%).
- HP5082-2810 clipping diodes recommended.
- Tektronix P6201 FET probe used at settling point.

FIGURE 4. SETTLING TIME TEST CIRCUIT

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$

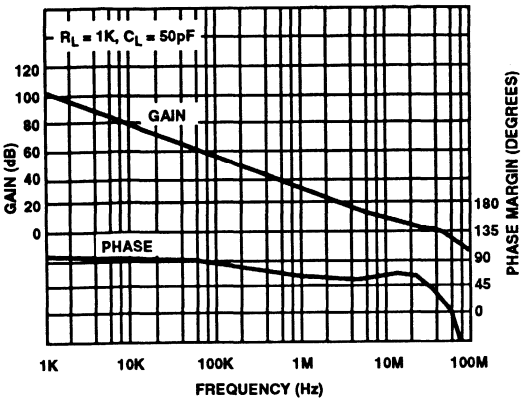


FIGURE 5. OPEN LOOP GAIN AND PHASE vs FREQUENCY

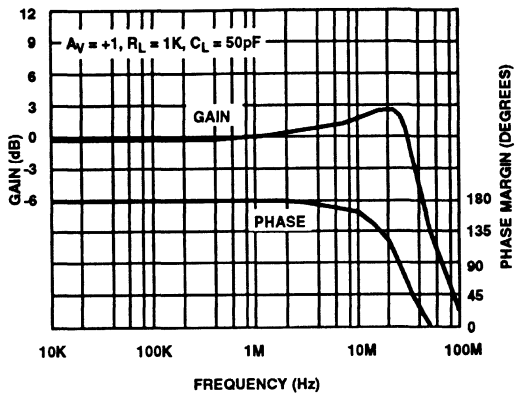


FIGURE 6. CLOSED LOOP GAIN vs FREQUENCY

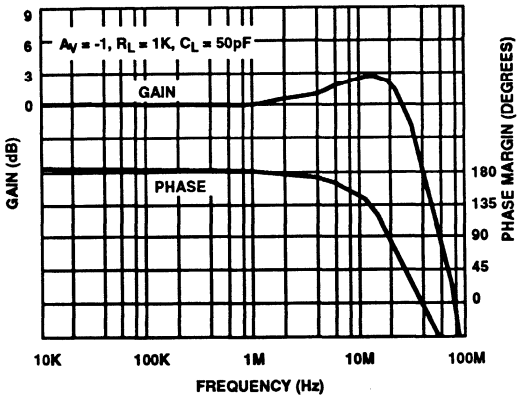


FIGURE 7. CLOSED LOOP GAIN vs FREQUENCY

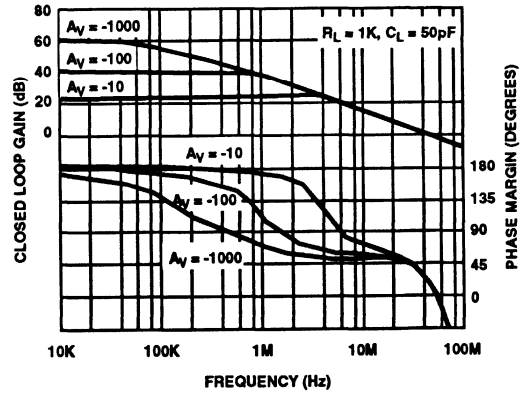


FIGURE 8. VARIOUS CLOSED LOOP GAINS vs FREQUENCY

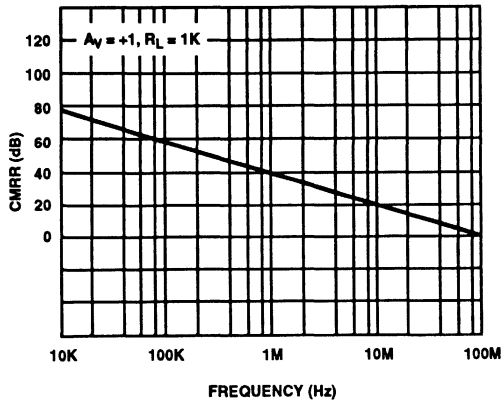


FIGURE 9. CMRR vs FREQUENCY

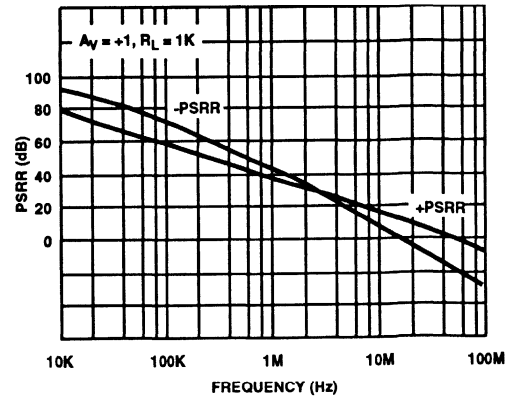


FIGURE 10. PSRR vs FREQUENCY

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$ (Continued)

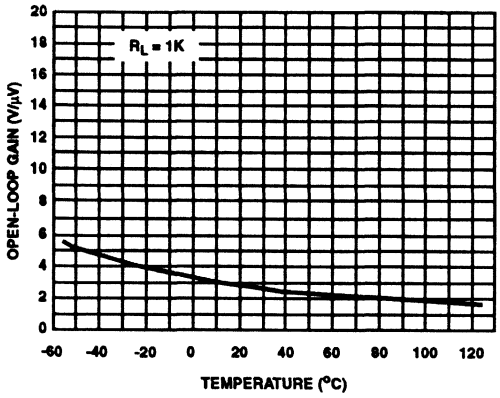


FIGURE 11. OPEN LOOP GAIN vs TEMPERATURE

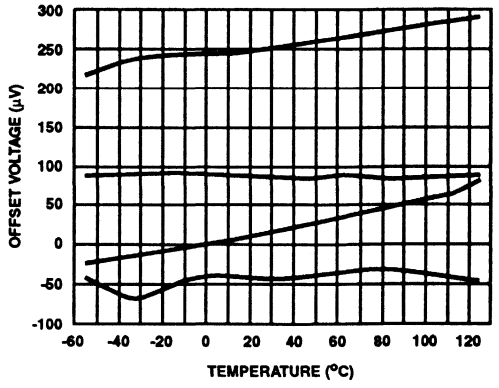


FIGURE 12. OFFSET VOLTAGE vs TEMPERATURE
4 Representative Units

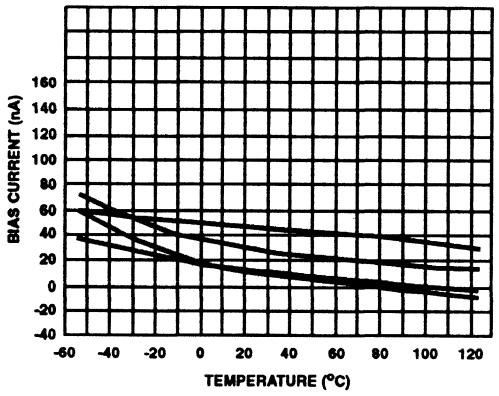


FIGURE 13. BIAS CURRENT vs TEMPERATURE
4 Representative Units

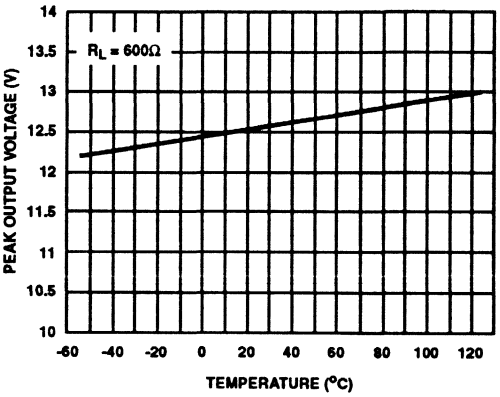


FIGURE 14. OUTPUT VOLTAGE SWING vs TEMPERATURE

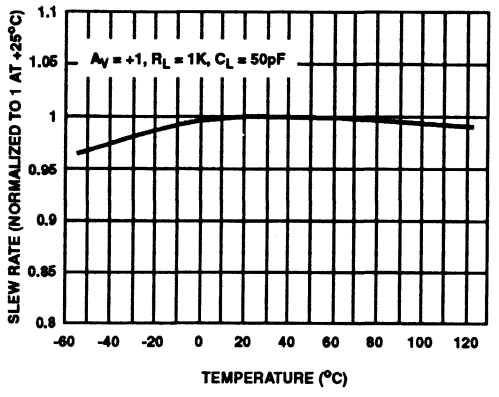


FIGURE 15. SLEW RATE vs TEMPERATURE

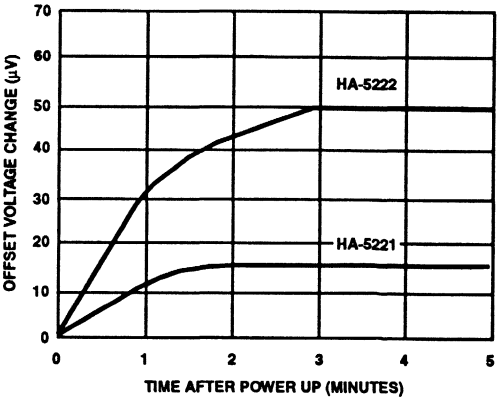


FIGURE 16. OFFSET VOLTAGE WARM-UP DRIFT
Ceramic DIP Packages

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$ (Continued)

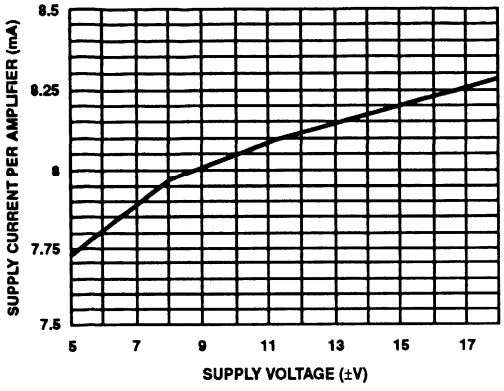


FIGURE 17. SUPPLY CURRENT vs SUPPLY VOLTAGE

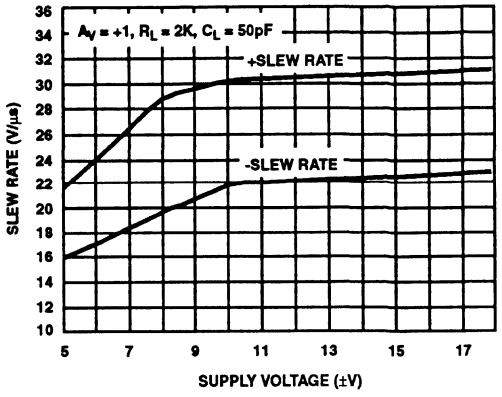


FIGURE 18. SLEW RATE vs SUPPLY VOLTAGE

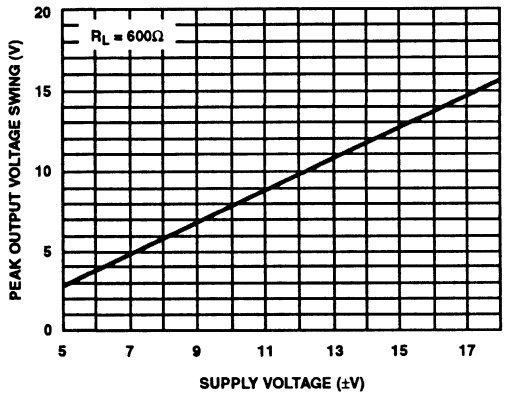


FIGURE 19. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

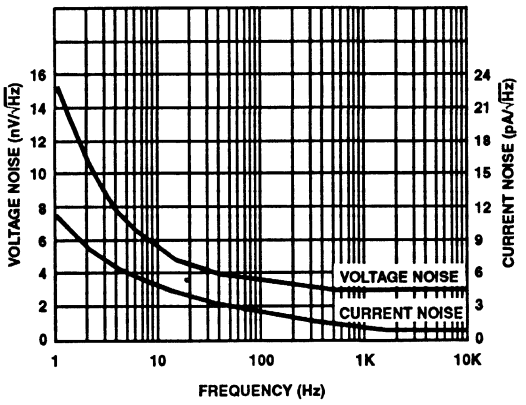


FIGURE 20. NOISE CHARACTERISTICS

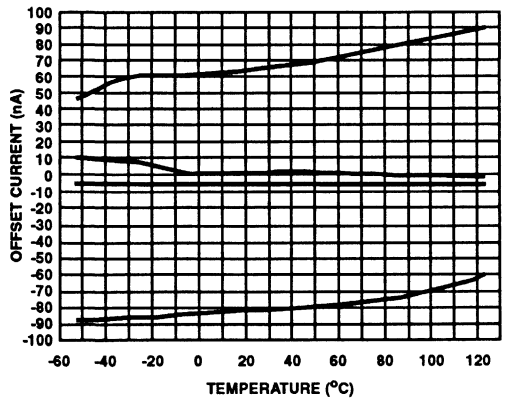


FIGURE 21. OFFSET CURRENT vs TEMPERATURE
4 Representative Units

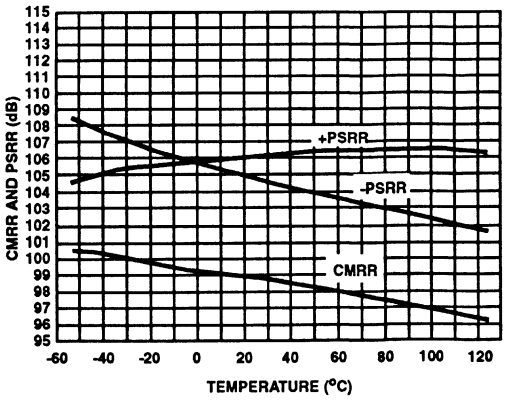


FIGURE 22. CMRR AND PSRR vs TEMPERATURE

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$ (Continued)

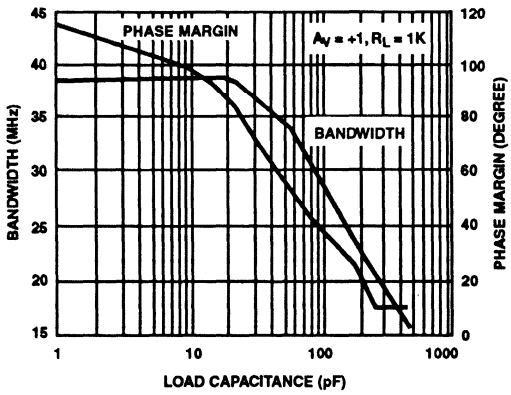


FIGURE 23. BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE

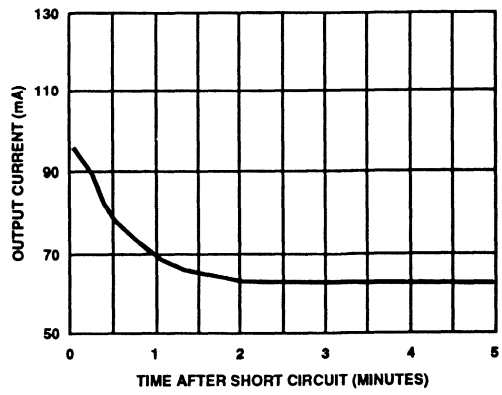


FIGURE 24. SHORT CIRCUIT OUTPUT CURRENT vs TIME

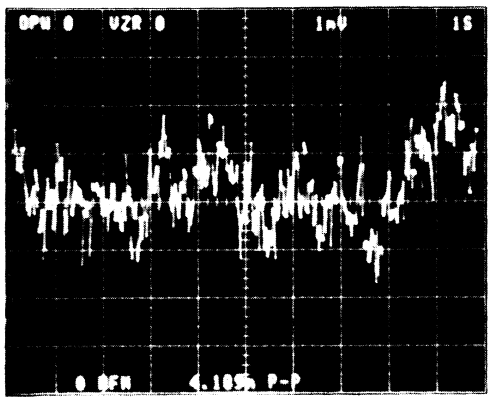


FIGURE 25. 0.1Hz TO 10Hz NOISE
Vertical Scale: 1mV/div Horizontal Scale: 1 S/div
A_V = +25,000 (E_N = 0.168μV_{P-P} RTI)

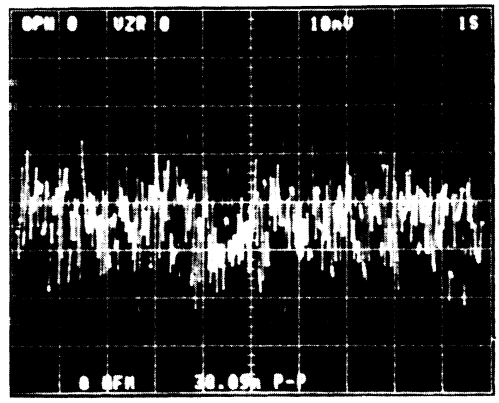


FIGURE 26. 0.1Hz TO 1MHz
Vertical Scale: 10mV/div Horizontal Scale: 1 S/div
A_V = +25,000 (E_N = 1.5μV_{P-P} RTI)

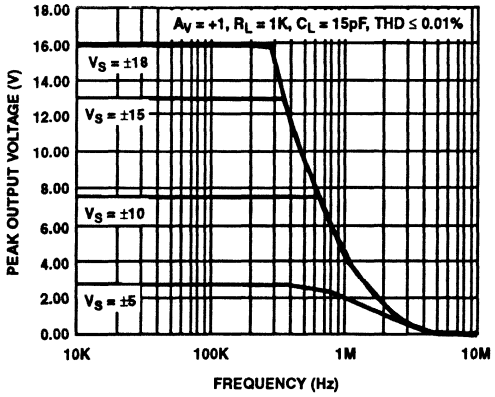


FIGURE 27. OUTPUT VOLTAGE SWING vs FREQUENCY

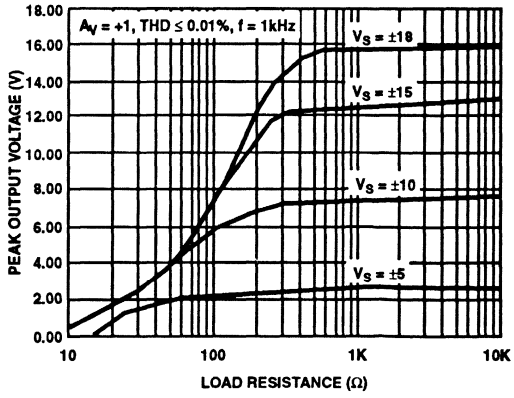


FIGURE 28. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$ (Continued)

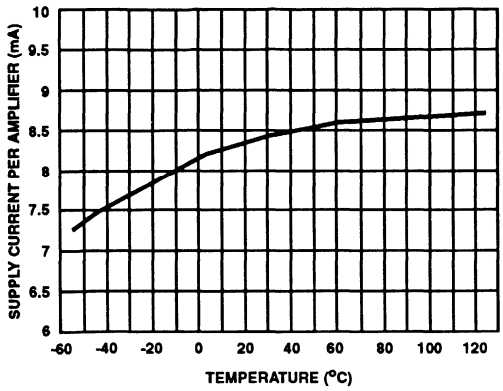


FIGURE 29. SUPPLY CURRENT/AMPLIFIER vs TEMPERATURE

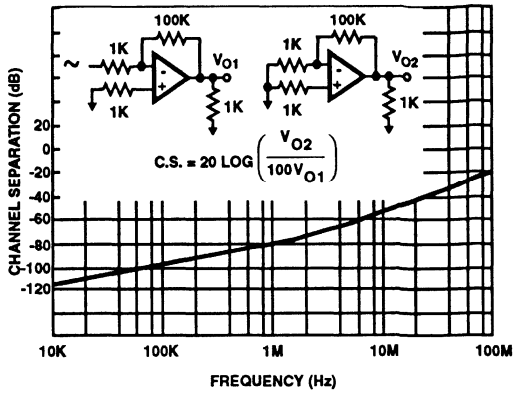


FIGURE 30. CHANNEL SEPARATION vs FREQUENCY (HA-5222 only)

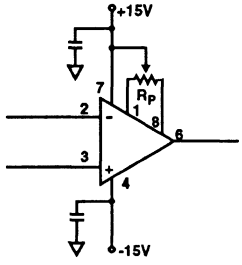
Applications Information

Operation at Various Supply Voltages

The HA-5221/5222 operates over a wide range of supply voltages with little variation in performance. The supplies may be varied from ±5 volts to ±15 volts. See typical performance curves for variations in supply current, slew rate and output voltage swing.

Offset Adjustment

The following diagram shows the offset voltage adjustment configuration for the HA-5221. By moving the potentiometer wiper towards pin 8 (+BAL), the op amps output voltage will increase; towards pin 1 (-BAL) decreases the output voltage. A 20kΩ trim pot will allow an offset voltage adjustment of about 10mV.



Capacitive Loading Considerations

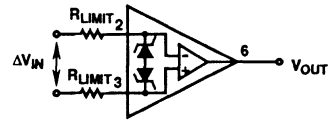
When driving capacitive loads >80pF, a small resistor, 50 to 100Ω, should be connected in series with the output and inside the feedback loop.

Saturation Recovery

When an op amp is over driven, output devices can saturate and sometimes take a long time to recover. By clamping the input, output saturation can be avoided. If output saturation can not be avoided, the maximum recovery time when overdriven into the positive rail is 10.6μs. When driven into the negative rail the maximum recovery time is 3.8μs.

Input Protection

The HA-5221/5222 has built in back-to-back protection diodes which limit the maximum allowable differential input voltage to approximately 5 volts. If the HA-5221/5222 will be used in circuits where the maximum differential voltage may be exceeded, then current limiting resistors must be used. The input current should be limited to a maximum of 10mA.



PC Board Layout Guidelines

When designing with the HA-5221 or the HA-5222, good high frequency (RF) techniques should be used when building a P.C. board. Use of ground plane is recommended. Power supply decoupling is very important. A 0.01μf to 0.1μF high quality ceramic capacitor at each power supply pin with a 2.2μF to 10μF tantalum close by will provide excellent decoupling. Chip capacitors produce the best results due to ease of placement next to the op amp and basically no lead inductance. If leaded capacitors are used, the leads should be kept as short as possible to minimize lead inductance.

HARRIS SEMICONDUCTOR

HA5232, HA5234

PRELIMINARY

March 1993

Precision Dual and Quad Operational Amplifiers

Features

- Low Offset Voltage.....200μV (Max)
- Low Offset Drift .....2μV/°C
- Low Supply Current.....<0.7mA/Amp
- High Gain, CMRR and PSRR

Applications

- Audio Amplifiers
- Low Impedance Sensors
- Universal Active Filters
- Process Control Equipment

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA5232IJ	-40°C to +85°C	8 Lead Ceramic DIP
HA5232IP	-40°C to +85°C	8 Lead Plastic DIP
HA5232IB	-40°C to +85°C	16 Lead Wide Body SOIC
HA5232AIJ	-40°C to +85°C	8 Lead Ceramic DIP
HA5232AIP	-40°C to +85°C	8 Lead Plastic DIP
HA5232AIB	-40°C to +85°C	16 Lead Wide Body SOIC
HA5234IJ	-40°C to +85°C	14 Lead Ceramic DIP
HA5234IP	-40°C to +85°C	14 Lead Plastic DIP
HA5234IB	-40°C to +85°C	16 Lead Wide Body SOIC
HA5234AIJ	-40°C to +85°C	14 Lead Ceramic DIP
HA5234AIP	-40°C to +85°C	14 Lead Plastic DIP
HA5234AIB	-40°C to +85°C	16 Lead Wide Body SOIC

Description

The HA5232 and HA5234 are dual and quad precision bipolar-input op amps. They are intended for use in multichannel data acquisition systems where moderate to high level of accuracy is required. This relatively high level of accuracy is maintained across temperature with an Average Offset Drift of 2μV/°C for the "A" grade product.

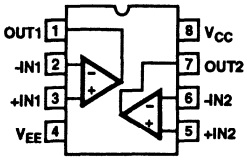
The HA5232 and HA5234 were designed to offer a solution/ enhancement over lower performance devices like the HA-4741 and CA324. These products will allow the designer to achieve a relatively high level of precision in his transducer preamp without concern for offset trimming. These devices are pin and performance compatible with the OP200, OP400, LT1013 and LT1014 operational amplifiers.

Applications will be in process control and environment monitoring where many low impedance sensors such as thermocouples, thermistors, strain gauges, and pressure transducers are used to assess the state of the system. Other systems with similar requirements include mainframe computers, aircraft, and semiconductor fab and test equipment.

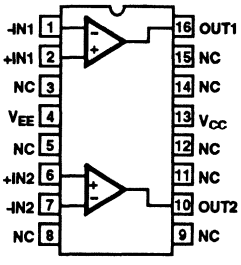
The HA5232 and HA5234 are available in industrial temperature ranges, and a choice of packages. For SOIC in tape and reel please add suffix "96" to the end of the part number.

Pinouts

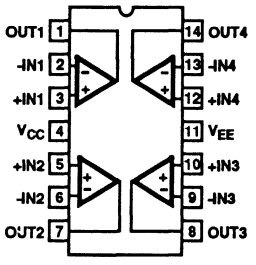
HA5232 (PDIP, CDIP)
TOP VIEW



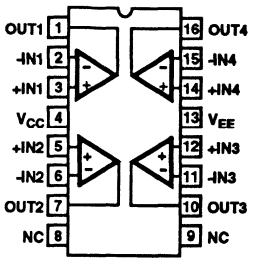
HA5232 (300 MIL SOIC)
TOP VIEW



HA5234 (PDIP)
HA5234 (CDIP)
TOP VIEW



HA5234 (300 MIL SOIC)
TOP VIEW



NOTE: The functional pinouts will comply to the JEDEC standards for dual and quad op amps as shown above

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2851.1**

Absolute Maximum Ratings

Voltage Between V+ and V- 36V
Input Voltage..... V_{SUPPLY}
Differential Input Voltage..... V_{SUPPLY}
Output Current ..... Short Circuit Protected
Junction Temperature (Plastic)..... +150°C
Junction Temperature (Hermetic)..... +175°C

Operating Temperature Ranges

HA5232I, HA5234I ..... -40°C ≤ TA ≤ +85°C
Storage Temperature Range..... -65°C ≤ TA ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

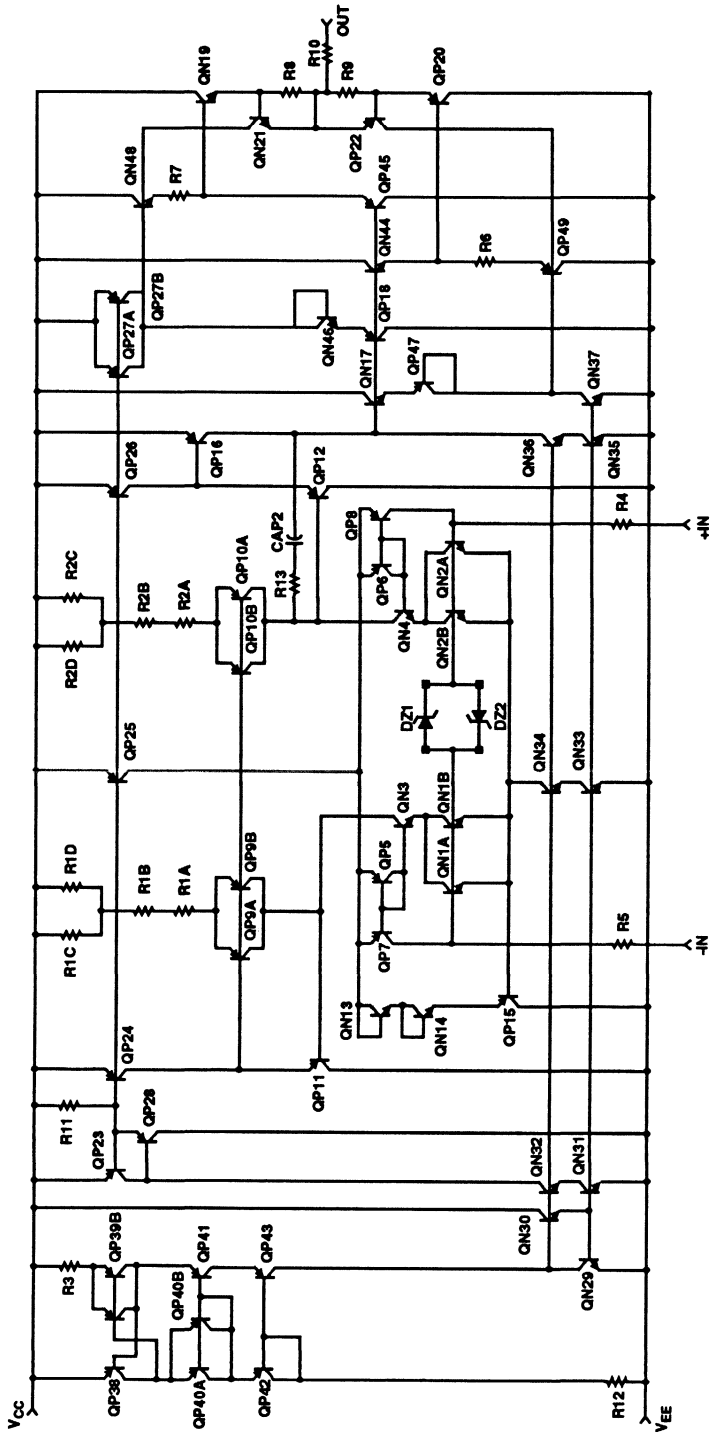
V_{SUPPLY} = ±15V, R_L = 100kΩ, C_L = 20pF, Unless Otherwise Specified

PARAMETER		TEMP	HA5232A, HA5234A			HA5232, HA5234			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage		+25°C	-	100	200	-	100	500	µV
		Full	-	-	300	-	-	725	µV
Average Offset Drift		Full	-	-	2	-	-	5	µV/°C
Input Bias Current		+25°C	-	5	-	-	10	-	nA
		Full	-	-	-	-	-	-	nA
Input Offset Current		+25°C	-	3.5	-	-	10	-	nA
		Full	-	-	-	-	-	-	nA
Common Mode Range		Full	±12	-	-	±12	-	-	V
CMRR (Note 1)		+25°C	110	-	-	100	-	-	dB
		Full	105	-	-	100	-	-	dB
Input Capacitance		+25°C	-	3	-	-	3	-	pF
Input Noise Voltage	0.1Hz - 10Hz	+25°C	-	0.5	-	-	0.5	-	μV_{P-P}
	f_O = 1kHz	+25°C	-	11	-	-	11	-	$nV/\sqrt{Hz}$
Input Noise Current	0.1Hz - 10Hz	+25°C	-	15	-	-	15	-	pA_{P-P}
	f_O = 1kHz	+25°C	-	0.4	-	-	0.4	-	$pA/\sqrt{Hz}$
Large Signal Gain (Note 2)		+25°C	1000	-	-	250	-	-	KV/V
		Full	1000	-	-	250	-	-	KV/V
Unity Gain Bandwidth		+25°C	-	0.8	-	-	0.8	-	MHz
Minimum Stable Gain		Full	1	-	-	1	-	-	V/V
Output Swing (Note 2)		Full	12	-	-	12	-	-	V
Short Circuit Current		Full	-	20	-	-	20	-	mA
Slew Rate (Note 3)		+25°C	-	0.15	-	-	0.15	-	V/µs
PSRR (Note 4)		+25°C	105	-	-	100	-	-	dB
		Full	100	-	-	100	-	-	dB
I_{CC}	HA5232	+25°C	-	-	1.45	-	-	1.45	mA
		Full	-	-	1.55	-	-	1.55	mA
	HA5234	+25°C	-	-	2.9	-	-	2.9	mA
		Full	-	-	3.1	-	-	3.1	mA

NOTES:

1. V_{CM} = ±12V
2. R_L = 2K
3. R_L = 2K, C_L = 100pF, V_{OUT} = ±10V, A_V = +1
4. $|V_S|$ = 3V to 18V

Schematic


OUT
QN19
R8
R10
R9
QP20
QN21
QP22
QN48
R7
QP45
QN44
R6
QP49
QP27B
QP27A
QP18
QN46
QN17
QP47
QN37
QP26
QP16
QP12
QN36
QN35
R4
+IN
CAP2
QP8
QP10A
R2C
R2B
R2A
R13
QP6
QN2A
QP10B
QN4
QN2B
R2D
DZ1
DZ2
QP25
QN34
QN33
QN3
QN1B
R1D
QP9B
QP5
QN1A
R1B
R1A
QP9A
R5
-IN
R1C
QP7
QN13
QN14
QP15
QP24
QP11
R11
QP28
QP23
QN32
QN31
QP39B
QP41
QP43
QN30
R3
QP40B
QN29
QP38
QP40A
QP42
R12
VCC
VEE

Die Characteristics

DIE DIMENSIONS:
87 x 105 x 21 ± 1mils

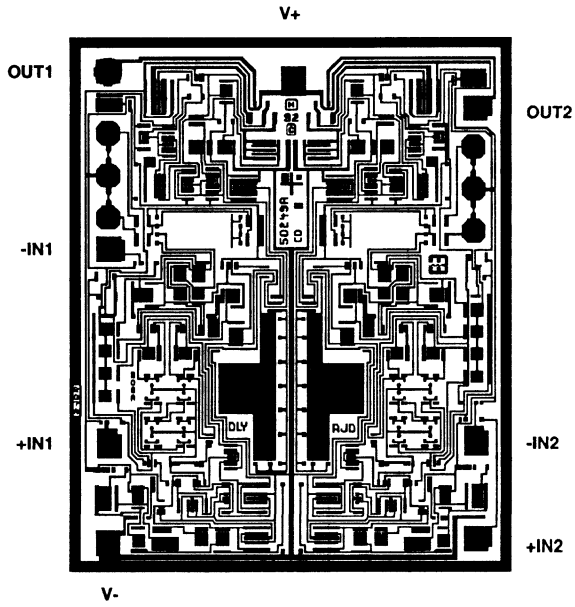
METALLIZATION:
Type: Al
Thickness: 19kÅ ± 4kÅ

GLASSIVATION:
Type: Silox (SiO_2)
Thickness: 13.5kÅ ± 2kÅ

DIE ATTACH:
Material: Silver Epoxy - Plastic DIP and SOIC
Glass - Ceramic DIP

Metallization Mask Layout

HA5232



Die Characteristics

DIE DIMENSIONS:
114 x 157 x 21 ± 1mils

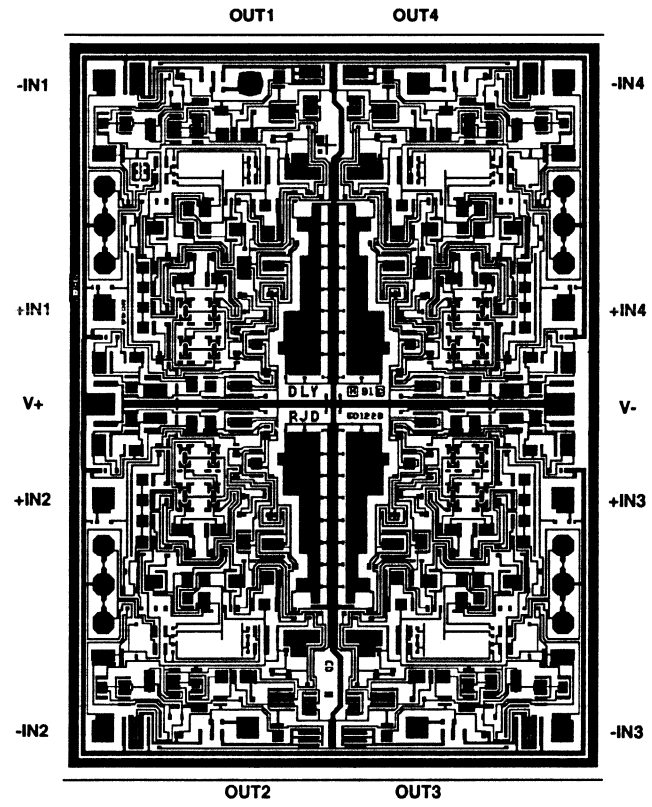
METALLIZATION:
Type: Al
Thickness: 19kÅ ± 4kÅ

GLASSIVATION:
Type: Silox (SiO_2)
Thickness: 13.5kÅ ± 2kÅ

DIE ATTACH:
Material: Silver Epoxy - Plastic DIP and SOIC
Glass - Ceramic DIP

Metallization Mask Layout

HA5234



HARRIS SEMICONDUCTOR

HFA-0001

Ultra High Slew Rate Operational Amplifier

March 1993

Features

- Unity Gain Bandwidth 350MHz
- Full Power Bandwidth 53MHz
- High Slew Rate 1000V/μs
- High Output Drive ..... ±50mA
- Monolithic Construction

Applications

- RF/IF Processors
- Video Amplifiers
- High Speed Cable Drivers
- Pulse Amplifiers
- High Speed Communications
- Fast Data Acquisition Systems

Description

The HFA-0001 is an all bipolar op amp featuring high slew rate (1000V/μs), and high unity gain bandwidth (350MHz). These features combined with fast settling time (25ns) make this product very useful in high speed data acquisition systems as well as RF, video, and pulse amplifier designs. Other outstanding characteristics include low bias currents (15μA), low offset current (18μA), and low offset voltage (6mV).

The HFA-0001 offers high performance at low cost. It can replace hybrids and RF transistor amplifiers, simplifying designs while providing increased reliability due to monolithic construction. To enhance the ease of design, the HFA-0001 has a 50Ω ±20% resistor connected from the output of the op amp to a separate pin. This can be used when driving 50Ω strip line, microstrip, or coax cable.

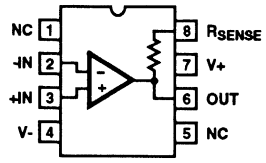
For MIL-STD-883 compliant product consult the HFA-0001/883 datasheet.

Ordering Information

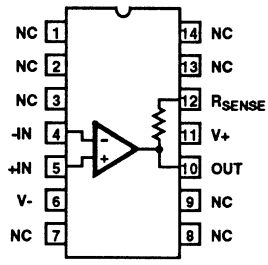
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1-0001-5	0°C to +75°C	14 Lead Ceramic Sidebraze DIP
HFA1-0001-9	-40°C to +85°C	14 Lead Ceramic Sidebraze DIP
HFA3-0001-5	0°C to +75°C	8 Lead Plastic DIP
HFA3-0001-9	-40°C to +85°C	8 Lead Plastic DIP
HFA9P0001-5	0°C to +75°C	16 Lead Widebody SOIC

Pinouts

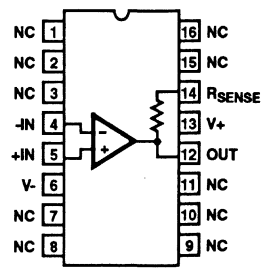
HFA-0001 (PDIP) TOP VIEW



HFA-0001 (CDIP) TOP VIEW



HFA-0001 (300 MIL SOIC) TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2916.1**

Specifications HFA-0001

Absolute Maximum Ratings (Note 1)

Supply Voltage (Between V+ and V- Terminals) 12V
Differential Input Voltage 5V
Input Voltage ..... ±4V
Output Current 60mA
Junction Temperature (Note 9) ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HFA-0001-9 ..... $-40°C \le T_A \le +85°C$
HFA-0001-5 ..... $0°C \le T_A \le +75°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = +5V, V- = -5V, Unless Otherwise Specified

PARAMETER		TEMP	HFA-0001-9 MIN	HFA-0001-9 TYP	HFA-0001-9 MAX	HFA-0001-5 MIN	HFA-0001-5 TYP	HFA-0001-5 MAX	UNITS
INPUT CHARACTERISTICS									
Offset Voltage		+25°C	-	6	15	-	6	30	mV
		High	-	4.5	20	-	4.5	30	mV
		Low	-	12.5	45	-	12.5	35	mV
Average Offset Voltage Drift		High	-	50	-	-	50	-	µV/°C
		Low	-	100	-	-	100	-	µV/°C
Bias Current		+25°C	-	15	50	-	15	100	µA
		Full	-	20	50	-	20	100	µA
Offset Current		+25°C	-	18	25	-	18	50	µA
		Full	-	22	50	-	22	50	µA
Common Mode Range		+25°C	±3	-	-	±3	-	-	V
Differential Input Resistance		+25°C	-	10	-	-	10	-	kΩ
Input Capacitance		+25°C	-	2	-	-	2	-	pF
Input Noise Voltage	0.1Hz to 10Hz	+25°C	-	3.5	-	-	3.5	-	µVrms
	10Hz to 1MHz	+25°C	-	6.7	-	-	6.7	-	µVrms
Input Noise Voltage	f_O = 10Hz	+25°C	-	640	-	-	640	-	nV/√Hz
	f_O = 100Hz	+25°C	-	170	-	-	170	-	nV/√Hz
	f_O = 100kHz	+25°C	-	6	-	-	6	-	nV/√Hz
Input Noise Current	f_O = 10Hz	+25°C	-	2.35	-	-	2.35	-	nA/√Hz
	f_O = 100Hz	+25°C	-	0.57	-	-	0.57	-	nA/√Hz
	f_O = 1000Hz	+25°C	-	0.16	-	-	0.16	-	nA/√Hz
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain (Note 2)		+25°C	150	200	-	150	200	-	V/V
		High	150	170	-	100	170	-	V/V
		Low	150	220	-	150	220	-	V/V
Common Mode Rejection Ratio (Note 3)		+25°C	45	47	-	42	47	-	dB
		High	40	45	-	40	45	-	dB
		Low	45	48	-	42	48	-	dB
Unity Gain Bandwidth		+25°C	-	350	-	-	350	-	MHz
Minimum Stable Gain		Full	1	-	-	1	-	-	V/V

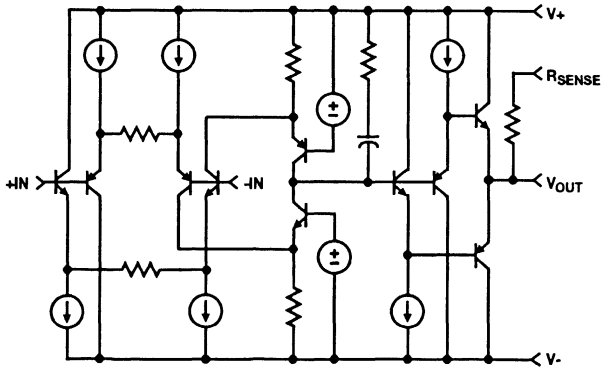
Electrical Specifications V+ = +5V, V- = -5V, Unless Otherwise Specified (Continued)

PARAMETER		TEMP	HFA-0001-9			HFA-0001-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 100Ω	+25°C	-	±3.5	-	-	±3.5	-	V
	R_L = 1kΩ	+25°C	±3.5	±3.7	-	±3.5	±3.7	-	V
		High	±3.0	±3.6	-	±3.0	±3.6	-	V
		Low	±3.5	±3.7	-	±3.5	±3.7	-	V
Full Power Bandwidth (Note 5)		+25°C	-	53	-	-	53	-	MHz
Output Resistance, Open Loop		+25°C	-	3	-	-	3	-	Ω
Output Current		Full	±30	±50	-	±30	±50	-	mA
TRANSIENT RESPONSE									
Rise Time (Note 4, 6)		+25°C	-	480	-	-	480	-	ps
Slew Rate (Note 4, 7)	R_L = 1kΩ	+25°C	-	1000	-	-	1000	-	V/µs
	R_L = 100Ω	+25°C	-	875	-	-	875	-	V/µs
Settling Time (3V Step)	0.1%	+25°C	-	25	-	-	25	-	ns
Overshoot (Note 4, 6)		+25°C	-	36	-	-	36	-	%
POWER SUPPLY CHARACTERISTICS									
Supply Current		Full	-	65	75	-	65	75	mA
Power Supply Rejection Ratio (Note 8)		+25°C	40	42	-	37	42	-	dB
		High	35	41	-	35	41	-	dB
		Low	40	42	-	37	42	-	dB

NOTES:

1. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = 0 to ±2V, R_L = 1kΩ.
3. ΔV_{CM} = ±2V.
4. R_L = 100Ω.
5. Full Power Bandwidth is calculated by equation: $FPBW = \frac{SlewRate}{2\pi V_{PEAK}}$, V_{PEAK} = 3.0V.
6. V_{OUT} = ±200mV, A_V = +1.
7. V_{OUT} = ±3V, A_V = +1.
8. ΔV_S = ±4V to ±6V.
9. See Thermal Constants in 'Applications Information' text. Maximum power dissipation, including output load, must be designed to maintain the junction temperature below +175°C for hermetic packages, and below +150°C for plastic packages.

Schematic Diagram



Die Characteristics

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
HFA1-0001-5/-9	75	13
HFA3-0001-5	98	36
HFA9P-0001-5/-9	96	27

Test Circuits

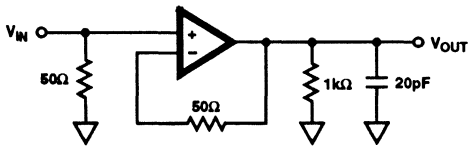


FIGURE 1. LARGE SIGNAL RESPONSE TEST CIRCUIT

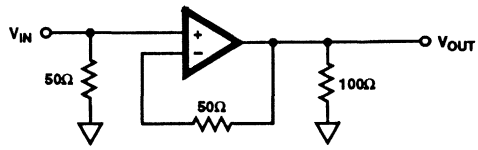
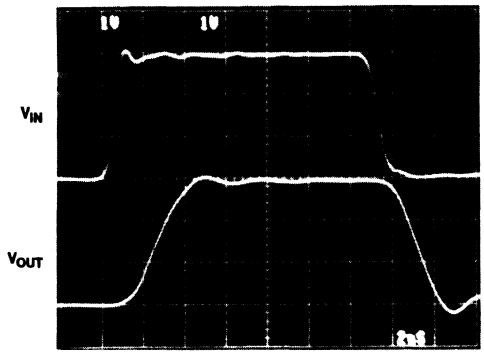
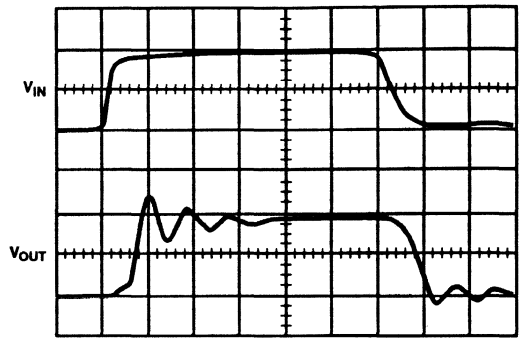


FIGURE 2. SMALL SIGNAL RESPONSE TEST CIRCUIT

LARGE SIGNAL RESPONSE
V_{OUT} = 0V to 3V
Vertical Scale: 1V/Div.
Horizontal Scale: 2ns/Div.



SMALL SIGNAL RESPONSE
V_{OUT} = 0mV to 200mV
Vertical Scale: 100mV/Div.
Horizontal Scale: 2ns/Div.



NOTE: Initial Step In Output Is Due To Fixture Feedthrough

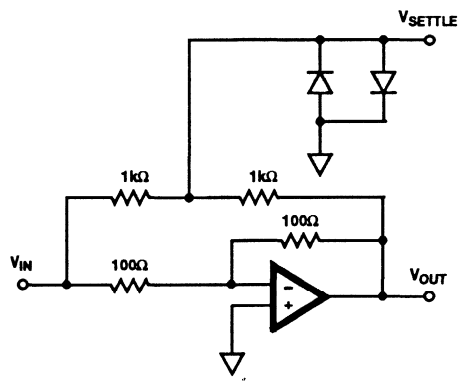


FIGURE 3. SETTLING TIME SCHEMATIC

PROPAGATION DELAY
Vertical Scale: 500mV/Div.
Horizontal Scale: 2ns/Div.
A_V = +1, R_L = 100Ω, V_{OUT} = 0V to 3V

NOTE: Test Fixture Delay of 450ps is Included

Typical Performance Curves $V_S = \pm5V$, $T_A = +25°C$, Unless Otherwise Specified

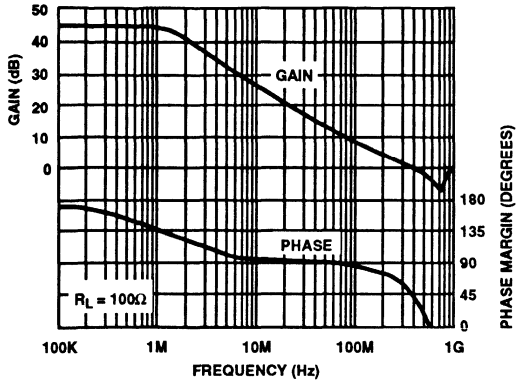


FIGURE 4. OPEN LOOP GAIN AND PHASE vs FREQUENCY

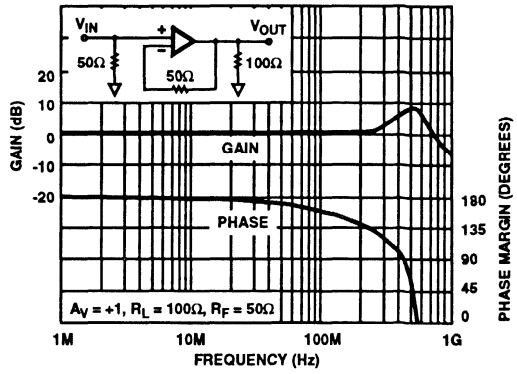


FIGURE 5. CLOSED LOOP GAIN vs FREQUENCY

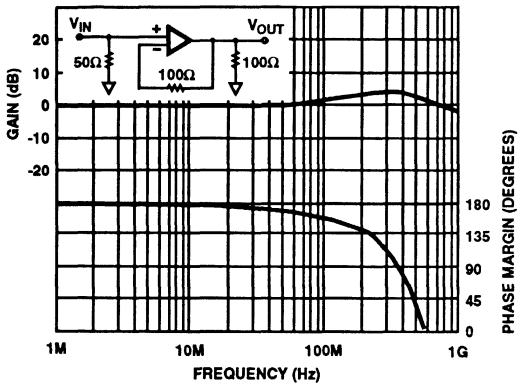


FIGURE 6. CLOSED LOOP GAIN vs FREQUENCY

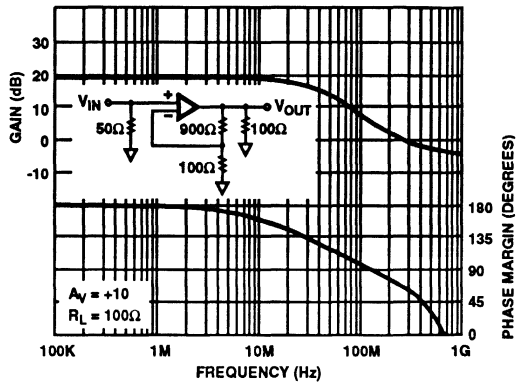


FIGURE 7. CLOSED LOOP GAIN vs FREQUENCY

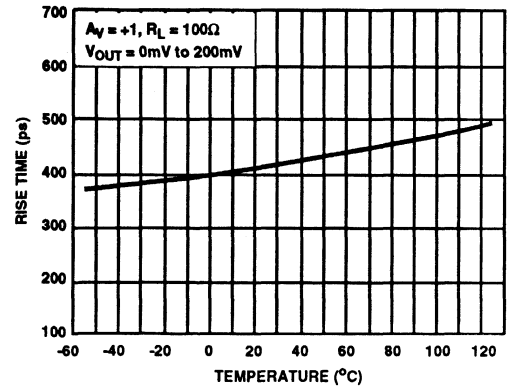


FIGURE 8. RISE TIME vs TEMPERATURE

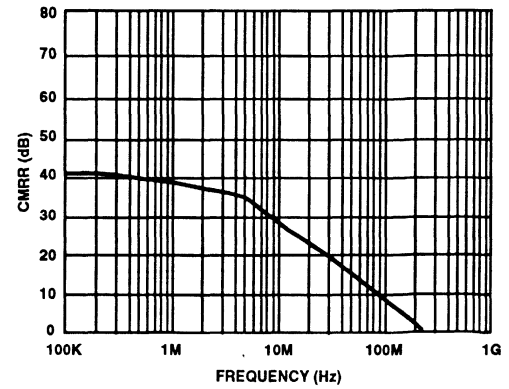


FIGURE 9. CMRR vs FREQUENCY

Typical Performance Curves $V_S = \pm5V$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

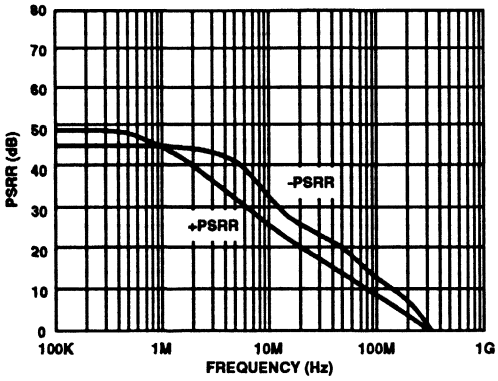


FIGURE 10. PSRR vs FREQUENCY

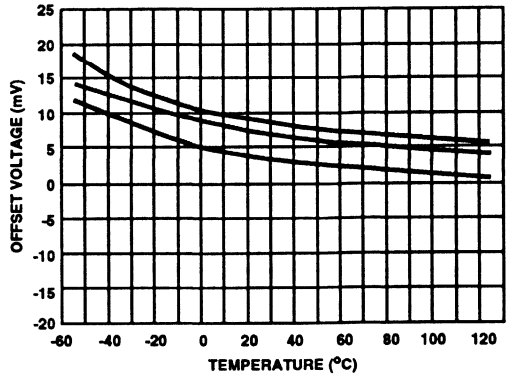


FIGURE 11. OFFSET VOLTAGE vs TEMPERATURE (3 REPRESENTATIVE UNITS)

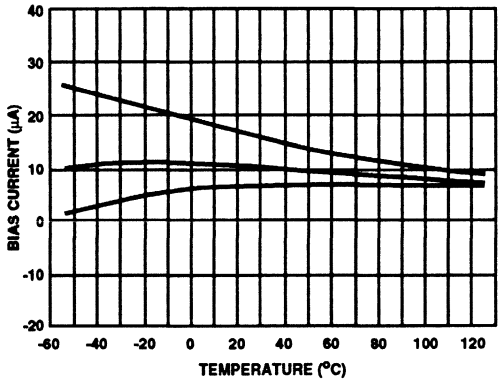


FIGURE 12. BIAS CURRENT vs TEMPERATURE (3 REPRESENTATIVE UNITS)

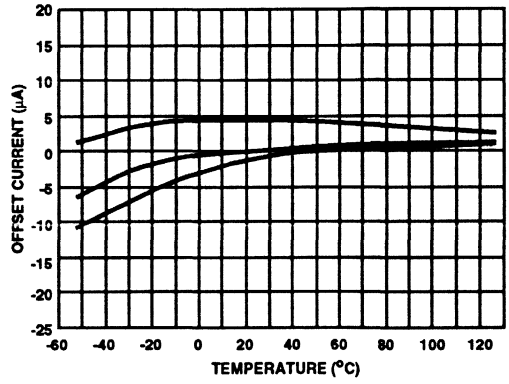


FIGURE 13. OFFSET CURRENT vs TEMPERATURE (3 REPRESENTATIVE UNITS)

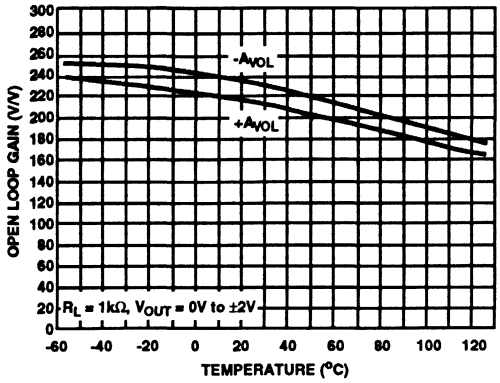


FIGURE 14. OPEN LOOP GAIN vs TEMPERATURE

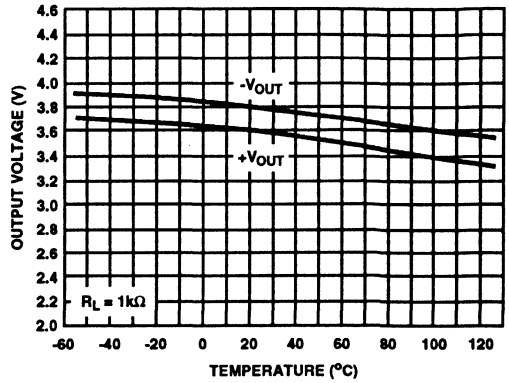


FIGURE 15. OUTPUT VOLTAGE SWING vs TEMPERATURE

Typical Performance Curves $V_S = \pm5V$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

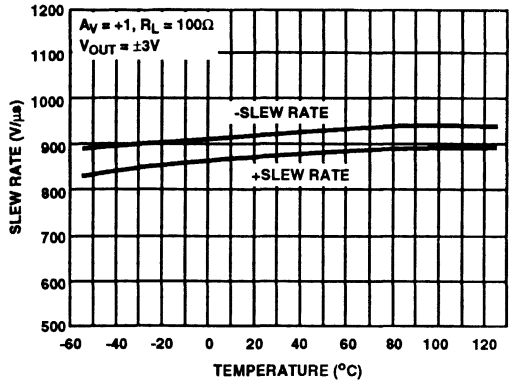


FIGURE 16. SLEW RATE vs TEMPERATURE

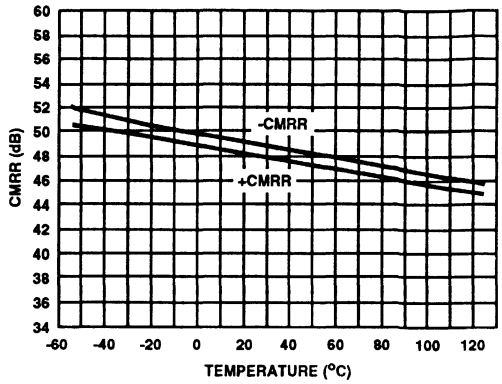


FIGURE 17. CMRR vs TEMPERATURE

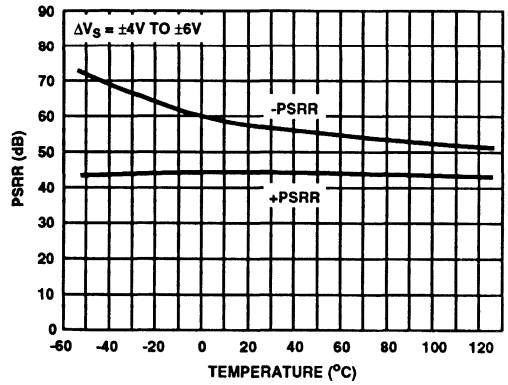


FIGURE 18. PSRR vs TEMPERATURE

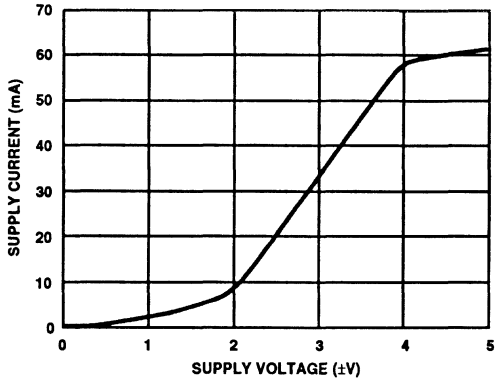


FIGURE 19. SUPPLY CURRENT vs SUPPLY VOLTAGE

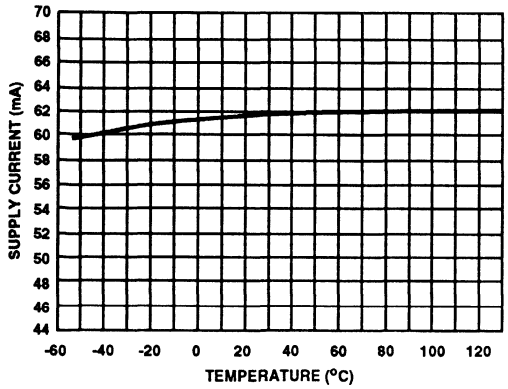


FIGURE 20. SUPPLY CURRENT vs TEMPERATURE

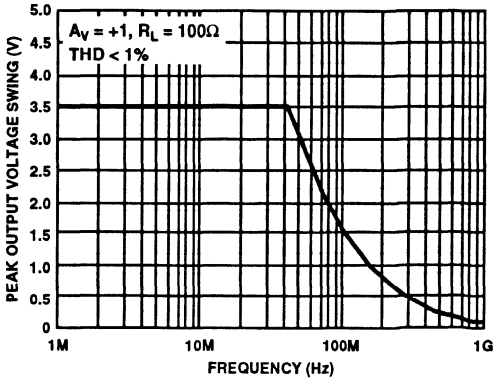


FIGURE 21. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

Typical Performance Curves $V_S = \pm5V$, $T_A = +25^oC$, Unless Otherwise Specified (Continued)

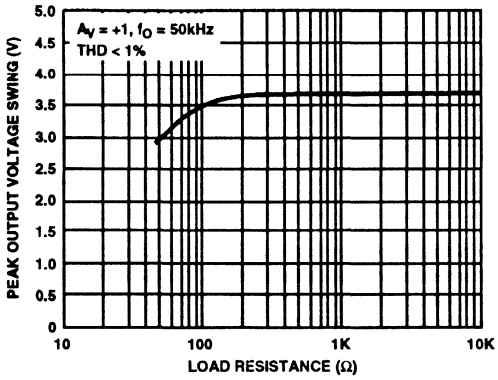


FIGURE 22. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

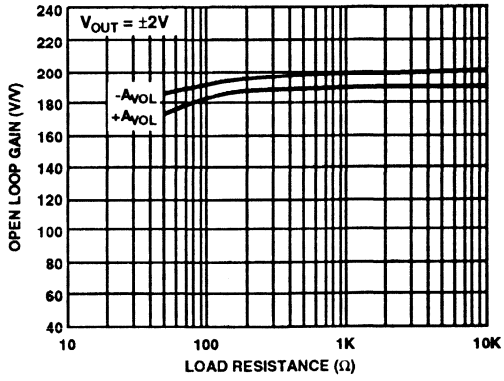


FIGURE 23. OPEN LOOP GAIN vs LOAD RESISTANCE

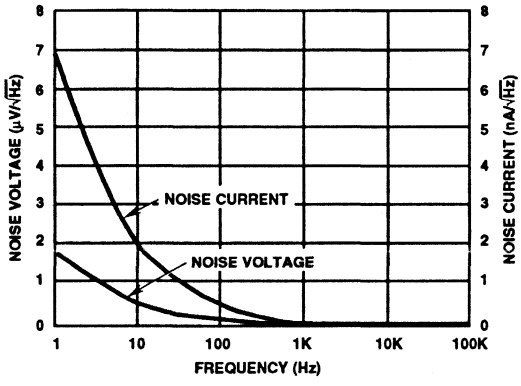


FIGURE 24. INPUT NOISE vs FREQUENCY

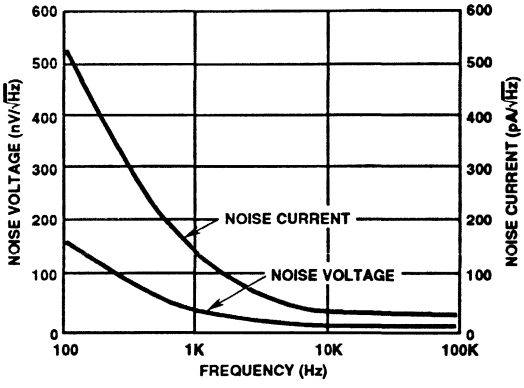


FIGURE 25. INPUT NOISE vs FREQUENCY

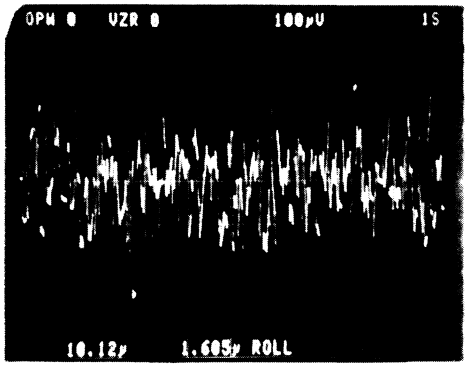


FIGURE 26. INPUT VOLTAGE NOISE 0.1Hz to 10Hz
A_V = 50, Noise Voltage = 1.605μVrms (RTI)
Noise Voltage = 10.12μV_{P-P}

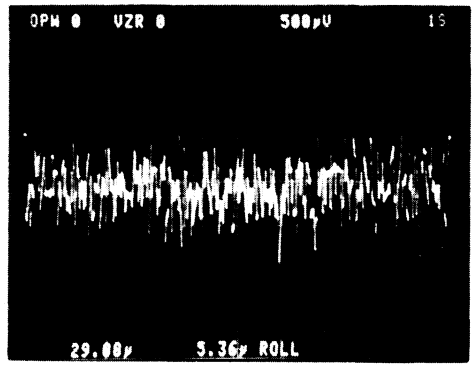


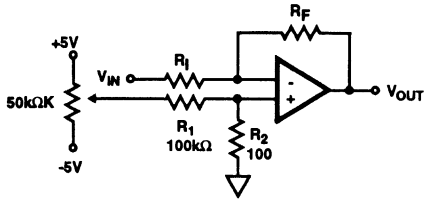
FIGURE 27. INPUT NOISE VOLTAGE 10Hz to 1MHz
A_V = 50, Noise Voltage = 5.36μVrms (RTI)
Noise Voltage = 29.88μV_{P-P}

Applications Information

Offset Adjustment

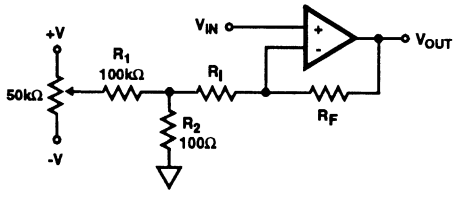
When applications require the offset voltage to be as low as possible, the figure below shows two possible schemes for adjusting offset voltage.

For a voltage follower application, use the circuit in Figure 29 without R_2 and with R_I shorted. R_1 should be 1MΩ to 10MΩ. The adjustment resistors will cause only a very small gain error.



$$\text{Adjustment Range} \cong \pm V\left(\frac{R_2}{R_1}\right)$$

FIGURE 28. INVERTING GAIN



$$\text{Adjustment Range} \cong \pm V\left(\frac{R_2}{R_1}\right) \qquad \text{Gain} \cong 1 + \left(\frac{R_F}{R_I + R_2}\right)$$

FIGURE 29. NON-INVERTING GAIN

PC Board Layout Guidelines

When designing with the HFA-0001, good high frequency (RF) techniques should be used when making a PC board. A massive ground plane should be used to maintain a low impedance ground. Proper shielding and use of short interconnection leads are also very important.

To achieve maximum high frequency performance, the use of low impedance transmission lines with impedance matching is recommended: 50Ω lines are common in communications and 75Ω lines in video systems. Impedance matching is important to minimize reflected energy therefore minimizing transmitted signal distortion. This is accomplished by using a series matching resistor (50Ω or 75Ω), matched transmission line (50Ω or 75Ω), and a matched terminating resistor, as shown in Figure 30. Note that there will be a 6dB loss from input to output. The HFA-0001 has an integral 50Ω ±20% resistor connected to the op amps output with the other end of the resistor pinned out. This 50Ω resistor can be used as the series resistor instead of an external resistor.

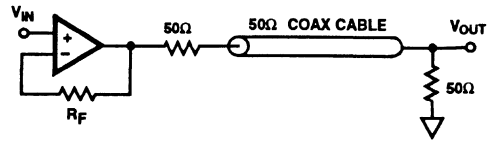


FIGURE 30.

PC board traces can be made to look like a 50Ω or 75Ω transmission line, called microstrip. Microstrip is a PC board trace with a ground plane directly beneath, on the opposite side of the board, as shown in Figure 31.

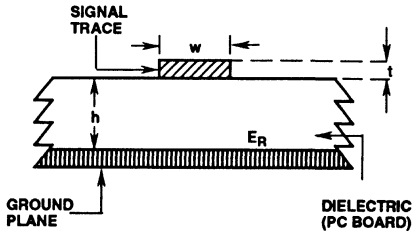


FIGURE 31.

When manufacturing pc boards, the trace width can be calculated based on a number of variables. The following equation is reasonably accurate for calculating the proper trace width for a 50Ω transmission line.

$$Z_O = \frac{87}{\sqrt{E_R + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)\Omega$$

Power supply decoupling is essential for high frequency op amps. A 0.01µF high quality ceramic capacitor at each supply pin in parallel with a 1µF tantalum capacitor will provide excellent decoupling as shown in Figure 32.

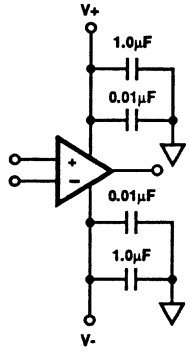


FIGURE 32. POWER SUPPLY DECOUPLING

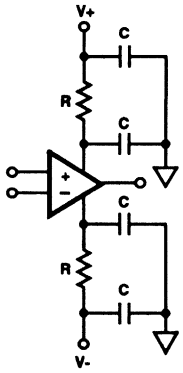


FIGURE 33. IMPROVED DECOUPLING/CURRENT LIMITING

Chip capacitors produce the best results due to ease of placement next to the op amp and they have negligible lead inductance. If leaded capacitors are used, the leads should be kept as short as possible to minimize lead inductance. Figures 32 and 33 illustrate two different decoupling schemes. Figure 33 improves the PSRR because the resistor and capacitors create low pass filters. Note that the supply current will create a voltage drop across the resistor.

Saturation Recovery

When an op amp is over driven output devices can saturate and sometimes take a long time to recover. By clamping the input to safe levels, output saturation can be avoided. If output saturation cannot be avoided, the recovery time from 25% over-drive is 20ns and 30ns from 50% over-drive.

Thermal Management

The HFA-0001 can sink and source a large amount of current making it very useful in many applications. Care must be taken not to exceed the power handling capability of the part to insure proper performance and maintain high reliability. The following graph shows the maximum power handling capability of the HFA-0001 without exceeding the maximum allowable junction temperature of +175°C. The curves also show the improved power handling capability when heatsinks are used based on AVVID heatsink #5801B for the 8 lead Plastic DIP and IERC heatsink #PEP50AB for the 14 lead Sidebraze DIP. These curves are based on natural convection. Forced air will greatly improve the power dissipation capabilities of a heatsink.

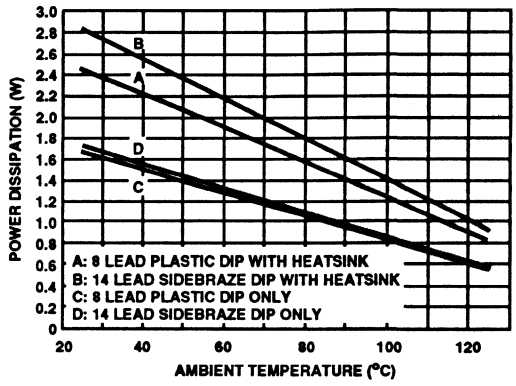


FIGURE 34.

HARRIS SEMICONDUCTOR

HFA-0002

Low Noise Wideband Operational Amplifier

March 1993

Features

- Wide Gain Bandwidth Product 1GHz
- High Slew Rate 250V/μs
- High Open Loop Gain 105V/mV
- Low Offset Voltage 0.6mV
- Low Power Consumption 143mW
- Low Input Voltage Noise at 1kHz ..... 2.7nV/$\sqrt{Hz}$
- Monolithic Construction

Applications

- RF/IF Processors
- Video Amplifiers
- Radar Systems
- Pulse Amplifiers
- High Speed Communications
- Fast Data Acquisition Systems

Description

The HFA-0002 is a very wideband, high slew rate, op amp, featuring precision DC characteristics. Stable in gains of 10 or greater this all bipolar op amp offers a combination of AC and DC performance never seen before in monolithic form.

The high gain bandwidth product (1GHz) and high slew rate (250V/μs) make this op amp ideal for use in video and RF circuits. The low offset voltage (0.6mV), low bias current (0.23μA), and low voltage noise (2.7nV/$\sqrt{Hz}$) specifications combined with the excellent AC characteristics make this op amp ideal for high speed data acquisition systems with high accuracy.

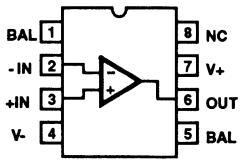
For MIL-STD-883 compliant product and Ceramic LCC package consult the HFA-0002/883 datasheet.

Ordering Information

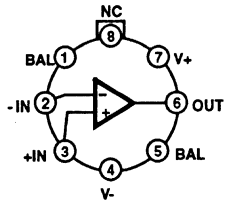
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA2-0002-5	0°C to +75°C	8 Pin CAN
HFA2-0002-9	-40°C to +85°C	8 Pin CAN
HFA3-0002-5	0°C to +75°C	8 Lead Plastic DIP
HFA3-0002-9	-40°C to +85°C	8 Lead Plastic DIP
HFA7-0002-5	0°C to +75°C	8 Lead Ceramic Sidebraze DIP
HFA7-0002-9	-40°C to +85°C	8 Lead Ceramic Sidebraze DIP
HFA9P0002-5	0°C to +75°C	8 Lead SOIC
HFA9P0002-9	-40°C to +85°C	8 Lead SOIC

Pinouts

HFA-0002
(PDIP, CDIP, SOIC)
TOP VIEW



HFA-0002
(TO-99 METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2917.1**

Absolute Maximum Ratings (Note 1)

Supply Voltage Between V+ and V-Terminals 12V
Differential Input Voltage..... 5V
Input Voltage..... ±5V
Output Current .....±20mA
Junction Temperature (Note 10)..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.)..... +300°C

Operating Conditions

Operating Temperature Range :
HFA-0002-9.....-40°C ≤ T_A ≤ +85°C
HFA-0002-5..... 0°C ≤ T_A ≤ +75°C
Storage Temperature Range.....-65°C ≤ T_A ≤ 150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +5V, V- = -5V, Unless Otherwise Specified

PARAMETER	TEMP	HFA-0002-5/-9 MIN	HFA-0002-5/-9 TYP	HFA-0002-5/-9 MAX	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	+25°C	-	0.6	1	mV
	Full	-	1.2	2	mV
Average Offset Voltage Drift	Full	-	2.0	-	µV/°C
Bias Current	+25°C	-	0.23	1.0	µA
	High	-	0.1	1.0	µA
	Low	-	0.32	2.0	µA
Offset Current	+25°C	-	0.12	1.0	µA
	Full	-	0.16	1.0	µA
Common Mode Range	Full	±2.5	-	-	V
Differential Input Resistance	+25°C	-	1	-	MΩ
Input Capacitance	+25°C	-	2	-	pF
Input Noise Voltage					
0.1Hz to 10Hz	+25°C	-	5.1	-	nV_{RMS}
10Hz to 1MHz	+25°C	-	2.02	-	μV_{RMS}
Input Noise Voltage					
f_O = 10Hz	+25°C	-	8.9	-	$nV/\sqrt{Hz}$
f_O = 100Hz	+25°C	-	3.7	-	$nV/\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	2.7	-	$nV/\sqrt{Hz}$
Input Noise Current					
f_O = 10Hz	+25°C	-	25	-	$pA/\sqrt{Hz}$
f_O = 100Hz	+25°C	-	8.4	-	$pA/\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	4.5	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Note 2, 4)	Full	80	105	-	V/mV
Common Mode Rejection Ratio (Note 3)	+25°C	100	110	-	dB
	Full	90	108	-	dB
Gain Bandwidth Product					
f_O = 1MHz	+25°C	-	1	-	GHz
Minimum Stable Gain	Full	10	-	-	V/V
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 4)	Full	±3.5	±3.9	-	V
Full Power Bandwidth (Note 5)	+25°C	10.6	13.3	-	MHz
Output Resistance, Open Loop	+25°C	-	5	-	Ω
Output Current	Full	±10	±12	-	mA

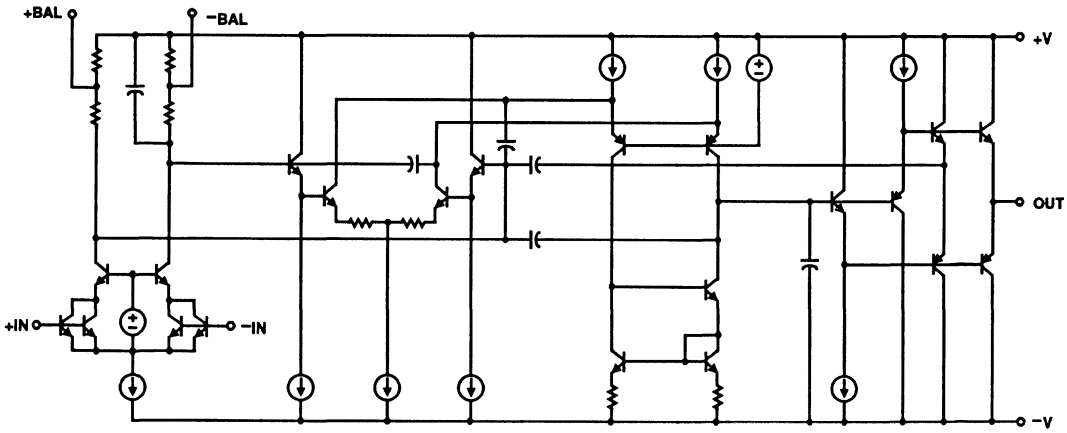
Electrical Specifications V+ = +5V, V- = -5V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	HFA-0002-5/-9			UNITS
		MIN	TYP	MAX	
TRANSIENT RESPONSE					
Rise Time (Note 4, 6)	+25°C	-	3.2	-	ns
Slew Rate (Note 4, 7, 9)	+25°C	200	250	-	V/µs
Settling Time (Note 4, 7)	+25°C	-	50	-	ns
Overshoot (Note 4, 6)	+25°C	-	30	-	%
POWER SUPPLY CHARACTERISTICS					
Supply Current	Full	-	14	20	mA
Power Supply Rejection Ratio (Note 8)	Full	90	99	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. $V_{OUT} = \pm 3V$.
3. $\Delta V_{CM} = \pm 2V$.
4. $R_L = 5K$, $C_L = 20pF$.
5. Full Power Bandwidth is guaranteed by equation: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$, $V_{peak} = 3.0V$.
6. $V_{OUT} = \pm 100mV$, $A_V = +10$.
7. $V_{OUT} = \pm 3V$, $A_V = +10$.
8. $\Delta V_S = \pm 4V$ to $\pm 6V$.
9. This parameter is not tested. This limit is guaranteed based on characterization and reflects lot to lot variation.
10. See Thermal Constants in "Applications Information" section. Maximum power dissipation, including output load, must be designed to maintain the junction temperature below +175°C for hermetic packages, and below +150°C for plastic packages.

Simplified Schematic Diagram



Die Characteristics

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
CAN	117	36
PDIP	96	34
CDIP	75	13
SOIC	158	43

Test Circuits

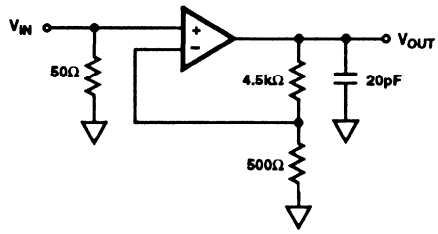
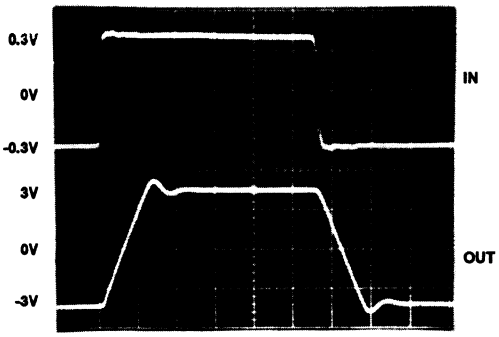
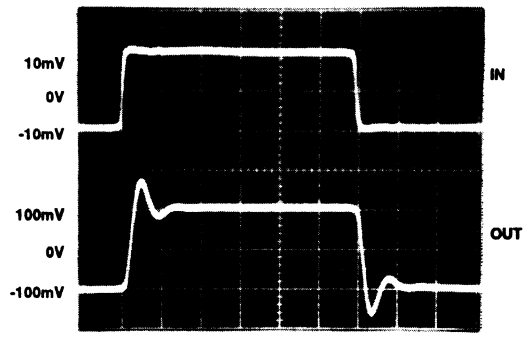


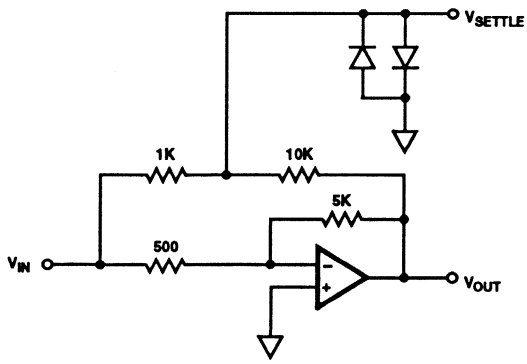
FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



LARGE SIGNAL RESPONSE
Input: 0.2V/Div. Output: 2V/Div.
Horizontal Scale: 20ns/Div.



SMALL SIGNAL RESPONSE
Input: 10mV/Div. Output: 100mV/Div.



- $A_V = -10$
- Feedback and summing resistors must be matched (0.1%)
- HP5082-2810 clipping diodes recommended
- Tektronix P6201 FET probe used at settling point

FIGURE 3. SETTLING TIME SCHEMATIC

Typical Performance Curves $V_S = \pm5V$, $T_A = +25°C$, Unless Otherwise Specified

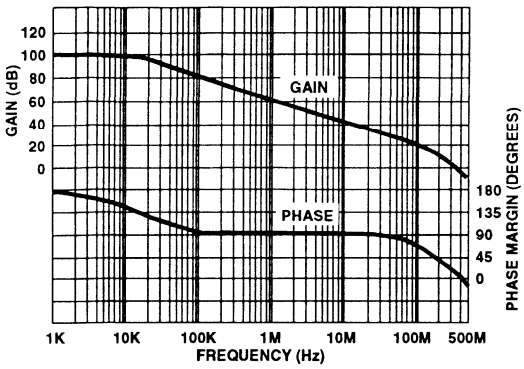


FIGURE 4. OPEN LOOP GAIN AND PHASE vs FREQUENCY

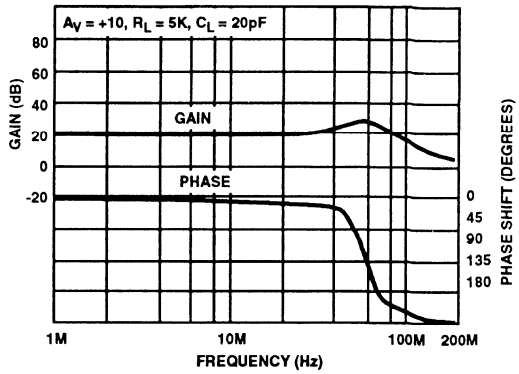


FIGURE 5. CLOSED LOOP GAIN vs FREQUENCY

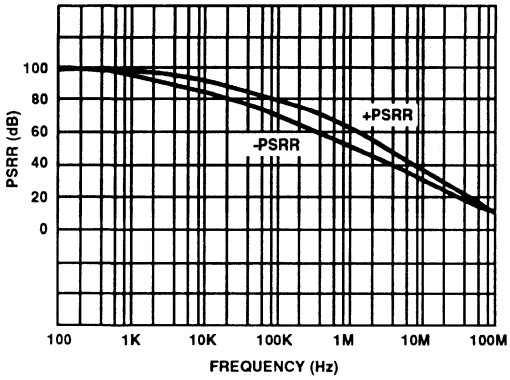


FIGURE 6. PSRR vs FREQUENCY

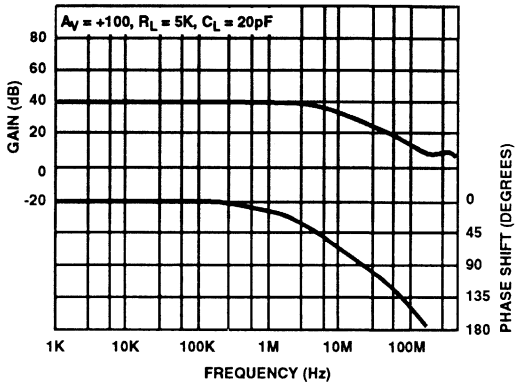


FIGURE 7. CLOSED LOOP GAIN vs FREQUENCY

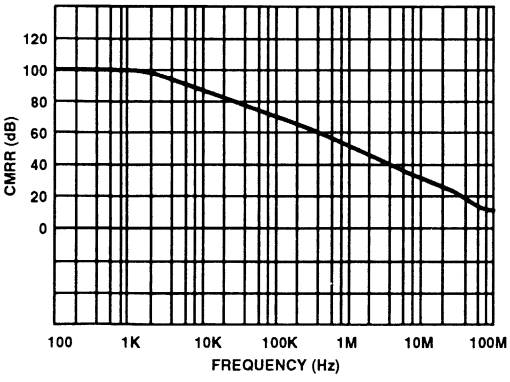


FIGURE 8. CMRR vs FREQUENCY

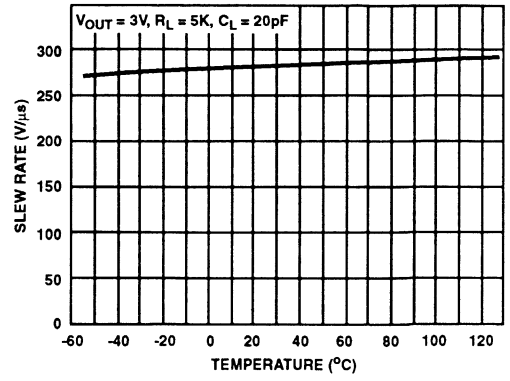


FIGURE 9. SLEW RATE vs TEMPERATURE

Typical Performance Curves $V_S = \pm5V$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

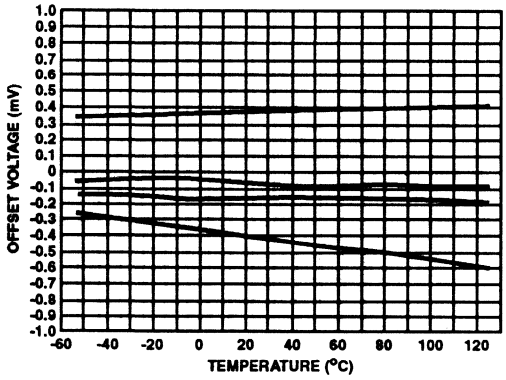


FIGURE 10. OFFSET VOLTAGE vs TEMPERATURE
4 Representative Units

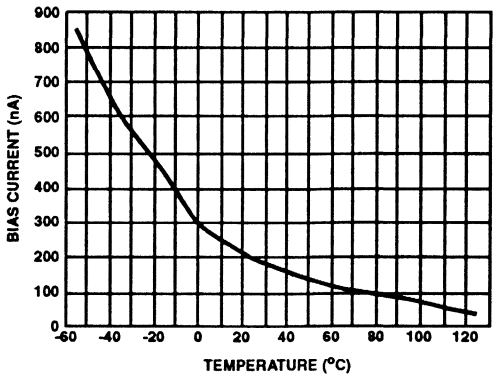


FIGURE 11. BIAS CURRENT vs TEMPERATURE

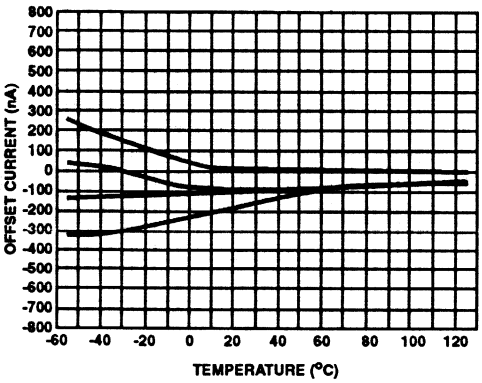


FIGURE 12. OFFSET CURRENT vs TEMPERATURE
4 Representative Units

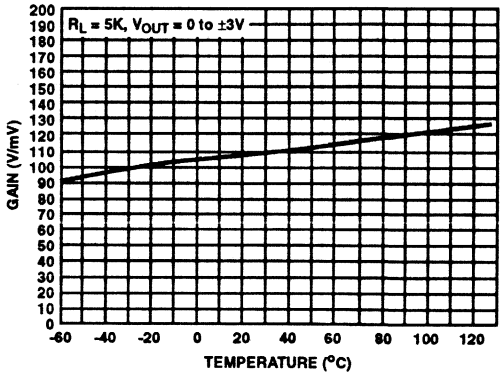


FIGURE 13. OPEN LOOP GAIN vs TEMPERATURE

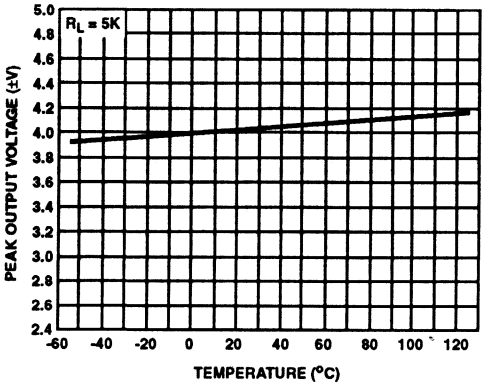


FIGURE 14. OUTPUT VOLTAGE SWING vs TEMPERATURE

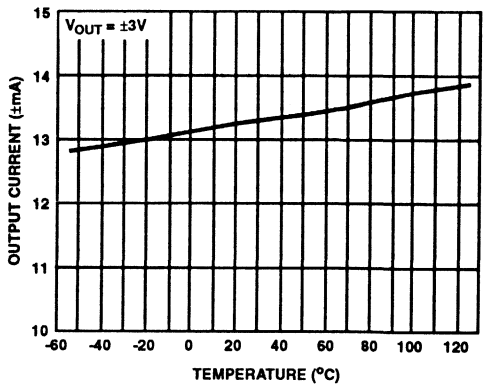


FIGURE 15. OUTPUT CURRENT vs TEMPERATURE

Typical Performance Curves $V_S = \pm5V$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

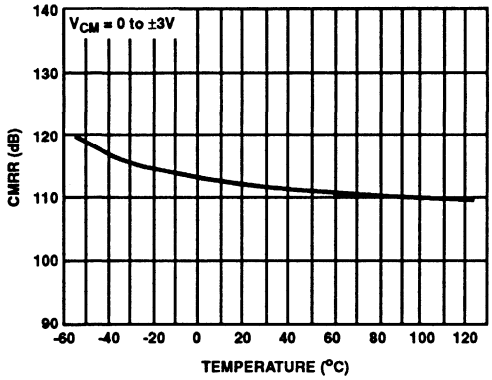


FIGURE 16. CMRR vs TEMPERATURE

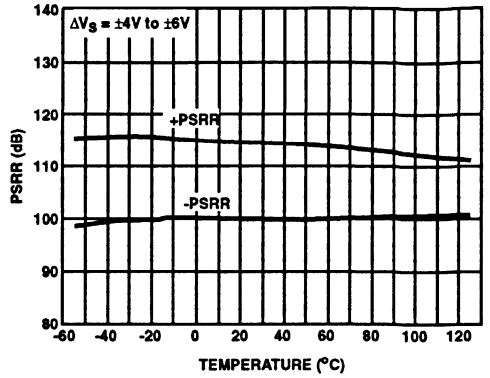


FIGURE 17. PSRR vs TEMPERATURE

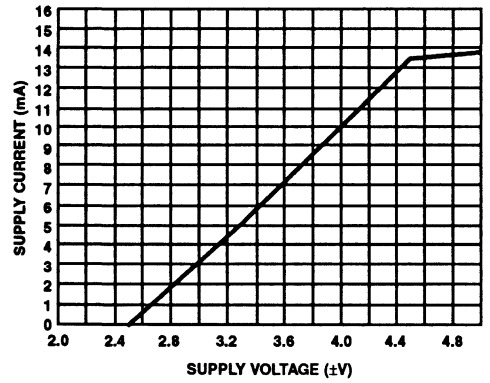


FIGURE 18. SUPPLY CURRENT vs SUPPLY VOLTAGE

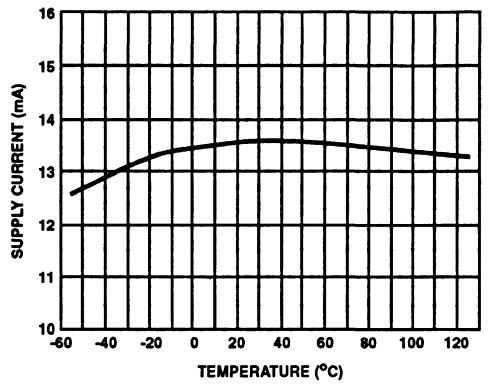


FIGURE 19. SUPPLY CURRENT vs TEMPERATURE

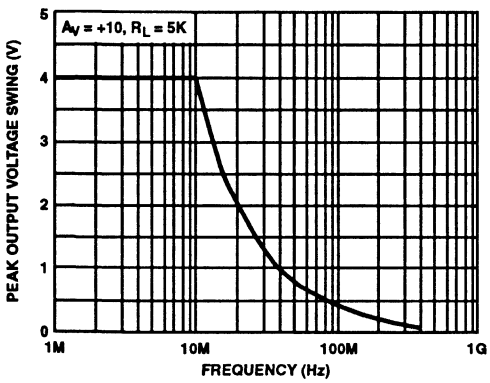


FIGURE 20. OUTPUT VOLTAGE SWING vs FREQUENCY

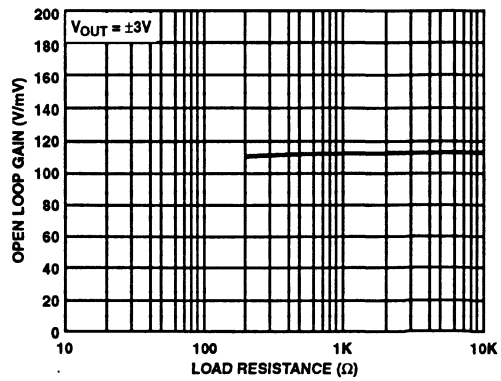


FIGURE 21. OPEN LOOP GAIN vs LOAD RESISTANCE

Typical Performance Curves $V_S = \pm5V$, $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

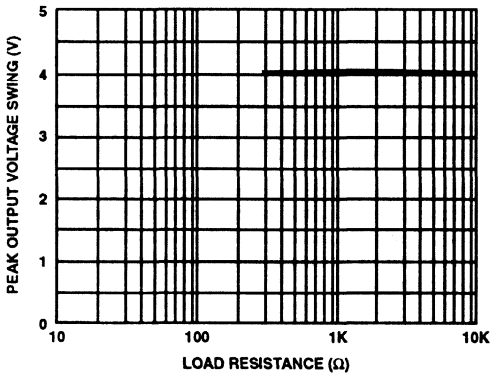


FIGURE 22. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

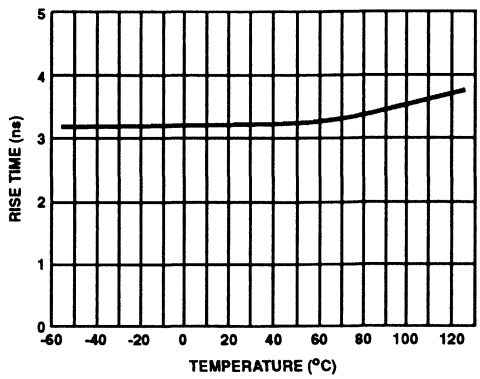


FIGURE 23. RISE TIME vs TEMPERATURE

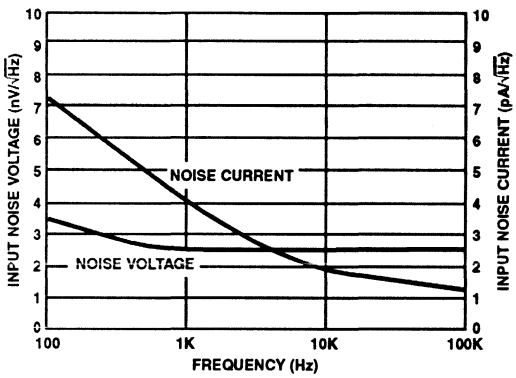


FIGURE 24. INPUT NOISE vs FREQUENCY

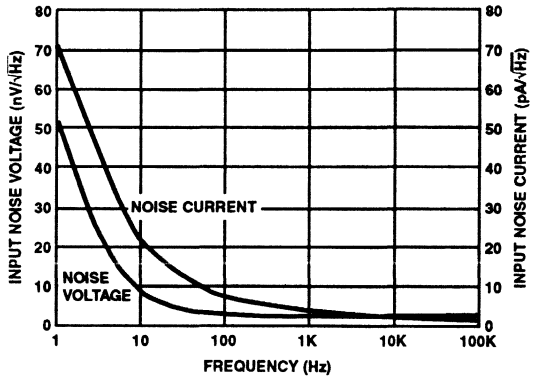


FIGURE 25. INPUT NOISE vs FREQUENCY

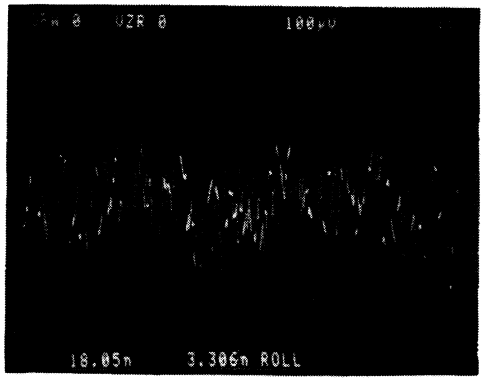


FIGURE 26. INPUT NOISE VOLTAGE
0.1Hz to 10Hz
$A_V = 25{,}000$, Noise Voltage = $3.31nV_{RMS}$ (RTI)

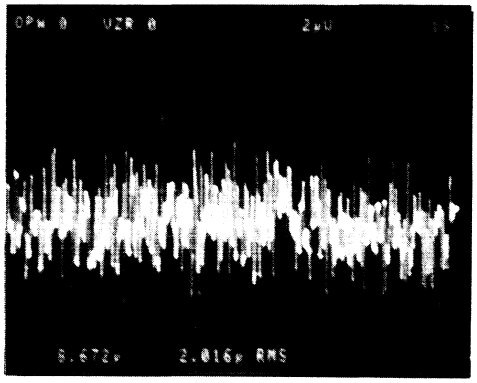


FIGURE 27. INPUT NOISE VOLTAGE
10Hz to 1MHz
$A_V = 500$, Noise Voltage = $2.02\mu V_{RMS}$ (RTI)

Applications Information

Offset Voltage Adjustment

The HFA-0002, due to its low offset voltage, will typically not require any external offset adjustment. If certain applications do require lower offset, the following diagram shows one possible configuration.

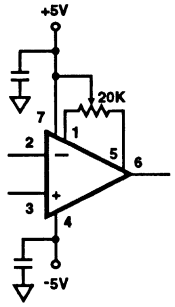


FIGURE 29.

The power supply lines must be well decoupled to filter any power supply noise. A 20K trim pot will allow an offset adjustment of about 3mV, referred to input.

PC Board Layout Guidelines

When designing with the HFA-0002, good high frequency (RF) techniques should be used when doing pc board layouts. A massive ground plane should be used to maintain a low impedance ground. PC board traces should be kept as short as possible and kept wide to minimize trace inductance and impedance. Stray capacitance at the op amps output and at the high impedance inputs should be kept to a minimum, to prevent any unwanted phase shift and bandwidth limiting.

When breadboarding remember to keep feedback resistor values low (≤5kΩ) for optimum performance. The use of metal film resistors for values over 200Ω and carbon film resistors under 200Ω typically gives the best performance. Remember to keep all lead lengths as short as possible to minimize lead inductance.

Sockets will add parasitic capacitance and inductance and therefore can limit AC performance as well as reduce stability. If sockets must be used, a low profile socket with minimum pin to pin capacitance will minimize any performance degradation.

Power supply decoupling is essential for high frequency op amps. A 0.01μF high quality ceramic capacitor at each supply pin in parallel with a 1μF tantalum capacitor will provide excellent decoupling. Chip capacitors produce the best results due to the ease of placement next to the op amp and they have negligible lead inductance. If leaded capacitors are used, again the lead lengths should be kept to a minimum.

Saturation Recovery

When an op amp is over driven output devices can saturate and sometime take a long time to recover. By clamping the input to safe levels, output saturation can be avoided. If output saturation cannot be avoided, the recovery time for an input sine wave at 25% overdrive is 100ns.

HARRIS SEMICONDUCTOR

HFA-0005

High Slew Rate Operational Amplifier

March 1993

Features

- Unity Gain Bandwidth 300MHz
- Full Power Bandwidth 22MHz
- High Slew Rate 420V/μs
- High Output Drive ..... ±50mA
- Monolithic Bipolar Construction

Applications

- RF/IF Processors
- Video Amplifiers
- Radar Systems
- Pulse Amplifiers
- High Speed Communications
- Fast Data Acquisition Systems

Description

The HFA-0005 is an all bipolar op amp featuring high slew rate (420V/μs), and high unity gain bandwidth (300MHz). These features combined with fast settling time (20ns) make this product very useful in high speed data acquisition systems as well as RF, video, and pulse amplifier designs.

Other outstanding characteristics include low bias currents (15μA), low offset current (6μA), and low offset voltage (6mV). These high performance characteristics are achieved with only 40mA of supply current.

The HFA-0005 offers high performance at low cost. It can replace hybrids and RF transistor amplifiers, simplifying designs while providing increased reliability due to monolithic construction. To enhance the ease of design, the HFA-0005 has a 50Ω ±20% resistor connected from the output of the op amp to a separate pin. This can be used when driving 50Ω strip line, microstrip, or coax cable.

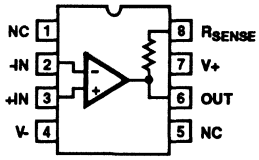
For MIL-STD-883 compliant product consult the HFA-0005/883 datasheet.

Ordering Information

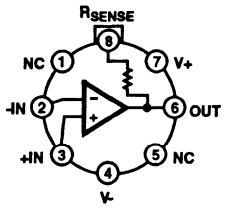
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA2-0005-5	0°C to +75°C	8 Pin Can
HFA2-0005-9	-40°C to +85°C	8 Pin Can
HFA3-0005-5	0°C to +75°C	8 Lead Plastic DIP
HFA3-0005-9	-40°C to +85°C	8 Lead Plastic DIP
HFA7-0005-5	0°C to +75°C	8 Lead Ceramic Sidebraze DIP
HFA7-0005-9	-40°C to +85°C	8 Lead Ceramic Sidebraze DIP
HFA9P0005-5	0°C to +75°C	8 Lead SOIC
HFA9P0005-9	-40°C to +85°C	8 Lead SOIC

Pinouts

HFA-0005 (PDIP, CDIP, SOIC)
TOP VIEW



HFA-0005 (TO-99 METAL CAN)
TOP VIEW



OPERATIONAL AMPLIFIERS

File Number **2918.1**

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 12V
Differential Input Voltage 5V
Input Voltage ..... ±4V
Output Current ..... ±60mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Packages) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... 300°C

Operating Conditions

Operating Temperature Range
HFA-0005-9 ..... $-40°C \le T_A \le +85°C$
HFA-0005-5 ..... $0°C \le T_A \le +75°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +5V, V- = -5V, Unless Otherwise Specified

PARAMETERS	TEMP	HFA-0005-9			HFA-0005-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	6	15	-	6	30	mV
	Full	-	11	45	-	11	35	mV
Average Offset Voltage Drift	Full	-	100	-	-	100	-	µV/°C
Bias Current	+25°C	-	15	50	-	15	100	µA
	Full	-	20	50	-	20	100	µA
Offset Current	+25°C	-	6	25	-	6	50	µA
	Full	-	12	50	-	12	50	µA
Common Mode Range	Full	±3	-	-	±3	-	-	V
Differential Input Resistance	+25°C	-	10	-	-	10	-	kΩ
Input Capacitance	+25°C	-	2	-	-	2	-	pF
Input Noise Voltage								
0.1Hz to 10Hz	+25°C	-	2.5	-	-	2.5	-	μV_{RMS}
10Hz to 1MHz	+25°C	-	5.8	-	-	5.8	-	μV_{RMS}
Input Noise Voltage								
f_O = 10Hz	+25°C	-	450	-	-	450	-	$nV/\sqrt{Hz}$
f_O = 100Hz	+25°C	-	160	-	-	160	-	$nV/\sqrt{Hz}$
f_O = 100kHz	+25°C	-	5	-	-	5	-	$nV/\sqrt{Hz}$
Input Noise Current								
f_O = 10Hz	+25°C	-	2.0	-	-	2.0	-	$nA/\sqrt{Hz}$
f_O = 100Hz	+25°C	-	0.57	-	-	0.57	-	$nA/\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	0.11	-	-	0.11	-	$nA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 2)	+25°C	150	230	-	150	230	-	V/V
	High	150	180	-	150	180	-	V/V
	Low	150	250	-	150	250	-	V/V
Common Mode Rejection Ratio (Note 3)	Full	45	47	-	42	45	-	dB
Unity Gain Bandwidth	+25°C	-	300	-	-	300	-	MHz
Minimum Stable Gain	Full	1	-	-	1	-	-	V/V
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
R_L = 100Ω	+25°C	-	±3.5	-	-	±3.5	-	V
R_L = 1kΩ	Full	±3.5	±4.0	-	±3.5	±4.0	-	V
Full Power Bandwidth (Note 5)	+25°C	-	22	-	-	22	-	MHz
Output Resistance, Open Loop	+25°C	-	3.0	-	-	3.0	-	Ω
Output Current	Full	±25	±50	-	±25	±50	-	mA

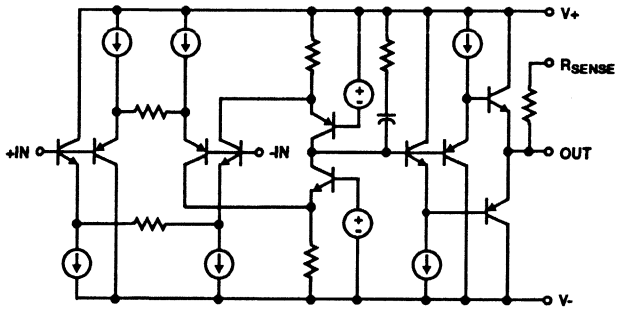
Electrical Specifications V+ = +5V, V- = -5V, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEMP	HFA-0005-9			HFA-0005-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE								
Rise Time (Note 4, 6)	+25°C	-	480	-	-	480	-	ps
Slew Rate (Note 7)	+25°C	-	420	-	-	420	-	V/µs
Settling Time (3V Step) 0.1%	+25°C	-	20	-	-	20	-	ns
Overshoot (Note 4, 6)	+25°C	-	30	-	-	30	-	%
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	35	40	-	35	40	mA
	Full	-	37	40	-	37	45	mA
Power Supply Rejection Ratio (Note 8)	+25°C	40	42	-	37	40	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = 0 to ±2V, R_L = 1kΩ.
3. ΔV_{CM} = ±2V.
4. R_L = 100Ω.
5. Full Power Bandwidth is calculated by equation: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$, V_{PEAK} = 3.0V.
6. V_{OUT} = ±200mV, A_V = +1.
7. V_{OUT} = ±3V, A_V = +1.
8. ΔV_S = ±4V to ±6V.
9. See Thermal Constants in "Applications Information" section. Maximum power dissipation, including output load, must be designed to maintain the junction temperature below +175°C for hermetic packages, and below +150°C for plastic packages.

Simplified Schematic Diagram



Die Characteristics

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
CAN	120	37
PDIP	98	36
CDIP	75	13
SOIC	158	43

Test Circuits

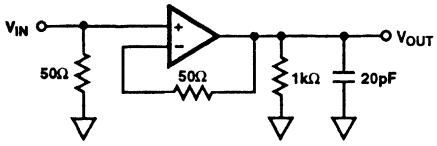


FIGURE 1. LARGE SIGNAL RESPONSE TEST CIRCUIT

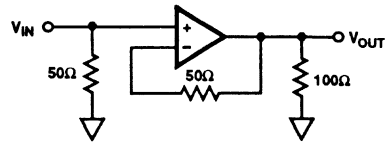
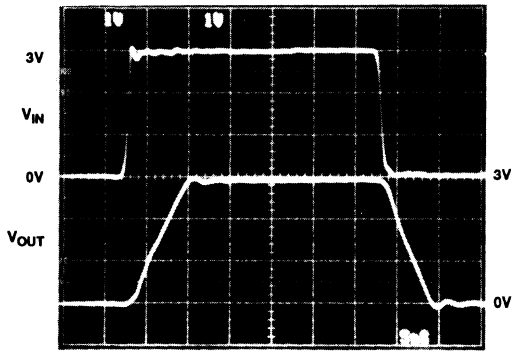


FIGURE 2. SMALL SIGNAL RESPONSE TEST CIRCUIT

LARGE SIGNAL RESPONSE

V_{OUT} = 0 to 3V

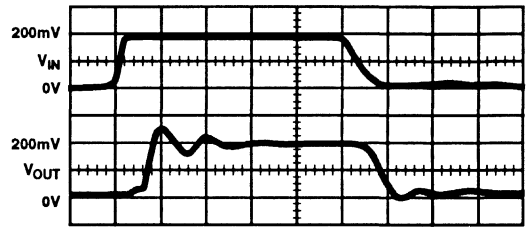
Vertical Scale: 1V/Div. Horizontal Scale: 5ns/Div.



SMALL SIGNAL RESPONSE

V_{OUT} = 0 to 200mV

Vertical Scale: 100mV/Div. Horizontal Scale: 2ns/Div.

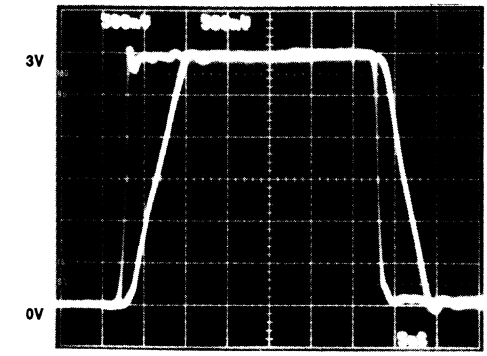


NOTE: Initial step in output is due to fixture feedthrough

PROPAGATION DELAY

Vertical Scale: 500mV/Div. Horizontal Scale: 5ns/Div.

A_V = +1, R_L = 1kΩ, V_{OUT} = 0 to 3V



NOTE: Test fixture delay of 450ps is included

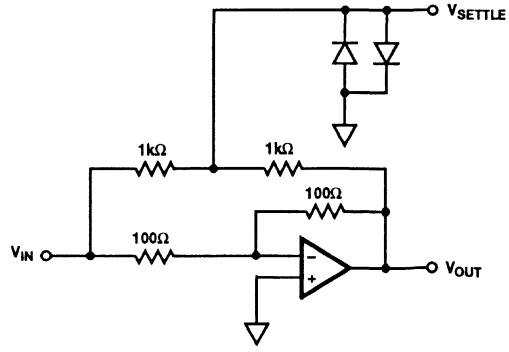


FIGURE 3. SETTLING TIME SCHEMATIC

Typical Performance Curves $V_S = \pm5V$, $T_A = +25°C$, Unless Otherwise Specified

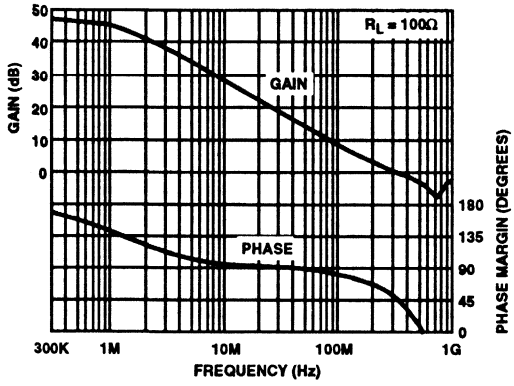


FIGURE 4. OPEN LOOP GAIN AND PHASE vs FREQUENCY

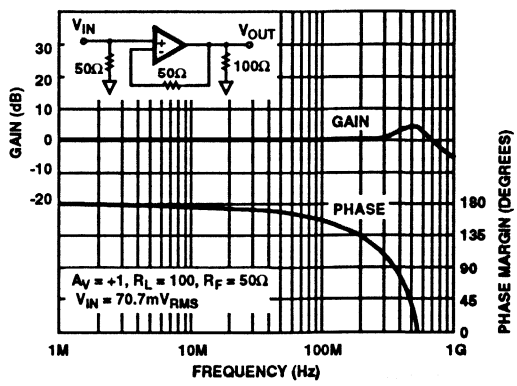


FIGURE 5. CLOSED LOOP GAIN vs FREQUENCY

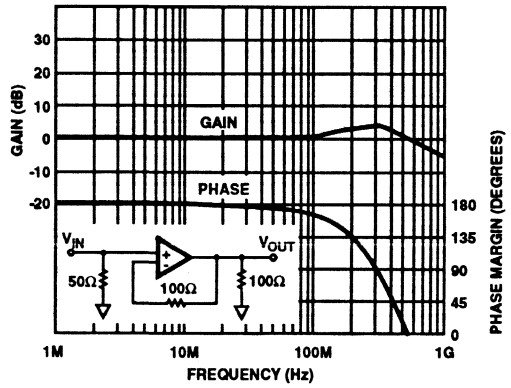


FIGURE 6. CLOSED LOOP GAIN vs FREQUENCY

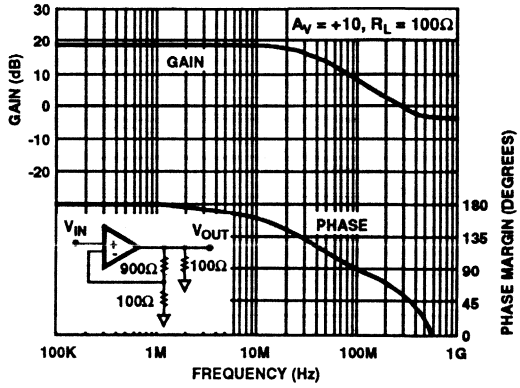


FIGURE 7. CLOSED LOOP GAIN vs FREQUENCY

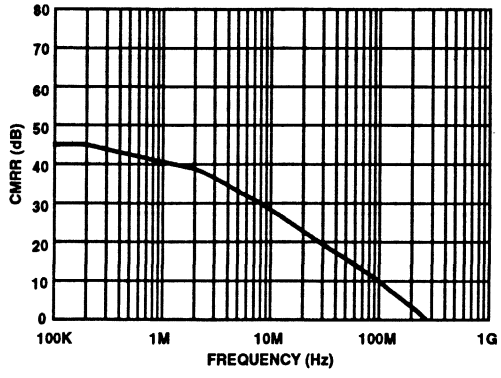


FIGURE 8. CMRR vs FREQUENCY

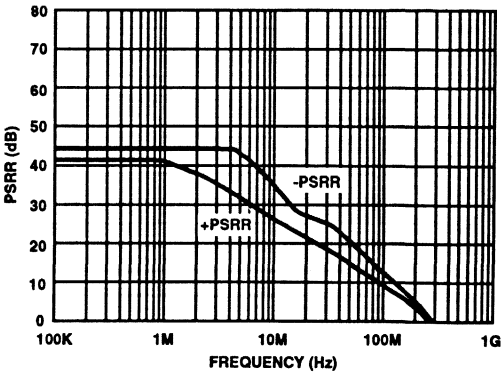


FIGURE 9. PSRR vs FREQUENCY

Typical Performance Curves $V_S = \pm5V$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

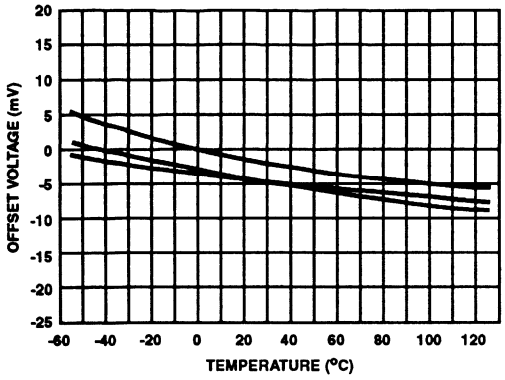


FIGURE 10. OFFSET VOLTAGE vs TEMPERATURE (3 REPRESENTATIVE UNITS)

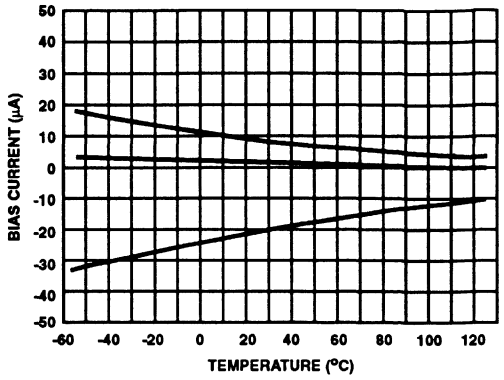


FIGURE 11. BIAS CURRENT vs TEMPERATURE (3 REPRESENTATIVE UNITS)

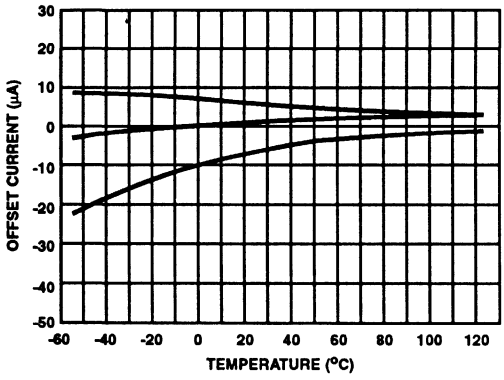


FIGURE 12. OFFSET CURRENT vs TEMPERATURE (3 REPRESENTATIVE UNITS)

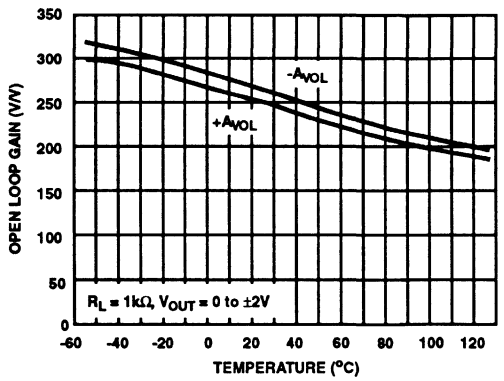


FIGURE 13. OPEN LOOP GAIN vs TEMPERATURE

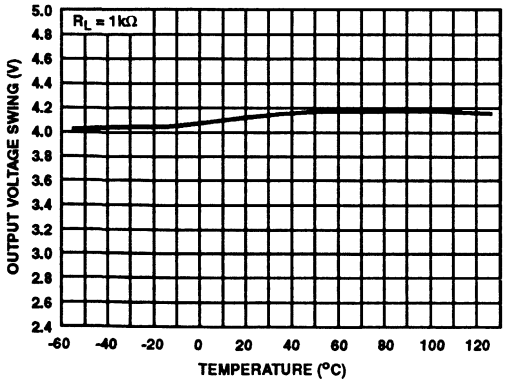


FIGURE 14. OUTPUT VOLTAGE SWING vs TEMPERATURE

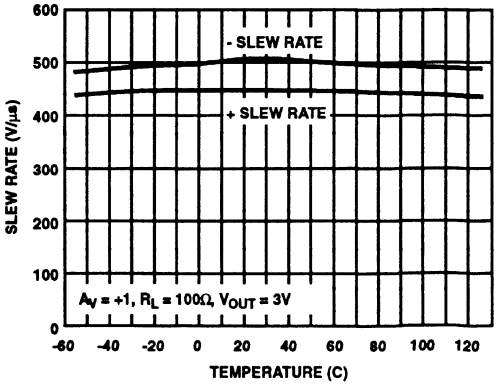


FIGURE 15. SLEW RATE vs TEMPERATURE

Typical Performance Curves $V_S = \pm5V$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

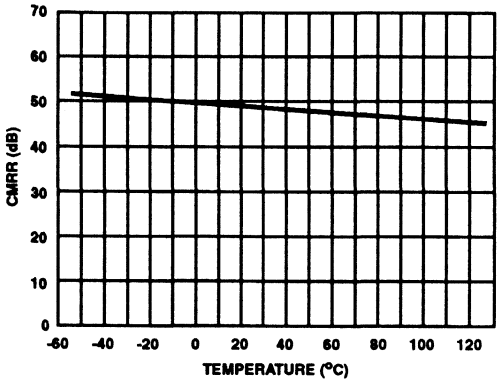


FIGURE 16. CMRR vs TEMPERATURE

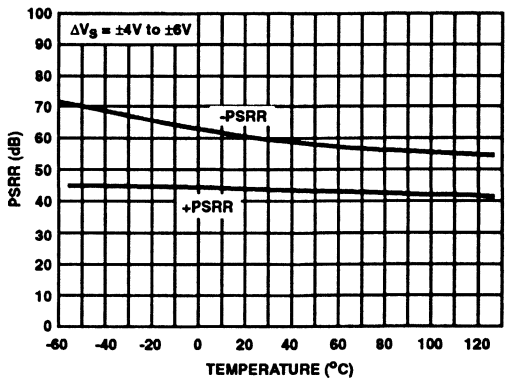


FIGURE 17. PSRR vs TEMPERATURE

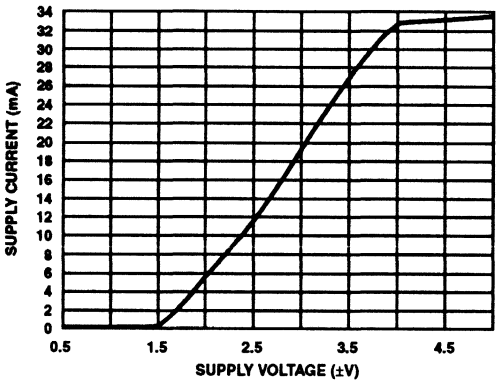


FIGURE 18. SUPPLY CURRENT vs SUPPLY VOLTAGE

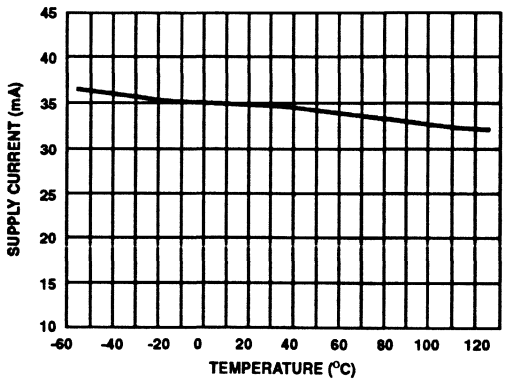


FIGURE 19. SUPPLY CURRENT vs TEMPERATURE

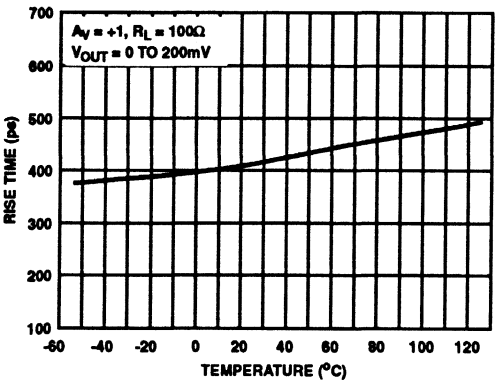


FIGURE 20. RISE TIME vs TEMPERATURE

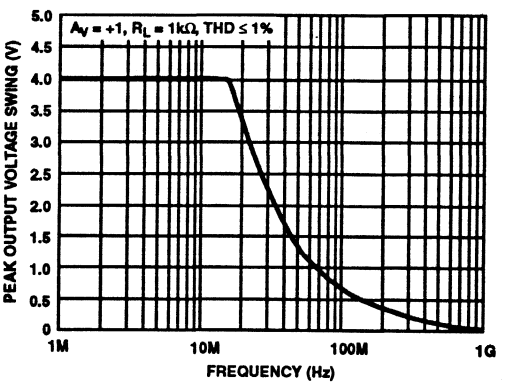


FIGURE 21. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

Typical Performance Curves $V_S = \pm5V$, $T_A = +25°C$, Unless Otherwise Specified (Continued)

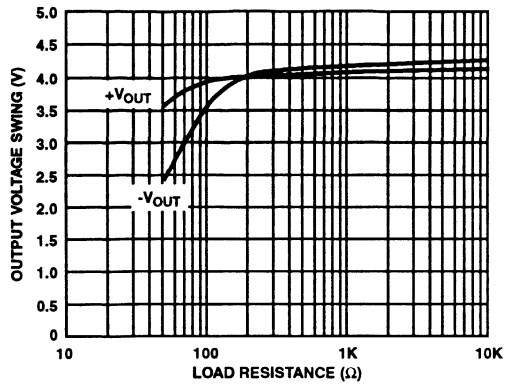


FIGURE 22. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

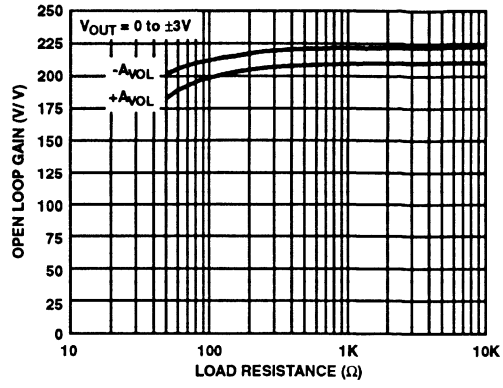


FIGURE 23. OPEN LOOP GAIN vs LOAD RESISTANCE

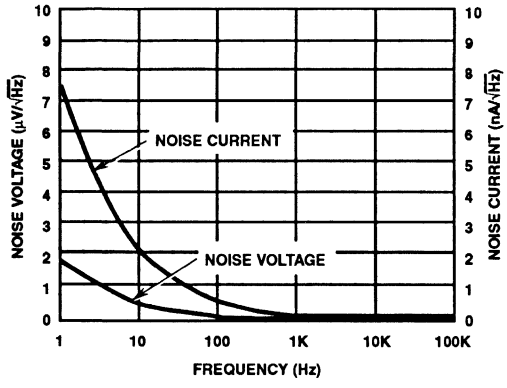


FIGURE 24. INPUT NOISE vs FREQUENCY

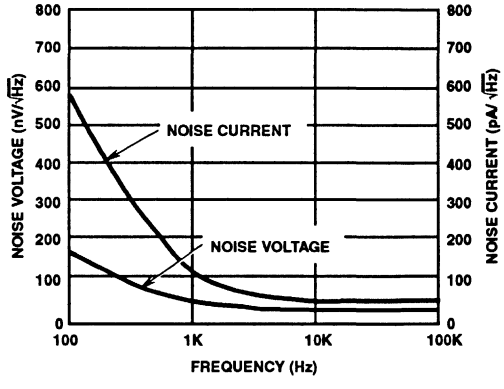


FIGURE 25. INPUT NOISE vs FREQUENCY

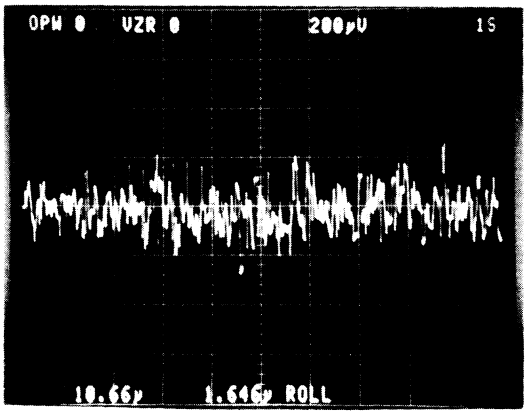


FIGURE 26. INPUT NOISE VOLTAGE
$A_V = 50$, Noise Voltage = $1.646\mu V_{RMS}$ (RTI)

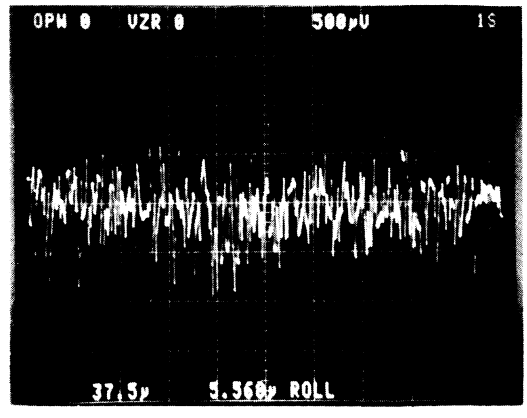
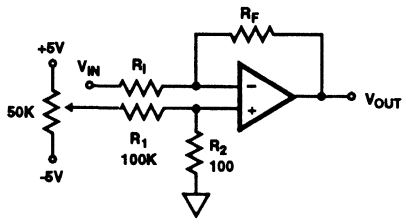


FIGURE 27. INPUT NOISE VOLTAGE
$A_V = 50$, Noise Voltage = $5.568\mu V_{RMS}$ (RTI)

Applications Information

Offset Adjustment

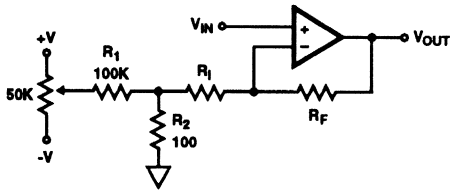
When applications require the offset voltage to be as low as possible, the figure below shows two possible schemes for adjusting offset voltage.



$$\text{Adjustment Range} \cong \pm V \left(\frac{R_2}{R_1}\right)$$

FIGURE 28. INVERTING GAIN

For a voltage follower application, use the circuit in Figure 29 without R_2 and with R_I shorted. R_1 should then be 1MΩ to 10MΩ, so the adjustment resistors will cause only a very small gain error.



$$\text{Adjustment Range} \cong \pm V \left(\frac{R_2}{R_1}\right) \quad \text{Gain} \cong 1 + \left(\frac{R_F}{R_I + R_2}\right)$$

FIGURE 29. NON-INVERTING GAIN

PC Board Layout Guidelines

When designing with the HFA-0005, good high frequency (RF) techniques should be used when making a PC board. A massive ground plane should be used to maintain a low impedance ground. Proper shielding and use of short interconnection leads are also very important.

To achieve maximum high frequency performance, the use of low impedance transmission lines with impedance matching is recommended: 50Ω lines are common in communications and 75Ω lines in video systems. Impedance matching is important to minimize reflected energy therefore minimizing transmitted signal distortion. This is accomplished by using a series matching resistor (50Ω or 75Ω), matched transmission line (50Ω or 75Ω), and a matched terminating resistor, as shown in Figure 30. Note that there will be a 6dB loss from input to output. The HFA-0005 has an integral 50Ω ±20% resistor connected to the op amp's output with the other end of the resistor pinned out. This 50Ω resistor can be used as the series resistor instead of an external resistor.

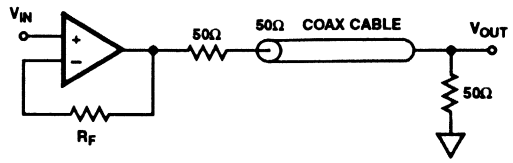


FIGURE 30.

PC board traces can be made to look like a 50Ω or 75Ω transmission line, called microstrip. Microstrip is a PC board trace with a ground plane directly beneath, on the opposite side of the board, as shown in Figure 31.

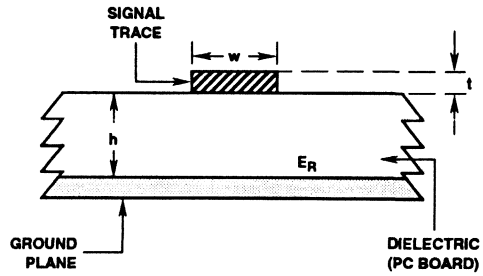


FIGURE 31.

When manufacturing pc boards the trace width can be calculated based on a number of variables.

The following equation is reasonably accurate for calculating the proper trace width for a 50Ω transmission line.

$$Z_0 = \frac{87}{\sqrt{E_R + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \Omega$$

Power supply decoupling is essential for high frequency op amps. A 0.01µF high quality ceramic capacitor at each supply pin in parallel with a 1µF tantalum capacitor will provide excellent decoupling. Chip capacitors produce the best results due to ease of placement next to the op amp and they have negligible lead inductance. If leaded capacitors are used, the leads should be kept as short as possible to minimize lead inductance. The figures that follow illustrate two different decoupling schemes. Figure 33 improves the PSRR because the resistor and capacitors create low pass filters. Note that the supply current will create a voltage drop across the resistor.

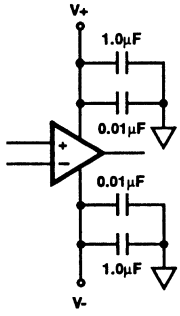


FIGURE 32.

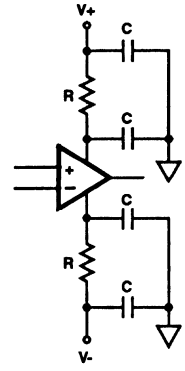


FIGURE 33.

Saturation Recovery

When an op amp is over driven output devices can saturate and sometimes take a long time to recover. By clamping the input to safe levels, output saturation can be avoided. If output saturation cannot be avoided, the recovery time from 25% overdrive is 20ns and 30ns from 50% overdrive.

HARRIS SEMICONDUCTOR

HFA1100
HFA1120

Ultra High-Speed Current Feedback Amplifiers

April 1993

Features

- Low Distortion (30MHz).....-56dBc
- -3dB Bandwidth.....850MHz
- Very Fast Slew Rate.....2300V/μs
- Fast Settling Time (0.1%).....11ns
- Excellent Gain Flatness
  - (100MHz).....0.14dB
  - (50MHz).....0.04dB
  - (30MHz).....0.01dB
- High Output Current.....60mA
- Overdrive Recovery.....<10ns

Applications

- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems

Description

The HFA1100, 1120 are a family of high-speed, wideband, fast settling current feedback amplifiers. Built with Harris' proprietary complementary bipolar UHF-1 process, these devices are the fastest monolithic amplifiers available from any semiconductor manufacturer.

The two devices, available in 8-pin CERDIP, PDIP, and SOIC packages, have similar performance, but each offers separate features.

The HFA1100 is a basic op amp with uncommitted pins 1, 5, and 8. The HFA1120 includes inverting input bias current adjust pins (pins 1 and 5) for adjusting the output offset voltage.

These devices offer a significant performance improvement over the AD811, AD9617/18, the CLC400-409, and the EL2070, EL2073, EL2030.

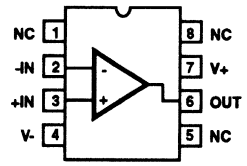
For Military grade product refer to the HFA1100/883, HFA1120/883 data sheet.

Ordering Information

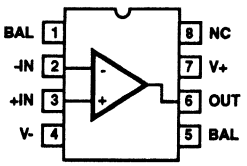
PART NUMBER	OPERATING TEMP RANGE	PRODUCT DESCRIPTION
HFA1100MJ, HFA1120MJ/883	-55°C to +125°C	8 Lead Ceramic DIP
HFA1100IJ, HFA1120IJ	-40°C to +85°C	8 Lead Ceramic DIP
HFA1100IP, HFA1120IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1100IB, HFA1120IB	-40°C to +85°C	8 Lead SOIC
HFA1100Y, HFA1120Y	-40°C to +85°C	Die

Pinouts

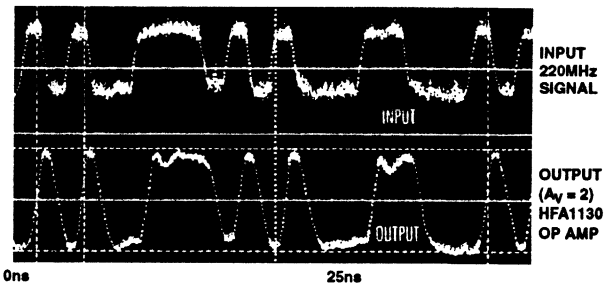
HFA1100
(PDIP, CDIP, SOIC)
TOP VIEW



HFA1120
(PDIP, CDIP, SOIC)
TOP VIEW



The Op Amps With Fastest Edges



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2945.3**

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Common Mode Voltage ..... V_{SUPPLY}
Differential Input Voltage 5V
Output Current (50% Duty Cycle) 60mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C

Operating Conditions

HFA1100I, HFA1120I ..... -40°C ≤ T_A ≤ +85°C.
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

Thermal Package Characteristics (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP Package	116	36
Plastic DIP Package	98	36
SOIC Package	158	43

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEMP	HFA1100I, HFA1120I MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Input Offset Voltage *	+25°C	-	2	6	mV
	Full	-	-	10	mV
Input Offset Voltage Drift	Full	-	10	-	µV/°C
V_{IO} CMRR (ΔV_{CM} = ±2V)	+25°C	40	46	-	dB
	Full	38	-	-	dB
V_{IO} PSRR (ΔV_S = ±1.25V)	+25°C	45	50	-	dB
	Full	42	-	-	dB
Non-Inv. Input Bias Current (+IN = 0V) *	+25°C	-	25	40	µA
	Full	-	-	65	µA
$+I_{BIAS}$ Drift	Full	-	40	-	nA/°C
$+I_{BIAS}$ CMS (ΔV_{CM} = ±2V)	+25°C	-	20	40	µA/V
	Full	-	-	50	µA/V
Inv. Input Bias Current (-IN = 0V) *	+25°C	-	12	50	µA
	Full	-	-	60	µA
$-I_{BIAS}$ Drift	Full	-	40	-	nA/°C
$-I_{BIAS}$ CMS (ΔV_{CM} = ±2V)	+25°C	-	1	7	µA/V
	Full	-	-	10	µA/V
$-I_{BIAS}$ PSS	+25°C	-	6	15	µA/V
	Full	-	-	27	µA/V
$-I_{BIAS}$ Adj. Range (HFA1120)	+25°C	±100	±200	-	µA
Non-Inv. Input Resistance	+25°C	25	50	-	kΩ
Inv. Input Resistance	+25°C	-	16	30	Ω
Input Capacitance (either input)	+25°C	-	2	-	pF
Input Common Mode Range	Full	±2.5	±3.0	-	V
Input Voltage Noise (100kHz) *	+25°C	-	4	-	$nV/\sqrt{Hz}$
+Input Current Noise (100kHz) *	+25°C	-	18	-	$pA/\sqrt{Hz}$
-Input Current Noise (100kHz) *	+25°C	-	21	-	$pA/\sqrt{Hz}$

*See Typical Performance Curves for more information.

Electrical Characteristics V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	HFA1100I, HFA1120I MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS A_V = +2, Unless Otherwise Specified					
Open Loop Transimpedance	+25°C	-	500	-	kΩ
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, A_V = +1) *	+25°C	530	850	-	MHz
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, A_V = +2, R_F = 360Ω)	+25°C	-	670	-	MHz
Gain Flatness (to 100MHz) *	+25°C	-	±0.14	-	dB
Gain Flatness (to 50MHz)	+25°C	-	±0.04	-	dB
Gain Flatness (to 30MHz)	+25°C	-	±0.01	-	dB
Linear Phase Deviation (DC to 100MHz) *	+25°C	-	0.6	-	Degrees
Differential Gain (NTSC, R_L = 75Ω)	+25°C	-	0.03	-	%
Differential Phase (NTSC, R_L = 75Ω)	+25°C	-	0.05	-	Degrees
Minimum Stable Gain	Full	1	-	-	V/V
OUTPUT CHARACTERISTICS A_V = +2, Unless Otherwise Specified					
Output Voltage (A_V = -1) *	+25°C	±3.0	±3.3	-	V
	Full	±2.5	±3.0	-	V
Output Current (R_L = 50Ω, A_V = -1)	+25°C, +85°C	50	65	-	mA
	-40°C	35	50	-	mA
DC Closed Loop Output Impedance	+25°C	-	0.1	-	Ω
2nd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P}) *	+25°C	-	-56	-	dBc
3rd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P}) *	+25°C	-	-80	-	dBc
3rd Order Intercept (100MHz) *	+25°C	20	30	-	dBm
1dB Compression (100MHz)	+25°C	15	20	-	dBm
TRANSIENT RESPONSE A_V = +2, Unless Otherwise Specified					
Rise Time (V_{OUT} = 2.0V Step)	+25°C	-	900	-	ps
Overshoot (V_{OUT} = 2.0V Step) *	+25°C	-	10	-	%
Slew Rate (A_V = +1, V_{OUT} = 5V_{P-P})	+25°C	-	1400	-	V/µs
Slew Rate (A_V = +2, V_{OUT} = 5V_{P-P})	+25°C	1950	2300	-	V/µs
0.1% Settling (V_{OUT} = 2V to 0V) *	+25°C	-	11	-	ns
0.2% Settling (V_{OUT} = 2V to 0V) *	+25°C	-	7	-	ns
Overdrive Recovery Time (2X Overdrive)	+25°C	-	7.5	10	ns
POWER SUPPLY CHARACTERISTICS					
Supply Voltage Range	Full	±4.5	-	±5.5	V
Supply Current *	+25°C	-	21	26	mA
	Full	-	-	33	mA

*See Typical Performance Curves for more information.

Application Information

Optimum Feedback Resistor (R_F)

The enclosed plots of inverting and non-inverting frequency response detail the performance of the HFA1100/1120 in various gains. Although the bandwidth dependency on A_{CL} isn't as severe as that of a voltage feedback amplifier, there is an appreciable decrease in bandwidth at higher gains. This decrease can be minimized by taking advantage of the current feedback (CFB) amplifier's unique property of bandwidth dependency on R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications The R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1100, 1120 designs are optimized for a 510Ω R_F, at a gain of +1. Decreasing R_F in a unity gain application decreases stability, leading to excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of bandwidth vs. stability. The table below lists recommended R_F values for various gains, and the expected bandwidth.

A_{CL}	R_F (Ω)	BW (MHz)
+1	510	850
-1	430	580
+2	360	670
+5	150	520
+10	180	240
+19	270	125

Offset Adjustment

The HFA1120 allows for adjustment of the inverting input bias current to null the output offset voltage. $-I_{BIAS}$ flows through R_F, so any change in bias current forces a corresponding change in output voltage. The amount of adjustment is a function of R_F . With R_F = 510Ω, the typical adjust range is ±100mV. For offset adjustment connect a 10KΩ potentiometer between pins 1 and 5 with the wiper connected to V-.

Use of Die in Hybrid Applications

These amplifiers are designed with compensation to negate the package parasitics that typically lead to instabilities. As a result, the use of die in hybrid applications results in overcompensated performance due to lower parasitic capacitances. Reducing R_F below the recommended values for packaged units will solve the problem. For A_V = +2 the recommended starting point is 300Ω, while unity gain applications should try 400Ω.

PC Board Layout

The frequency performance of these amplifiers depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value chip (0.1μF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

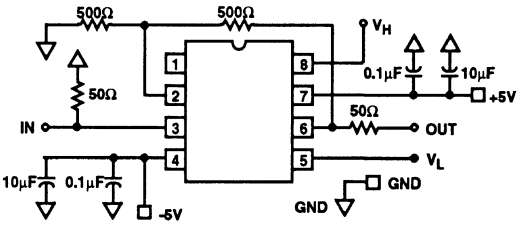
Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown below.

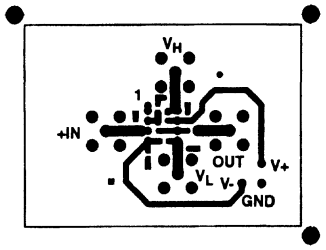
Evaluation Board

An evaluation board is available for the HFA1100. Please contact your local sales office for information.

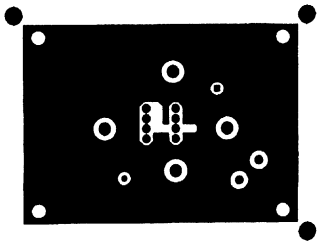
The layout and schematic of the board are shown below:



TOP LAYOUT



BOTTOM LAYOUT



Die Characteristics

DIE DIMENSIONS:
63 x 44 x 19 ± 1mils
1600µm x 1130µm ±25.4µm

METALLIZATION:
Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu (2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC
Gold Eutectic - Ceramic DIP

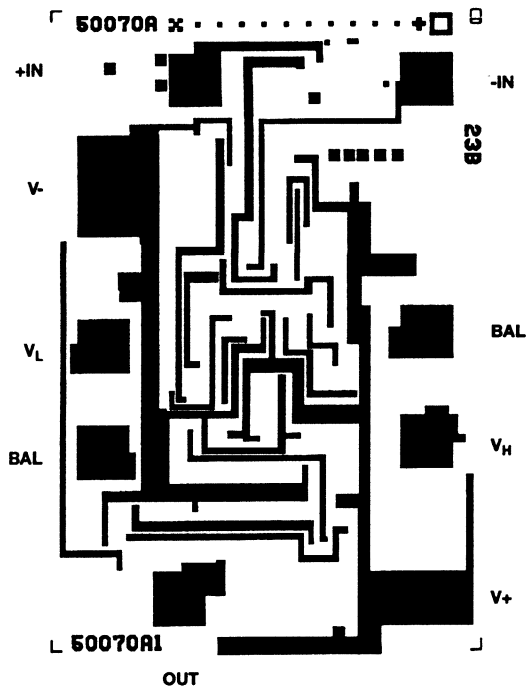
WORST CASE CURRENT DENSITY:
0.909×10^5 A/cm^2

TRANSISTOR COUNT: 52

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1100, HFA1120



Typical Performance Curves V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = +25°C, R_L = 100Ω Unless Otherwise Specified.

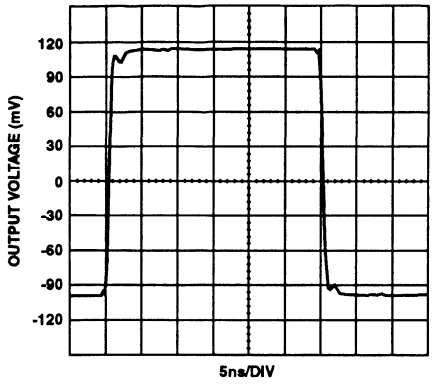


FIGURE 1. SMALL SIGNAL PULSE (A_V = +2)

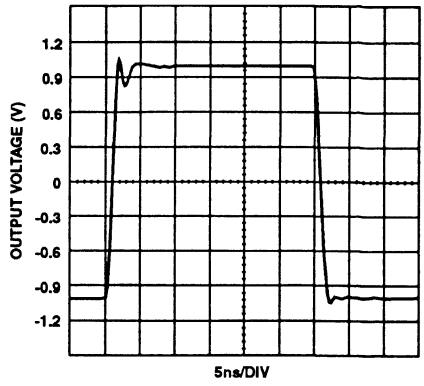


FIGURE 2. LARGE SIGNAL PULSE (A_V = +2)

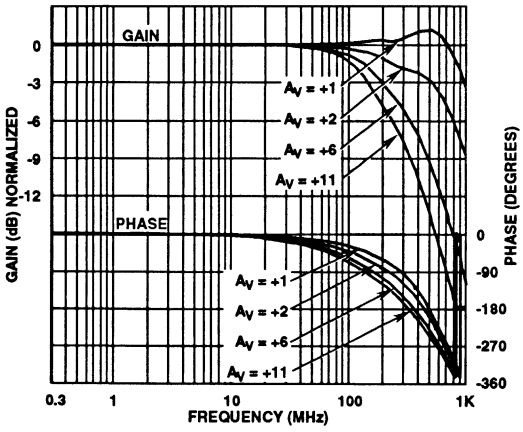


FIGURE 3. NON-INVERTING FREQUENCY RESPONSE (V_{OUT} = 200mV$_{P-P}$)

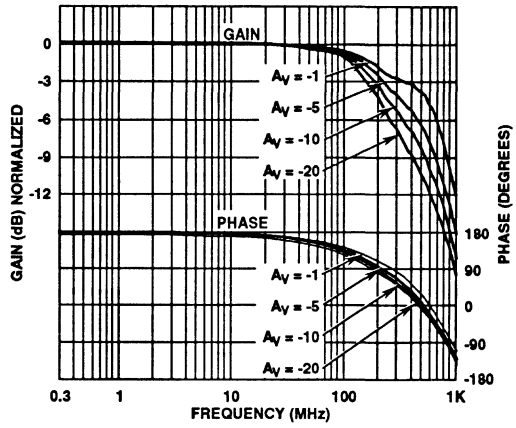


FIGURE 4. INVERTING FREQUENCY RESPONSE (V_{OUT} = 200mV$_{P-P}$)

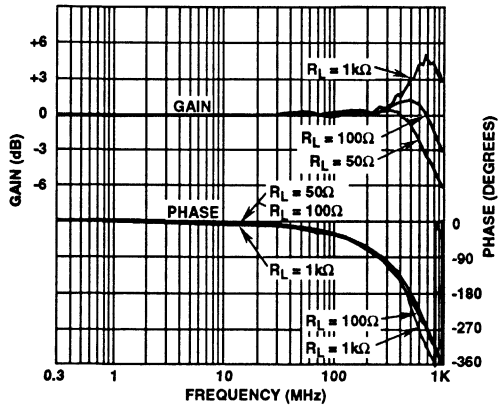


FIGURE 5. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS (A_V = +1, V_{OUT} = 200mV$_{P-P}$)

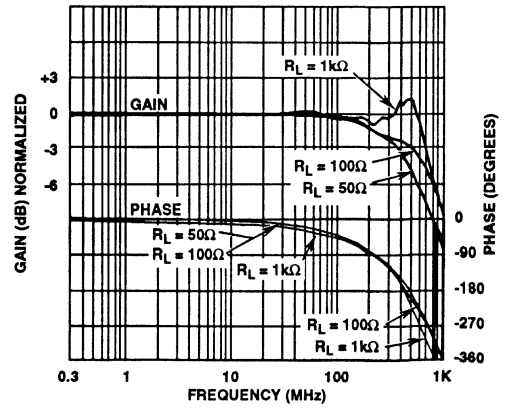


FIGURE 6. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS (A_V = +2, V_{OUT} = 200mV$_{P-P}$)

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25°C$, $R_L = 100\Omega$ Unless Otherwise Specified. (Continued)

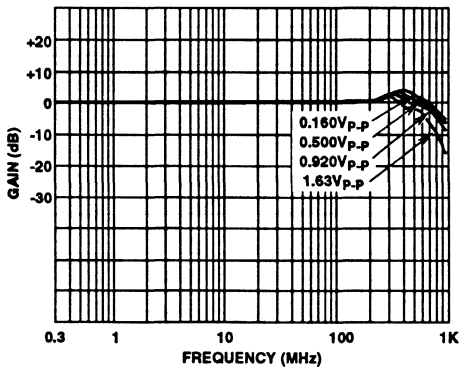


FIGURE 7. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES ($A_V = +1$)

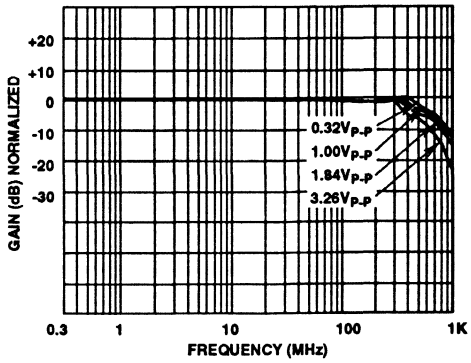


FIGURE 8. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES ($A_V = +2$)

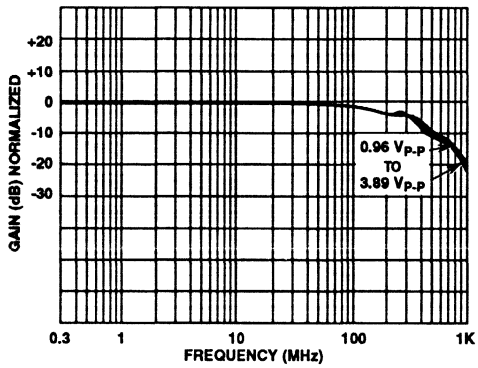


FIGURE 9. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES ($A_V = +6$)

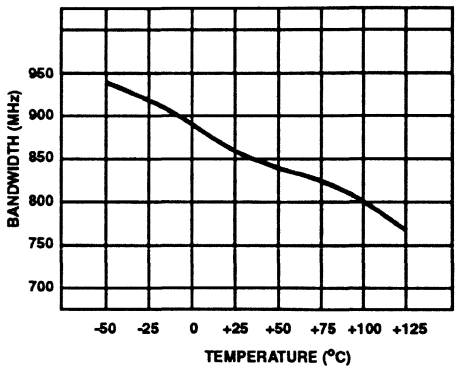


FIGURE 10. -3dB BANDWIDTH vs TEMPERATURE ($A_V = +1$)

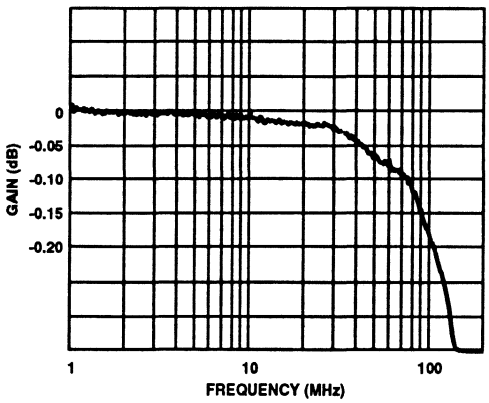


FIGURE 11. GAIN FLATNESS ($A_V = +2$)

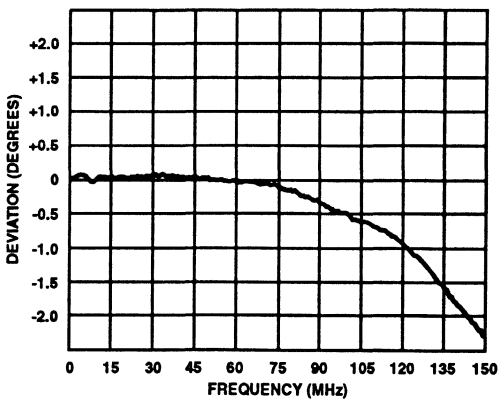


FIGURE 12. DEVIATION FROM LINEAR PHASE ($A_V = +2$)

Typical Performance Curves V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = +25°C, R_L = 100Ω Unless Otherwise Specified. (Continued)

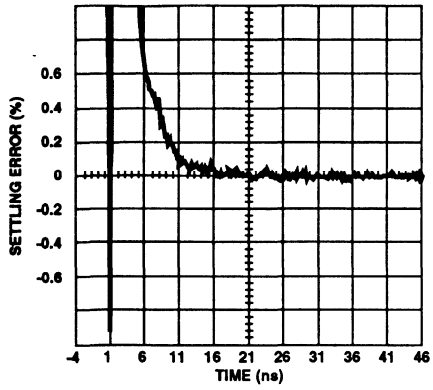


FIGURE 13. SETTLING RESPONSE (A_V = +2, V_{OUT} = 2V)

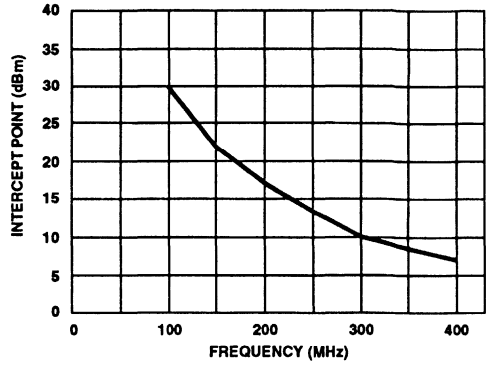


FIGURE 14. 3rd ORDER INTERMODULATION INTERCEPT (2-TONE)

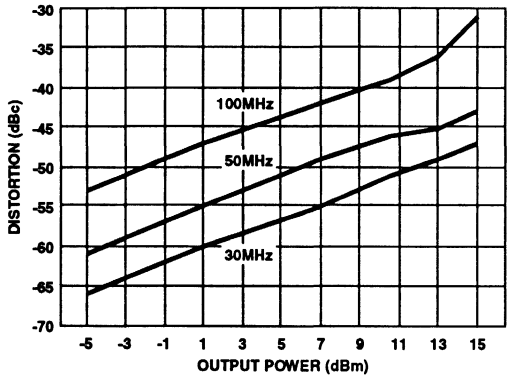


FIGURE 15. 2nd HARMONIC DISTORTION vs P_{OUT}

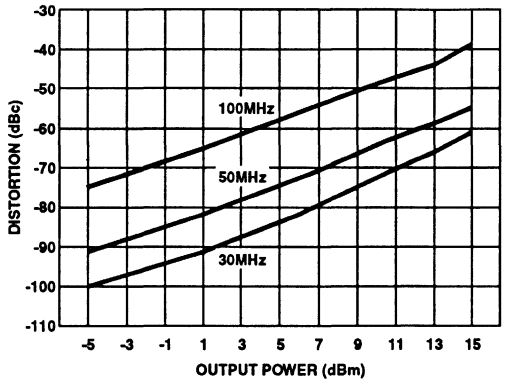


FIGURE 16. 3rd HARMONIC DISTORTION vs P_{OUT}

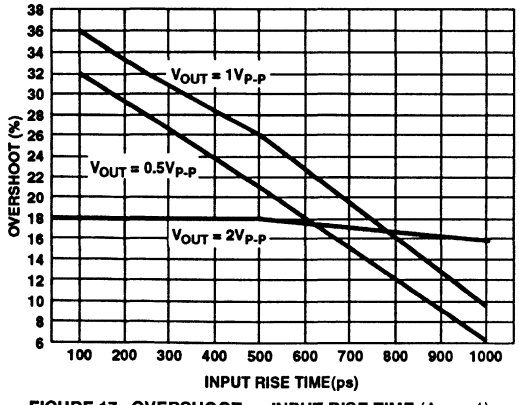


FIGURE 17. OVERSHOOT vs INPUT RISE TIME (A_V = +1)

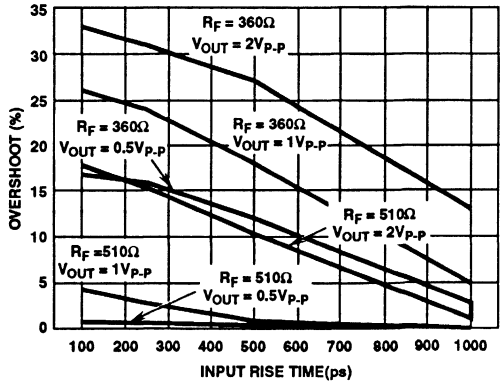


FIGURE 18. OVERSHOOT vs INPUT RISE TIME (A_V = +2)

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25°C$, $R_L = 100\Omega$ Unless Otherwise Specified. (Continued)

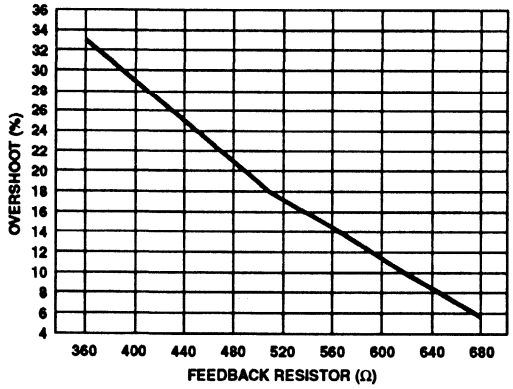


FIGURE 19. OVERSHOOT vs FEEDBACK RESISTOR ($A_V = +2$, $t_r = 200ps$, $V_{OUT} = 2V_{PP}$)

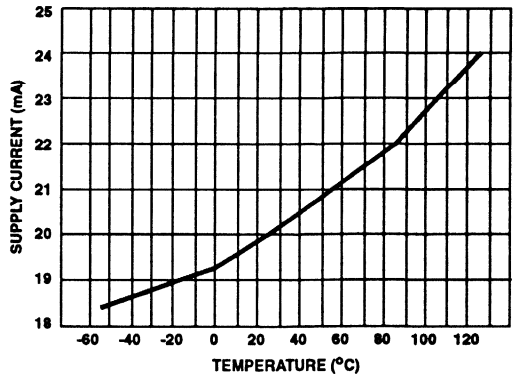


FIGURE 20. SUPPLY CURRENT vs TEMPERATURE

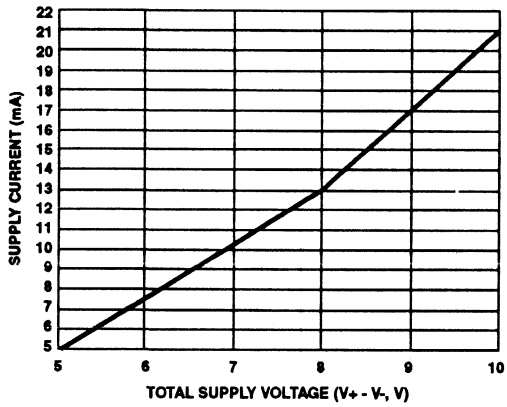


FIGURE 21. SUPPLY CURRENT vs SUPPLY VOLTAGE

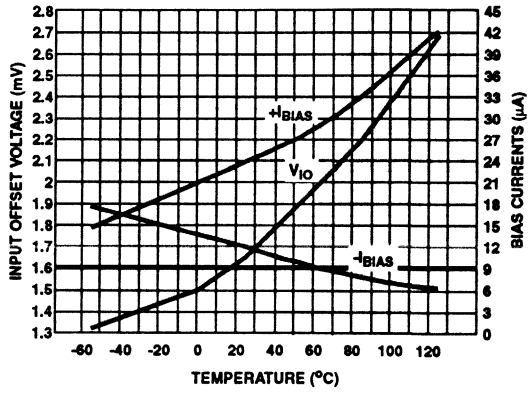


FIGURE 22. V_{IO} AND BIAS CURRENTS vs TEMPERATURE

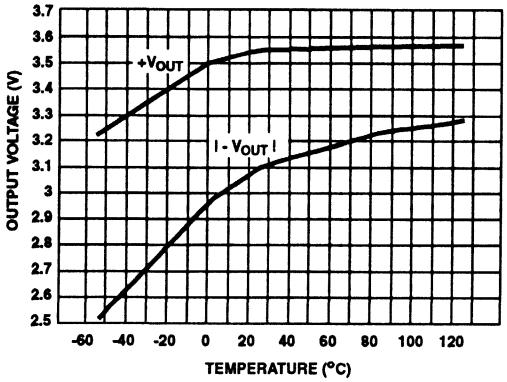


FIGURE 23. OUTPUT VOLTAGE vs TEMPERATURE ($A_V = -1$, $R_L = 50\Omega$)

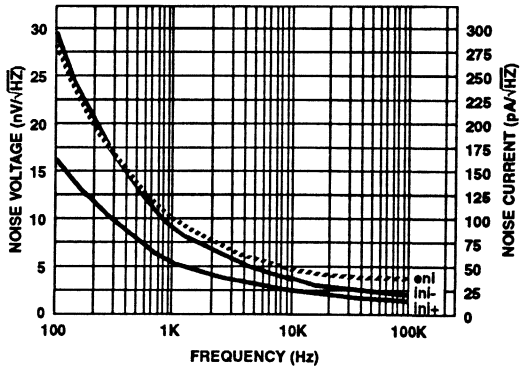


FIGURE 24. INPUT NOISE vs FREQUENCY

HARRIS SEMICONDUCTOR

HFA1105, HFA1106 HFA1135, HFA1145

ADVANCE INFORMATION

March 1993

High-Speed, Low Power, Current Feedback Operational Amplifiers

Features

- Wide -3dB Bandwidth 350MHz
- Very Fast Slew Rate..... 1500V/us
- Low Supply Current (HFA1105/06/45) ..... <6mA
- Supply Current (HFA1135) ..... <7mA
- Short Circuit Protected
- Compensation Pin Available - HFA1106
- Programmable Output Voltage Clamps - HFA1135
- Output Enable / Disable - HFA1145

Applications

- High Resolution Monitors
- Professional Video Processing
- Medical Imaging
- Video Digitizing Boards/Systems
- Heads Up Displays and Simulators
- Radar/IF Processing
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications
- Flash Converter Drivers
- High Speed Pulse Amplifiers

Description

The HFA1105, HFA1106, HFA1135, and HFA1145 are wide bandwidth, high speed, low power current feedback operational amplifiers built in Harris's proprietary complementary bipolar UHF-1 process.

The HFA1105 comes in a standard op amp pinout. The HFA1106 features a compensation pin for bandwidth limiting or external clamping applications. The HFA1135 features adjustable negative and positive output voltage clamps via pins 5 and 8. The HFA1145 features a TTL/CMOS compatible disable control, pin 8, that when pulled low, reduces the supply current and puts the output into a high impedance state.

The devices offer improved performance over the CLC406, CLC409, CLC420, CLC502, EL2070, AD9617, and AD9618.

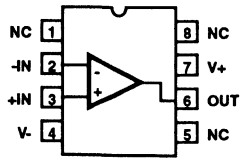
See the "Ordering Information" section below for package and temperature options. For military grade product, please refer to the HFA1105/883, HFA1106/883, HFA1135/883, HFA1145/883 datasheet.

Ordering Information

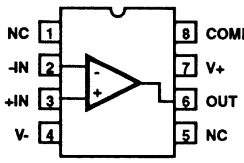
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1105IJ, HFA1106IJ HFA1135IJ, HFA1145IJ	-40°C to +85°C	8 Lead Ceramic DIP
HFA1105IP, HFA1106IP HFA1135IP, HFA1145IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1105IB, HFA1106IB HFA1135IB, HFA1145IB	-40°C to +85°C	8 Lead SOIC

Pinouts

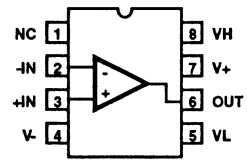
HFA1105
(PDIP, CDIP, SOIC)
TOP VIEW



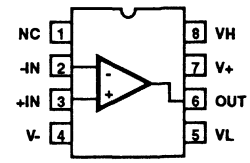
HFA1106
(PDIP, CDIP, SOIC)
TOP VIEW



HFA1135
(PDIP, CDIP, SOIC)
TOP VIEW



HFA1135
(PDIP, CDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3395**

HARRIS SEMICONDUCTOR

HFA1110

750MHz Low Distortion Unity Gain, Closed Loop Buffer

March 1993

Features

- Wide -3dB Bandwidth 750MHz
- Very Fast Slew Rate 1300V/μs
- Fast Settling Time (0.2%) 7ns
- High Output Current 60mA
- Fixed Gain of +1
- Gain Flatness (100MHz) 0.03dB
- Differential Phase ..... 0.025 deg.
- Differential Gain 0.04%
- 3rd Harmonic Distortion (50MHz) ..... -80dBc
- 3rd Order Intercept (100MHz) 30dBm

Applications

- Video Switching and Routing
- RF/IF Processors
- Driving Flash A/D Converters
- High-Speed Communications
- Impedance Transformation
- Line Driving
- Radar Systems

Description

The HFA1110 is a unity gain closed loop buffer that achieves -3dB bandwidth of 750MHz, while offering excellent video performance and low distortion. Manufactured on Harris' proprietary complementary bipolar UHF-1 process, the HFA1110 also offers very fast slew rate, and high output current. It is one more example of Harris' intent to enhance its leadership position in products for high speed signal processing applications.

The HFA1110's settling time of 11ns to 0.1%, low distortion and ability to drive capacitive loads make it an ideal flash A/D driver.

The HFA1110 is an enhanced, pin compatible upgrade for the AD9620, AD9630, CLC110, EL2072, BUF600 and BUF601.

For buffer applications requiring a standard op amp pinout, or selectable gain (-1, +1, +2), see the HFA1112 datasheet, for output clamping see the HFA1113 datasheet.

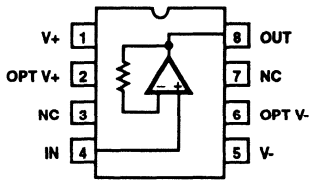
For military grade product please refer to the HFA1110/883 datasheet.

Ordering Information

PART NUMBER	OPERATING TEMP. RANGE	PRODUCT DESCRIPTION
HFA1110MJ/883	-55°C to +125°C	8 Lead Ceramic DIP
HFA1110IJ	-40°C to +85°C	8 Lead Ceramic DIP
HFA1110IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1110IB	-40°C to +85°C	8 Lead SOIC
HFA1110Y	-40°C to +85°C	DIE

Pinout

HFA1110
(PDIP, CDIP, SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
V+	1	Positive Supply
Opt V+	2	Optional Positive Supply
NC	3	No Connection
IN	4	Input
V-	5	Negative Supply
Opt V-	6	Optional Negative Supply
NC	7	No Connection
OUT	8	Output

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2944.4**

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Input Voltage ..... V_{SUPPLY}
Differential Input Voltage 5V
Output Current 60mA
Lead Temperature (Soldering 10 Sec.) ..... +300°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C

Operating Conditions

Operating Temperature Range
HFA1110I ..... $-40°C \leq T_A \leq +85°C$
Storage Temperature ..... $-65°C \leq T_A \leq +150°C$

Thermal Resistance (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP Package	116	36
Plastic DIP Package	98	36
SOIC Package	158	43

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

$V_{SUPPLY} = \pm5V$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEMP.	HFA1110I MIN	HFA1110I TYP	HFA1110I MAX	UNITS
INPUT CHARACTERISTICS					
Output Offset Voltage*	+25°C	-	8	25	mV
	Full	-	-	35	mV
Output Offset Voltage Drift	Full	-	10	-	µV/°C
PSRR	+25°C	39	45	-	dB
	Full	35	-	-	dB
Input Voltage Noise (100kHz)*	+25°C	-	14	-	$nV/\sqrt{Hz}$
Input Current Noise (100kHz)*	+25°C	-	51	-	$pA/\sqrt{Hz}$
Input Bias Current*	+25°C	-	10	40	µA
	Full	-	-	65	µA
Non-Inv. Input Resistance	+25°C	25	50	-	kΩ
Input Capacitance	+25°C	-	2	-	pF
TRANSFER CHARACTERISTICS					
Gain ($V_{OUT} = 2V_{P-P}$)	+25°C	0.980	0.990	-	V/V
	Full	0.975	-	-	V/V
DC Non-Linearity (±2V Full Scale)*	+25°C	-	0.003	-	%
OUTPUT CHARACTERISTICS					
Output Voltage*	+25°C	3.0	3.3	-	±V
	Full	2.5	3.0	-	±V
Output Current ($R_L = 50\Omega$)*	+25°C, +85°C	50	60	-	mA
	-40°C	35	50	-	mA
POWER SUPPLY CHARACTERISTICS					
Supply Voltage Range	Full	4.5	-	5.5	±V
Supply Current*	+25°C	-	21	26	mA
	Full	-	-	33	mA

Electrical Characteristics V_{SUPPLY} = ±5V, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP.	HFA1110I			UNITS
		MIN	TYP	MAX	
AC CHARACTERISTICS					
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P})*	+25°C	-	750	-	MHz
Slew Rate (V_{OUT} = 5V_{P-P})	+25°C	-	1300	-	V/µs
Full Power Bandwidth (4V_{P-P})*	+25°C	-	100	-	MHz
Gain Flatness (to 100MHz)*	+25°C	-	±0.03	-	dB
Gain Flatness (to 30MHz)	+25°C	-	±0.01	-	dB
Linear Phase Deviation (DC to 100MHz)*	+25°C	-	0.6	-	Degrees
2nd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P})*	+25°C	-	-60	-	dBc
3rd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P})*	+25°C	-	-80	-	dBc
3rd Order Intercept (100MHz)*	+25°C	-	30	-	dBm
-1dB Gain Compression (100MHz)	+25°C	-	14	-	dBm
Reverse Gain (S12 at 100MHz, V_{OUT} = 1V_{P-P})*	+25°C	-	-60	-	dB
Rise Time (V_{OUT} = 0.5V Step)	+25°C	-	0.5	-	ns
Overshoot (V_{OUT} = 1.0V Step)* Input Signal Rise/Fall = 1ns	+25°C	-	2.5	-	%
0.2% Settling (V_{OUT} = 1V to 0V)*	+25°C	-	7	-	ns
0.1% Settling (V_{OUT} = 1V to 0V)*	+25°C	-	11	-	ns
Overdrive Recovery Time	+25°C	-	15	-	ns
Differential Gain (3.58MHz, R_L = 75Ω)	+25°C	-	0.04	-	%
Differential Phase (3.58MHz, R_L = 75Ω)	+25°C		0.025		Degrees

* See Typical Performance Curves for more information.

Application Information

PC Board Layout

The frequency performance of this amplifier depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value chip (0.1µF) capacitor works well in most cases.

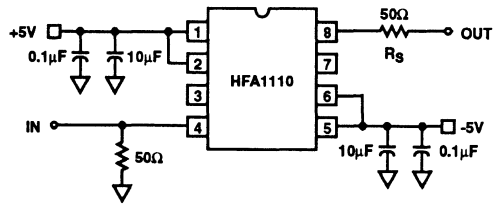
Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output. See the "Recommended R_S vs Load Capacitance" graph for specific recommendations.

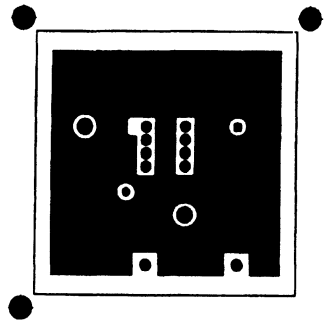
An example of a good high frequency layout is the Evaluation Board shown below.

Evaluation Board

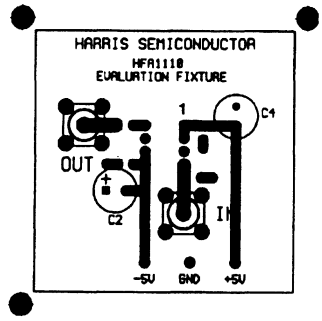
An evaluation board is available for the HFA1110. Please contact your local sales office for information.

The layout and schematic of the board are shown here:





BOTTOM LAYOUT



TOP LAYOUT

Die Characteristics

DIE DIMENSIONS:
63 x 44 x 19 ± 1mils
1600µm x 1130µm ±25.4µm

METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC
Gold Eutectic - Ceramic DIP

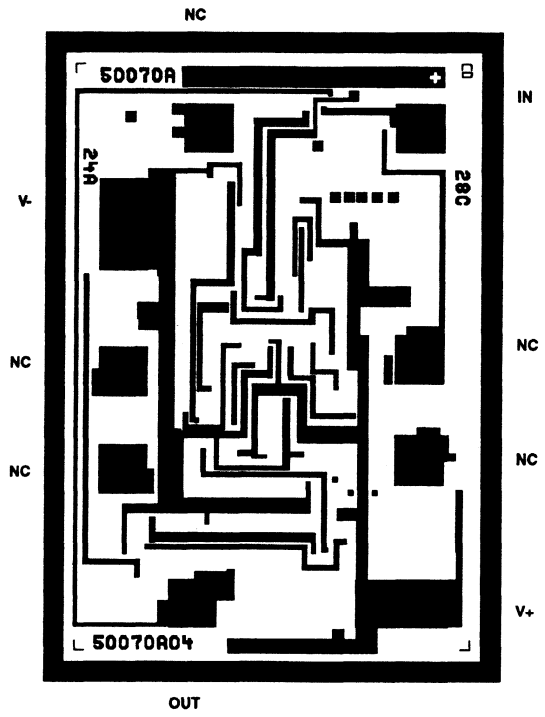
WORST CASE CURRENT DENSITY:
0.909×10^5 A/cm^2

TRANSISTOR COUNT: 52

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1110



Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25°C$, $R_L = 100\Omega$ Unless Otherwise Specified.

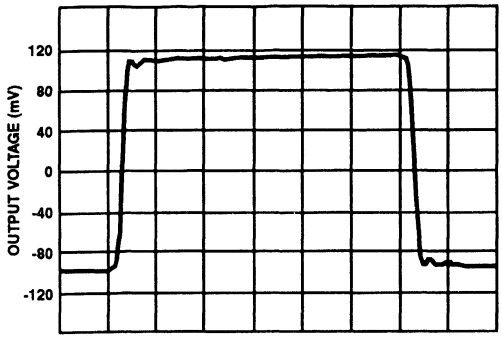


FIGURE 1. SMALL SIGNAL PULSE RESPONSE

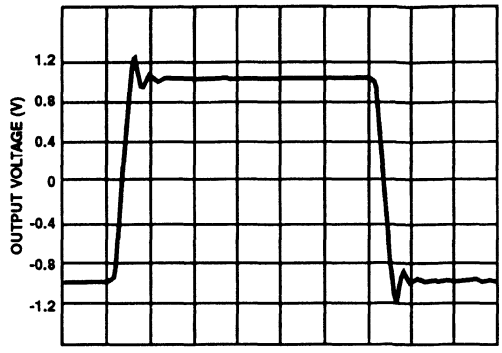


FIGURE 2. LARGE SIGNAL PULSE RESPONSE

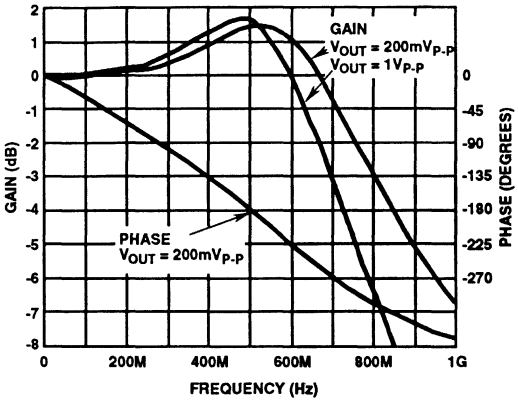


FIGURE 3. FORWARD GAIN AND PHASE

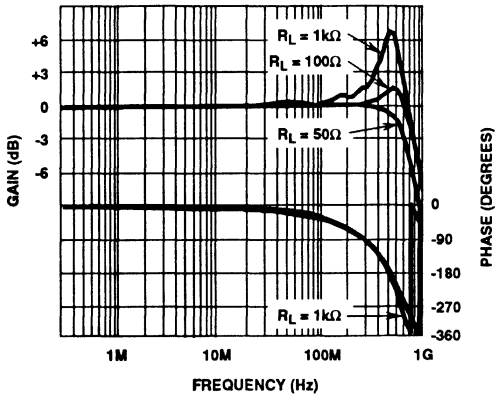


FIGURE 4. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

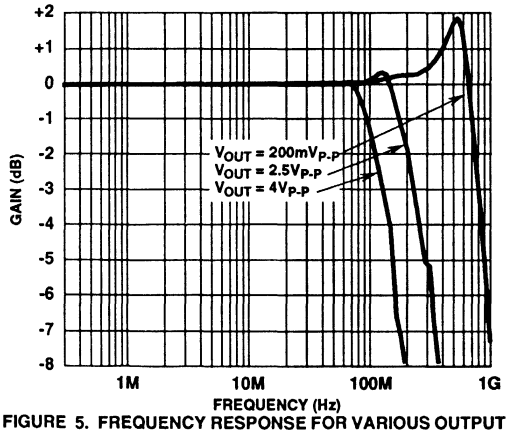


FIGURE 5. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

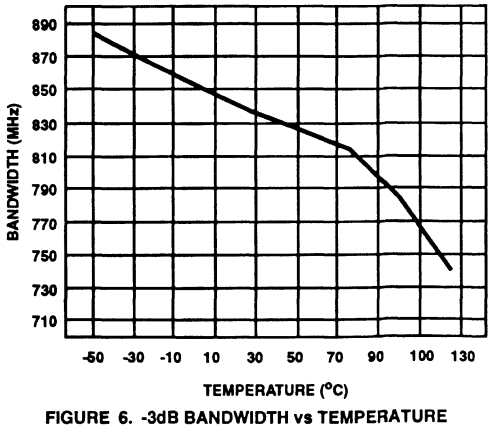


FIGURE 6. -3dB BANDWIDTH vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25°C$, $R_L = 100\Omega$ Unless Otherwise Specified. (Continued)

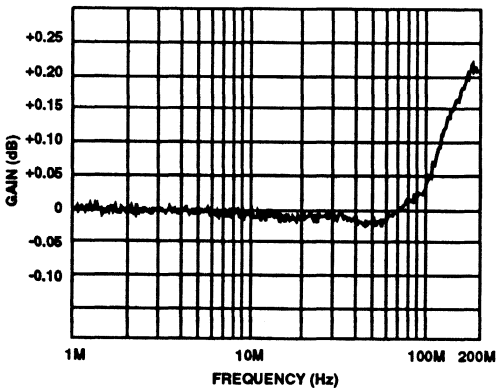


FIGURE 7. GAIN FLATNESS

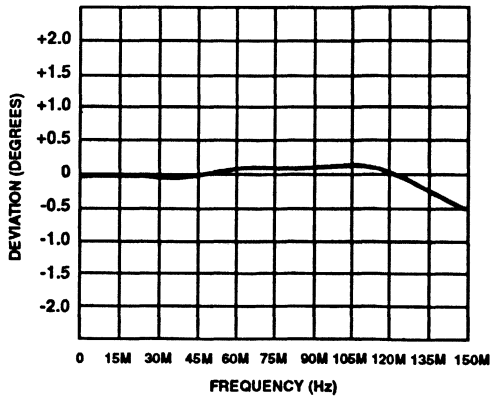


FIGURE 8. DEVIATION FROM LINEAR PHASE

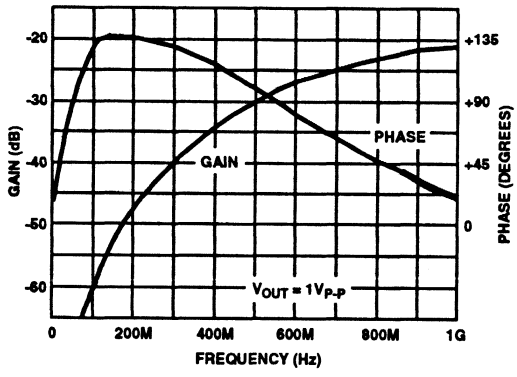


FIGURE 9. REVERSE GAIN AND PHASE

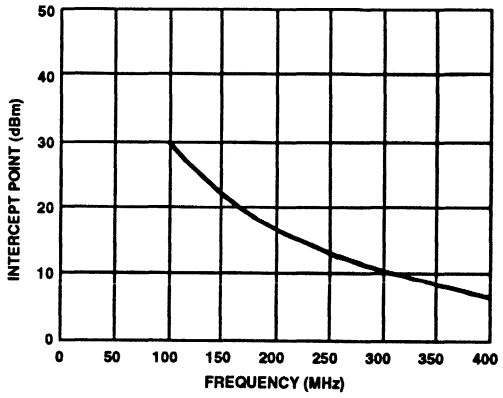


FIGURE 10. 2-TONE, 3RD ORDER INTERMODULATION INTERCEPT

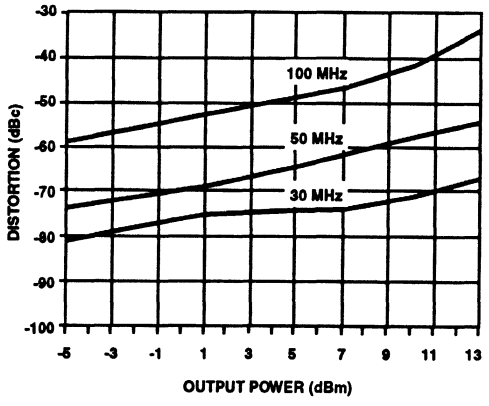


FIGURE 11. 2nd HARMONIC DISTORTION vs P_{OUT}

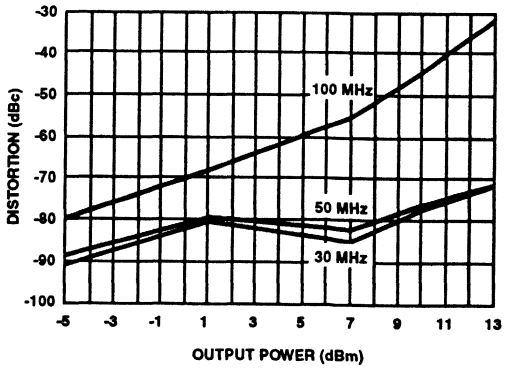


FIGURE 12. 3rd HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25°C$, $R_L = 100\Omega$ Unless Otherwise Specified. (Continued)

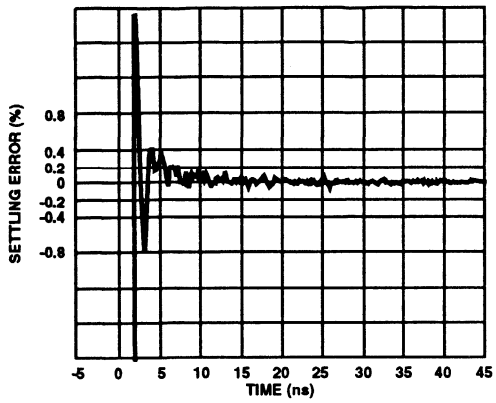


FIGURE 13. SETTLING RESPONSE ($V_{OUT} = 1V$)

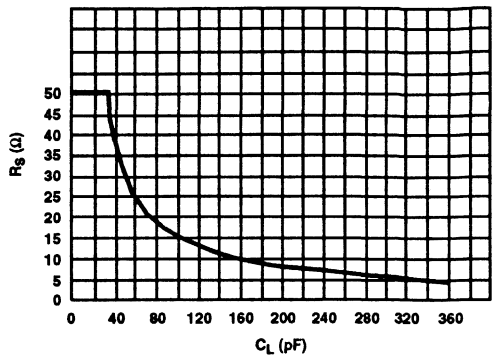


FIGURE 14. RECOMMENDED SERIES OUTPUT RESISTOR vs C_{LOAD}

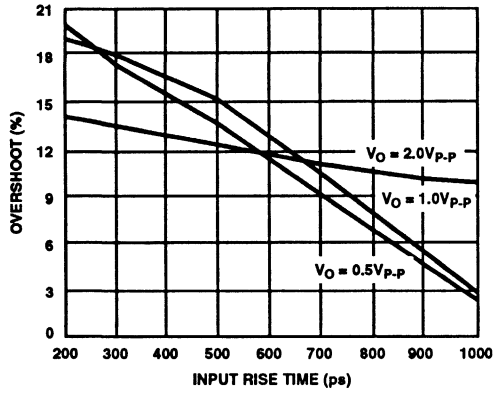


FIGURE 15. OVERSHOOT vs INPUT RISETIME

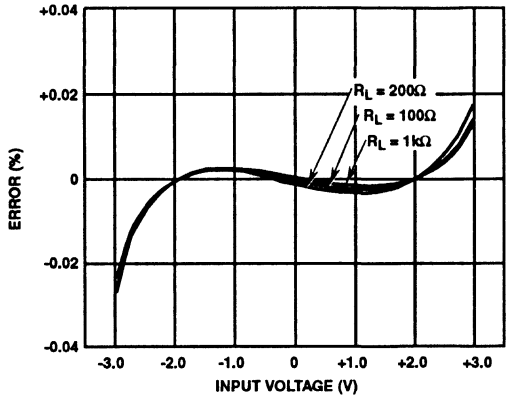


FIGURE 16. INTEGRAL LINEARITY ERROR

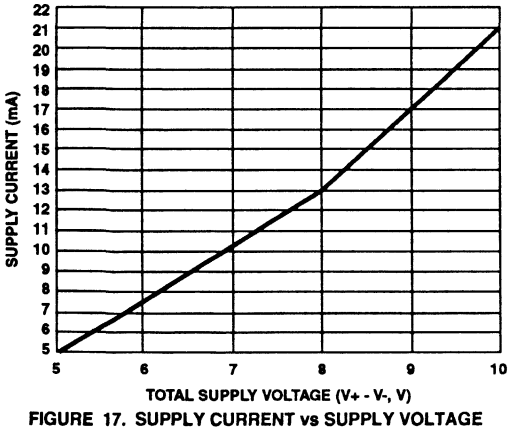


FIGURE 17. SUPPLY CURRENT vs SUPPLY VOLTAGE

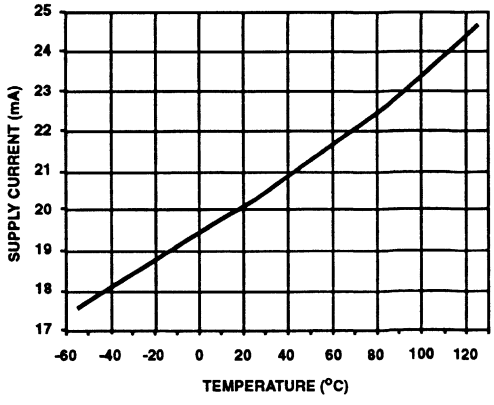


FIGURE 18. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = +25°C, R_L = 100Ω Unless Otherwise Specified. (Continued)

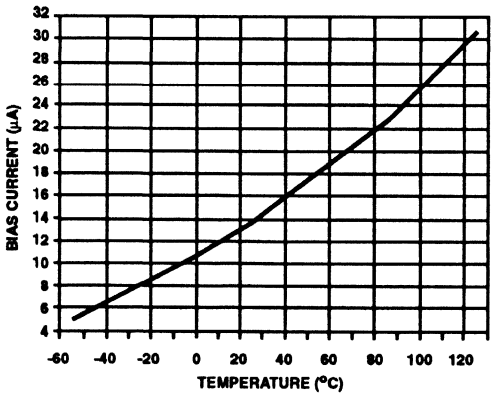


FIGURE 19. BIAS CURRENT vs TEMPERATURE

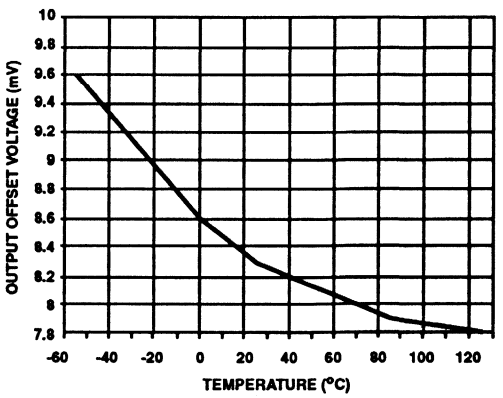


FIGURE 20. OFFSET VOLTAGE vs TEMPERATURE

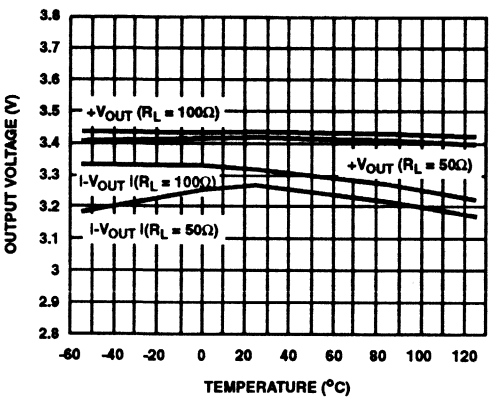


FIGURE 21. OUTPUT VOLTAGE vs TEMPERATURE

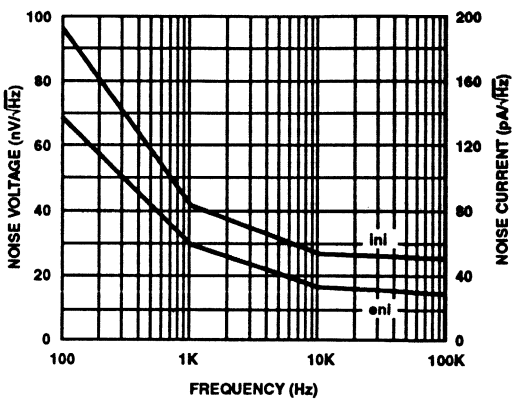


FIGURE 22. INPUT NOISE vs FREQUENCY

HARRIS SEMICONDUCTOR

HFA1112

Ultra High-Speed Closed Loop Buffer Amplifier

March 1993

Features

- Wide -3dB Bandwidth 850MHz
- Very Fast Slew Rate (A_V = +2)..... 2050V/µs
- Fast Settling Time (0.1%) 11ns
- High Output Current 60mA
- Excellent Gain Accuracy.....0.99V/V
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Standard Operational Amplifier Pinout

Applications

- RF/IF Processors
- Driving Flash A/D Converters
- High-Speed Communications
- Impedance Transformation
- Line Driving
- Video Switching and Routing
- Radar Systems

Description

The HFA1112 is a closed loop current feedback buffer amplifier that achieves a high degree of gain accuracy, wide bandwidth, and low distortion. Manufactured on the Harris proprietary complementary bipolar UHF-1 process, the HFA1112 also offers very fast slew rate, excellent gain flatness, and high output current.

A unique feature of the circuit pinout allows for voltage gains of +1, +2, and -1, while maintaining compatibility with the standard op amp pinout (see Pinout). By leaving pin 2 open and applying the input to pin 3, the circuit defaults to the standard gain of +1. Grounding pin 2 and applying the input to pin 3, results in a gain of +2. Finally, by using pin 2 as an input and grounding pin 3, a gain of -1 can be achieved.

The HFA1112 offers performance and functionality advantages over the AD9620, AD9630, CLC110, and EL2072.

For standard buffer pinout applications see HFA1110 datasheet.

The device is available in 8-pin CERDIP, PDIP, and SOIC packages.

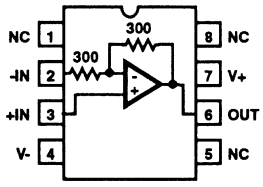
For military grade product, refer to the HFA1112/883 datasheet.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1112MJ/883	-55°C to +125°C	8 Lead Ceramic DIP
HFA1112IJ	-40°C to +85°C	8 Lead Ceramic DIP
HFA1112IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1112IB	-40°C to +85°C	8 Lead SOIC

Pinout

HFA1112
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1, 5, 8	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
OUT	6	Output
V+	7	Positive Supply

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2992.1**

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage ..... V_{SUPPLY}
Differential Input Voltage 5V
Output Current 60mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HFA1112I ..... $-40°C \le T_A \le +85°C$
Storage Temperature ..... $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP Package	116	36
Plastic DIP Package	98	36
SOIC Package	158	43

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEMP.	HFA1112I MIN	HFA1112I TYP	HFA1112I MAX	UNITS
INPUT CHARACTERISTICS					
Output Offset Voltage	+25°C	-	8	25	mV
	Full	-	-	35	mV
Output Offset Voltage Drift	Full	-	10	-	µV/°C
PSRR	+25°C	39	45	-	dB
	Full	35	-	-	dB
Input Voltage Noise (100kHz)	+25°C	-	9	-	$nV/\sqrt{Hz}$
+Input Current Noise (100kHz)	+25°C	-	19	-	$pA/\sqrt{Hz}$
Non-Inv. Input Bias Current	+25°C	-	25	35	µA
	Full	-	-	60	µA
Non-Inv. Input Resistance	+25°C	30	50	-	kΩ
Inv. Input Resistance	+25°C	240	300	360	Ω
Input Capacitance (Either Input)	+25°C	-	2	-	pF
Input Common Mode Range	Full	2.5	2.8	-	±V
TRANSFER CHARACTERISTICS					
Gain ($A_V = +1$, $V_{IN} = +2V$)	+25°C	0.980	0.990	-	V/V
	Full	0.975	-	-	V/V
Gain ($A_V = +2$, $V_{IN} = +1V$)	+25°C	1.96	1.98	-	V/V
	Full	1.95	-	-	V/V
DC Non-Linearity ($A_V = +2$, ±2V Full Scale)	+25°C	-	0.02	-	%
OUTPUT CHARACTERISTICS					
Output Voltage ($A_V = -1$)	+25°C	3.0	3.3	-	±V
	Full	2.7	3.0	-	±V
Output Current ($R_L = 50\Omega$)	+25°C, +85°C	50	60	-	mA
	-40°C	35	50	-	mA
DC Closed Loop Output Impedance	+25°C	-	0.1	-	Ω
POWER SUPPLY CHARACTERISTICS					
Supply Voltage Range	Full	4.5	-	5.5	±V
Supply Current	+25°C	-	21	26	mA
	Full	-	-	33	mA

Electrical Characteristics V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMP.	HFA1112I MIN	HFA1112I TYP	HFA1112I MAX	UNITS
AC CHARACTERISTICS						
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P})	A_V = -1	+25°C	-	600	-	MHz
	A_V = +1	+25°C	-	850	-	MHz
	A_V = +2	+25°C	-	530	-	MHz
Slew Rate (V_{OUT} = 5V_{P-P})	A_V = -1	+25°C	-	2400	-	V/µs
	A_V = +1	+25°C	-	1700	-	V/µs
	A_V = +2	+25°C	-	2050	-	V/µs
Full Power BW (5Vp-p, A_V = +2)		+25°C	-	260	-	MHz
Gain Flatness (to 100MHz, A_V = +2)		+25°C	-	±0.06	-	dB
Gain Flatness (to 30MHz, A_V = +2)		+25°C	-	±0.015	-	dB
2nd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P})		+25°C	-	-60	-	dBc
3rd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P})		+25°C	-	-80	-	dBc
3rd Order Intercept (100MHz)		+25°C	-	30	-	dBm
1dB Compression (100MHz, A_V = +2)		+25°C	-	18	-	dBm
Rise Time (V_{OUT} = 0.5V Step)	A_V = +2	+25°C	-	700	-	ps
	A_V = +1	+25°C	-	500	-	ps
Overshoot (V_{OUT} = 0.5V Step)		+25°C	-	0.5	-	%
0.1% Settling (V_{OUT} = 2V to 0V)		+25°C	-	11	-	ns
0.05% Settling (V_{OUT} = 2V to 0V)		+25°C	-	15	-	ns
Overdrive Recovery Time (V_{IN} = 5V_{P-P})		+25°C	-	8.5	-	ns
Differential Gain	A_V = +1, 3.58MHz, R_L = 150Ω	+25°C	-	0.03	-	%
	A_V = +2, 3.58MHz, R_L = 150Ω	+25°C	-	0.02	-	%
Differential Phase	A_V = +1, 3.58MHz, R_L = 150Ω	+25°C	-	0.05	-	Degrees
	A_V = +2, 3.58MHz, R_L = 150Ω	+25°C	-	0.04	-	Degrees

Connections

DESIRED GAIN	CONNECTION
+1	Float -IN (pin 2). Apply Signal to +IN (pin 3).
+2	Ground -IN. Apply Signal to +IN.
-1	Ground +IN. Apply Signal to -IN.

Application Hints

The frequency performance of the HFA1112 can depend a great deal on the amount of care taken in designing the PC board.

Attention should be given to decoupling the power supplies. A large value (5µF) tantalum in parallel with a small value chip (0.1µF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended.**

Die Characteristics

DIE DIMENSIONS:
63 x 44 x 19 ± 1mils
1600µm x 1130µm ±25.4µm

METALLIZATION:
Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu (2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC
Gold Eutectic - Ceramic DIP

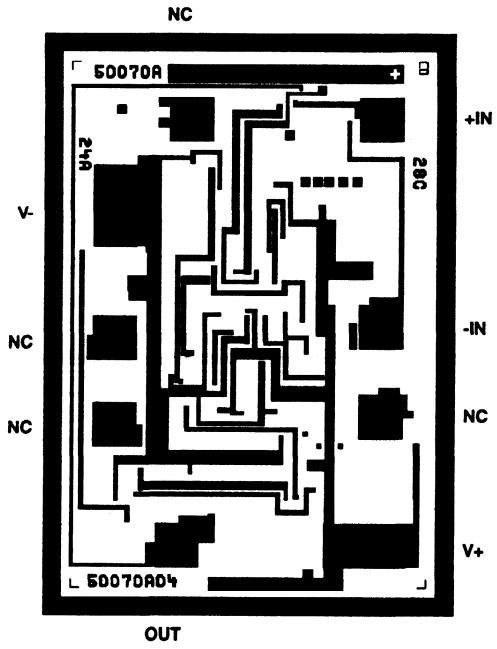
WORST CASE CURRENT DENSITY:
0.909×10^5 A/cm^2

TRANSISTOR COUNT: 52

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1112



Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +2$, $T_A = +25°C$, Unless Otherwise Specified

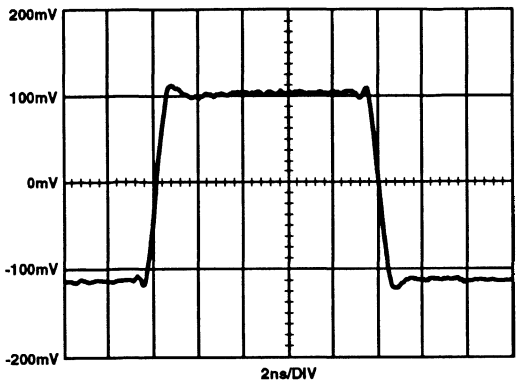


FIGURE 1. SMALL SIGNAL PULSE RESPONSE

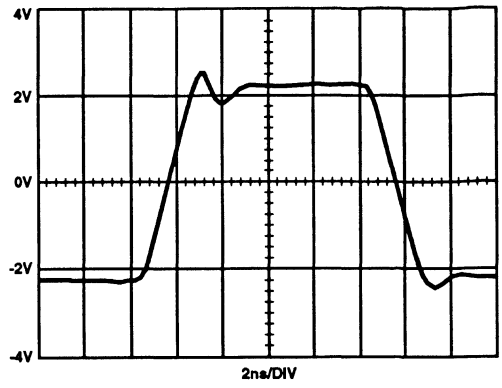


FIGURE 2. LARGE SIGNAL PULSE RESPONSE

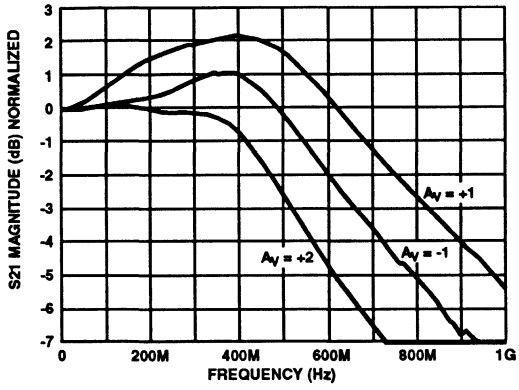


FIGURE 3. FORWARD GAIN

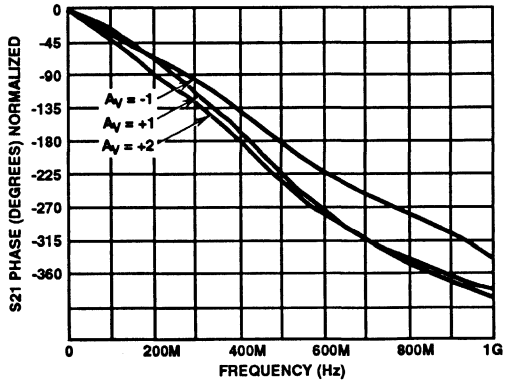


FIGURE 4. FORWARD PHASE

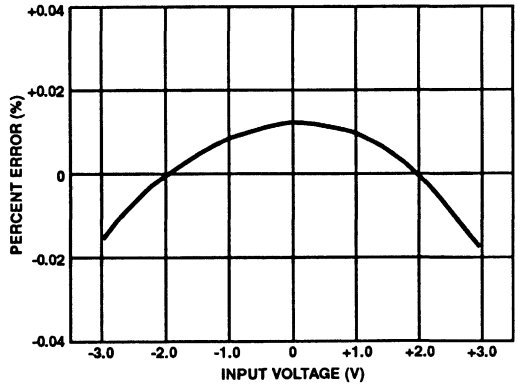


FIGURE 5. INTEGRAL LINEARITY ERROR

HARRIS SEMICONDUCTOR

HFA1113

High-Speed, Output Clamping Closed Loop Buffer

March 1993

Features

- User Programmable Output Voltage Clamp
- Wide -3dB Bandwidth 850MHz
- Very Fast Slew Rate (A_V = +2) 2050V/µs
- Fast Settling Time (0.1%) 11ns
- High Output Current 60mA
- Excellent Gain Accuracy 0.99V/V
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Overdrive Recovery ..... <1ns
- Standard Operational Amplifier Pinout

Applications

- RF/IF Processors
- Driving Flash A/D Converters
- High-Speed Communications
- Impedance Transformation
- Line Driving
- Video Switching and Routing
- Radar Systems
- Medical Imaging Systems

Description

The HFA1113 is a high speed closed loop Buffer featuring both user programmable gain and output clamping. Manufactured on Harris' proprietary complementary bipolar UHF-1 process, the HFA1113 also offers a wide -3dB bandwidth of 850MHz, very fast slew rate, excellent gain flatness, low distortion and high output current.

This buffer is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overload recovery times. The output clamp allows the designer to set the maximum positive and negative output levels, thereby protecting later stages from damage or input saturation. The HFA1113 also allows for voltage gains of +2, +1, and -1, without the use of external resistors. By leaving pin 2 open and applying the input to pin 3, the circuit defaults to the standard gain of +1. Grounding pin 2, and applying the input to pin 3, results in a gain of +2. Finally, by using pin 2 as an input and grounding pin 3, a gain of -1 can be achieved.

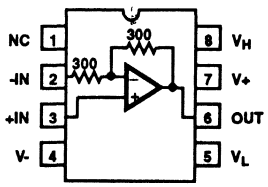
Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the std pinout provides an upgrade path, should a higher closed loop gain be needed at a future date. For Military product, refer to the HFA1113/883 data sheet.

Ordering Information

PART NUMBER	OPERATING TEMP. RANGE	PRODUCT DESCRIPTION
HFA1113MJ/883	-55°C to +125°C	8 Lead Ceramic DIP
HFA1113IJ	-40°C to +85°C	8 Lead Ceramic DIP
HFA1113IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1113IB	-40°C to +85°C	8 Lead SOIC

Pinout

HFA1113
(PDIP, CDIP,SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
V_L	5	Lower Output Limit
OUT	6	Output
V+	7	Positive Supply
V_H	8	Upper Output Limit

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1342

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Input Voltage ..... V_{SUPPLY}
Differential Input Voltage 5V
Output Current 60mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 sec.) ..... +300°C

Operating Conditions

HFA1113I ..... -40°C ≤ T_A ≤ +85°C
Storage Temperature ..... -65°C ≤ T_A ≤ +150°C

Thermal Resistance (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP Package	116	36
Plastic DIP Package	98	36
SOIC Package	158	43

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEMP.	HFA1113I MIN	HFA1113I TYP	HFA1113I MAX	UNITS
INPUT CHARACTERISTICS					
Output Offset Voltage	+25°C	-	8	25	mV
	Full	-	-	35	mV
Output Offset Voltage Drift	Full	-	10	-	µV/°C
PSRR	+25°C	39	45	-	dB
	Full	35	-	-	dB
Input Voltage Noise (100kHz)	+25°C	-	9	-	$nV/\sqrt{Hz}$
+Input Current Noise (100kHz)	+25°C	-	19	-	$pA/\sqrt{Hz}$
Non-Inv. Input Bias Current	+25°C	-	25	35	µA
	Full	-	-	60	µA
Non-Inv. Input Resistance	+25°C	30	50	-	kΩ
Inv. Input Resistance	+25°C	240	300	360	Ω
Input Capacitance (Either Input)	+25°C	-	2	-	pF
Input Common Mode Range	Full	2.5	2.8	-	±V
TRANSFER CHARACTERISTICS					
Gain (A_V = +1, V_{IN} = +2V)	+25°C	0.980	0.990	-	V/V
	Full	0.975	-	-	V/V
Gain (A_V = +2, V_{IN} = +1V)	+25°C	1.96	1.98	-	V/V
	Full	1.95	-	-	V/V
DC Non-Linearity (A_V = +2, ±2V Full Scale)	+25°C	-	0.02	-	%
OUTPUT CHARACTERISTICS					
Output Voltage (A_V = -1)	+25°C	3.0	3.3	-	±V
	Full	2.7	3.0	-	±V
Output Current (R_L = 50Ω)	+25°C, 85°C	50	60	-	mA
	-40°C	35	50	-	mA
DC Closed Loop Output Impedance	+25°C	-	0.1	-	Ω
POWER SUPPLY CHARACTERISTICS					
Supply Voltage Range	Full	4.5	-	5.5	±V
Supply Current	+25°C	-	21	26	mA
	Full	-	-	33	mA

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMP.	HFA1113I			UNITS
			MIN	TYP	MAX	
AC CHARACTERISTICS						
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P})	A_V = -1	+25°C	-	600	-	MHz
	A_V = +1	+25°C	-	850	-	MHz
	A_V = +2	+25°C	-	530	-	MHz
Slew Rate (V_{OUT} = 5V_{P-P})	A_V = -1	+25°C	-	2400	-	V/µs
	A_V = +1	+25°C	-	1700	-	V/µs
	A_V = +2	+25°C	-	2050	-	V/µs
Full Power BW (5V_{P-P}, A_V = +2)		+25°C	-	260	-	MHz
Gain Flatness (to 200MHz, A_V = +2)		+25°C	-	±0.07	-	dB
Gain Flatness (to 30MHz, A_V = +2)		+25°C	-	±0.015	-	dB
2nd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P})		+25°C	-	-60	-	dBc
3rd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P})		+25°C	-	-80	-	dBc
3rd Order Intercept (100MHz)		+25°C	-	30	-	dBm
1dB Compression (100MHz, A_V = +2)		+25°C	-	18	-	dBm
Rise Time (V_{OUT} = 0.5V Step)	A_V = +2	+25°C	-	700	-	ps
	A_V = +1	+25°C	-	500	-	ps
Overshoot (V_{OUT} = 0.5V Step)		+25°C	-	0.5	-	%
0.1% Settling (V_{OUT} = 2V to 0V)		+25°C	-	11	-	ns
0.05% Settling (V_{OUT} = 2V to 0V)		+25°C	-	15	-	ns
Differential Gain	A_V = +1, 3.58MHz, R_L = 150Ω	+25°C	-	0.03	-	%
	A_V = +2, 3.58MHz, R_L = 150Ω	+25°C	-	0.02	-	%
Differential Phase	A_V = +1, 3.58MHz, R_L = 150Ω	+25°C	-	0.05	-	Degrees
	A_V = +2, 3.58MHz, R_L = 150Ω	+25°C	-	0.04	-	Degrees
CLAMP CHARACTERISTICS A_V = +2, V_H = +1V, V_L = -1V, Unless Otherwise Specified.						
Clamp Accuracy (V_{IN} = ±2V, A_V = -1)		+25°C	-	80	±150	mV
Clamp Overshoot (V_{IN} = ±1V, Input t_r/t_f = 2ns)		+25°C	-	4	-	%
Overdrive Recovery Time (V_{IN} = ±1V)		+25°C	-	0.75	1.5	ns
Negative Clamp Range		+25°C	-	-5.0 to +2.0	-	V
Positive Clamp Range		+25°C	-	-2.0 to +5.0	-	V
Clamp Input Bias Current		+25°C	-	50	200	µA
Clamp Input Bandwidth (V_H or V_L = 100mV_{P-P})		+25°C	-	300	-	MHz

Die Characteristics

DIE DIMENSIONS:
63 x 44 x 19 ± 1mils
1600µm x 1130µm ± 25.4µm

METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC
Gold Eutectic - Ceramic DIP

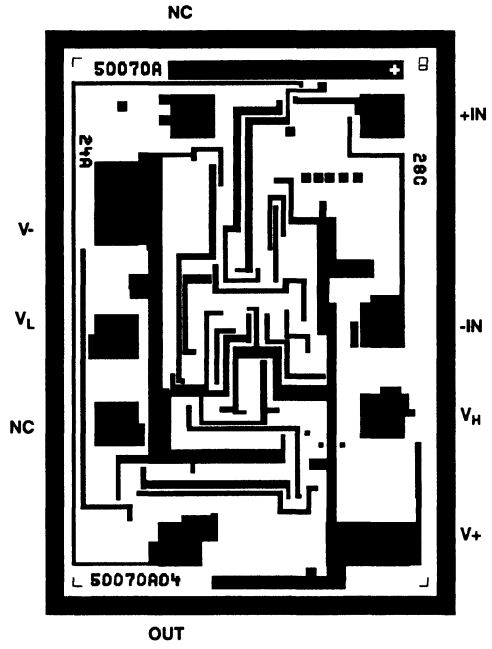
WORST CASE CURRENT DENSITY:
0.909×10^5 A/cm^2

TRANSISTOR COUNT: 52

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1113



Application Information

Closed Loop Gain Selection

The HFA1113 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

This "buffer" operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the ±Inputs. Applying the input signal to +IN and floating -IN selects a gain of +1, while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded.

The table below sumarizes these connections..

GAIN (A_{CL})	CONNECTIONS	
	+INPUT (PIN 3)	-INPUT (PIN 2)
-1	GND	Input
+1	Input	NC (Floating)
+2	Input	GND

Clamp Operation

General

The HFA1113 features user programmable output clamps to limit output voltage excursions. Clamping action is obtained by applying voltages to the V_H and V_L terminals (pins 8 & 5) of the amplifier. V_H sets the upper output limit, while V_L sets the lower clamp level. If the amplifier tries to drive the output above V_H, or below V_L, the clamp circuitry limits the output voltage at V_H or V_L (± the clamp accuracy), respectively. The low input bias currents of the clamp pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or DACs.

Clamp Circuitry

Figure 1 shows a simplified schematic of the HFA1113 input stage, and the high clamp (VH) circuitry. As with all current feedback amplifiers, there is a unity gain buffer (QX1 - QX2) between the positive and negative inputs. This buffer forces -IN to track +IN, and sets up a slewing current of (V-IN - VOUT)/RF. This current is mirrored onto the high impedance node (Z) by QX3-QX4, where it is converted to a voltage and fed to the output via another unity gain buffer. If no clamping is utilized, the high impedance node may swing within the limits defined by QP4 and QN4. Note that when the output reaches it's quiescent value, the current flowing through -IN is reduced to only that small current (-IBIAS) required to keep the output at the final voltage.

Tracing the path from V_H to Z illustrates the effect of the clamp voltage on the high impedance node. V_H decreases by $2V_{BE}$ (QN6 and QP6) to set up the base voltage on QP5. QP5 begins to conduct whenever the high impedance node reaches a voltage equal to QP5's base + $2V_{BE}$ (QP5 and QN5). Thus, QP5 clamps node Z whenever Z reaches V_H.

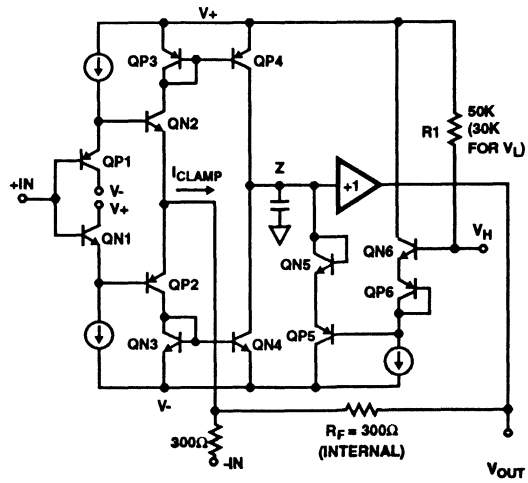


FIGURE 1. HFA1113 SIMPLIFIED V_H CLAMP CIRCUITRY

R1 provides a pull-up network to ensure functionality with the clamp inputs floating. A similar description applies to the symmetrical low clamp circuitry controlled by V_L.

When the output is clamped, the negative input continues to source a slewing current (I_{CLAMP}) in an attempt to force the output to the quiescent voltage defined by the input. QP5 must sink this current while clamping, because the -IN current is always mirrored onto the high impedance node. The clamping current is calculated as (V_{-IN} - V_{OUT}) / 300Ω. As an example, a unity gain circuit with V_{IN} = 2V, and V_H = 1V, would have I_{CLAMP} = (2-1)/300Ω = 3.27mA. Note that Icc will increase by I_{CLAMP} when the output is clamp limited.

Clamp Accuracy

The clamped output voltage will not be exactly equal to the voltage applied to V_H or V_L. Offset errors, mostly due to V_{BE} mismatches, necessitate a clamp accuracy parameter which is found in the device specifications. Clamp accuracy is a function of the clamping conditions. Referring again to Figure 1, it can be seen that one component of clamp accuracy is the V_{BE} mismatch between the QX6 transistors, and the QX5 transistors. If the transistors always ran at the same current level there would be no V_{BE} mismatch, and no contribution to the inaccuracy. The QX6 transistors are biased at a constant current, but as described earlier, the current through QX5 is equivalent to I_{CLAMP}. V_{BE} increases as I_{CLAMP} increases, causing the clamped output voltage to increase as well. I_{CLAMP} is a function of the overdrive level (V_{-IN} - $V_{OUT\ CLAMPED}$), so clamp accuracy degrades as the overdrive increases. As an example, the specified accuracy of ±80mV for a 2X overdrive degrades to ±250mV for a 3X overdrive.

Consideration must also be given to the fact that the clamp voltages have an effect on amplifier linearity. The "Nonlinearity Near Clamp Voltage" curve in the data sheet illustrates the impact of several clamp levels on linearity.

Clamp Range

Unlike some competitor devices, both V_H and V_L have usable ranges that cross 0V. While V_H must be more positive than V_L, both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HFA1113 could be limited to ECL output levels by setting V_H = -0.8V and V_L = -1.8V. V_H and V_L may be connected to the same voltage (GND for instance) but the result won't be in a DC output voltage from an AC input signal. A 150 - 200mV AC signal will still be present at the output.

Recovery from Overdrive

The output voltage remains at the clamp level as long as the overdrive condition remains. When the input voltage drops below the overdrive level (V_{CLAMP} / A_{VCL}) the amplifier will return to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. The plots of "Unclamped Performance" and "Clamped Performance" highlight the HFA1113's subnanosecond recovery time. The difference between the unclamped and clamped propagation delays is the overdrive recovery time. The appropriate propagation delays are 4.0ns for the unclamped pulse, and 4.8ns for the clamped (2X overdrive) pulse yielding an overdrive recovery time of 800ps. The measurement uses the 90% point of the output transition to ensure that linear operation has resumed. Note: The propagation delay illustrated is dominated by the fixturing. The delta shown is accurate, but the true HFA1113 propagation delay is 500ps.

PC Board Layout

The frequency performance of this amplifier depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value chip (0.1µF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

For unity gain applications, care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. At higher frequencies this capacitance will tend to short the -INPUT to GND, resulting in a closed loop gain which increases with frequency. This will cause excessive high frequency peaking and potentially other problems as well.

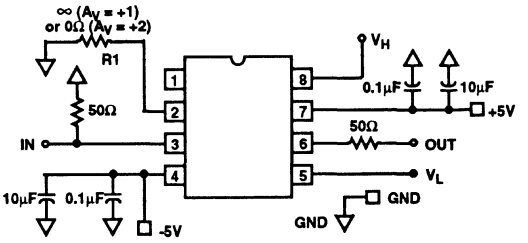
An example of a good high frequency layout is the Evaluation Board shown below.

Evaluation Board

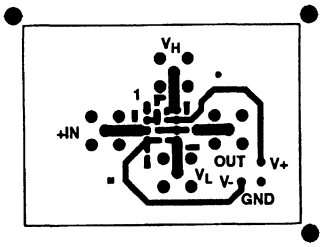
The performance of the HFA1113 may be evaluated using the HA1130 Evaluation Board, slightly modified as follows:

1. Remove the 500Ω feedback resistor (R2), and leave the connection open.
2. a. For A_V = +1 evaluation, remove the 500Ω gain setting resistor (R1), and leave pin 2 floating.
   b. For A_V = +2, replace the 500Ω gain setting resistor with a 0Ω resistor to GND.

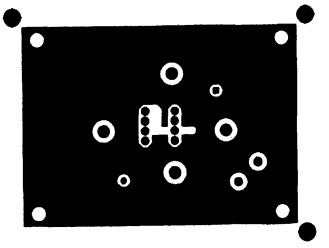
The layout and modified schematic of the board are shown here:



TOP LAYOUT

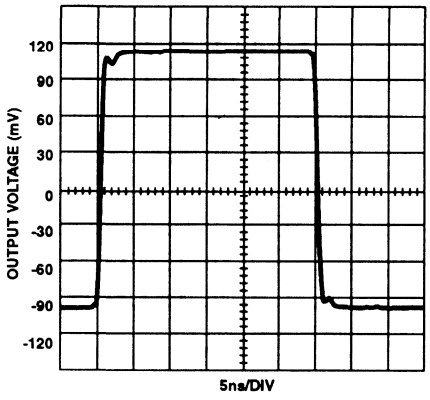


BOTTOM LAYOUT

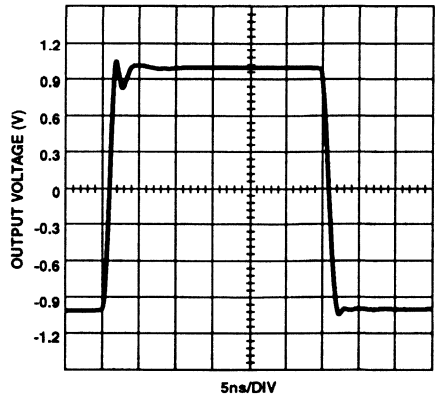


Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25°C$, $R_L = 100\Omega$ Unless Otherwise Specified.

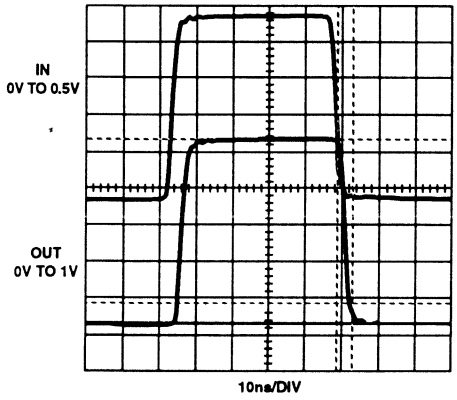
SMALL SIGNAL PULSE RESPONSE
($A_V = +2$)



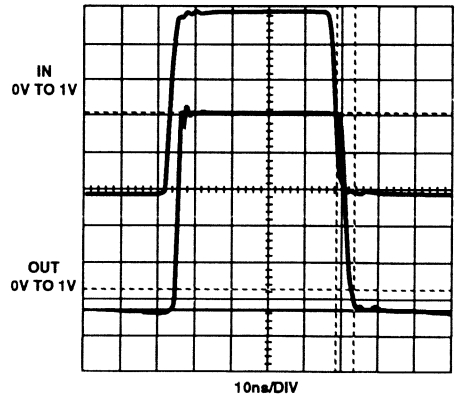
LARGE SIGNAL PULSE RESPONSE
($A_V = +2$)



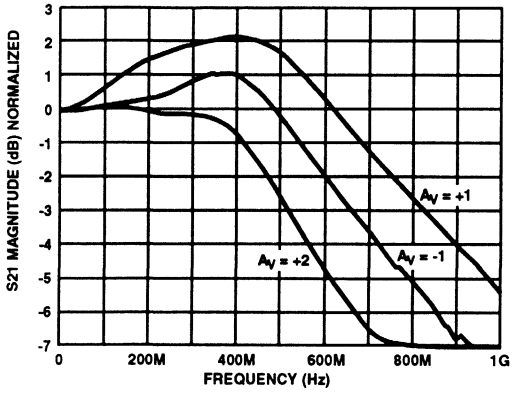
UNCLAMPED PERFORMANCE
($A_V = +2$, $V_H = 2V$, $V_L = -2V$)



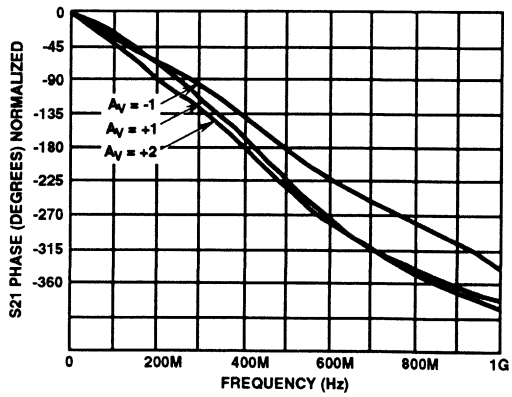
CLAMPED PERFORMANCE
($A_V = +2$, $V_H = 1V$, $V_L = -1V$, 2X Overdrive)



FORWARD GAIN

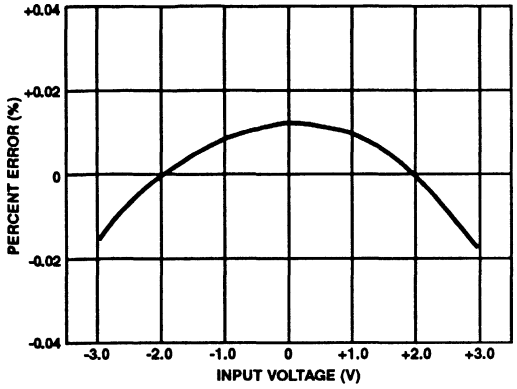


FORWARD PHASE

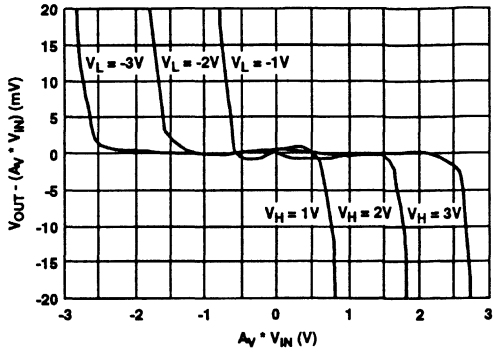


Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25°C$, $R_L = 100\Omega$ Unless Otherwise Specified. (Continued)

INTEGRAL LINEARITY ERROR



NON-LINEARITY NEAR CLAMP VOLTAGE
($A_V = -1$, $R_L = 100\Omega$)



HARRIS SEMICONDUCTOR

HFA1130

Output Clamping, Ultra High-Speed Current Feedback Amplifier

March 1993

Features

- User Programmable Output Voltage Clamp
- Low Distortion (30MHz).....-56dBc
- -3dB Bandwidth 850MHz
- Very Fast Slew Rate.....2300V/μs
- Fast Settling Time (0.1%) 11ns
- Excellent Gain Flatness
  - (100MHz).....0.14dB
  - (50MHz).....0.04dB
  - (30MHz).....0.01dB
- High Output Current 60mA
- Overdrive Recovery.....<1ns

Applications

- Residue Amplifier
- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems

Description

The HFA1130 is a high speed wideband current feedback amplifier featuring programmable output clamps. Built with Harris' proprietary complementary bipolar UHF-1 process, it is the fastest monolithic amplifier available from any semiconductor manufacturer.

This amplifier is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overdrive recovery times. The output clamp function allows the designer to set the maximum positive and negative output levels, thereby protecting later stages from damage or input saturation. The sub-nanosecond overdrive recovery time quickly returns the amplifier to linear operation, following an overdrive condition.

The HFA1130 offers significant performance improvements over the CLC500/501/502.

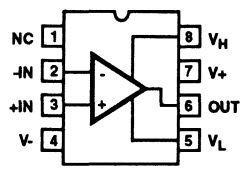
A variety of packages and temperature grades are available. See the ordering information below for details. For /883 product refer to the HFA1130/883 datasheet.

Ordering Information

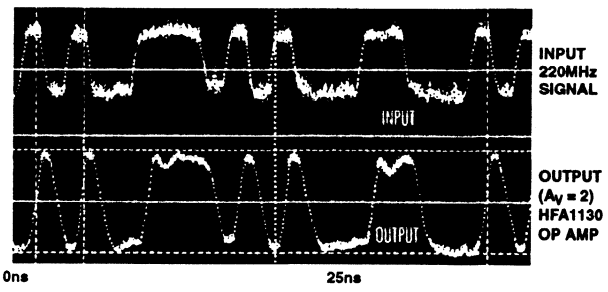
PART NUMBER	OPERATING TEMP RANGE	PRODUCT DESCRIPTION
HFA1130MJ/883	-55°C to +125°C	8 Lead Ceramic DIP
HFA1130IJ	-40°C to +85°C	8 Lead Ceramic DIP
HFA1130IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1130IB	-40°C to +85°C	8 Lead SOIC
HFA1130Y	-40°C to +85°C	Die

Pinout

HFA1130
(PDIP, CDIP, SOIC)
TOP VIEW



The Op Amps With Fastest Edges



INPUT 220MHz SIGNAL

OUTPUT (A_V = 2) HFA1130 OP AMP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3369

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Input Voltage ..... V_{SUPPLY}
Differential Input Voltage 5V
Output Current (50% Duty Cycle) 60mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HFA1130I ..... $-40°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP Package	116	36
Plastic DIP Package	98	36
SOIC Package	158	43

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEMP	HFA1130I MIN	HFA1130I TYP	HFA1130I MAX	UNITS
INPUT CHARACTERISTICS					
Input Offset Voltage *	+25°C	-	2	6	mV
	Full	-	-	10	mV
Input Offset Voltage Drift	Full	-	10	-	µV/°C
V_{IO} CMRR ($\Delta V_{CM} = \pm2V$)	+25°C	40	46	-	dB
	Full	38	-	-	dB
V_{IO} PSRR ($\Delta V_S = \pm1.25V$)	+25°C	45	50	-	dB
	Full	42	-	-	dB
Non-Inv. Input Bias Current (+IN = 0V) *	+25°C	-	25	40	µA
	Full	-	-	65	µA
$+I_{BIAS}$ Drift	Full	-	40	-	nA/°C
$+I_{BIAS}$ CMS ($\Delta V_{CM} = \pm2V$)	+25°C	-	20	40	µA/V
	Full	-	-	50	µA/V
Inv. Input Bias Current (-IN = 0V) *	+25°C	-	12	50	µA
	Full	-	-	60	µA
$-I_{BIAS}$ Drift	Full	-	40	-	nA/°C
$-I_{BIAS}$ CMS ($\Delta V_{CM} = \pm2V$)	+25°C	-	1	7	µA/V
	Full	-	-	10	µA/V
$-I_{BIAS}$ PSS ($\Delta V_S = \pm1.25V$)	+25°C	-	6	15	µA/V
	Full	-	-	27	µA/V
Non-Inv. Input Resistance	+25°C	25	50	-	kΩ
Inv. Input Resistance	+25°C	-	16	30	Ω
Input Capacitance (either input)	+25°C	-	2	-	pF
Input Common Mode Range	Full	±2.5	±3.0	-	V
Input Voltage Noise (100kHz) *	+25°C	-	4	-	$nV/\sqrt{Hz}$
+Input Current Noise (100kHz) *	+25°C	-	18	-	$pA/\sqrt{Hz}$
-Input Current Noise (100kHz) *	+25°C	-	21	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS $A_V = +2$, Unless Otherwise Specified					
Open Loop Transimpedance	+25°C	-	500	-	kΩ
-3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$, $A_V = +1$) *	+25°C	530	850	-	MHz
-3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$, $A_V = +2$, $R_F = 360\Omega$)	+25°C	-	670	-	MHz

* See Typical Performance Curve for more information.

Electrical Characteristics V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	HFA1130I MIN	HFA1130I TYP	HFA1130I MAX	UNITS
Gain Flatness (to 100MHz) *	+25°C	-	±0.14	-	dB
Gain Flatness (to 50MHz)	+25°C	-	±0.04	-	dB
Gain Flatness (to 30MHz)	+25°C	-	±0.01	-	dB
Linear Phase Deviation (DC to 100MHz) *	+25°C	-	0.6	-	Degrees
Differential Gain (NTSC, R_L = 75Ω)	+25°C	-	0.03	-	%
Differential Phase (NTSC, R_L = 75Ω)	+25°C	-	0.05	-	Degrees
Minimum Stable Gain	Full	1	-	-	V/V
OUTPUT CHARACTERISTICS A_V = +2, Unless Otherwise Specified					
Output Voltage (A_V = -1) *	+25°C	±3.0	±3.3	-	V
	Full	±2.5	±3.0	-	V
Output Current (R_L = 50Ω, A_V = -1)	+25°C, +85°C	50	65	-	mA
	-40°C	35	50	-	mA
DC Closed Loop Output Impedance	+25°C	-	0.1	-	Ω
2nd Harmonic Distortion (30MHz, V_{OUT} = $2V_{P-P}$) *	+25°C	-	-56	-	dBc
3rd Harmonic Distortion (30MHz, V_{OUT} = $2V_{P-P}$) *	+25°C	-	-80	-	dBc
3rd Order Intercept (100MHz) *	+25°C	20	30	-	dBm
1dB Compression (100MHz)	+25°C	15	20	-	dBm
TRANSIENT RESPONSE A_V = +2, Unless Otherwise Specified					
Rise Time (V_{OUT} = 2.0V Step)	+25°C	-	900	-	ps
Overshoot (V_{OUT} = 2.0V Step) *	+25°C	-	10	-	%
Slew Rate (A_V = +1, V_{OUT} = $5V_{P-P}$)	+25°C	-	1400	-	V/µs
Slew Rate (A_V = +2, V_{OUT} = $5V_{P-P}$)	+25°C	1950	2300	-	V/µs
0.1% Settling (V_{OUT} = 2V to 0V) *	+25°C	-	11	-	ns
0.2% Settling (V_{OUT} = 2V to 0V) *	+25°C	-	7	-	ns
POWER SUPPLY CHARACTERISTICS					
Supply Voltage Range	Full	±4.5	-	±5.5	V
Supply Current*	+25°C	-	21	26	mA
	Full	-	-	33	mA
CLAMP CHARACTERISTICS A_V = +2, V_H = +1V, V_L = -1V, Unless Otherwise Specified					
Clamp Accuracy (V_{IN} = ±2V, A_V = -1)	+25°C	-	60	±125	mV
Clamped Overshoot (V_{IN} = ±1V, Input t_R/t_F = 2ns)	+25°C	-	4	-	%
Overdrive Recovery Time (V_{IN} = ±1V)	+25°C	-	0.75	1.5	ns
Negative Clamp Range	+25°C	-	-5.0 to +2.0	-	V
Positive Clamp Range	+25°C	-	-2.0 to +5.0	-	V
Clamp Input Bias Current	+25°C	-	50	200	µA
Clamp Input Bandwidth (V_H or V_L = $100mV_{P-P}$)	+25°C	-	300	-	MHz

* See Typical Performance Curve for more information.

Application Information

Optimum Feedback Resistor (R_F)

The enclosed plots of inverting and non-inverting frequency response detail the performance of the HFA1130 in various gains. Although the bandwidth dependency on A_{CL} isn't as severe as that of a voltage feedback amplifier, there is an appreciable decrease in bandwidth at higher gains. This decrease can be minimized by taking advantage of the current feedback (CFB) amplifier's unique property of bandwidth dependency on R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications. The R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1130 design is optimized for a 510Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, leading to excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of bandwidth vs. stability. The table below lists recommended R_F values for various gains, and the expected bandwidth.

A_{CL}	R_F (Ω)	BW (MHz)
+1	510	850
-1	430	580
+2	360	670
+5	150	520
+10	180	240
+19	270	125

Clamp Operation

General

The HFA1130 features user programmable output clamps to limit output voltage excursions. Clamping action is obtained by applying voltages to the V_H and V_L terminals (pins 8 & 5) of the amplifier. V_H sets the upper output limit, while V_L sets the lower clamp level. If the amplifier tries to drive the output above V_H, or below V_L, the clamp circuitry limits the output voltage at V_H or V_L (± the clamp accuracy), respectively. The low input bias currents of the clamp pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or DACs.

Clamp Circuitry

Figure 1 shows a simplified schematic of the HFA1130 input stage, and the high clamp (V_H) circuitry. As with all current feedback amplifiers, there is a unity gain buffer (QX1 - QX2) between the positive and negative inputs. This buffer forces -IN to track +IN, and sets up a slewing current of $(V_{-IN} - V_{OUT})/R_F$. This current is mirrored onto the high impedance node (Z) by QX3-QX4, where it is converted to a voltage and fed to the output via another unity gain buffer. If no clamping is utilized, the high impedance node may swing within the limits defined by QP4 and QN4. Note that when the output reaches it's quiescent value, the current flowing through -IN is reduced to only that small current ($-I_{BIAS}$) required to keep the output at the final voltage.

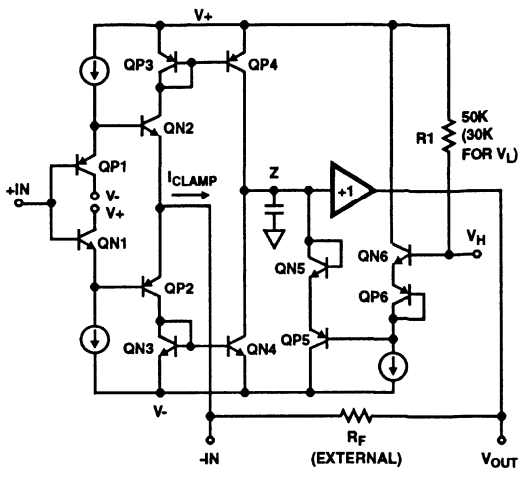


FIGURE 1. HFA1130 SIMPLIFIED V_H CLAMP CIRCUITRY

Tracing the path from V_H to Z illustrates the effect of the clamp voltage on the high impedance node. V_H decreases by $2V_{BE}$ (QN6 and QP6) to set up the base voltage on QP5. QP5 begins to conduct whenever the high impedance node reaches a voltage equal to QP5's base + $2V_{BE}$ (QP5 and QN5). Thus, QP5 clamps node Z whenever Z reaches V_H. R1 provides a pull-up network to ensure functionality with the clamp inputs floating. A similar description applies to the symmetrical low clamp circuitry controlled by V_L.

When the output is clamped, the negative input continues to source a slewing current (I_{CLAMP}) in an attempt to force the output to the quiescent voltage defined by the input. QP5 must sink this current while clamping, because the -IN current is always mirrored onto the high impedance node. The clamping current is calculated as $(V_{-IN} - V_{OUT}) / R_F$. As an example, a unity gain circuit with V_{IN} = 2V, V_H = 1V, and R_F = 510Ω would have $I_{CLAMP} = (2-1)/510\Omega = 1.96mA$. Note that Icc will increase by I_{CLAMP} when the output is clamp limited.

Clamp Accuracy

The clamped output voltage will not be exactly equal to the voltage applied to V_H or V_L. Offset errors, mostly due to V_{BE} mismatches, necessitate a clamp accuracy parameter which is found in the device specifications. Clamp accuracy is a function of the clamping conditions. Referring again to Figure 1, it can be seen that one component of clamp accuracy is the V_{BE} mismatch between the QX6 transistors, and the QX5 transistors. If the transistors always ran at the same current level there would be no V_{BE} mismatch, and no contribution to the inaccuracy. The QX6 transistors are biased at a constant current, but as described earlier, the current through QX5 is equivalent to I_{CLAMP}. V_{BE} increases as I_{CLAMP} increases, causing the clamped output voltage to increase as well. I_{CLAMP} is a function of the overdrive level ($V_{-IN} - V_{OUT\ clamped}$) and R_F, so clamp accuracy degrades as the overdrive increases, or as R_F decreases. As an example, the specified accuracy of ±60mV for a 2X overdrive with R_F = 510Ω

degrades to ±220mV for R_F = 240Ω at the same overdrive, or to ±250mV for a 3X overdrive with R_F = 510Ω.

Consideration must also be given to the fact that the clamp voltages have an effect on amplifier linearity. The "Nonlinearity Near Clamp Voltage" curve in the data sheet illustrates the impact of several clamp levels on linearity.

Clamp Range

Unlike some competitor devices, both V_H and V_L have usable ranges that cross 0V. While V_H must be more positive than V_L, both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HFA1130 could be limited to ECL output levels by setting V_H = -0.8V and V_L = -1.8V. V_H and V_L may be connected to the same voltage (GND for instance) but the result won't be in a DC output voltage from an AC input signal. A 150 - 200mV AC signal will still be present at the output.

Recovery from Overdrive

The output voltage remains at the clamp level as long as the overdrive condition remains. When the input voltage drops below the overdrive level (V_{CLAMP} / A_{VCL}) the amplifier will return to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. The plots of "Unclamped Performance" and "Clamped Performance" highlight the HFA1130's subnanosecond recovery time. The difference between the unclamped and clamped propagation delays is the overdrive recovery time. The appropriate propagation delays are 4.0ns for the unclamped pulse, and 4.8ns for the clamped (2X overdrive) pulse yielding an overdrive recovery time of 800ps. The measurement uses the 90% point of the output transition to ensure that linear operation has resumed. Note: The propagation delay illustrated is dominated by the fixturing. The delta shown is accurate, but the true HFA1130 propagation delay is 500ps.

Use of Die in Hybrid Applications

This amplifier is designed with compensation to negate the package parasitics that typically lead to instabilities. As a result, the use of die in hybrid applications results in overcompensated performance due to lower parasitic capacitances. Reducing R_F below the recommended values for packaged units will solve the problem. For A_V = +2 the recommended starting point is 300Ω, while unity gain applications should try 400Ω.

PC Board Layout

The frequency performance of this amplifier depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value chip (0.1μF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown below.

Evaluation Board

An evaluation board is available for the HFA1130. Please contact your local sales office for information.

The layout and schematic of the board are shown here:

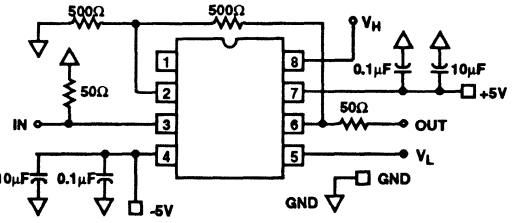
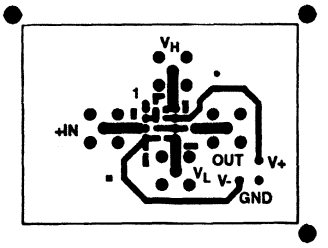
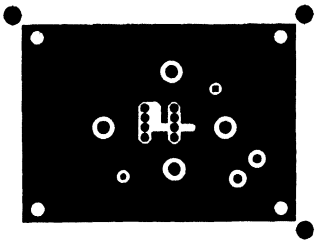


FIGURE 2. BOARD SCHEMATIC

TOP LAYOUT



BOTTOM LAYOUT



Die Characteristics

DIE DIMENSIONS:
63 x 44 x 19 ± 1mils
1600µm x 1130µm ±25.4µm

METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: ALCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC
Gold Eutectic - Ceramic DIP

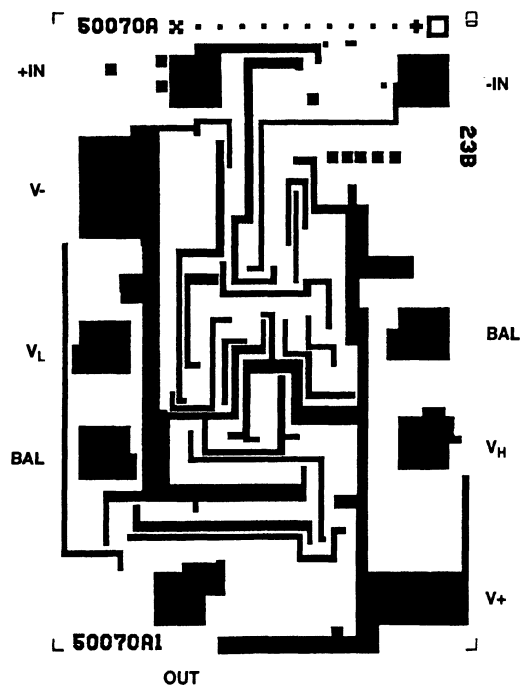
WORST CASE CURRENT DENSITY:
0.909×10^5 A/cm^2

TRANSISTOR COUNT: 52

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1130



Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25°C$, $R_L = 100\Omega$ Unless Otherwise Specified.

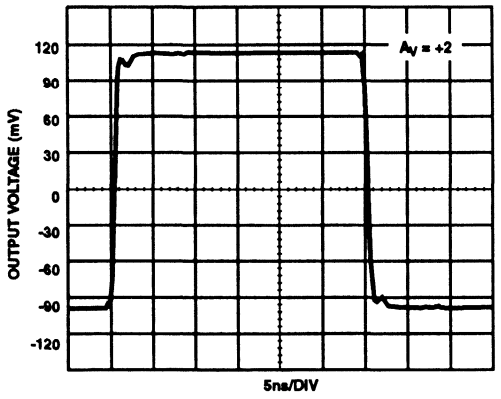


FIGURE 3. SMALL SIGNAL PULSE RESPONSE

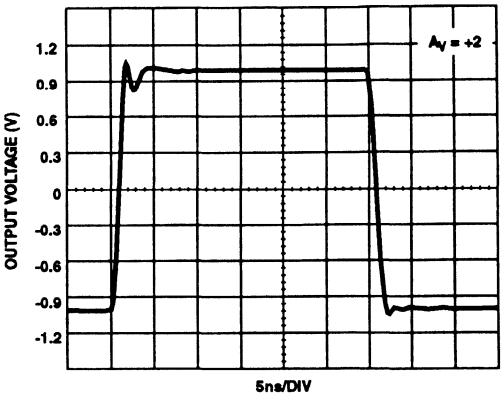


FIGURE 4. LARGE SIGNAL PULSE RESPONSE

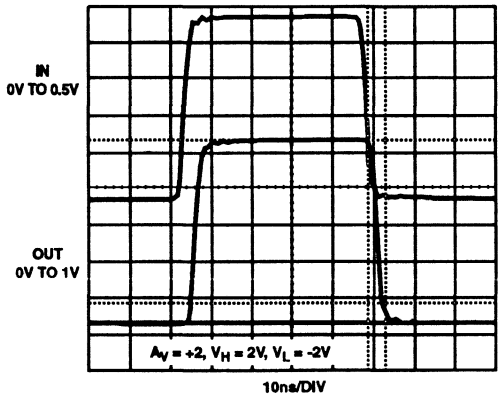


FIGURE 5. UNCLAMPED PERFORMANCE

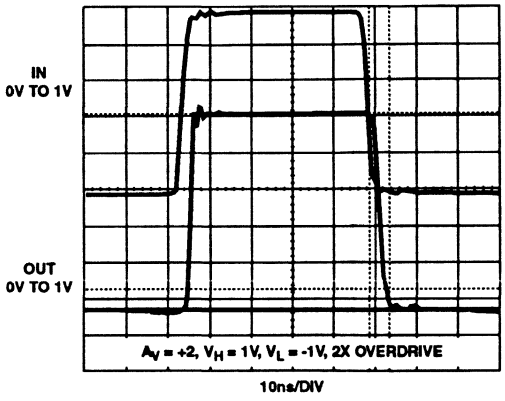


FIGURE 6. CLAMPED PERFORMANCE

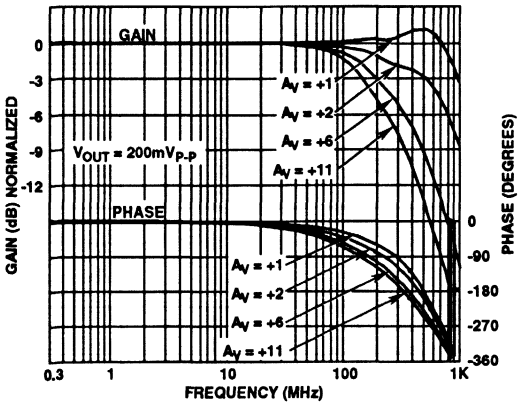


FIGURE 7. NON-INVERTING FREQUENCY RESPONSE

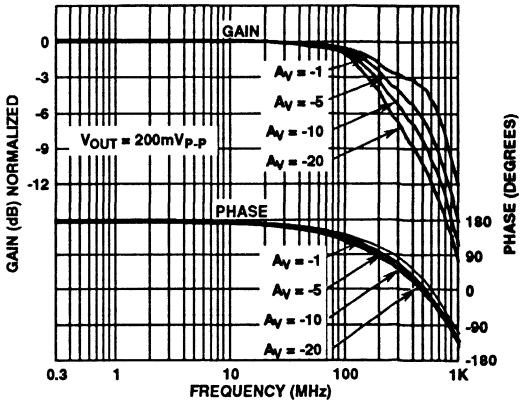


FIGURE 8. INVERTING FREQUENCY RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25°C$, $R_L = 100\Omega$ Unless Otherwise Specified. (Continued)

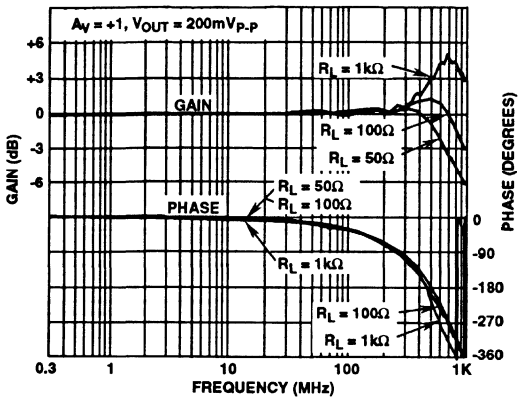


FIGURE 9. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

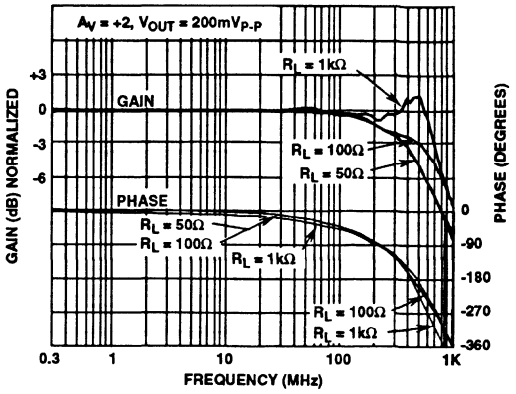


FIGURE 10. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

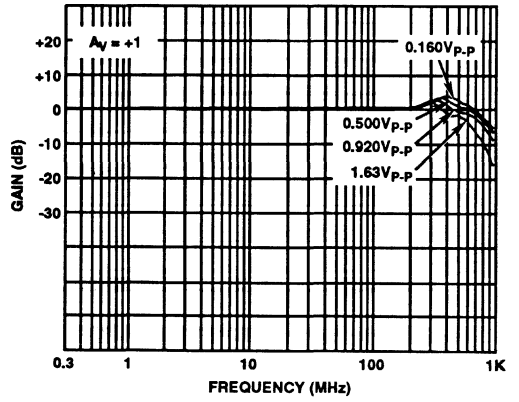


FIGURE 11. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

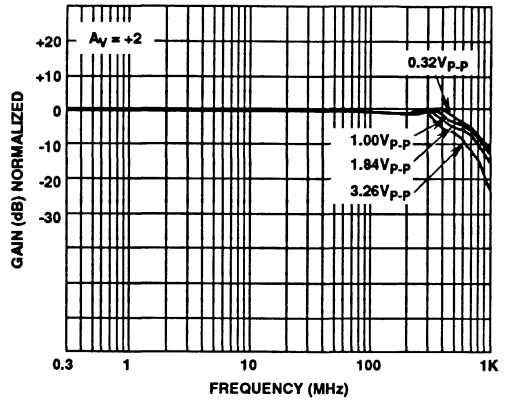


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

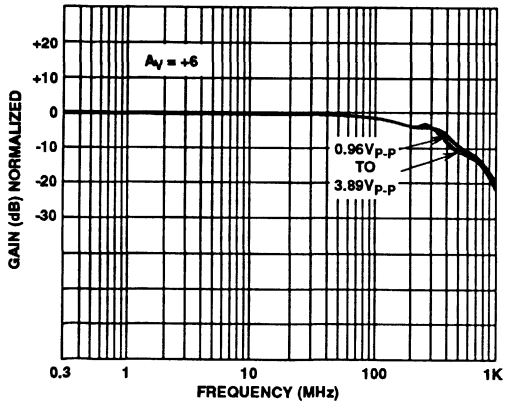


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

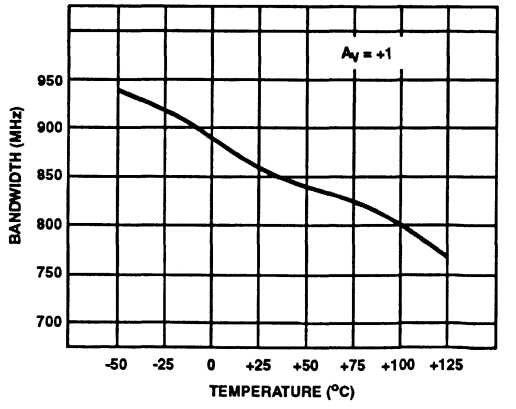


FIGURE 14. -3dB BANDWIDTH vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25°C$, $R_L = 100\Omega$ Unless Otherwise Specified. (Continued)

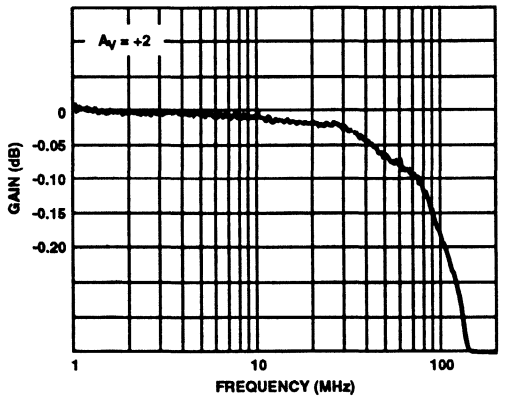


FIGURE 15. GAIN FLATNESS

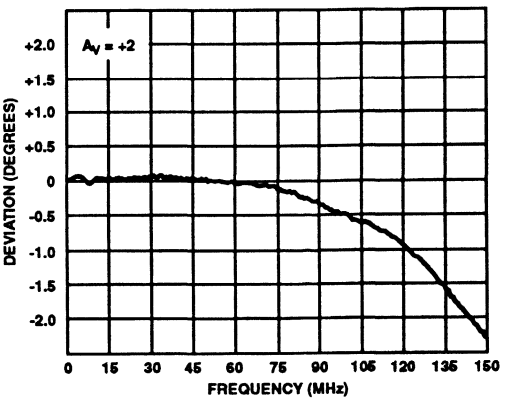


FIGURE 16. DEVIATION FROM LINEAR PHASE

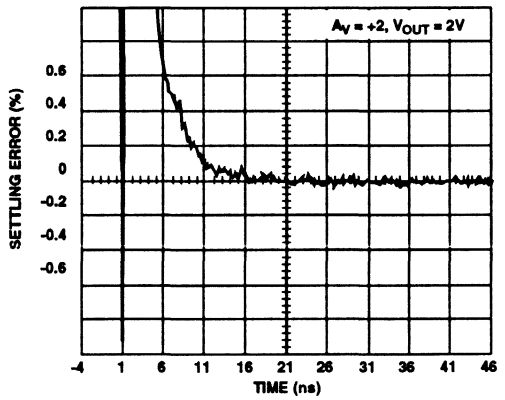


FIGURE 17. SETTLING RESPONSE

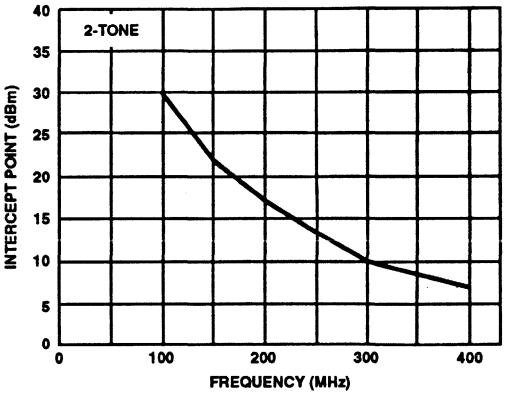


FIGURE 18. 3rd ORDER INTERMODULATION INTERCEPT

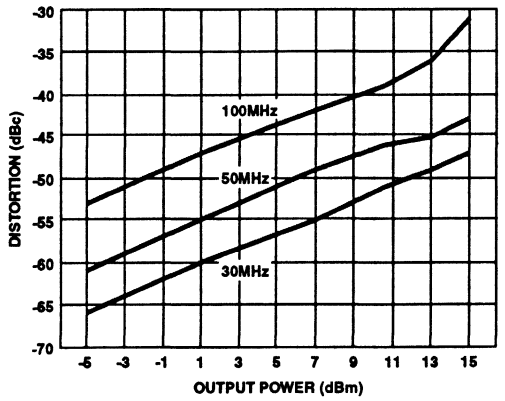


FIGURE 19. 2nd HARMONIC DISTORTION vs P_{OUT}

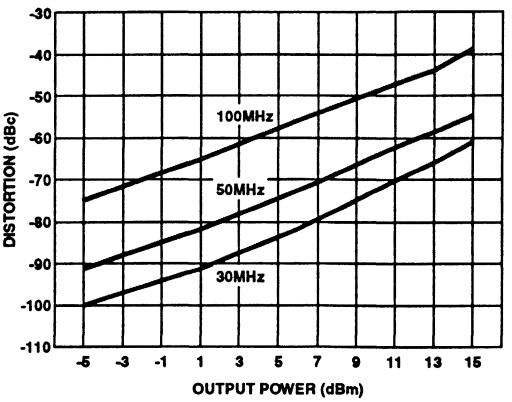


FIGURE 20. 3rd HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25°C$, $R_L = 100\Omega$ Unless Otherwise Specified. (Continued)

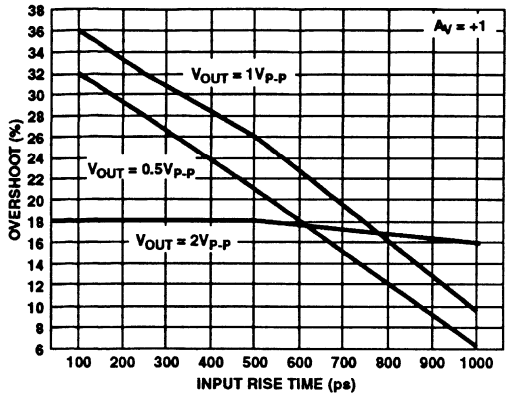


FIGURE 21. OVERSHOOT vs INPUT RISE TIME

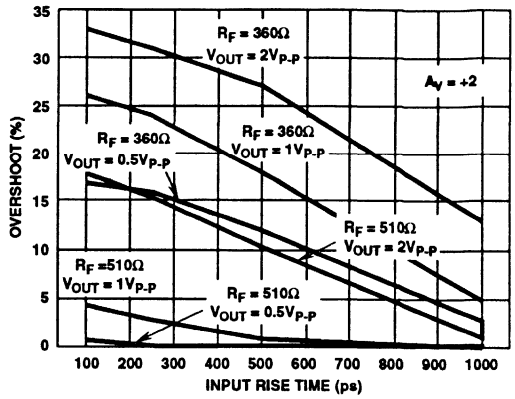


FIGURE 22. OVERSHOOT vs INPUT RISE TIME

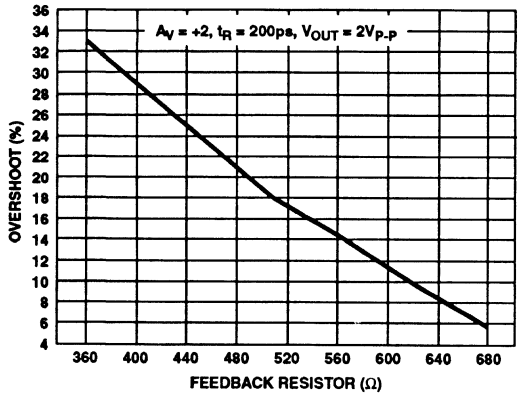


FIGURE 23. OVERSHOOT vs FEEDBACK RESISTOR

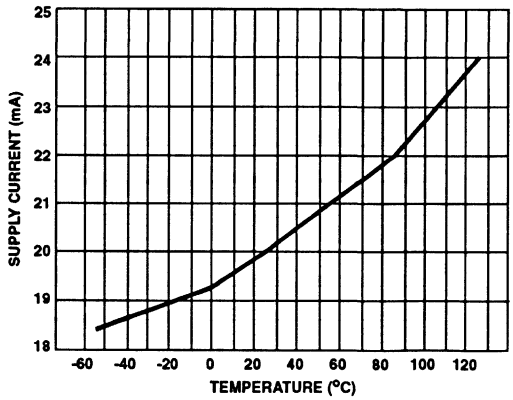


FIGURE 24. SUPPLY CURRENT vs TEMPERATURE

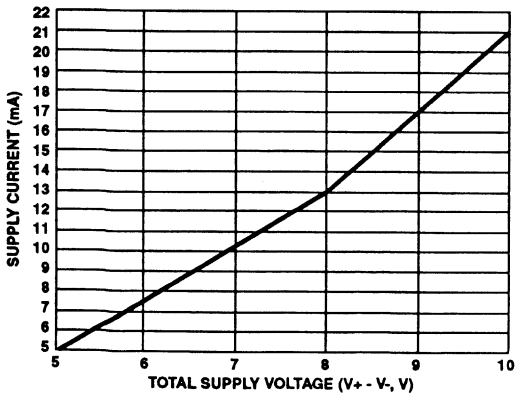


FIGURE 25. SUPPLY CURRENT vs SUPPLY VOLTAGE

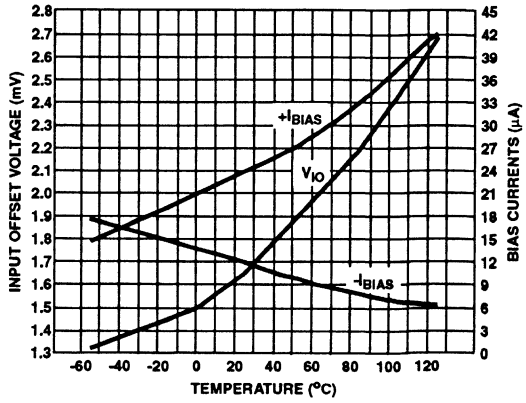


FIGURE 26. V_{IO} AND BIAS CURRENTS vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25°C$, $R_L = 100\Omega$ Unless Otherwise Specified. (Continued)

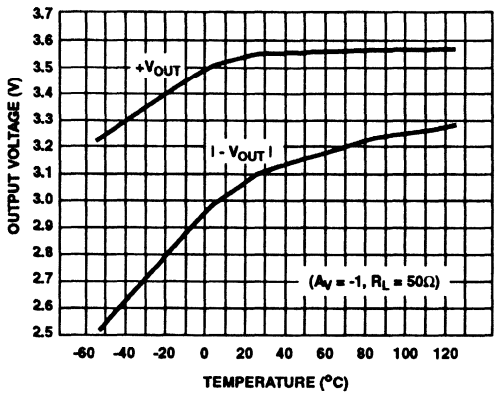


FIGURE 27. OUTPUT VOLTAGE vs TEMPERATURE

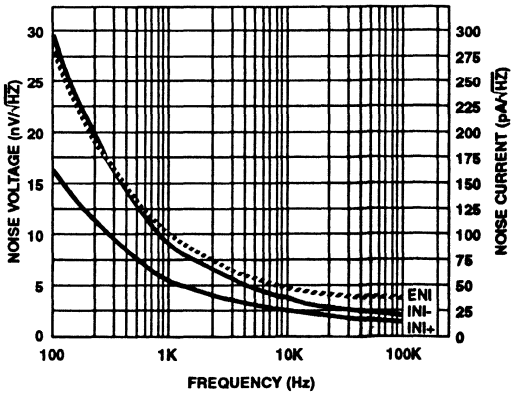


FIGURE 28. INPUT NOISE vs FREQUENCY

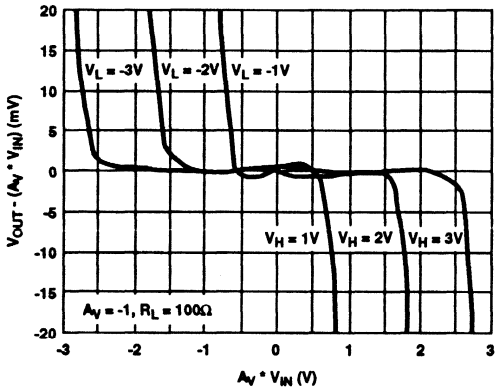


FIGURE 29. NON-LINEARITY NEAR CLAMP VOLTAGE

HARRIS SEMICONDUCTOR

ICL7611, ICL7612

ICL76XX Series Low Power CMOS Operational Amplifiers

March 1993

Features

- **Wide Operating Voltage Range** . . . . . ±1V to ±8V
- **High Input Impedance** . . . . . $10^{12}\ \Omega$
- **Programmable Power Consumption** . . . . Low as 20µW
- **Input Current Lower Than BIFIETs** . . . . . 1pA Typ
- **Output Voltage Swing** . . . . . V+ and V-
- **Input Common Mode Voltage Range Greater Than Supply Rails (ICL7612)**

Applications

- **Portable Instruments**
- **Telephone Headsets**
- **Hearing Aid/Microphone Amplifiers**
- **Meter Amplifiers**
- **Medical Instruments**
- **High Impedance Buffers**

Description

The ICL761X/762X/764X series is a family of monolithic CMOS operational amplifiers. These devices provide the designer with high performance operation at low supply voltages and selectable quiescent currents, and are an ideal design tool when ultra low input current and low power dissipation are desired.

The basic amplifier will operate at supply voltages ranging from ±1V to ±8V, and may be operated from a single Lithium cell.

A unique quiescent current programming pin allows setting of standby current to 1mA, 100µA, or 10µA, with no external components. This results in power consumption as low as 20µW. The output swing ranges to within a few millivolts of the supply voltages.

Of particular significance is the extremely low (1pA) input current, input noise current of $0.01pA/\sqrt{Hz}$, and $10^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications.

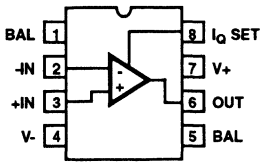
The inputs are internally protected. Outputs are fully protected against short circuits to ground or to either supply.

AC performance is excellent, with a slew rate of 1.6V/µs, and unity gain bandwidth of 1MHz at I_Q = 1mA.

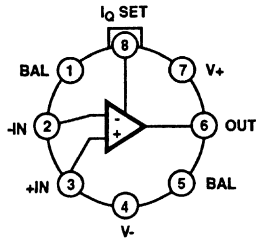
Because of the low power dissipation, junction temperature rise and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

Pinouts (See Ordering Information on Next Page)

ICL7611, ICL7612
(PDIP, SOIC)
TOP VIEW



ICL7611, ICL7612
(METAL CAN)
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7611ACPA	0°C to +70°C	8 Lead Plastic DIP - A Grade
ICL7611BCPA	0°C to +70°C	8 Lead Plastic DIP - B Grade
ICL7611DCPA	0°C to +70°C	8 Lead Plastic DIP - D Grade
ICL7611ACTV	0°C to +70°C	8 Pin TO-99 Metal Can - A Grade
ICL7611BCTV	0°C to +70°C	8 Pin TO-99 Metal Can - B Grade
ICL7611DCTV	0°C to +70°C	8 Pin TO-99 Metal Can - D Grade
ICL7611AMTV	-55°C to +125°C	8 Pin TO-99 Metal Can - A Grade
ICL7611BMTV	-55°C to +125°C	8 Pin TO-99 Metal Can - B Grade
ICL7611DMTV	-55°C to +125°C	8 Pin TO-99 Metal Can - D Grade
ICL7611DCBA	0°C to +70°C	8 Lead SOIC - D Grade
ICL7611DCBA-T	0°C to +70°C	8 Lead SOIC - D Grade - Tape and Reel
ICL7612ACPA	0°C to +70°C	8 Lead Plastic DIP - A Grade
ICL7612BCPA	0°C to +70°C	8 Lead Plastic DIP - B Grade
ICL7612DCPA	0°C to +70°C	8 Lead Plastic DIP - D Grade
ICL7612ACTV	0°C to +70°C	8 Lead TO-99 Metal Can - A Grade
ICL7612BCTV	0°C to +70°C	8 Lead TO-99 Metal Can - B Grade
ICL7612DCTV	0°C to +70°C	8 Lead TO-99 Metal Can - D Grade
ICL7612AMTV	-55°C to +125°C	8 Lead TO-99 Metal Can - A Grade
ICL7612BMTV	-55°C to +125°C	8 Lead TO-99 Metal Can - B Grade
ICL7612DMTV	-55°C to +125°C	8 Lead TO-99 Metal Can - D Grade
ICL7612DCBA	0°C to +70°C	8 Lead SOIC - D Grade
ICL7612DCBA-T	0°C to +70°C	8 Lead SOIC - D Grade - Tape and Reel

Absolute Maximum Ratings

Supply Voltage V+ to V- 18V
Input Voltage ..... V- -0.3 to V+ +0.3V
Differential Input Voltage (Note 1) ..... [(V+ +0.3) - (V- -0.3)]V
Duration of Output Short Circuit (Note 2) ..... Unlimited
Power Dissipation
  At T_A = +25°C 250mW
  Above T_A = +25°C ..... Derate Linearly 2mW/°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
  ICL76XXM ..... -55°C ≤ T_A ≤ +125°C
  ICL76XXC ..... 0°C ≤ T_A ≤ +70°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{SUPPLY} = ±5.0V, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		ICL7611A, ICL7612A			ICL7611B, ICL7612B			ICL7611D, ICL7612D			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \le 100k\Omega$, T_A = +25°C		-	-	2	-	-	5	-	-	15	mV
		$T_{MIN} \le T_A \le T_{MAX}$		-	-	3	-	-	7	-	-	20	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \le 100k\Omega$		-	10	-	-	15	-	-	25	-	µV/°C
Input Offset Current	I_{OS}	T_A = +25°C		-	0.5	30	-	0.5	30	-	0.5	30	pA
		0°C to +70°C		-	-	300	-	-	300	-	-	300	pA
		-55°C to +125°C		-	-	800	-		800	-		800	pA
Input Bias Current	I_{BIAS}	T_A = +25°C		-	1.0	50	-	1.0	50	-	1.0	50	pA
		0°C to +70°C		-	-	400	-	-	400	-	-	400	pA
		-55°C to +125°C		-	-	4000	-	-	4000	-	-	4000	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}	I_Q = 10µA		±4.4	-	-	±4.4	-	-	±4.4	-	-	V
		I_Q = 100µA		±4.2	-	-	±4.2	-	-	±4.2	-	-	V
		I_Q = 1mA		±3.7	-	-	±3.7	-	-	±3.7	-	-	V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}	I_Q = 10µA		±5.3	-	-	±5.3	-	-	±5.3	-	-	V
		I_Q = 100µA		+5.3, -5.1	-	-	+5.3, -5.1	-	-	+5.3, -5.1	-	-	V
		I_Q = 1mA		+5.3, -4.5	-	-	+5.3, -4.5	-	-	+5.3, -4.5	-	-	V
Output Voltage Swing	V_{OUT}	I_Q = 10µA, R_L = 1MΩ	T_A = +25°C	±4.9	-	-	±4.9	-	-	±4.9	-	-	V
			0°C to 70°C	±4.8	-	-	±4.8	-	-	±4.8	-	-	V
			-55°C to +125°C	±4.7	-	-	±4.7	-	-	±4.7	-	-	V
		I_Q = 100µA, R_L = 100kΩ	T_A = +25°C	±4.9	-	-	±4.9	-	-	±4.9	-	-	V
			0°C to 70°C	±4.8	-	-	±4.8	-	-	±4.8	-	-	V
			-55°C to +125°C	±4.5	-	-	±4.5	-	-	±4.5	-	-	V
		I_Q = 1mA, R_L = 10kΩ	T_A = +25°C	±4.5	-	-	±4.5	-	-	±4.5	-	-	V
			0°C to 70°C	±4.3	-	-	±4.3	-	-	±4.3	-	-	V
			-55°C to +125°C	±4.0	-	-	±4.0	-	-	±4.0	-	-	V

Electrical Specifications V_{SUPPLY} = ±5.0V, T_A= +25°C, Unless Otherwise Specified (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS		ICL7611A, ICL7612A			ICL7611B, ICL7612B			ICL7611D, ICL7612D			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Large Signal Voltage Gain	A_{VOL}	V_O = ±4.0V, R_L = 1MΩ, I_Q = 10µA	T_A = +25°C	86	104	-	80	104	-	80	104	-	dB
			0°C to 70°C	80	-	-	75	-	-	75	-	-	dB
			-55°C to +125°C	74	-	-	68	-	-	68	-	-	dB
		V_O = ±4.0V, R_L = 100kΩ, I_Q = 100µA	T_A = +25°C	86	102	-	80	102	-	80	102	-	dB
			0°C to 70°C	80	-	-	75	-	-	75	-	-	dB
			-55°C to +125°C	74	-	-	68	-	-	68	-	-	dB
		V_O = ±4.0V, R_L = 10kΩ, I_Q = 1mA	T_A = +25°C	80	83	-	76	83	-	76	83	-	dB
			0°C to 70°C	76	-	-	72	-	-	72	-	-	dB
			-55°C to +125°C	72	-	-	68	-	-	68	-	-	dB
Unity Gain Bandwidth	GBW	I_Q = 10µA		-	0.044	-	-	0.044	-	-	0.044	-	MHz
		I_Q = 100µA		-	0.48	-	-	0.48	-	-	0.48	-	MHz
		I_Q = 1mA		-	1.4	-	-	1.4	-	-	1.4	-	MHz
Input Resistance	R_{IN}			-	10^{12}	-	-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	R_S ≤ 100kΩ, I_Q = 10µA		76	96	-	70	96	-	70	96	-	dB
		R_S ≤ 100kΩ, I_Q = 100µA		76	91	-	70	91	-	70	91	-	dB
		R_S ≤ 100kΩ, I_Q = 1mA		66	87	-	60	87	-	60	87	-	dB
Power Supply Rejection Ratio V_{SUPPLY} = ±8V to ±2V	PSRR	R_S ≤ 100kΩ, I_Q = 10µA		80	94	-	80	94	-	80	94	-	dB
		R_S ≤ 100kΩ, I_Q = 100µA		80	86	-	80	86	-	80	86	-	dB
		R_S ≤ 100kΩ, I_Q = 1mA		70	77	-	70	77	-	70	77	-	dB
Input Referred Noise Voltage	e_N	R_S = 100Ω, f = 1kHz		-	100	-	-	100	-	-	100	-	$nV/\sqrt{Hz}$
Input Referred Noise Current	i_N	R_S = 100Ω, f = 1kHz		-	0.01	-	-	0.01	-	-	0.01	-	$pA/\sqrt{Hz}$
Supply Current	I_{SUPPLY}	No Signal, No Load	I_Q SET = +5V, Low Bias	-	0.01	0.02	-	0.01	0.02	-	0.01	0.02	mA
			I_Q SET = 0V, Medium Bias	-	0.1	0.25	-	0.1	0.25	-	0.1	0.25	mA
			I_Q SET = -5V , High Bias	-	1.0	2.5	-	1.0	2.5	-	1.0	2.5	mA
Channel Separation	V_{O1}/V_{O2}	A_V = 100		-	120	-	-	120	-	-	120	-	dB
Slew Rate	SR	A_V = 1, C_L = 100pF V_{IN} = $8V_{P-P}$	I_Q = 10µA, R_L = 1MΩ	-	0.016	-	-	0.016	-	-	0.016	-	V/µs
			I_Q = 100µA, R_L = 100kΩ	-	0.16	-	-	0.16	-	-	0.16	-	V/µs
			I_Q = 1mA, R_L = 10kΩ	-	1.6	-	-	1.6	-	-	1.6	-	V/µs
Rise Time	t_R	V_{IN} = 50mV, C_L = 100pF	I_Q = 10µA, R_L = 1MΩ	-	20	-	-	20	-	-	20	-	µs
			I_Q = 100µA, R_L = 100kΩ	-	2	-	-	2	-	-	2	-	µs
			I_Q = 1mA, R_L = 10kΩ	-	0.9	-	-	0.9	-	-	0.9	-	µs

Electrical Specifications V_{SUPPLY} = ±5.0V, T_A= +25°C, Unless Otherwise Specified (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS		ICL7611A, ICL7612A			ICL7611B, ICL7612B			ICL7611D, ICL7612D			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Overshoot Factor	OS	V_{IN} = 50mV, C_L = 100pF	I_Q = 10µA, R_L = 1MΩ	-	5	-	-	5	-	-	5	-	%
			I_Q = 100µA, R_L = 100kΩ	-	10	-	-	10	-	-	10	-	%
			I_Q = 1mA, R_L = 10kΩ	-	40	-	-	40	-	-	40	-	%

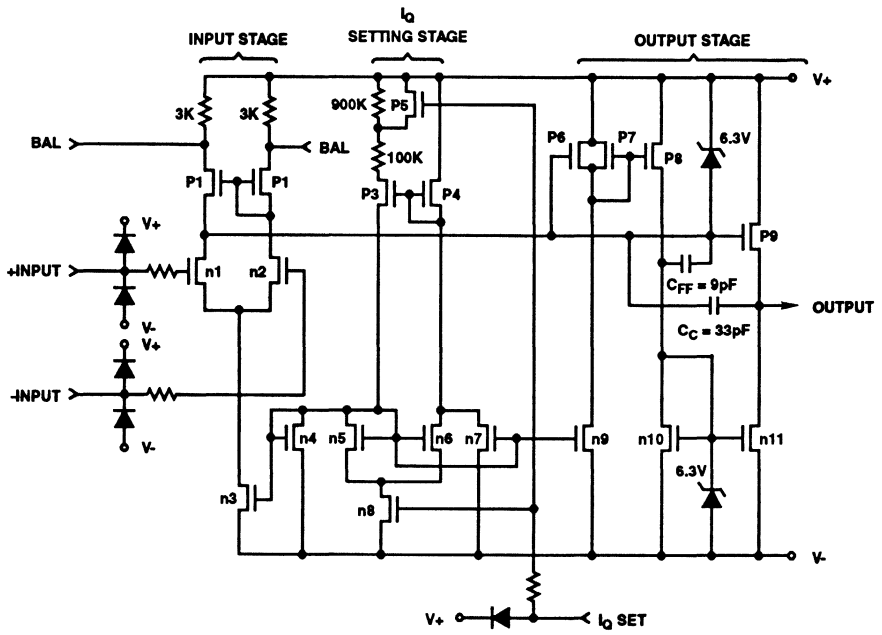
NOTES:

1. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
2. The outputs may be shorted to ground or to either supply, for $V_{SUPP} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.

Electrical Specifications V_{SUPPLY} = ±1.0V, I_Q = 10µA, T_A= +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		ICL7611A, ICL7612A			ICL7611B, ICL7612B			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$	T_A = +25°C	-	-	2	-	-	5	mV
			$T_{MIN} \leq T_A \leq T_{MAX}$	-	-	3	-	-	7	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$		-	10	-	-	15	-	µV/°C
Input Offset Current	I_{OS}	T_A = +25°C		-	0.5	30	-	0.5	30	pA
		0°C to +70°C		-	-	300	-	-	300	pA
Input Bias Current	I_{BIAS}	T_A = +25°C		-	1.0	50	-	1.0	50	pA
		0°C to +70°C		-	-	500	-	-	500	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}			±0.6	-	-	±0.6	-	-	V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}			+0.6 to -1.1	-	-	+0.6 to -1.1	-	-	V
Output Voltage Swing	V_{OUT}	R_L = 1MΩ	T_A = +25°C	±0.98	-	-	±0.98	-	-	V
			0°C to +70°C	±0.96	-	-	±0.96	-	-	V
Large Signal Voltage Gain	A_{VOL}	V_O = ±0.1V, R_L = 1MΩ	T_A = +25°C	-	90	-	-	90	-	dB
			0°C to +70°C	-	80	-	-	80	-	dB
Unity Gain Bandwidth	GBW			-	0.044	-	-	0.044	-	MHz
Input Resistance	R_{IN}			-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega$		-	80	-	-	80	-	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 100k\Omega$		-	80	-	-	80	-	dB
Input Referred Noise Voltage	e_N	R_S = 100Ω, f = 1kHz		-	100	-	-	100	-	$nV/\sqrt{Hz}$
Input Referred Noise Current	i_N	R_S = 100Ω, f = 1kHz		-	0.01	-	-	0.01	-	$pA/\sqrt{Hz}$
Supply Current	I_{SUPPLY}	No Signal, No Load		-	6	15	-	6	15	µA
Slew Rate	SR	A_V = 1, C_L = 100pF, V_{IN} = 0.2V_{P-P}, R_L = 1MΩ		-	0.016	-	-	0.016	-	V/µs
Rise Time	t_R	V_{IN} = 50mV, C_L = 100pF R_L = 1MΩ		-	20	-	-	20	-	µs
Overshoot Factor	OS	V_{IN} = 50mV, C_L = 100pF, R_L = 1MΩ		-	5	-	-	5	-	%

Functional Diagram



Typical Performance Curves

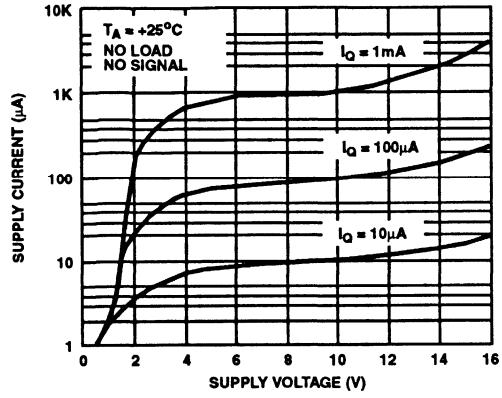


FIGURE 1. SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

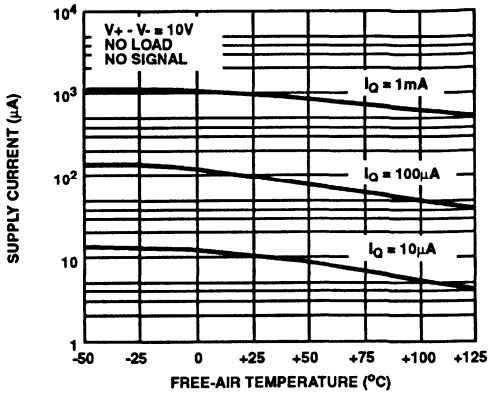


FIGURE 2. SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE

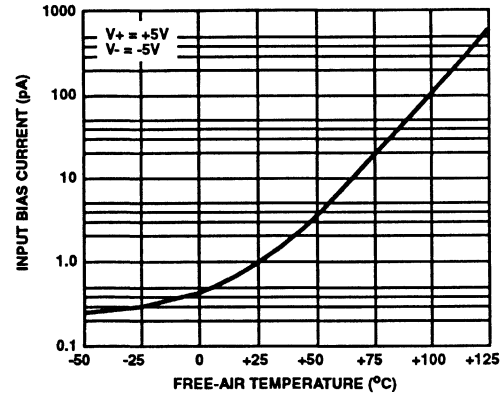


FIGURE 3. INPUT BIAS CURRENT vs TEMPERATURE

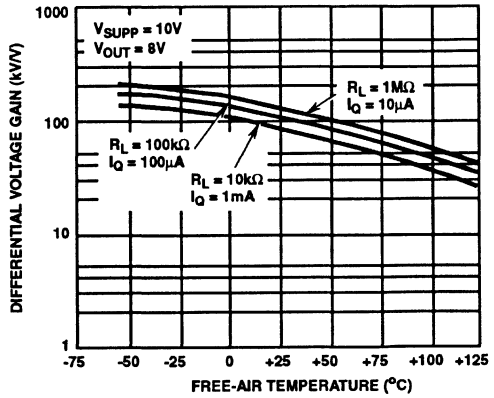


FIGURE 4. LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN vs FREE-AIR TEMPERATURE

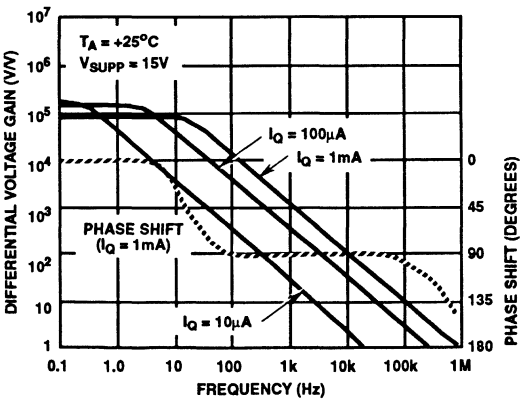


FIGURE 5. LARGE SIGNAL FREQUENCY RESPONSE

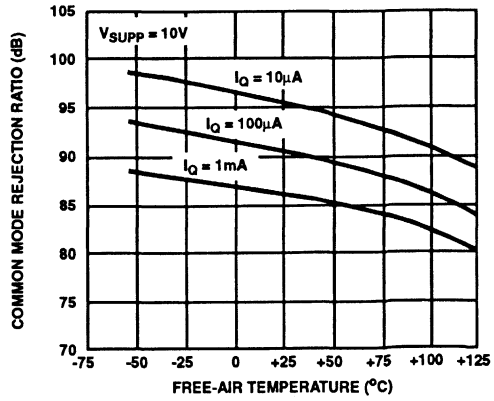


FIGURE 6. COMMON MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

Typical Performance Curves (Continued)

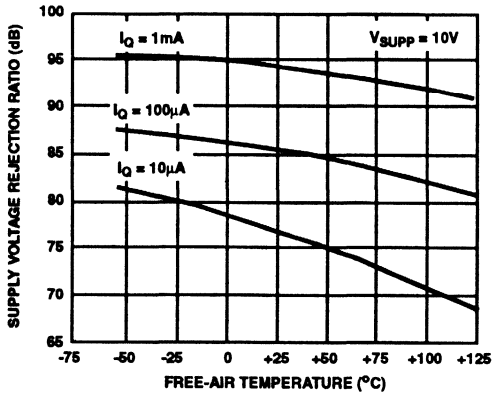


FIGURE 7. POWER SUPPLY REJECTION RATIO vs FREE-AIR TEMPERATURE

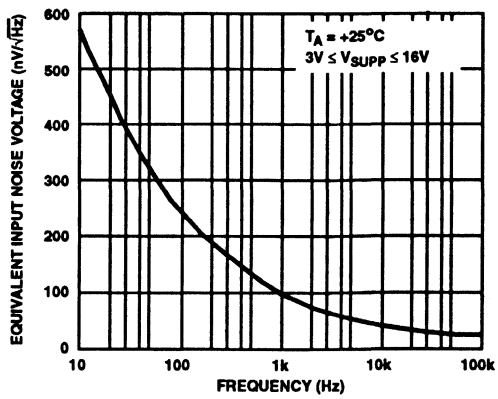


FIGURE 8. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

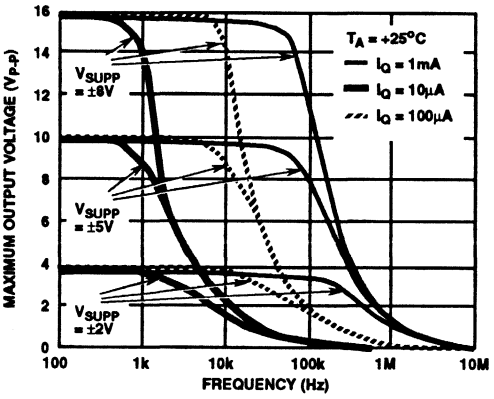


FIGURE 9. OUTPUT VOLTAGE vs FREQUENCY

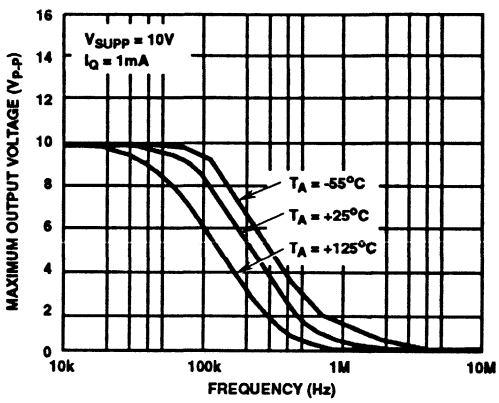


FIGURE 10. OUTPUT VOLTAGE vs FREQUENCY

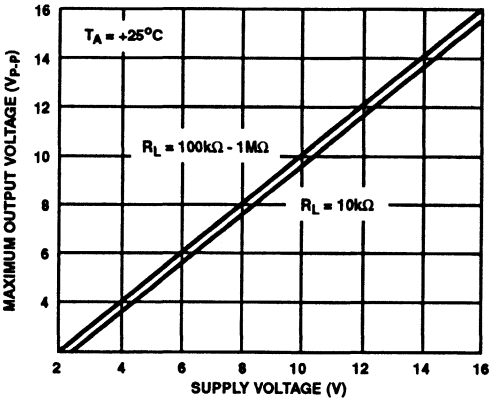


FIGURE 11. OUTPUT VOLTAGE vs SUPPLY VOLTAGE

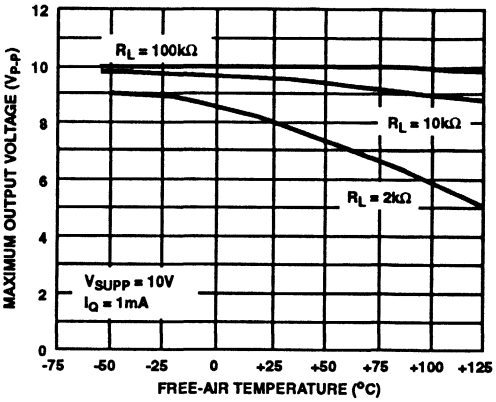


FIGURE 12. OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

Typical Performance Curves (Continued)

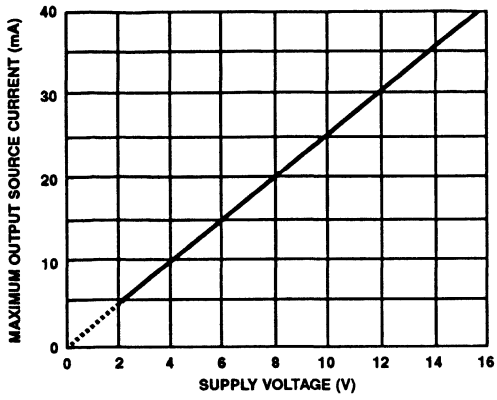


FIGURE 13. OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE

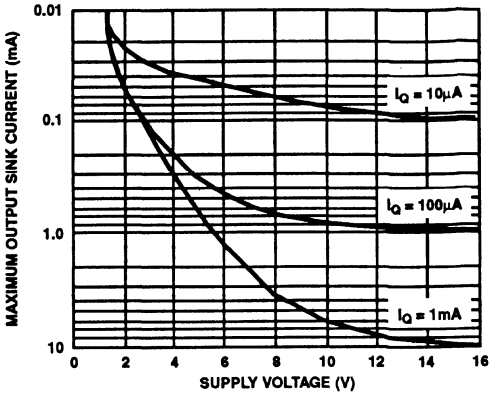


FIGURE 14. OUTPUT SINK CURRENT vs SUPPLY VOLTAGE

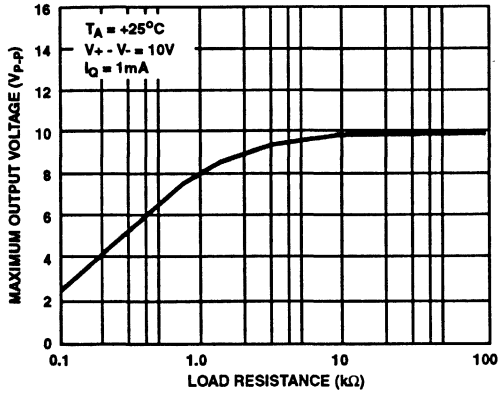


FIGURE 15. OUTPUT VOLTAGE vs LOAD RESISTANCE

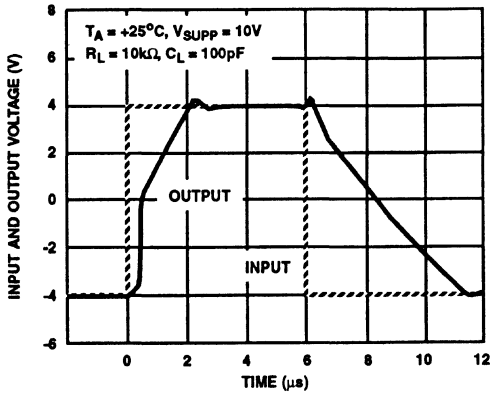


FIGURE 16. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 1mA)

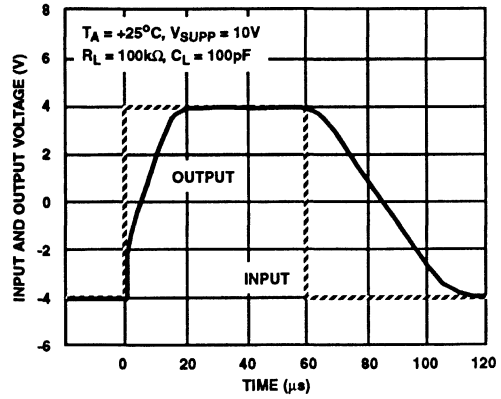


FIGURE 17. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 100µA)

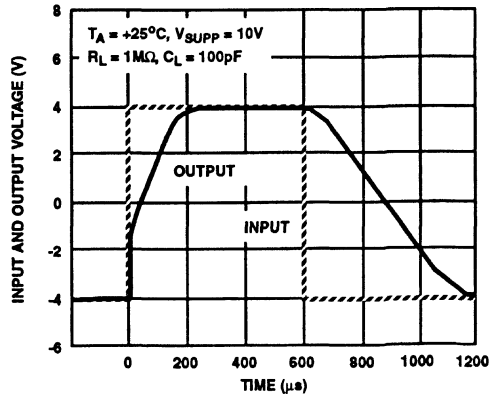


FIGURE 18. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 10µA)

Detailed Description

Static Protection

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

Latchup Avoidance

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (p-n-p-n) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. In general, the op-amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2mA to prevent latchup.

Choosing the Proper I_Q

The ICL7611 and ICL7612 have a similar I_Q set-up scheme, which allows the amplifier to be set to nominal quiescent currents of 10µA, 100µA or 1mA. These current settings change only very slightly over the entire supply voltage range. The ICL7611/12 have an external I_Q control terminal, permitting user selection of quiescent current. To set the I_Q connect the I_Q terminal as follows:

I_Q = 10µA - I_Q pin to V+

I_Q = 100µA - I_Q pin to ground. If this is not possible, any voltage from V+ - 0.8 to V- +0.8 can be used.

I_Q = 1mA - I_Q pin to V-

NOTE: The output current available is a function of the quiescent current setting. For maximum p-p output voltage swings into low impedance loads, I_Q of 1mA should be selected.

Output Stage and Load Driving Considerations

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the I_Q settings. This allows output swings to almost the supply rails for output loads of 1MΩ, 100kΩ, and 10kΩ, using the output stage in a highly linear class A mode. In this mode, cross-over distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB for higher output currents. (See graphs under Typical Operating Characteristics). During the transition from Class A to Class B operation, the output transfer characteristic is non-linear and the voltage gain decreases.

Input Offset Nulling

Offset nulling may be achieved by connecting a 25K pot between the BAL terminals with the wiper connected to V+. At quiescent currents of 1mA the nulling range provided is adequate for all V_{OS} selections; however with I_Q = 10µA and 100µA, nulling may not be possible with higher values of V_{OS}.

Frequency Compensation

The ICL7611 and ICL7612 are internally compensated, and are stable for closed loop gains as low as unity with capacitive loads up to 100pF.

Extended Common Mode Input Range

The ICL7612 incorporates additional processing which allows the input CMVR to exceed each power supply rail by 0.1V for applications where $V_{SUPP} \geq \pm 1.5V$. For those applications where $V_{SUPP} \leq \pm 1.5V$ the input CMVR is limited in the positive direction, but may exceed the negative supply rail by 0.1V in the negative direction (e.g. for $V_{SUPP} = \pm 1.0V$, the input CMVR would be +0.6V to -1.1V).

Operation At $V_{SUPP} = \pm 1.0V$

Operation at $V_{SUPP} = \pm 1.0V$ is guaranteed at I_Q = 10µA for A and B grades only.

Output swings to within a few millivolts of the supply rails are achievable for $R_L \geq 1M\Omega$. Guaranteed input CMVR is ±0.6V minimum and typically +0.9V to -0.7V at $V_{SUPP} = \pm 1.0V$. For applications where greater common mode range is desirable, refer to the description of ICL7612 above.

Applications

The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup.

Note that in no case is I_Q shown. The value of I_Q must be chosen by the designer with regard to frequency response and power dissipation.

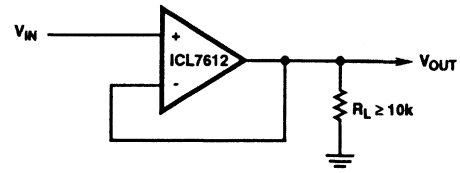


FIGURE 19. SIMPLE FOLLOWER*

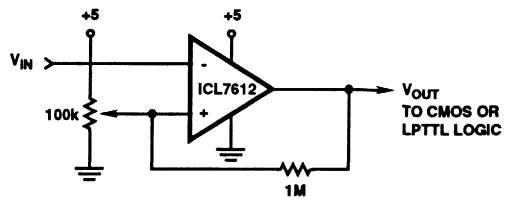
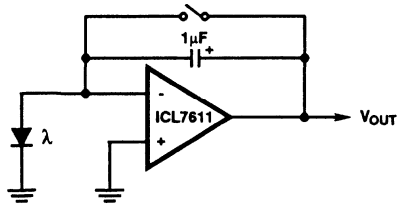


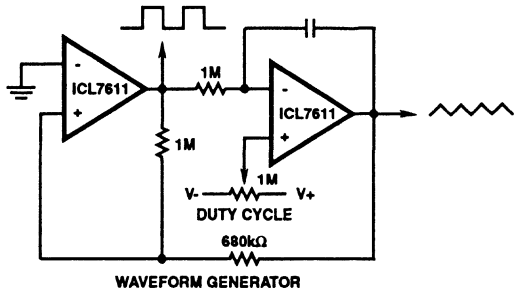
FIGURE 20. LEVEL DETECTOR*

* By using the ICL7612 in this application, the circuit will follow rail to rail inputs.



* Low leakage currents allow integration times up to several hours.

FIGURE 21. PHOTOCURRENT INTEGRATOR



Since the output range swings exactly from rail to rail, frequency and duty cycle are virtually independent of power supply variations.

FIGURE 22. PRECISE TRIANGLE/SQUARE WAVE GENERATOR

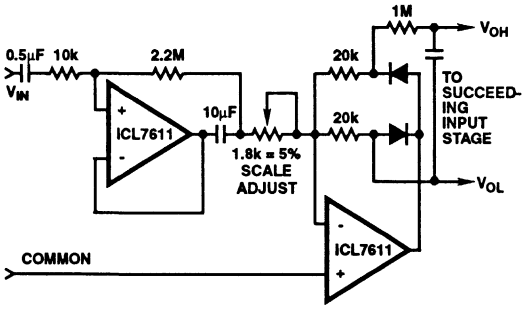


FIGURE 23. AVERAGING AC TO DC CONVERTER FOR A/D CONVERTERS SUCH AS ICL7106, ICL7107, ICL7109, ICL7116, ICL7117

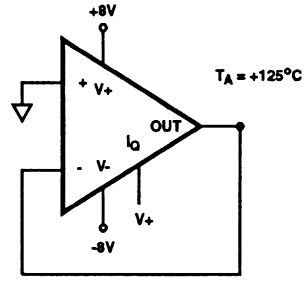


FIGURE 24. BURN-IN AND LIFE TEST CIRCUIT

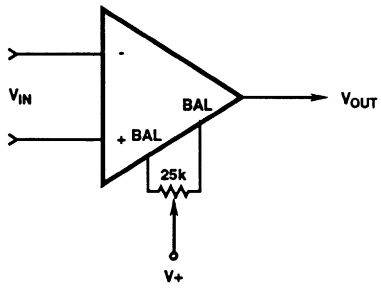
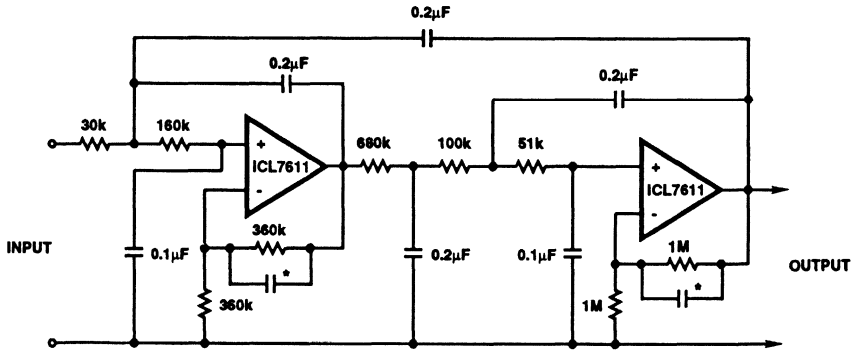


FIGURE 25. V_{OS} NULL CIRCUIT



The low bias currents permit high resistance and low capacitance values to be used to achieve low frequency cutoff. f_C = 10Hz, A_{VCL} = 4, Passband ripple = 0.1dB.

*Note that small capacitors (25 - 50pF) may be needed for stability in some cases.

FIGURE 26. FIFTH ORDER CHEBYSHEV MULTIPLE FEEDBACK LOW PASS FILTER

HARRIS SEMICONDUCTOR

ICL7621,ICL7641 ICL7642

ICL76XX Series Low Power CMOS Operational Amplifiers

March 1993

Features

- Wide Operating Voltage Range ..... ±1V to ±8V
- High Input Impedance ..... $10^{12}\ \Omega$
- Input Current Lower Than BIFIETs ..... 1pA Typ
- Output Voltage Swing ..... V+ and V-
- Available as Duals and Quads (Refer to ICL7611 for Singles)
- Low Power Replacement for Many Standard Op Amps

Applications

- Portable Instruments
- Telephone Headsets
- Hearing Aid/Microphone Amplifiers
- Meter Amplifiers
- Medical Instruments
- High Impedance Buffers

Description

The ICL761X/762X/764X series is a family of monolithic CMOS operational amplifiers. These devices provide the designer with high performance operation at low supply voltages and selectable quiescent currents. They are an ideal design tool when ultra low input current and low power dissipation are desired.

The basic amplifier will operate at supply voltages ranging from ±1V to ±8V, and may be operated from a single Lithium cell. The output swing ranges to within a few millivolts of the supply voltages.

The quiescent supply current of these amplifiers is set to 3 different ranges at the factory. Both amps of the dual ICL7621 are set to an I_Q of 100µA, while each amplifier of the quad ICL7641 and ICL7642 are set to an I_Q of 1mA and 10µA respectively. This results in power consumption as low as 20µW per amplifier.

Of particular significance is the extremely low (1pA) input current, input noise current of $0.01pA/\sqrt{Hz}$, and $10^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications.

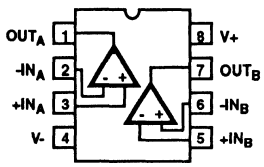
The inputs are internally protected. Outputs are fully protected against short circuits to ground or to either supply.

AC performance is excellent, with a slew rate of 1.6V/µs, and unity gain bandwidth of 1MHz at I_Q = 1mA.

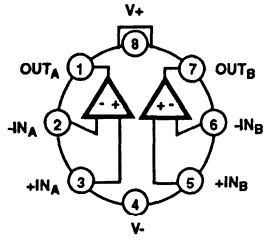
Because of the low power dissipation, junction temperature rise and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

Pinouts (See Ordering Information on Next Page)

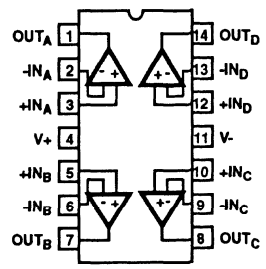
ICL7621 (PDIP, SOIC) TOP VIEW



ICL7621 (METAL CAN) TOP VIEW



ICL7641 (PDIP)
ICL7642 (CDIP, PDIP) TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3403**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7621ACPA	0°C to +70°C	8 Lead Plastic DIP - A Grade - I_Q = 100µA
ICL7621BCPA	0°C to +70°C	8 Lead Plastic DIP - B Grade - I_Q = 100µA
ICL7621DCPA	0°C to +70°C	8 Lead Plastic DIP - D Grade - I_Q = 100µA
ICL7621ACTV	0°C to +70°C	8 Pin TO-99 Metal Can - A Grade - I_Q = 100µA
ICL7621BCTV	0°C to +70°C	8 Pin TO-99 Metal Can - B Grade - I_Q = 100µA
ICL7621DCTV	0°C to +70°C	8 Pin TO-99 Metal Can - D Grade - I_Q = 100µA
ICL7621AMTV	-55°C to +125°C	8 Pin TO-99 Metal Can - A Grade - I_Q = 100µA
ICL7621BMTV	-55°C to +125°C	8 Pin TO-99 Metal Can - B Grade - I_Q = 100µA
ICL7621DMTV	-55°C to +125°C	8 Pin TO-99 Metal Can - D Grade - I_Q = 100µA
ICL7621DCBA	0°C to +70°C	8 Lead SOIC - D Grade - I_Q = 100µA
ICL7621DCBA-T	0°C to +70°C	8 Lead SOIC - D Grade - Tape and Reel - I_Q = 100µA
ICL7641CCPD	0°C to +70°C	14 Lead Plastic DIP - C Grade - I_Q = 1mA
ICL7641ECPD	0°C to +70°C	14 Lead Plastic DIP - E Grade - I_Q = 1mA
ICL7642CCPD	0°C to +70°C	14 Lead Plastic DIP - C Grade - I_Q = 10µA
ICL7642ECPD	0°C to +70°C	14 Lead Plastic DIP - E Grade - I_Q = 10µA
ICL7642CCJD	0°C to +70°C	14 Lead Ceramic DIP - C Grade - I_Q = 10µA
ICL7642CMJD	-55°C to +125°C	14 Lead Ceramic DIP - C Grade - I_Q = 10µA
ICL7642EMJD	-55°C to +125°C	14 Lead Ceramic DIP - E Grade - I_Q = 10µA

Absolute Maximum Ratings

Supply Voltage V+ to V- 18V
Input Voltage ..... V- -0.3 to V+ +0.3V
Differential Input Voltage (Note 1) ..... [(V+ +0.3) - (V- -0.3)]V
Duration of Output Short Circuit (Note 2) ..... Unlimited
Power Dissipation
8 Lead Mini Dip and TO-99:
At T_A = +25°C 250mW
Above T_A = +25°C ..... Derate Linearly 2mW/°C
14 Lead Plastic DIP:
At T_A = +25°C 375mW
Above T_A = +25°C ..... Derate Linearly 3mW/°C
14 Lead Ceramic DIP:
At T_A = +25°C 500mW
Above T_A = +25°C ..... Derate Linearly 4mW/°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
ICL76XXM ..... -55°C ≤ T_A ≤ +125°C
ICL76XXC ..... 0°C ≤ T_A ≤ +70°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{SUPPLY} = ±5.0V, T_A= +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		ICL7621A			ICL7621B			ICL7621D			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \le 100k\Omega$	T_A = +25°C	-	-	2	-	-	5	-	-	15	mV
			$T_{MIN} \le T_A \le T_{MAX}$	-	-	3	-	-	7	-	-	20	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \le 100k\Omega$		-	10	-	-	15	-	-	25	-	µV/°C
Input Offset Current	I_{OS}	T_A = +25°C		-	0.5	30	-	0.5	30	-	0.5	30	pA
		0°C to +70°C		-	-	300	-	-	300	-	-	300	pA
		-55°C to +125°C		-	-	800	-		800	-		800	pA
Input Bias Current	I_{BIAS}	T_A = +25°C		-	1.0	50	-	1.0	50	-	1.0	50	pA
		0°C to +70°C		-	-	400	-	-	400	-	-	400	pA
		-55°C to +125°C		-	-	4000	-	-	4000	-	-	4000	pA
Common Mode Voltage Range	V_{CMR}	I_Q = 100µA		±4.2	-	-	±4.2	-	-	±4.2	-	-	V
Output Voltage Swing	V_{OUT}	I_Q = 100µA, R_L = 100kΩ	T_A = +25°C	±4.9	-	-	±4.9	-	-	±4.9	-	-	V
			0°C to 70°C	±4.8	-	-	±4.8	-	-	±4.8	-	-	V
			-55°C to +125°C	±4.5	-	-	±4.5	-	-	±4.5	-	-	V
Large Signal Voltage Gain	A_{VOL}	V_O = ±4.0V, R_L = 100kΩ, I_Q = 100µA	T_A = +25°C	86	102	-	80	102	-	80	102	-	dB
			0°C to +70°C	80	-	-	75	-	-	75	-	-	dB
			-55°C to +125°C	74	-	-	68	-	-	68	-	-	dB
Unity Gain Bandwidth	GBW	I_Q = 100µA		-	0.48	-	-	0.48	-	-	0.48	-	MHz
Input Resistance	R_{IN}			-	10^{12}	-	-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	$R_S \le 100k\Omega$, I_Q = 100µA		76	91	-	70	91	-	70	91	-	dB

Electrical Specifications V_{SUPPLY} = ±5.0V, T_A= +25°C, Unless Otherwise Specified (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS	ICL7621A			ICL7621B			ICL7621D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Rejection Ratio V_{SUPPLY} = ±8V to ±2V	PSRR	$R_S \leq 100k\Omega$, I_Q = 100µA	80	86	-	80	86	-	80	86	-	dB
Input Referred Noise Voltage	e_N	R_S = 100Ω, f = 1kHz	-	100	-	-	100	-	-	100	-	$nV/\sqrt{Hz}$
Input Referred Noise Current	i_N	R_S = 100Ω, f = 1kHz	-	0.01	-	-	0.01	-	-	0.01	-	$pA/\sqrt{Hz}$
Supply Current (per Amplifier)	I_{SUPPLY}	No Signal, No Load, I_Q = 100µA	-	0.1	0.25	-	0.1	0.25	-	0.1	0.25	mA
Channel Separation	V_{O1}/V_{O2}	A_V = 100	-	120	-	-	120	-	-	120	-	dB
Slew Rate	SR	A_V = 1, C_L = 100pF V_{IN} = 8Vp-p, I_Q = 100µA, R_L = 100kΩ	-	0.16	-	-	0.16	-	-	0.16	-	V/µs
Rise Time	t_R	V_{IN} = 50mV, C_L = 100pF I_Q = 100µA, R_L = 100kΩ	-	2	-	-	2	-	-	2	-	µs
Overshoot Factor	OS	V_{IN} = 50mV, C_L = 100pF I_Q = 100µA, R_L = 100kΩ	-	10	-	-	10	-	-	10	-	%

NOTES:

1. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
2. The outputs may be shorted to ground or to either supply, for $V_{SUPP} \leq$ 10V. Care must be taken to insure that the dissipation rating is not exceeded.

Electrical Specifications V_{SUPPLY} = ±5.0V, T_A= +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		ICL7641C, ICL7642C			ICL7641E, ICL7642E			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$	T_A = +25°C	-	-	10	-	-	20	mV
			$T_{MIN} \leq T_A \leq T_{MAX}$	-	-	15	-	-	25	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$		-	20	-	-	30	-	µV/°C
Input Offset Current	I_{OS}	T_A = +25°C		-	0.5	30	-	0.5	30	pA
		0°C to +70°C		-	-	300	-	-	300	pA
		-55°C to +125°C		-	-	800	-		800	pA
Input Bias Current	I_{BIAS}	T_A = +25°C		-	1.0	50	-	1.0	50	pA
		0°C to +70°C		-	-	500	-	-	500	pA
		-55°C to +125°C		-	-	4000	-	-	4000	pA
Common Mode Voltage Range	V_{CMR}	I_Q = 10µA, ICL7642		±4.4	-	-	±4.4	-	-	V
		I_Q = 1mA, ICL7641		±3.7	-	-	±3.7	-	-	V

Electrical Specifications V_{SUPPLY} = ±5.0V, T_A= +25°C, Unless Otherwise Specified (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS		ICL7641C, ICL7642C MIN	ICL7641C, ICL7642C TYP	ICL7641C, ICL7642C MAX	ICL7641E, ICL7642E MIN	ICL7641E, ICL7642E TYP	ICL7641E, ICL7642E MAX	UNITS
Output Voltage Swing	V_{OUT}	ICL7642, I_Q = 10µA, R_L = 1MΩ,	T_A = +25°C	±4.9	-	-	±4.9	-	-	V
			0°C to 70°C	±4.8	-	-	±4.8	-	-	V
			-55°C to +125°C	±4.7	-	-	±4.7	-	-	V
		ICL7641, I_Q = 1mA, R_L = 10kΩ,	T_A = +25°C	±4.5	-	-	±4.5	-	-	V
			0°C to 70°C	±4.3	-	-	±4.3	-	-	V
			-55°C to +125°C	±4.0	-	-	±4.0	-	-	V
Large Signal Voltage Gain	A_{VOL}	ICL7642, V_O = ±4.0V, R_L = 1MΩ, I_Q = 10µA	T_A = +25°C	80	104	-	80	104	-	dB
			0°C to +70°C	75	-	-	75	-	-	dB
			-55°C to +125°C	68	-	-	68	-	-	dB
		ICL7641, V_O = ±4.0V, R_L = 10kΩ, I_Q = 1mA	T_A = +25°C	76	98	-	76	98	-	dB
			0°C to +70°C	72	-	-	72	-	-	dB
			-55°C to +125°C	68	-	-	68	-	-	dB
Unity Gain Bandwidth	GBW	ICL 7642, I_Q = 10µA		-	0.044	-	-	0.044	-	MHz
		ICL 7641, I_Q = 1mA		-	1.4	-	-	1.4	-	MHz
Input Resistance	R_{IN}			-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	ICL7642, R_S ≤ 100kΩ, I_Q = 10µA		70	96	-	70	96	-	dB
		ICL7641, R_S ≤ 100kΩ, I_Q = 1mA		60	87	-	60	87	-	dB
Power Supply Rejection Ratio V_{SUPPLY} = ±8V to ±2V	PSRR	ICL7642, R_S ≤ 100kΩ, I_Q = 10µA		80	94	-	80	94	-	dB
		ICL7641, R_S ≤ 100kΩ, I_Q = 1mA		70	77	-	70	77	-	dB
Input Referred Noise Voltage	e_N	R_S = 100Ω, f = 1kHz		-	100	-	-	100	-	nV/√Hz
Input Referred Noise Current	i_N	R_S = 100Ω, f = 1kHz		-	0.01	-	-	0.01	-	pA/√Hz
Supply Current (per Amplifier)	I_{SUPPLY}	No Signal, No Load	ICL7642, I_Q = 10µA Low Bias	-	0.01	0.03	-	0.01	0.03	mA
			ICL7641, I_Q = 1mA High Bias	-	1.0	2.5	-	1.0	2.5	mA
Channel Separation	V_{O1}/V_{O2}	A_V = 100		-	120	-	-	120	-	dB
Slew Rate	SR	A_V = 1, C_L = 100pF V_{IN} = 8V_{P-P}	ICL7642, I_Q = 10µA, R_L = 1MΩ	-	0.016	-	-	0.016	-	V/µs
			ICL7641, I_Q = 1mA, R_L = 10kΩ	-	1.6	-	-	1.6	-	V/µs
Rise Time	t_R	V_{IN} = 50mV, C_L = 100pF	ICL7642, I_Q = 10µA, R_L = 1MΩ	-	20	-	-	20	-	µs
			ICL7641, I_Q = 1mA, R_L = 10kΩ	-	0.9	-	-	0.9	-	µs

Electrical Specifications V_{SUPPLY} = ±5.0V, T_A= +25°C, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS		ICL7641C, ICL7642C			ICL7641E, ICL7642E			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Overshoot Factor	OS	V_{IN} = 50mV, C_L = 100pF	ICL7642, I_Q = 10µA, R_L = 1MΩ	-	5	-	-	5	-	%
			ICL7641, I_Q = 1mA, R_L = 10kΩ	-	40	-	-	40	-	%

NOTES:

1. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
2. The outputs may be shorted to ground or to either supply, for $V_{SUPP} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.

Electrical Specifications V_{SUPPLY} = ±1.0V, I_Q = 10µA, T_A= +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		ICL7642C			UNITS
				MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$	T_A = +25°C	-	-	10	mV
			$T_{MIN} \leq T_A \leq T_{MAX}$	-	-	12	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$		-	20	-	µV/°C
Input Offset Current	I_{OS}	T_A = +25°C		-	0.5	30	pA
		0°C to +70°C		-	-	300	pA
Input Bias Current	I_{BIAS}	T_A = +25°C		-	1.0	50	pA
		0°C to +70°C		-	-	500	pA
Common Mode Voltage Range	V_{CMR}			±0.6	-	-	V
Output Voltage Swing	V_{OUT}	R_L = 1MΩ	T_A = +25°C	-	±0.98	-	V
			0°C to 70°C	-	±0.96	-	V
Large Signal Voltage Gain	A_{VOL}	V_O = ±0.1V, R_L = 1MΩ	T_A = +25°C	-	90	-	dB
			0°C to +70°C	-	80	-	dB
Unity Gain Bandwidth	GBW			-	0.044	-	MHz
Input Resistance	R_{IN}			-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega$		-	80	-	dB
Power Supply Rejection Ratio	PSRR			-	80	-	dB
Input Referred Noise Voltage	e_N	R_S = 100Ω, f = 1kHz		-	100	-	$nV/\sqrt{Hz}$
Input Referred Noise Current	i_N	R_S = 100Ω, f = 1kHz		-	0.01	-	$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPPLY}	No Signal, No Load		-	6	15	µA
Channel Separation	V_{01}/V_{02}	A_V = 100		-	120	-	dB
Slew Rate	SR	A_V = 1, C_L = 100pF, V_{IN} = $0.2V_{P-P}$, R_L = 1MΩ		-	0.016	-	V/µs
Rise Time	t_R	V_{IN} = 50mV, C_L = 100pF R_L = 1MΩ		-	20	-	µs
Overshoot Factor	OS	V_{IN} = 50mV, C_L = 100pF, R_L = 1MΩ		-	5	-	%

Functional Diagram

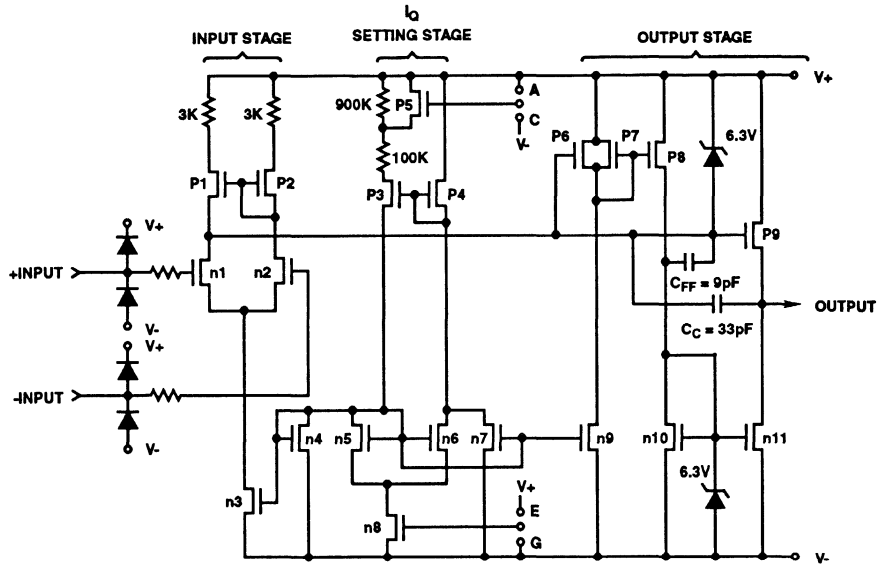


TABLE OF JUMPERS		I_Q
ICL7621	C, E	100µA
ICL7641	C, G	1mA
ICL7642	A, E	10µA

Typical Performance Curves

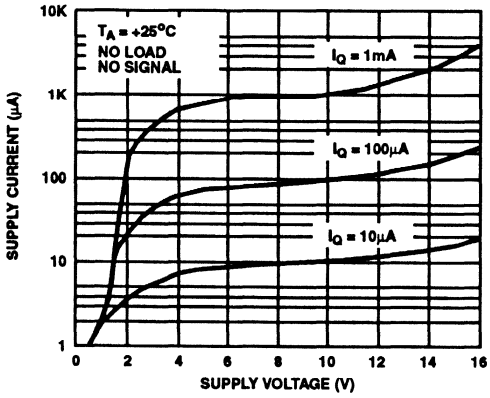


FIGURE 1. SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

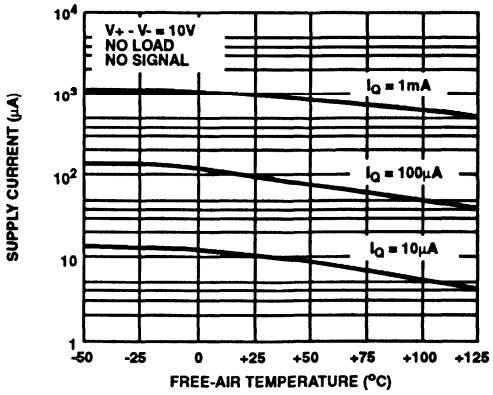


FIGURE 2. SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE

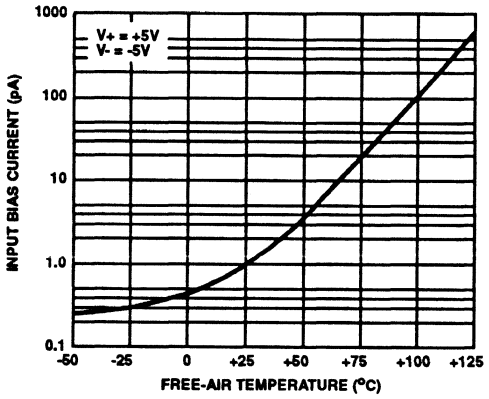


FIGURE 3. INPUT BIAS CURRENT vs TEMPERATURE

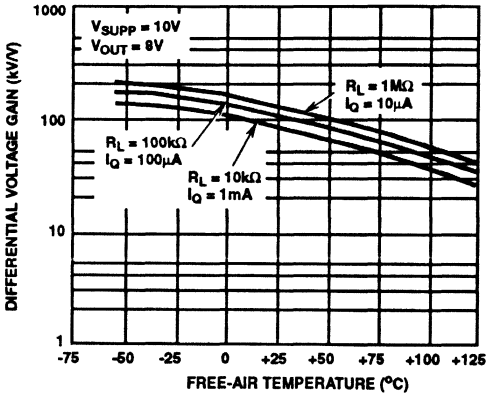


FIGURE 4. LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN vs FREE-AIR TEMPERATURE

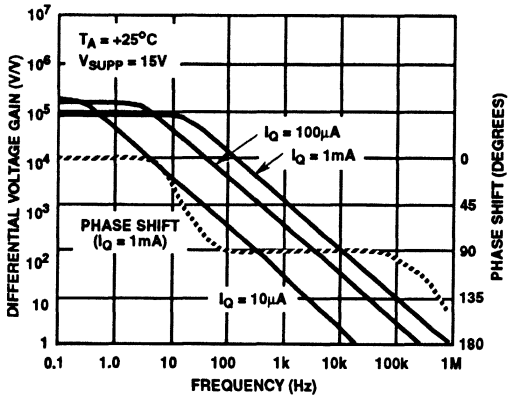


FIGURE 5. LARGE SIGNAL FREQUENCY RESPONSE

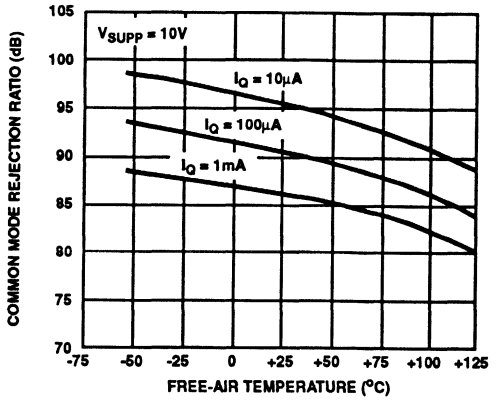


FIGURE 6. COMMON MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

Typical Performance Curves (Continued)

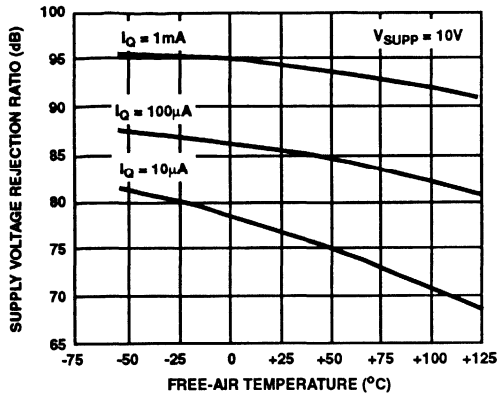


FIGURE 7. POWER SUPPLY REJECTION RATIO vs FREE-AIR TEMPERATURE

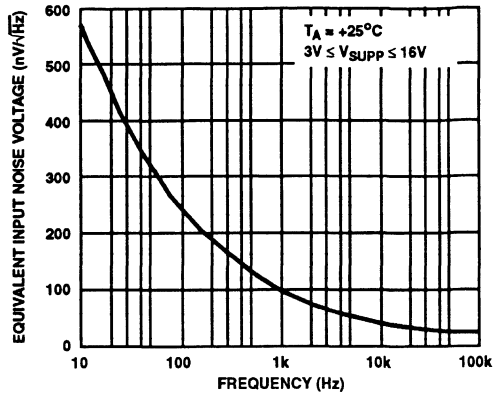


FIGURE 8. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

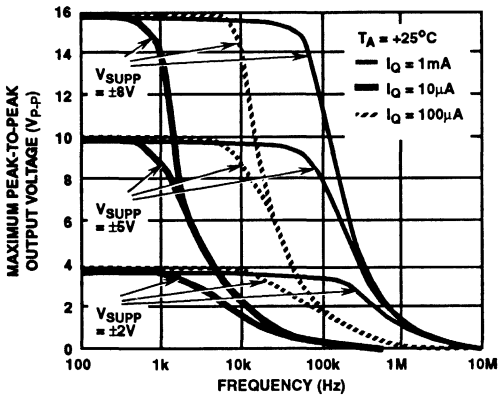


FIGURE 9. OUTPUT VOLTAGE vs FREQUENCY

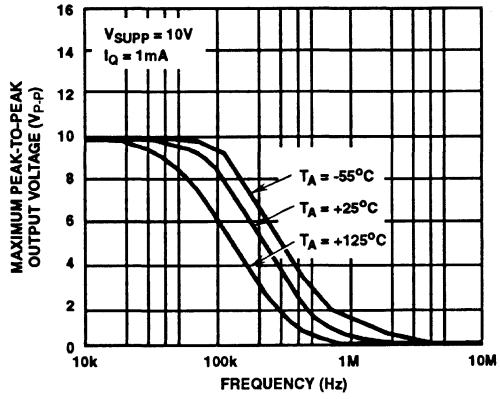


FIGURE 10. OUTPUT VOLTAGE vs FREQUENCY

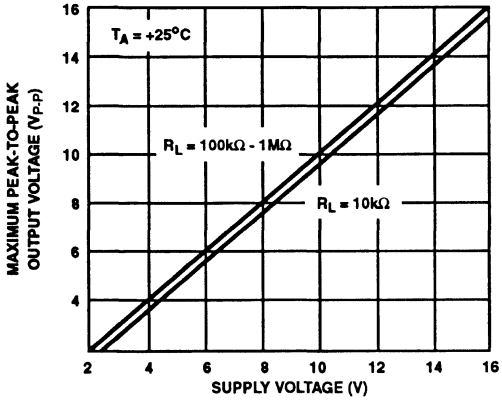


FIGURE 11. OUTPUT VOLTAGE vs SUPPLY VOLTAGE

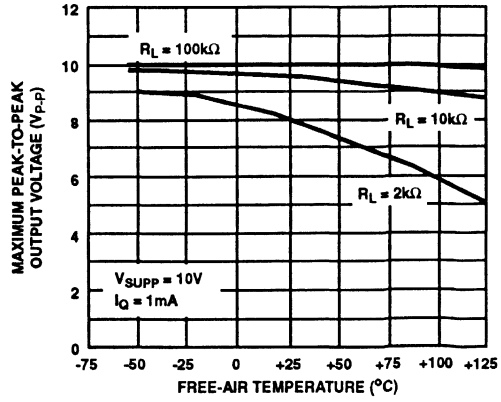


FIGURE 12. OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

Typical Performance Curves (Continued)

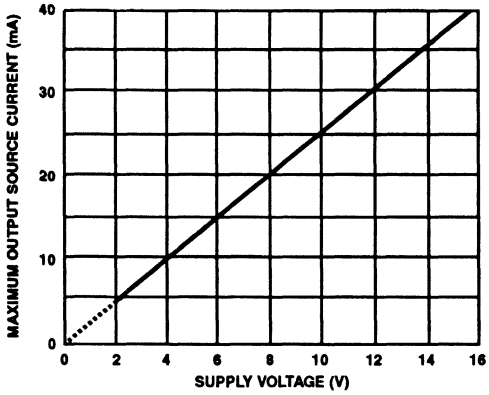


FIGURE 13. OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE

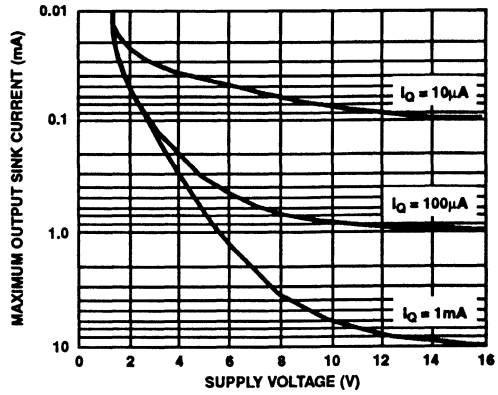


FIGURE 14. OUTPUT SINK CURRENT vs SUPPLY VOLTAGE

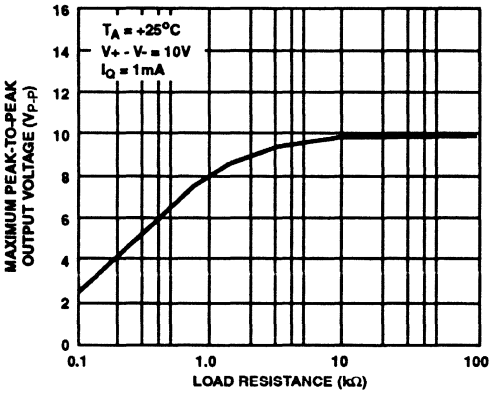


FIGURE 15. OUTPUT VOLTAGE vs LOAD RESISTANCE

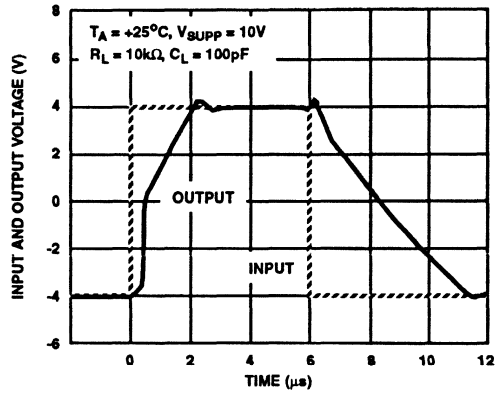


FIGURE 16. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 1mA)

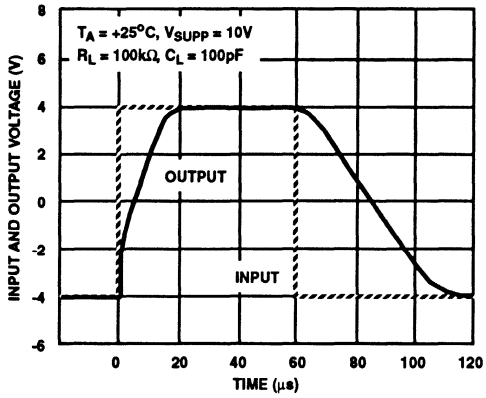


FIGURE 17. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 100µA)

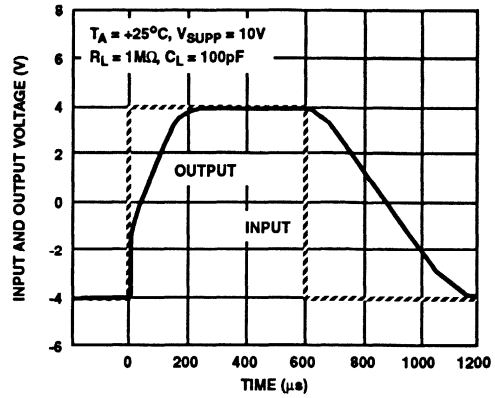


FIGURE 18. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 10µA)

Detailed Description

Static Protection

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

Latchup Avoidance

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (p-n-p-n) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. In general, the op-amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2mA to prevent latchup.

Choosing the Proper I_Q

Each device in the ICL76XX family has a similar I_Q set-up scheme, which allows the amplifier to be set to nominal quiescent currents of 10µA, 100µA or 1mA. These current settings change only very slightly over the entire supply voltage range. The ICL7611/12 have an external I_Q control terminal, permitting user selection of each amplifiers' quiescent current. The ICL7621 and ICL7641/7642 have fixed I_Q settings:

ICL7621 (Dual) - I_Q = 100µA

ICL7641 (Quad) - I_Q = 1mA

ICL7642 (Quad) - I_Q = 10µA

NOTE: The output current available is a function of the quiescent current setting. For maximum p-p output voltage swings into low impedance loads, I_Q of 1mA should be selected.

Output Stage and Load Driving Considerations

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the I_Q settings. This allows output swings to almost the supply rails for output loads of 1MΩ, 100kΩ, and 10kΩ, using the output stage in a highly linear class A mode. In this mode, crossover distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB for higher output currents. (See graphs under Typical Operating Characteristics). During the transition from Class A to Class B operation, the output transfer characteristic is non-linear and the voltage gain decreases.

Frequency Compensation

The ICL76XX are internally compensated, and are stable for closed loop gains as low as unity with capacitive loads up to 100pF.

Operation At V_{SUPP} = ±1.0V

Operation at V_{SUPP} = ±1.0V is guaranteed for the ICL7642C only.

Output swings to within a few millivolts of the supply rails are achievable for $R_L \geq 1M\Omega$ Guaranteed input CMVR is ±0.6V minimum and typically +0.9V to -0.7V at V_{SUPP} = ±1.0V. For applications where greater common mode range is desirable, refer to the ICL7612 data sheet.

Applications

The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup.

Note that in no case is I_Q shown. The value of I_Q must be chosen by the designer with regard to frequency response and power dissipation.

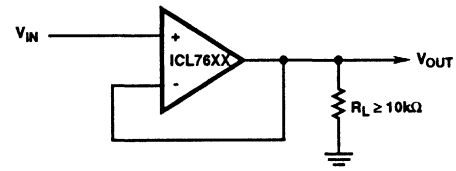


FIGURE 19. SIMPLE FOLLOWER

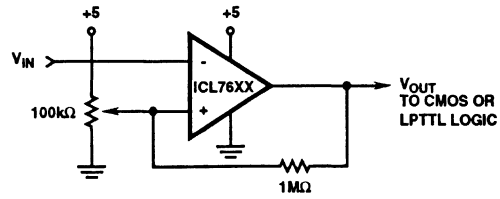
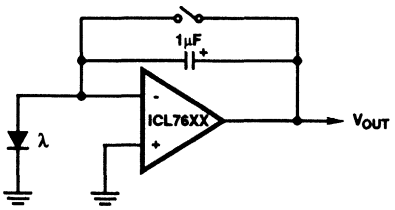


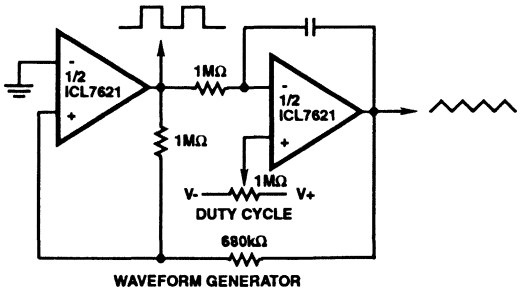
FIGURE 20. LEVEL DETECTOR*

* By using the ICL7612 in this application, the circuit will follow rail to rail inputs.



* Low leakage currents allow integration times up to several hours.

FIGURE 21. PHOTOCURRENT INTEGRATOR



Since the output range swings exactly from rail to rail, frequency and duty cycle are virtually independent of power supply variations.

FIGURE 22. PRECISE TRIANGLE/SQUARE WAVE GENERATOR

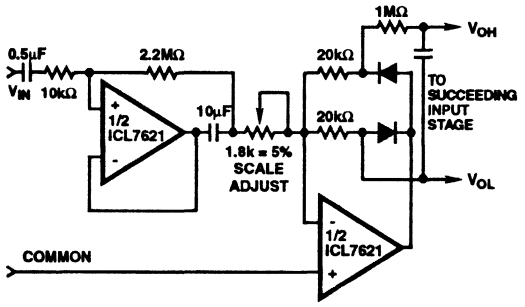


FIGURE 23. AVERAGING AC TO DC CONVERTER FOR A/D CONVERTERS SUCH AS ICL7106, ICL7107, ICL7109, ICL7116, ICL7117

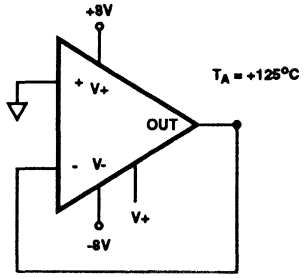
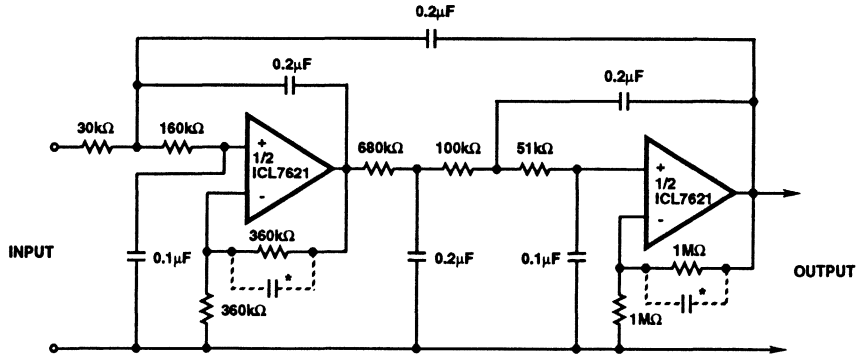


FIGURE 24. BURN-IN AND LIFE TEST CIRCUIT



The low bias currents permit high resistance and low capacitance values to be used to achieve low frequency cutoff.
f_C = 10Hz, A_{VCL} = 4, Passband ripple = 0.1dB

*Note that small capacitors (25 - 50pF) may be needed for stability in some cases.

FIGURE 26. FIFTH ORDER CHEBYSHEV MULTIPLE FEEDBACK LOW PASS FILTER

HARRIS SEMICONDUCTOR

ICL7650S

Super Chopper-Stabilized Operational Amplifier

March 1993

Features

- ***Guaranteed*** **Max Input Offset Voltage for *All* Temperature Ranges**
- **Low Long-Term and Temperature Drifts of Input Offset Voltage**
- ***Guaranteed*** **Max Input Bias Current.....10pA**
- ***Extremely Wide*** **Common Mode Voltage Range: +3.5 to -5V**
- ***Reduced*** **Supply Current..... 2mA**
- ***Guaranteed*** **Minimum Output Source/Sink Current**
- **Extremely High Gain 150dB**
- **Extremely High CMRR and PSRR.....140dB**
- **High Slew Rate.....2.5V/μs**
- **Wide Bandwidth..... 2MHz**
- **Unity-Gain Compensated**
- **Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use**
- **Extremely Low Chopping Spikes at Input and Output**
- **Characterized Fully *Over All* Temperature Ranges**
- ***Improved, Direct*** **Replacement for Industry-Standard ICL7650 and other Second-Source Parts**

Description

The ICL7650S Super Chopper-Stabilized Amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature. It is a direct replacement for the industry-standard ICL7650 offering ***Improved*** input offset voltage, ***lower*** input offset voltage temperature coefficient, ***reduced*** input bias current, and ***wider*** common mode voltage range. All improvements are highlighted in ***bold italics*** in the Electrical Characteristics section. ***Critical parameters are guaranteed over the entire commercial, industrial and military temperature ranges.***

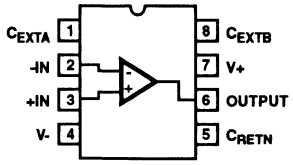
Harris' unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lock-up.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

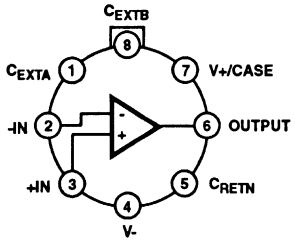
The clock oscillator and all the other control circuitry is entirely self-contained. However the 14-lead version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7650S is internally compensated for unity-gain operation.

Pinouts (See Ordering Information on Next Page)

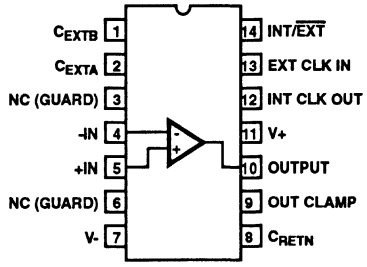
ICL7650S (PDIP, SOIC) TOP VIEW



ICL7650S (TO-99 CAN) TOP VIEW



ICL7650S (PDIP, CDIP, SOIC) TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

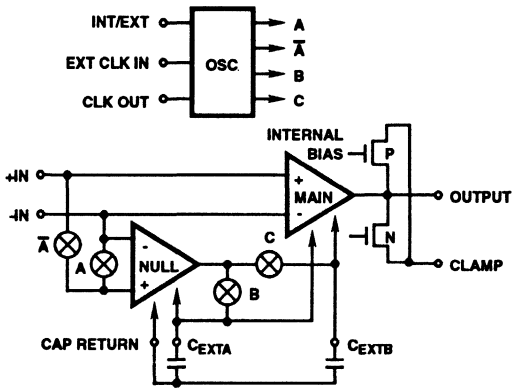
File Number **2920.1**

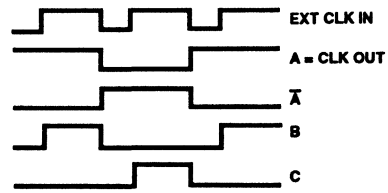
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7650SCPA-1	0°C to +70°C	8 Lead Plastic DIP
ICL7650SCBD	0°C to +70°C	14 Lead SOIC
ICL7650SCPD	0°C to +70°C	14 Lead Plastic DIP
ICL7650SCBA-1	0°C to +70°C	8 Lead SOIC
ICL7650SCTV-1	0°C to +70°C	8 Pin TO-99 Can
ICL7650SIPA-1	-25°C to +85°C	8 Lead Plastic DIP

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7650SIPD	-25°C to +85°C	14 Lead Plastic DIP
ICL7650SIJD	-25°C to +85°C	14 Lead Ceramic DIP
ICL7650SITV-1	-25°C to +85°C	8 Pin TO-99 Can
ICL7650SMJD	-55°C to +125°C	14 Lead Ceramic DIP
ICL7650SMTV-1	-55°C to +125°C	8 Pin TO-99 Can

Functional Diagram





Absolute Maximum Ratings

Supply Voltage (V+ to V-) 18V
Input Voltage ..... (V+ +0.3) to (V- -0.3)
Voltage on Oscillator Control Pins ..... V+ to V-
Duration of Output Short Circuit ..... Indefinite
Current to Any Pin 10mA
  While Operating (Note 1) 100µA
Continuous Total Power Dissipation (T_A = +25°C)
  Ceramic Package 500mW
  Plastic Package 375mW
  TO-99 Can 250mW
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
  ICL7650SC ..... 0°C ≤ T_A ≤ +70°C
  ICL7650SI ..... -25°C ≤ T_A ≤ +85°C
  ICL7650SM ..... -55°C ≤ T_A ≤ +125°C
Storage Temperature Range ..... -55°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +5V, V- = -5V, T_A = +25°C, See Test Circuit, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Offset Voltage (Note 2)	V_{OS}	T_A = +25°C	-	±0.7	±5	µV
		0°C ≤ T_A ≤ +70°C	-	±1	±8	µV
		-25°C ≤ T_A ≤ +85°C	-	±2	±10	µV
		-55°C ≤ T_A ≤ +125°C	-	±4	±20	µV
Average Temperature Coefficient of Input Offset Voltage (Note 2)	$\Delta V_{OS}/\Delta T$	0°C ≤ T_A ≤ +70°C	-	0.02	-	µV/°C
		-25°C ≤ T_A ≤ +85°C	-	0.02	-	µV/°C
		-55°C ≤ T_A ≤ +125°C	-	0.03	0.1	µV/°C
Change in Input Offset with Time	$\Delta V_{OS}/\Delta T$		-	100	-	nV/√month
Input Bias Current |I(+)|, |I(-)|	I_{BIAS}	T_A = + 25°C	-	4	10	pA
		0°C ≤ T_A ≤ +70°C	-	5	20	pA
		-25°C ≤ T_A ≤ +85°C	-	20	50	pA
		-55°C ≤ T_A ≤ +125°C	-	20	50	pA
		+85°C ≤ T_A ≤ +125°C	-	100	500	pA
Input Offset Current |I(-), I(+)|	I_{OS}	T_A = + 25°C	-	8	20	pA
		0°C ≤ T_A ≤ +70°C	-	10	40	pA
		-25°C ≤ T_A ≤ +85°C	-	20	40	pA
		-55°C ≤ T_A ≤ +125°C	-	20	40	pA
		+85°C ≤ T_A ≤ +125°C	-	20	50	pA
Input Resistance	R_{IN}			10^{12}		Ω

Electrical Specifications V+ = +5V, V- = -5V, T_A = +25°C, See Test Circuit, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Large Signal Voltage Gain (Note 2)	A_{VOL}	R_L = 10kΩ, V_O = ±4V, T_A = +25°C	*135*	*150*	-	dB
		0°C ≤ T_A ≤ +70°C	*130*	-	-	dB
		-25°C ≤ T_A ≤ +85°C	*130*	-	-	dB
		-55°C ≤ T_A ≤ +125°C	*120*	-	-	dB
Output Voltage Swing (Note 3)	V_{OUT}	R_L = 10kΩ	±4.7	±4.85	-	V
		R_L = 100kΩ	-	±4.95	-	V
Common Mode Voltage Range (Note 2)	*CMVR*	T_A = +25°C	-5	*-5.2 to +4*	*+3.5*	V
		0°C ≤ T_A ≤ +70°C	-5	-	*+3.5*	V
		-25°C ≤ T_A ≤ +85°C	-5	-	*+3.5*	V
		-55°C ≤ T_A ≤ +125°C	-5	-	*+3.5*	V
Common Mode Rejection Ratio (Note 2)	*CMRR*	CMVR = -5V to +3.5V T_A = +25°C	*120*	*140*	-	dB
		0°C ≤ T_A ≤ +70°C	*120*	-	-	dB
		-25°C ≤ T_A ≤ +85°C	*115*	-	-	dB
		-55°C ≤ T_A ≤ +125°C	*110*	-	-	dB
Power Supply Rejection Ratio	*PSRR*	V+, V- = ±3V to ±8V	120	*140*	-	dB
Input Noise Voltage	e_N	R_S = 100Ω, f = DC to 10Hz	-	2	-	μV_{P-P}
Input Noise Current	i_N	f = 10Hz	-	0.01	-	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBW		-	2	-	MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ	-	2.5	-	V/µs
Rise Time	t_R		-	0.2	-	µs
Overshoot	OS		-	20	-	%
Operating Supply Range	V+ to V-		4.5	-	16	V
Supply Current	I_{SUPP}	No Load, T_A = +25°C	-	2	*3*	mA
		0°C ≤ T_A ≤ +70°C	-	-	*3.2*	mA
		-25°C ≤ T_A ≤ +85°C	-	-	*3.5*	mA
		-55°C ≤ T_A ≤ +125°C	-	-	*4*	mA

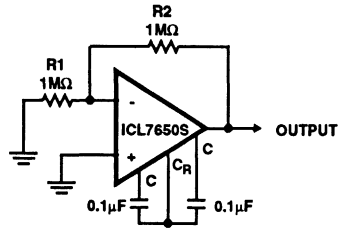
Electrical Specifications V+ = +5V, V- = -5V, T_A = +25°C, See Test Circuit, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Output Source Current	$I_{O\ SOURCE}$	T_A = +25°C	2.9	4.5	-	mA
		0°C ≤ T_A ≤ +70°C	2.3	-	-	mA
		-25°C ≤ T_A ≤ +85°C	2.2	-	-	mA
		-55°C ≤ T_A ≤ +125°C	2	-	-	mA
Output Sink Current	$I_{O\ SINK}$	T_A = +25°C	25	30	-	mA
		0°C ≤ T_A ≤ +70°C	20	-	-	mA
		-25°C ≤ T_A ≤ +85°C	19	-	-	mA
		-55°C ≤ T_A ≤ +125°C	17	-	-	mA
Internal Chopping Frequency	f_{CH}	Pins 13 and 14 Open	120	250	375	Hz
Clamp ON Current (Note 4)		R_L = 100kΩ, T_A = +25°C	25	70	-	µA
Clamp OFF Current (Note 4)		-4V ≤ V_{OUT} ≤ +4V, T_A = +25°C	-	***0.001***	***5***	nA
		0°C ≤ T_A ≤ +70°C	-	-	***10***	nA
		-25°C ≤ T_A ≤ +85°C	-	-	***10***	nA
		-55°C ≤ T_A ≤ +125°C	-	-	***15***	nA

NOTES:

1. Limiting input current to 100µA is recommended to avoid latchup problems. Typically 1mA is safe, however this is not guaranteed.
2. These parameters are guaranteed by design and characterization, but not tested at temperature extremes because thermocouple effects prevent precise measurement of these voltages in automatic test equipment.
3. OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.
4. See OUTPUT CLAMP under detailed description.
5. All significant improvements over the industry-standard ICL7650 are highlighted in ***bold italics***.

Test Circuit



Typical Performance Curves

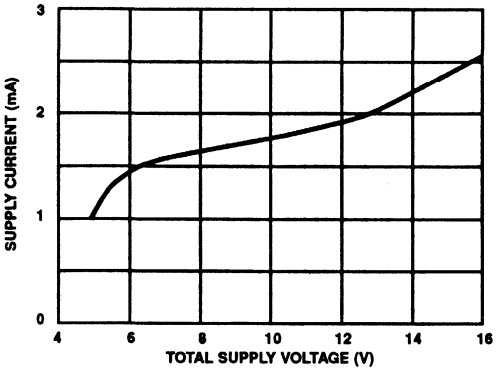


FIGURE 1. SUPPLY CURRENT vs SUPPLY VOLTAGE

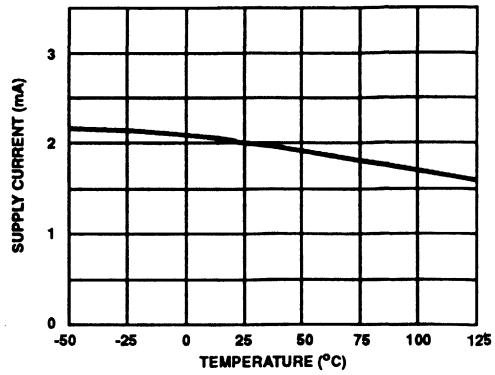


FIGURE 2. SUPPLY CURRENT vs AMBIENT TEMPERATURE

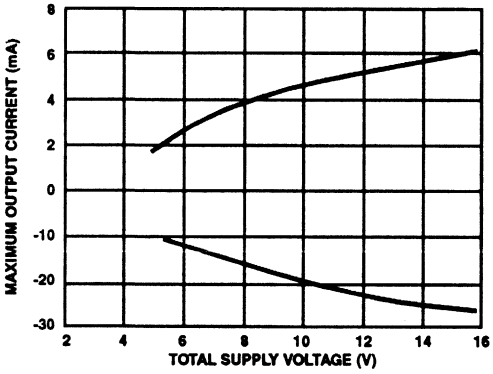


FIGURE 3. MAXIMUM OUTPUT CURRENT vs SUPPLY VOLTAGE

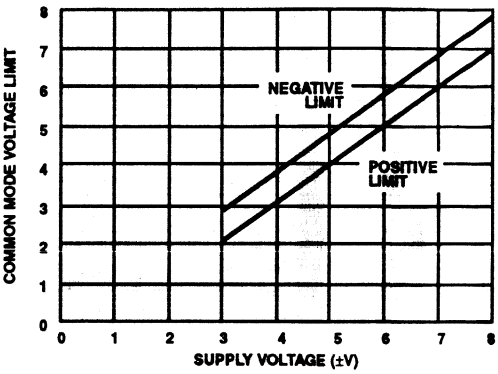


FIGURE 4. COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

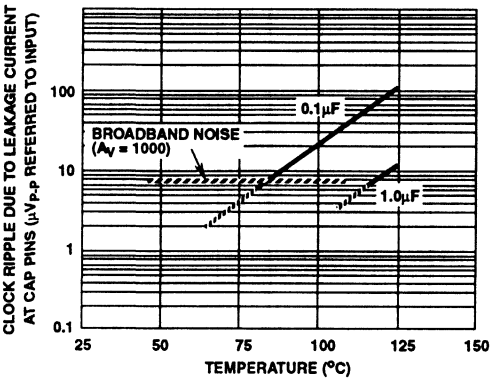


FIGURE 5. CLOCK RIPPLE REFERRED TO THE INPUT vs TEMPERATURE

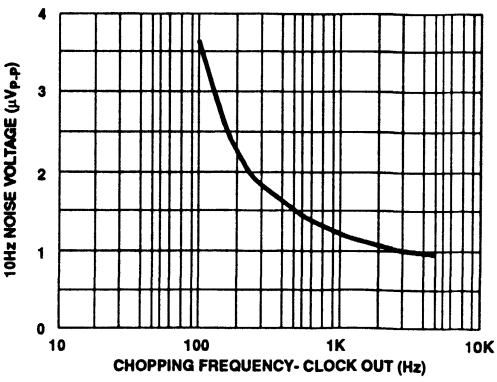


FIGURE 6. 10Hz NOISE VOLTAGE vs CHOPPING FREQUENCY

Typical Performance Curves (Continued)

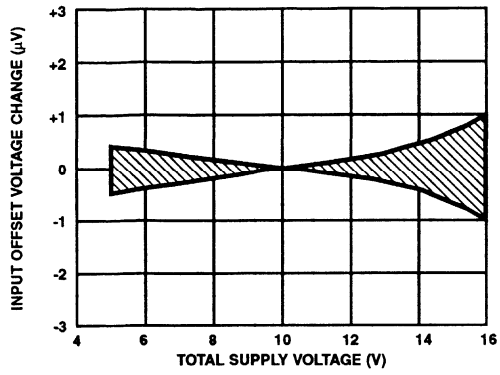


FIGURE 7. INPUT OFFSET VOLTAGE CHANGE vs SUPPLY VOLTAGE

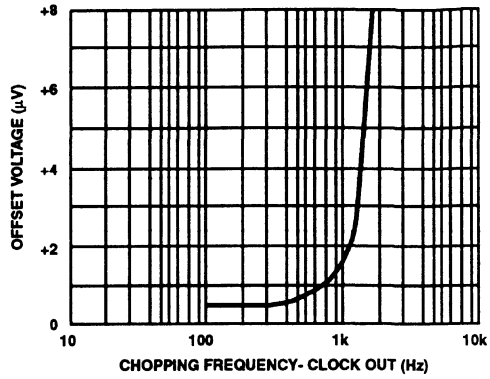


FIGURE 8. INPUT OFFSET VOLTAGE vs CHOPPING FREQUENCY

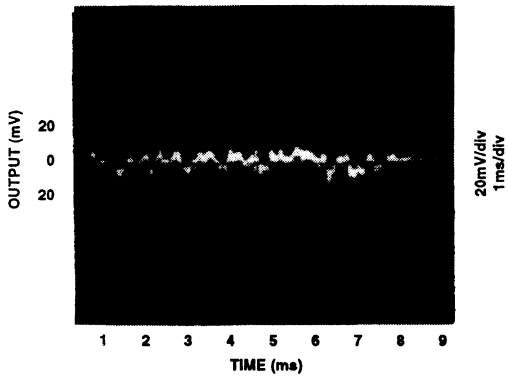


FIGURE 9. OUTPUT WITH ZERO INPUT; GAIN = 1000; BALANCED SOURCE IMPEDANCE = 10kΩ

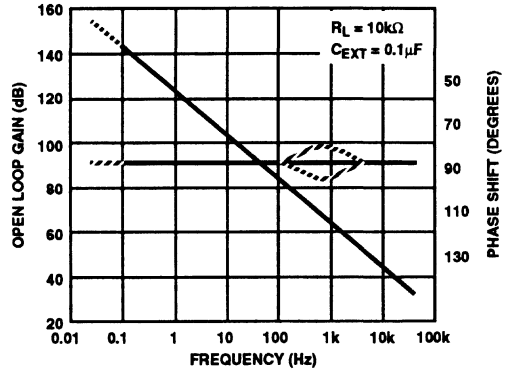


FIGURE 10. OPEN LOOP GAIN AND PHASE SHIFT vs FREQUENCY

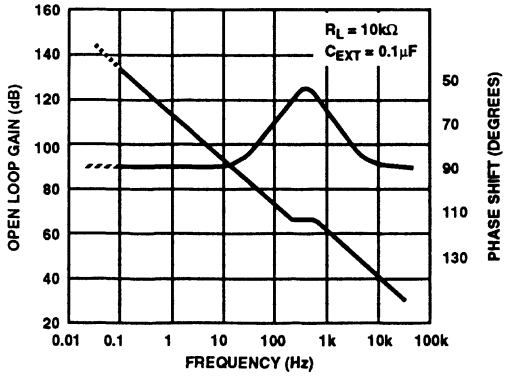


FIGURE 11. OPEN LOOP GAIN AND PHASE SHIFT vs FREQUENCY

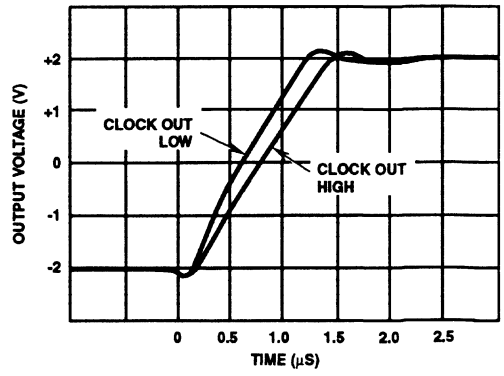


FIGURE 12. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE*

* The two different responses correspond to the two phases of the clock.

Typical Performance Curves (Continued)

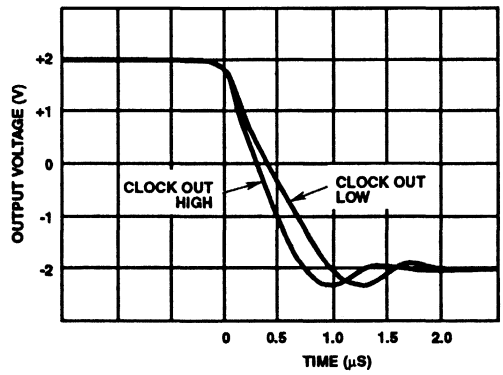


FIGURE 13. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE*

* The two different responses correspond to the two phases of the clock.

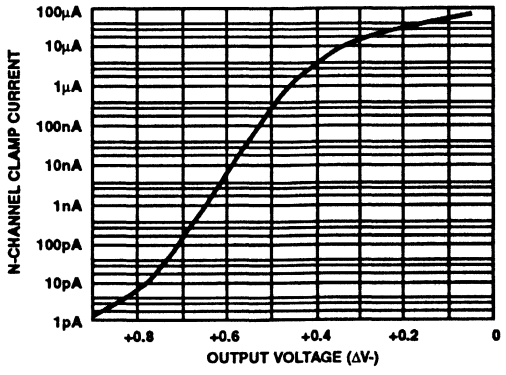


FIGURE 14. N-CHANNEL CLAMP CURRENT vs OUTPUT VOLTAGE

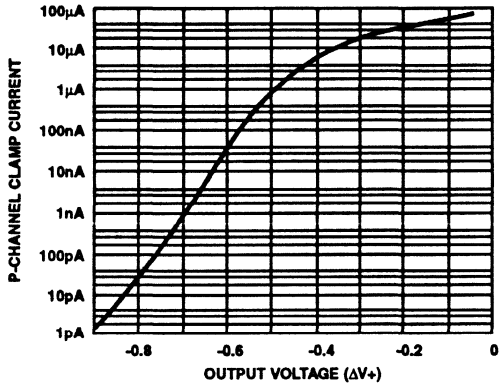


FIGURE 15. P-CHANNEL CLAMP CURRENT vs OUTPUT VOLTAGE

Detailed Description

Amplifier

The functional diagram shows the major elements of the ICL7650S. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output, while the nulling amplifier, under the control of the chopping oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches, and the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals, and also the feed forward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7650S by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650S, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Capacitor Connection

The null/storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN}.

Output Clamp

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differentials are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

Clock

The ICL7650S has an internal oscillator, giving a chopping frequency of 200Hz, available at the CLOCK OUT pin on the 14 pin devices. Provision has also been made for the use of an external clock in these parts. The INT/$\overline{EXT}$ pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V- to disable the internal clock. The external clock signal may then be applied to the EXT CLOCK IN pin. An internal divide-by-two provides the desired 50% input switching duty cycle. Since the capacitors are charged only when EXT CLOCK IN is high, a 50% - 80% positive duty cycle is recommended, especially for higher frequencies. The external clock can swing between V+ and V-. The logic threshold will be at about 2.5V below V+. Note also that a signal of about 400 Hz, with a 70% duty cycle, will be present at the EXT CLOCK IN pin with INT/$\overline{EXT}$ high or open. This is the internal clock signal before being fed to the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10µV/sec, and relatively long measurements can be made with little change in offset.

Brief Application Notes

Component Selection

The two required capacitors, C_{EXTA} and C_{EXTB}, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1µF, and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion if an external clock is used. A high quality film type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1µV.

Static Protection

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input-leakage currents.

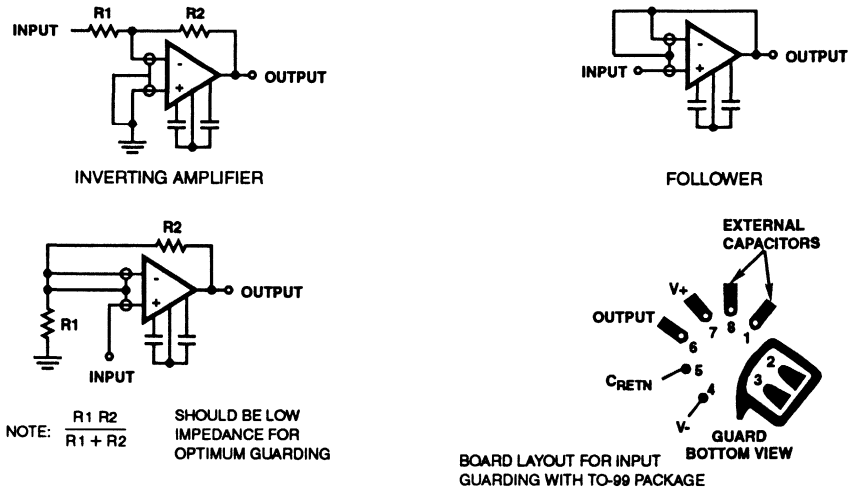


FIGURE 16. CONNECTION OF INPUT GUARDS

Latchup Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latchup, even under fault conditions.

Output Stage/Load Driving

The output circuit is a high-impedance type (approximately 18kΩ), and therefore with loads less than this value, the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17dB lower with a 1kΩ load than with a 10kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a 1kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10kΩ or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

Thermo-Electric Effects

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1μV/°C, but up to tens of mV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-efficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

Guarding

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7650S. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8 pin TO-99 package is accomplished by using a 10 lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the 14 pin dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

Pin Compatibility

The basic pinout of the 8 pin device corresponds, where possible, to that of the industry standard 8 pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, usually used for offset null or compensation capacitors, or simply not connected. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V+, by two capacitors from those pins to pin 5, will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to pin 5 is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, μA748, and similar parts.

The 14 pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert it to the ICL7650S.

Typical Applications

Clearly the applications of the ICL7650S will mirror those of other op-amps. Anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7650S is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 17 and 18. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op amps by the ICL7650S are the supply voltage (±8V max.) and the output drive capability (10kΩ load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 19, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7650S. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.

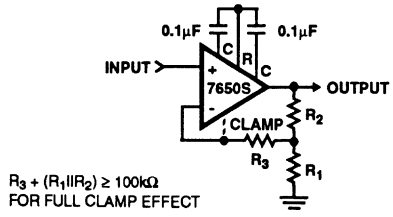


FIGURE 17. NON INVERTING AMPLIFIER WITH OPTIONAL CLAMP

NOTE: R1IIR2 indicates the parallel combination of R1 and R2.

Figure 20 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current ≈ V_{IN}/R without disturbing other portions of the system.

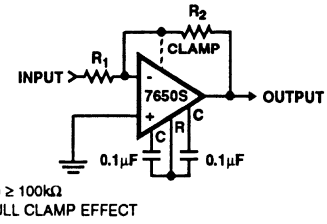


FIGURE 18. INVERTING AMPLIFIER WITH (OPTIONAL) CLAMP

NOTE: R1IIR2 indicates the parallel combination of R1 and R2.

Normal logarithmic amplifiers are limited in dynamic range in the voltage-input mode by their input-offset voltage. The built-in temperature compensation and convenience features of the ICL8048 can be extended to a voltage-input dynamic range of close to 6 decades by using the ICL7650S to offset-null the ICL8048, as shown in Figure 21. The same concept can also be used with such devices as the HA2500 or HA2600 families of op-amps to add very low offset voltage capability to their very high slew rates and bandwidths. Note that these circuits will also have their DC gains, CMRR, and PSRR enhanced.

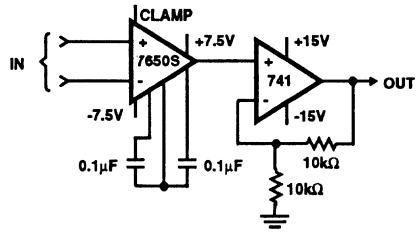


FIGURE 19. USING 741 TO BOOST OUTPUT DRIVE CAPACITY

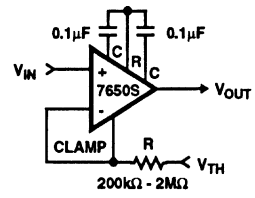


FIGURE 20. LOW OFFSET COMPARATOR

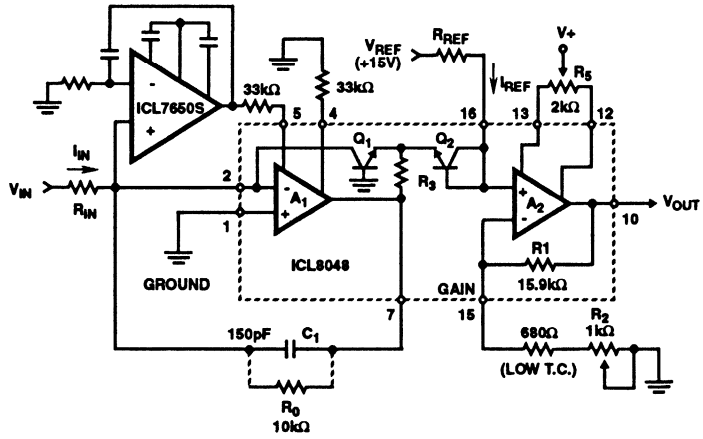


FIGURE 21. ICL8048 OFFSET NULLED BY ICL7650S

NOTE: For further Applications Assistance, see A053 and R017.

Operational Amplifiers Glossary of Terms

AVERAGE INPUT OFFSET CURRENT DRIFT - The average change in offset current between room (+25°C) and high temperature (+125°C, +85°C or +75°C) or between room temperature and low temperature (0°C, -25°C or -55°C) divided by the temperature difference.

AVERAGE OFFSET VOLTAGE DRIFT - The average change in offset voltage between room (+25°C) and high temperature (+125°C, +85°C or +75°C) or between room temperature and low temperature (0°C, -25°C or -55°C) divided by the temperature difference.

CHANNEL SEPARATION - The ratio of the output of a driven amplifier to the output (referred to input) of an adjacent undriven amplifier.

COMMON MODE INPUT VOLTAGE (V_{IC}) - The average of the voltages present at the differential input terminals.

COMMON MODE INPUT VOLTAGE RANGE (V_{ICR}) - The range of voltage that if exceeded at either input terminal will cause the amplifier to cease operating properly.

COMMON MODE REJECTION RATIO (CMRR) - The ratio of change in input offset voltage to change in input common mode voltage, expressed in dB.

$$CMRR = 20 \times \log_{10}\left[\frac{V_{IO}}{V_{CM}}\right]$$

COMMON MODE RESISTANCE (r_{IC}) - The ratio of change in input common mode voltage to the resulting change in input current.

DIFFERENTIAL INPUT RESISTANCE (r_{ID}) - The ratio of change in input differential voltage (small signal, assumes amplifier operating linearly) to the resulting change in differential input current.

FULL POWER BANDWIDTH (FPBW) - The maximum frequency at which a full scale undistorted (THD < 1%) sine wave can be obtained at the output of the amplifier.

GAIN BANDWIDTH (GBW) - The open loop gain of an op amp (in V/V) at a mid-band, linear region frequency (usually between 1kHz and 10kHz) times that frequency (in Hz). GBW = $[A_{VOL}] \bullet f$.

INPUT BIAS CURRENT (I_{BIAS}) - The average of the currents flowing into or out of the input terminals when the output is at zero volts.

INPUT CAPACITANCE (C_{IN}) - The equivalent capacitance seen looking into either input terminal.

INPUT NOISE CURRENT (I_N) - The input noise current that would reproduce the noise seen at the output if all amplifier noise sources were set to zero and the source impedances were large compared to the optimum source impedance.

INPUT OFFSET CURRENT (I_{OS}) - The difference in the currents flowing into the two input terminals when the output is at zero volts.

INPUT OFFSET VOLTAGE (V_{IO}) - The differential DC voltage required to zero the output voltage with no input signal or load. Input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT NOISE VOLTAGE (e_N) - The input noise voltage that would reproduce the noise seen at the output if all the amplifier noise sources and source resistances were set to zero.

LARGE SIGNAL VOLTAGE GAIN (A_V) - The ratio of the peak to peak output voltage swing (over a specified range) to the change in input voltage required to drive the output.

OUTPUT CURRENT (I_{OUT}) - The output current available from the amplifier at some specified output voltage.

OUTPUT RESISTANCE (RO) - The ratio of the change in output voltage to the change in output current.

OUTPUT SHORT CIRCUIT CURRENT (I_{SC}) - The output current available from the amplifier with the output shorted to ground (or other specified potential).

OUTPUT VOLTAGE SWING (V_{OUT}) - The maximum output voltage swing, referred to ground, that can be obtained under specified loading conditions.

OVERSHOOT - Peak excursion above final value of an output step response.

POWER SUPPLY REJECTION RATIO (PSRR) - The ratio of the change in input offset voltage to the change in power supply voltage producing it.

RISE TIME (t_R) - The time required for an output voltage step to change from 10% to 90% of its final value, when the input is subjected to a small signal voltage pulse.

SETTLING TIME (t_{SET}) - The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE (SR) - The rate of change of the output under large signal conditions. Slew rate may be specified separately for both positive and negative going changes.

SUPPLY CURRENT (I_S) - The current required from the power supply to operate the amplifier with no load and the output at zero volts.

SUPPLY VOLTAGE RANGE - The range of power supply voltage over which the amplifier may be safely operated.

UNITY GAIN BANDWIDTH - The frequency range from DC to that frequency where the amplifiers open loop gain is unity.

LINEAR 3

COMPARATORS

NOTE: Bold Type Designates a New Product from Harris.

Selection Guide

COMPARATORS

General Purpose Electrical Characteristics, T_A = +25°C

TYPE	V_{IO} MAX (mV)	I_I MAX (nA)	I_+ MAX (mA)	MAX V+, V-	A_{OL} MIN (dB)	RESPONSE TIME	LEAD COUNT AND PACKAGE TYPE*	COMMENTS
SINGLE UNIT TYPE								
CA3098	15	100	0.8	±8	-	900ns	8E	Dual input level detector with Schmitt Trigger
DUAL UNIT TYPES								
CA3290	20	50pA	3	±18	88	t_R = 1.2µs, t_R = 200ns	8E, 8S, 8T, 14E1	
CA3290A	10	40pA	3	±18	88		8E, 8S, 8T, 14E1	
QUAD UNIT TYPES								
CA139	5	100	8	±18	-	t_R = 1.3µs, t_R = 750ns	14E	
CA139A	2	100	8	±18	94		14E	
CA239	5	250	2	±18	-		14E	
CA239A	2	250	2	±18	94		14E	
CA339	5	250	2	±18	94		14E	
CA339A	2	250	2	±18	94		14E	

TYPE	V_{IO} (mV)	I_{IO} (nA)	RESPONSE TIME	LEAD COUNT AND PACKAGE TYPE*	COMMENTS
HA-4900	2	10	130ns	16	Single or dual supply. Analog and logic supplies separated for easier interface and noise immunity.
HA-4902	2	10	130ns	16	
HA-4905	4	25	130ns	16	

* See Packaging Information in Section 11.

ULTRA HIGH SPEED COMPARATORS

TYPE	PROPAGATION DELAY (ns)	TRACKING BANDWIDTH (MHz)	V_{IO} (mV)	LARGE SIGNAL VOLTAGE GAIN (V/V)	COMMENTS
HFA-0003	2.0	270	1	3100	Direct Output Version
HFA-0003L	2.1	270	1	3100	Latched output version with user Programmable Hysteresis Control

HARRIS SEMICONDUCTOR

CA139, CA239 CA339, LM339*

Quad Voltage Comparators for Industrial, Commercial and Military Applications

March 1993

Features

- Operation from Single or Dual Supplies
- Common Mode Input voltage Range to GND
- Output Voltage Compatible with TTL, DTL, ECL, MOS and CMOS
- Differential Input Voltage Range Equal to the Supply Voltage
- Maximum Input Offset Voltage (V_{IO})
  - CA139A, CA239A, CA339A 2mV
  - CA139, CA239, CA339 ..... 5mV
- Replacement for Industry Types 139, 239, 339, 139A, 239A, 339A

Applications

- Square Wave Generator
- Time Delay Generators
- Pulse Generators
- Multivibrators
- High Voltage Digital Logic Gates
- A/D Converters
- MOS Clock Timers

Description

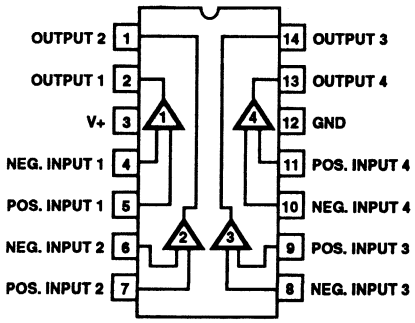
The CA139, CA239, CA339, CA139A, CA239A, and CA339A types consist of four independent single or dual supply voltage comparators on a single monolithic substrate. The common mode input voltage range includes ground even when operated from a single supply, and the low power supply current drain makes these comparators suitable for battery operation. These types were designed to directly interface with TTL and CMOS.

Types CA139A, CA239A, and CA339A have all the features and characteristics of their prototype counterparts CA139, CA239, and CA339 plus an even lower input offset voltage characteristic. These devices are supplied in a 14 lead Small Outline package (M suffix), in a 14 lead dual-in-line plastic package (E suffix) and in a 14 lead dual-in-line hermetic (frit seal) ceramic package (F suffix). The CA339 is also available in chip form (H suffix).

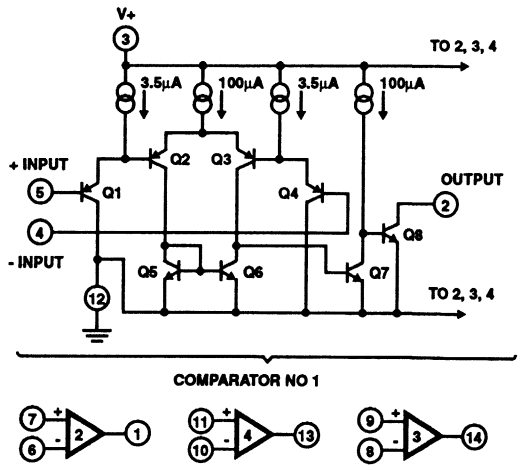
*Technical data on LM339 is identical to CA339.

Pinout

CA139, CA139A, CA239, CA239A, CA339 (PDIP, CDIP, SOIC)
CA339A (PDIP SOIC)
LM339, LM339A (PDIP)
TOP VIEW



Schematic Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 795.1

Absolute Maximum Ratings

Supply Voltage ..... 36V or ±18V
Differential Input Voltage 36V
Input Voltage ..... -0.3V to +36V
Input Current (V_I < -0.3V) Note 4 ..... 50mA
Output Short Circuit Duration (Single Supply) Note 5 .. Continuous
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

Thermal Package Characteristics (°C/W) ..	θ_{JA}	θ_{JC}
Ceramic DIP Package	71	14
Plastic DIP Package	107	38
SOIC Package	119	36

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = 5V, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITION		LIMITS CA139 MIN	CA139 TYP	CA139 MAX	CA139A MIN	CA139A TYP	CA139A MAX	UNITS
Input Offset Voltage	V_{IO}	V_{REF} = 1.4V, R_S = 0, Output Switch Point V ≅ 1.4V	T_A = +25°C	-	2	5	-	1	2	mV
			Note 1	-	-	9	-	-	4	mV
Differential Input Voltage	V_{ID}	Keep All Inputs ≥ 0V for V- (if used), Notes 1, 2		-	-	36	-	-	36	V
Saturation Voltage	V_{SAT}	V_I- = 1V, V_I+ = 0V, I_{SINK} ≤ 4mA	T_A = +25°C	-	250	400	-	250	400	mV
			Note 1	-	-	700	-	-	700	mV
Common Mode Input Voltage Range	V_{ICR}	Note 3	T_A = +25°C	0	-	V+ - 1.5	0	-	V+ - 1.5	V
			Note 1	0	-	V+ - 2	0	-	V+ - 2	V
Input Offset Current	I_{IO}	I_I+ - I_I-	T_A = +25°C	-	3	25	-	3	25	nA
			Note 1	-	-	100	-	-	100	nA
Input Bias Current	I_{IB}	I_I+ or I_I- with Output in Linear Range	T_A = +25°C	-	25	100	-	25	100	nA
			Note 1	-	-	300	-	-	300	nA
Total Supply Current	I+	R_L = ∞ on All Comparators, T_A = +25°C		-	0.8	2	-	0.8	2	mA
Output Leakage Current		V_I+ ≥ 1V, V_I- = 0V, V_O = 5V	T_A = +25°C	-	0.1	-	-	0.1	-	nA
		V_I+ ≥ 1V, V_I- = 0V, V_O = 30V	Note 1	-	-	1	-	-	1	µA
Output Sink Current		V_I- ≥ 1V, V_I+ = 0V, V_O ≤ 1.5V, T_A = +25°C		6	16	-	6	16	-	mA
Voltage Gain	A_{OL}	R_L ≥ 15kΩ, V+ = 15V, T_A = +25°C		-	200	-	50	200	-	V/mV
Large Signal Response Time		V_I = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1kΩ, T_A = +25°C		-	300	-	-	300	-	ns
Response Time (Figures 3 and 4)		V_{RL} = 5V, R_L = 5.1kΩ, T_A = +25°C		-	1.3	-	-	1.3	-	µs

Electrical Specifications V+ = 5V, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITION		LIMITS CA239, CA339 MIN	CA239, CA339 TYP	CA239, CA339 MAX	CA239A, CA339A MIN	CA239A, CA339A TYP	CA239A, CA339A MAX	UNITS
Input Offset Voltage	V_{IO}	V_{REF} = 1.4V, R_S = 0, Output Switch Point V ≅ 1.4V	T_A = +25°C	-	2	5	-	1	2	mV
			Note 1	-	-	9	-	-	4	mV

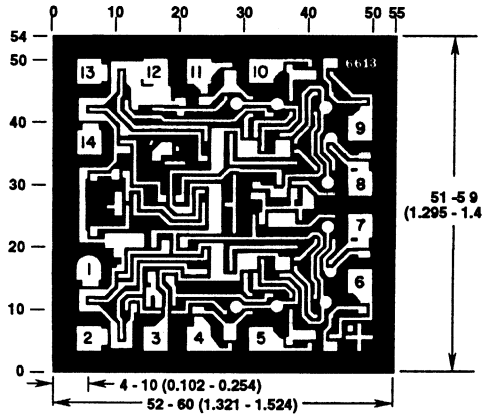
Electrical Specifications V+ = 5V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	CONDITION		LIMITS CA239, CA339 MIN	CA239, CA339 TYP	CA239, CA339 MAX	CA239A, CA339A MIN	CA239A, CA339A TYP	CA239A, CA339A MAX	UNITS
Differential Input Voltage	V_{ID}	Keep All Inputs ≥ 0V for V- (if used), Notes 1, 2		-	-	36	-	-	36	V
Saturation Voltage	V_{SAT}	V_I- = 1V, V_I+ = 0V, I_{SINK} ≤ 4mA	T_A = +25°C	-	250	400	-	250	400	mV
			Note 1	-	-	700	-	-	700	mV
Common Mode Input Voltage Range	V_{ICR}	Note 3	T_A = +25°C	0	-	V+ - 1.5	0	-	V+ - 1.5	V
			Note 1	0	-	V+ - 2	0	-	V+ - 2	V
Input Offset Current	I_{IO}	I_I+ - I_I-	T_A = +25°C	-	5	50	-	5	50	nA
			Note 1	-	-	150	-	-	150	nA
Input Bias Current	I_{IB}	I_I+ or I_I- with Output in Linear Range	T_A = +25°C	-	25	250	-	25	250	nA
			Note 1	-	-	400	-	-	400	nA
Total Supply Current	I+	R_L = ∞ on All Comparators, T_A = +25°C		-	0.8	2	-	0.8	2	mA
Output Leakage Current		V_I+ ≥ 1V, V_I- = 0V, V_O = 5V	T_A = +25°C	-	0.1	-	-	0.1	-	nA
		V_I+ ≥ 1V, V_I- = 0V, V_O = 30V	Note 1	-	-	1	-	-	1	µA
Output Sink Current		V_I- ≥ 1V, V_I+ = 0V, V_O ≤ 1.5V, T_A = +25°C		6	16	-	6	16	-	mA
Voltage Gain	A_{OL}	R_L ≥ 15kΩ, V+ = 15V, T_A = +25°C		-	200	-	50	200	-	V/mV
Large Signal Response Time		V_I = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1kΩ, T_A = +25°C		-	300	-	-	300	-	ns
Response Time (Figures 3 and 4)		V_{RL} = 5V, R_L = 5.1kΩ, T_A = +25°C		-	1.3	-	-	1.3	-	µs

NOTES:

1. Ambient Temperature (T_A) applicable over operating temperature range as shown below.
   CA139, CA139A = -55°C to +125°C; CA239, CA239A = -25°C to +85°C; CA339, CA339A = 0°C to +70°C
2. The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common mode voltage range. The low input voltage state must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
3. The upper end of the common mode voltage range is (V+) - 1.5V, but either or both inputs can go to +30V without damage.
4. Inputs must not go more negative than -0.3V.
5. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current independent of V+ is approximately 20mA.

Metallization Mask Layout



NOTE: Dimensions in parentheses are in mm and are derived from the basic in. dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Typical Performance Curves

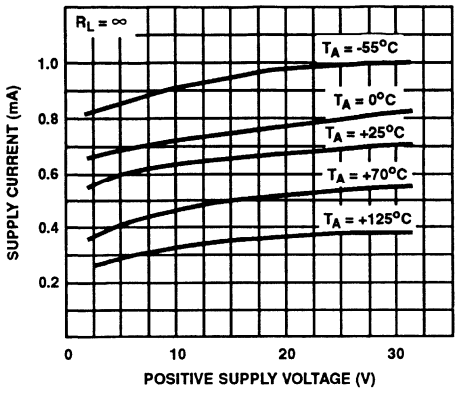


FIGURE 1. SUPPLY CURRENT vs SUPPLY VOLTAGE

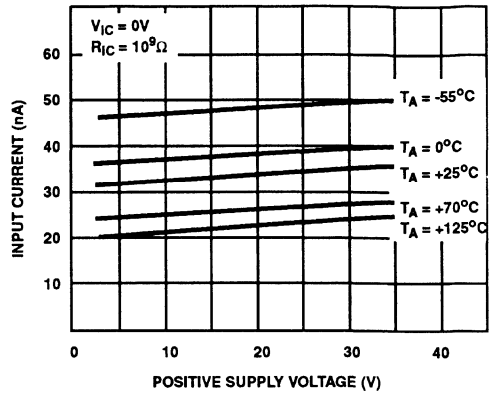


FIGURE 2. INPUT CURRENT vs SUPPLY VOLTAGE

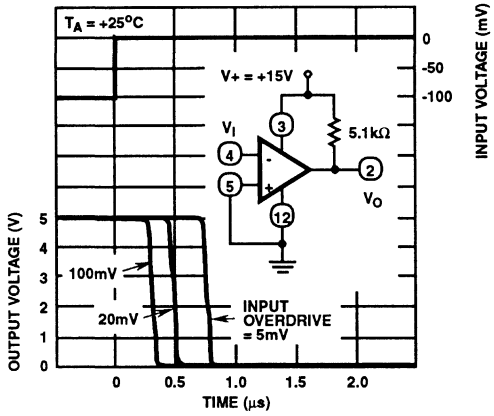


FIGURE 3. RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - NEGATIVE TRANSITION

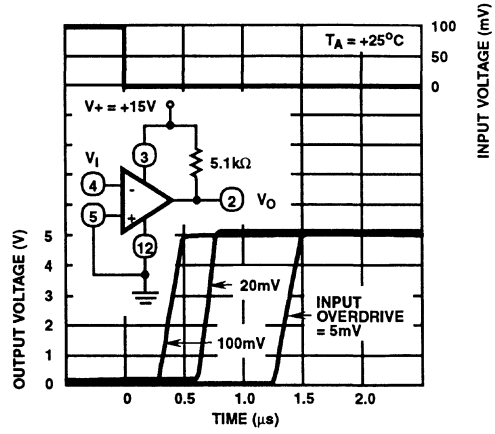


FIGURE 4. RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - POSITIVE TRANSITION

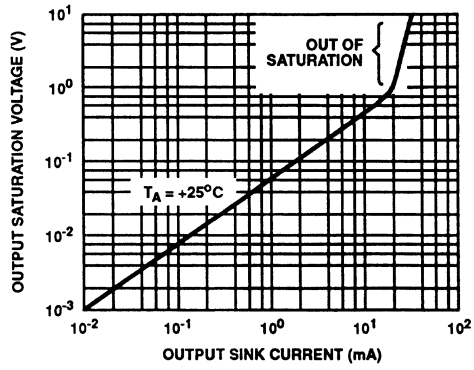


FIGURE 7. OUTPUT SATURATION VOLTAGE vs OUTPUT SINK CURRENT

HARRIS SEMICONDUCTOR

CA3098

Programmable Schmitt Trigger - with Memory Dual Input Precision Level Detectors

March 1993

Features

- Programmable Operating Current
- Micropower Standby Dissipation
- Direct Control of Currents Up to 150mA
- Low Input On/Off Current of Less Than 1nA for Programmable Bias Current of 1μA
- Built-in Hysteresis ..... 20mV (Max)

Applications

- Control of Relays, Heaters, LEDs, Lamps, Photosensitive Devices, Thyristors, Solenoids, etc.
- Signal Reconditioning
- Phase and Frequency Modulators
- On/Off Motor Switching
- Schmitt Triggers, Level Detectors
- Time Delays
- Overvoltage, Overcurrent, Overtemperature Protection
- Battery-Operated Equipment
- Square and Triangular-Wave Generators

Ordering Information

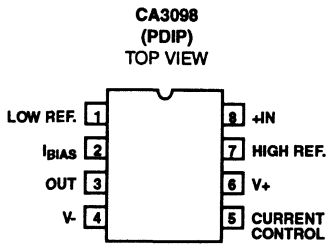
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3098E	-55°C to +125°C	8 Lead Plastic DIP

Description

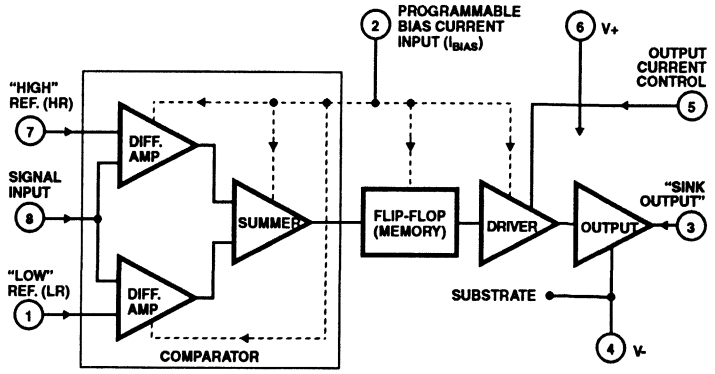
The CA3098 Programmable Schmitt Trigger is a monolithic silicon integrated circuit designed to control high operating current loads such as thyristors, lamps, relays, etc. The CA3098 can be operated with either a single power supply with maximum operating voltage of 16V, or a dual power supply with maximum operating voltage of ±8V. It can directly control currents up to 150mA and operates with microwatt standby power dissipation when the current to be controlled is less than 30mA. The CA3098 contains the following major circuit function features (see Block Diagram):

1. Differential amplifiers and summer: the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.
2. Flip-flop: the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. Driver and output stages: these stages permit the circuit to "sink" maximum peak load currents up to 150mA at terminal 3.
4. Programmable operating current: the circuit incorporates access at terminal 2 to permit programming the desired quiescent operating current and performance parameters.

Pinout



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **896.2**

Absolute Maximum Ratings

Supply Voltage Between V+ and V- 16V
Voltage Between High Reference or Sink Output and V- 16V
Differential Input Voltage Between Terminals 8 and 1 ..... 10V
and Terminals 7 and 8
Load Current (Terminal 3) (Duty Cycle ≤25%) 150mA
Input Current to Voltage Regulator (Terminal 5) 25mA
Programmable Bias Current (Terminal 2) 1mA
Output Current Control (Terminal 5) 15mA
Power Dissipation
Up to T_A = +55°C 990mW
Above T_A = +55°C ..... Derate Linearly at 10.42mW/°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -55°C ≤ T_A ≤ +125°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C
Operating Voltage Range
+IN ..... V- to V+
HIGH REF ..... (V- + 2.0V) to V+
LOW REF ..... (V-) to (V+ - 2.0V)

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
Plastic DIP Package	96	34

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

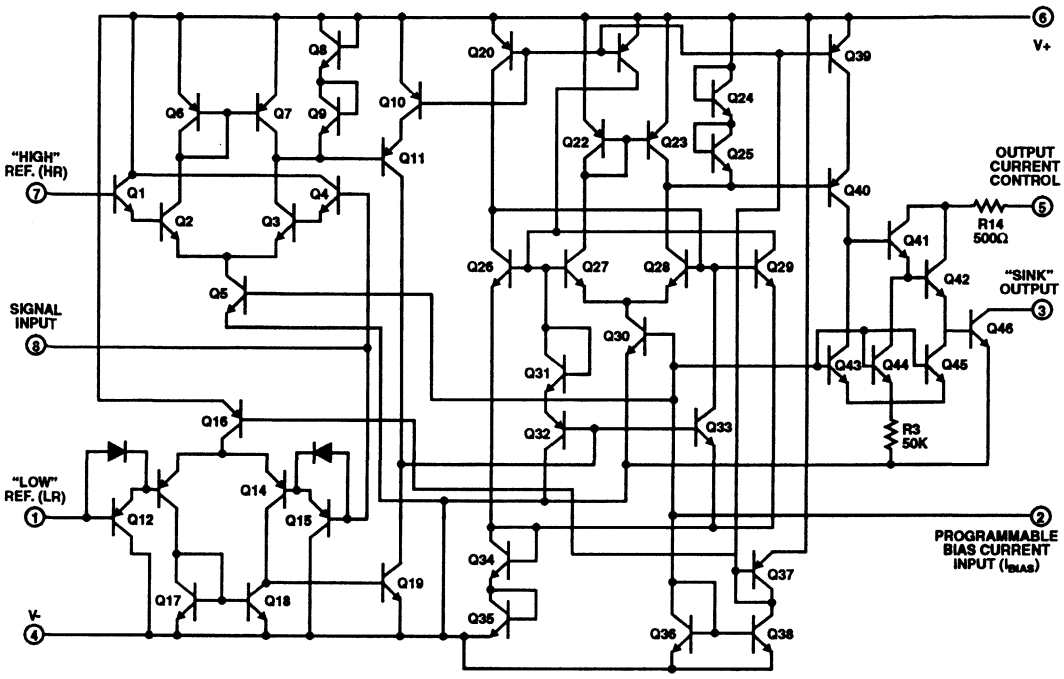
Electrical Specifications T_A = +25°C Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Offset Voltage						
"Low" Reference (See Figures 2, 5)	$V_{IO(LR)}$	V_{LR} = GND, V_{HR} = V+ to (V- + 2V), I_{BIAS} = 100µA	-15	-3	6	mV
"High Reference (See Figures 2, 6)	$V_{IO(HR)}$	V_{HR} = GND, V_{LR} = V- to (V+ - 2V), I_{BIAS} = 100µA	-10	-1	10	mV
Temperature Coefficient						
"Low" Reference (See Figure 7)		-55°C to +125°C	-	4.5	-	µV/°C
"High" Reference (See Figure 8)		-55°C to +125°C	-	±8.2	-	µV/°C
Minimum Hysteresis						
Voltage (Figure 9)	$V_{IO(HR-LR)}$	V_{REG} = 0V (Note 1), V+ = 4V, V- = -4V, I_{BIAS} = 1µA	-	3	20	mV
Temperature Coefficient (Figure 10)		-55°C to +125°C	-	6.7	-	µV/°C
Output Saturation Voltage (Figures 11, 12)	$V_{CE(SAT)}$	V_I = 5V, V_{REG} = 6V (Note 1), V+ = 12V, I_{BIAS} = 100µA	-	0.72	1.2	V
Total Supply Current	I_{TOTAL}					
"ON" (Figures 3, 13, 14)		V_I = 6V, V_{REG} > 6V (Note 1), V+ = 16V, I_{BIAS} = 100µA	500	710	800	µA
"OFF" (Figures 3, 13, 14)		V_I = 10V, V_{REG} < 10V (Note 1), V+ = 16V, I_{BIAS} = 100µA	400	560	750	µA
Input Bias Current (Figures 3, 15)	I_{IB}					
$I_{B(PNP)}$		V_I = 16V, V_{REG} < 16V (Note 1), V+ = 16V, I_{BIAS} = 100µA	-	42	100	nA
$I_{B(NPN)}$		V_I = 6V, V_{REG} > 6V (Note 1), V+ = 16V, I_{BIAS} = 100µA	-	28	100	nA
Output Leakage Current	$I_{CE(OFF)}$	Current from Terminal 3 when Q46 is "OFF"	-	-	10	µA
Switching Times (Figures 4, 16-27)		I_{BIAS} = 100µA, V+ = 5V, V_{REG} = 2.5V (Note 1)				
Delay Time	t_D		-	900	-	ns
Fall Time	t_F		-	30	-	ns
Rise Time	t_R		-	2000	-	ns
Storage Time	t_S		-	6.5	-	µs
Output Current (Note 2)	I_O		100	-	-	mA

NOTES:

1. For definition of V_{REG} see Figure 3.
2. Continuous (DC) output current must be limited to ≤40mA. For 100mA output current, the duty cycle must be ≤40%.

Schematic Diagram

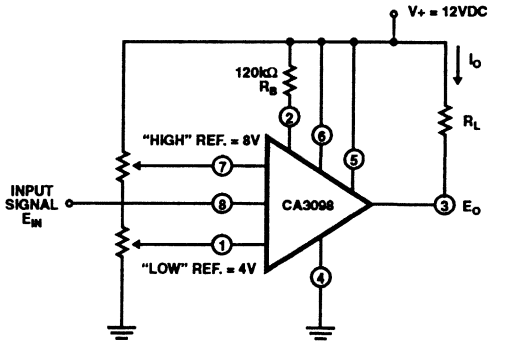


General Description of Circuit Operation

When the signal input voltage of the CA3098 is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to Terminal 3 ("sink" output). This condition is maintained until the signal input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage.

The CA3098 comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{BIAS}) supplied to Terminal 2.

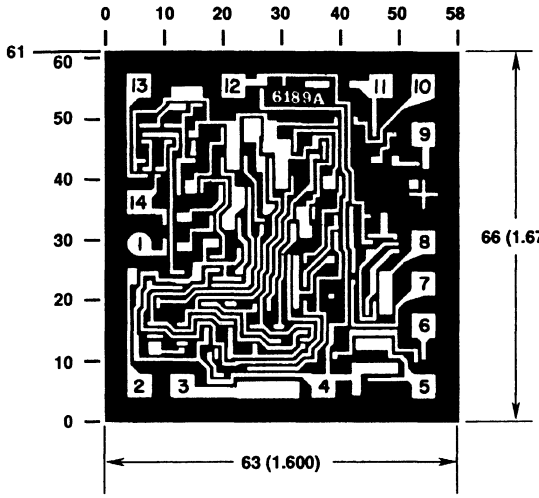
An auxiliary means of controlling the magnitude of load current flow at Terminal 3 is provided by "sinking" current into Terminal 5. Figure 1 highlights the operation of the CA3098 when connected as a simple hysteresis switch (Schmitt trigger).



SEQUENCE	INPUT SIGNAL LEVEL	OUTPUT VOLTAGE (V) (TERMINAL 3)
1	$4 \geq E_{IN} > 0$	0
2	$8 \geq E_{IN} > 4$	0
3	$E_{IN} > 8$	12
2	$8 \geq E_{IN} > 4$	12
1	$4 \geq E_{IN} > 0$	0

FIGURE 1. BASIC HYSTERESIS SWITCH (SCHMITT TRIGGER) AND RESULTANT OUTPUT STATES

Metallization Mask Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

Test Circuits

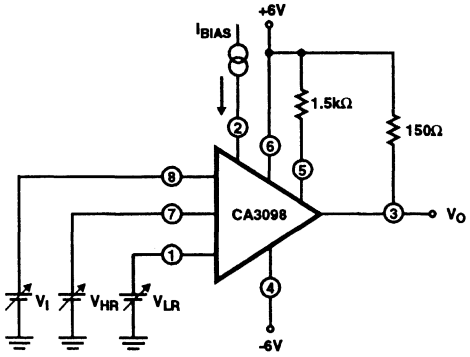


FIGURE 2. INPUT OFFSET VOLTAGE TEST CIRCUIT

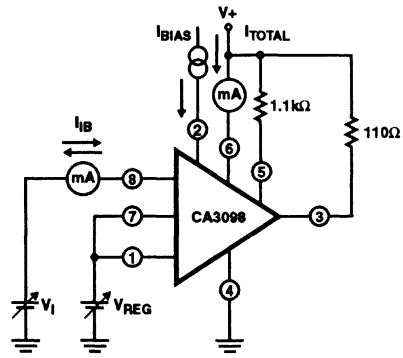
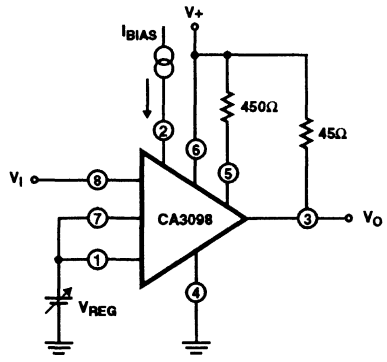


FIGURE 3. TOTAL SUPPLY CURRENT, AND INPUT BIAS CURRENT TEST CIRCUIT



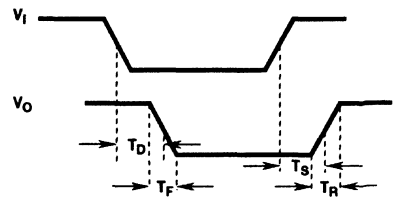


FIGURE 4. SWITCHING TIME TEST CIRCUIT

Typical Performance Curves

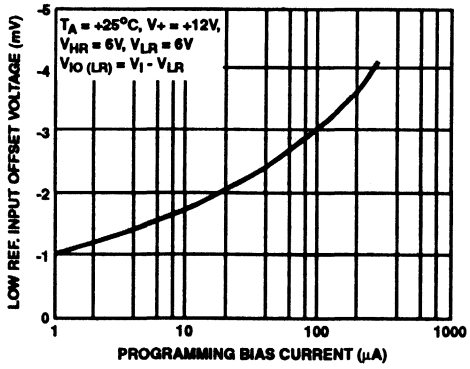


FIGURE 5. INPUT OFFSET VOLTAGE ("LOW" REFERENCE) vs PROGRAMMING BIAS CURRENT

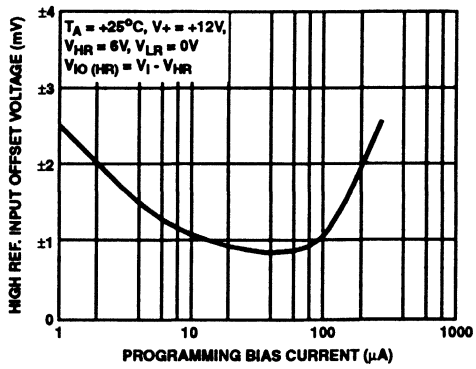


FIGURE 6. INPUT OFFSET VOLTAGE ("HIGH" REFERENCE) vs PROGRAMMING BIAS CURRENT

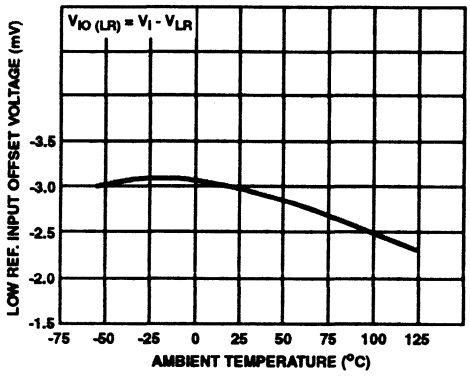


FIGURE 7. INPUT OFFSET VOLTAGE ("LOW" REFERENCE) vs AMBIENT TEMPERATURE

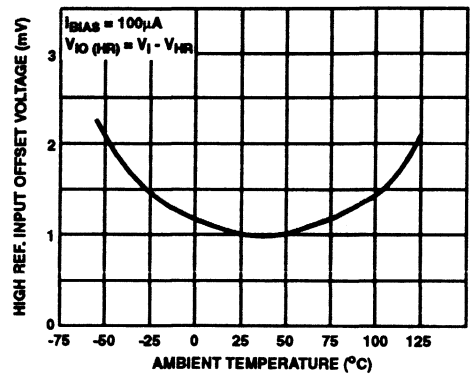


FIGURE 8. INPUT OFFFSET VOLTAGE ("HIGH" REFERENCE) vs AMBIENT TEMPERATURE

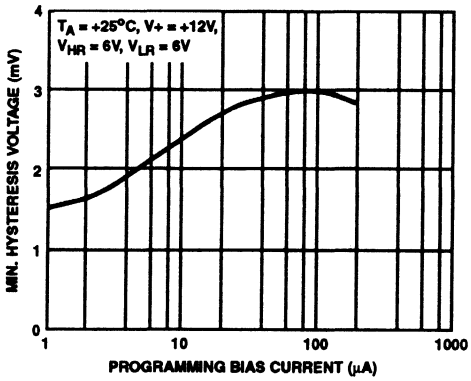


FIGURE 9. MINIMUM HYSTERESIS VOLTAGE vs PROGRAMMING BIAS CURRENT

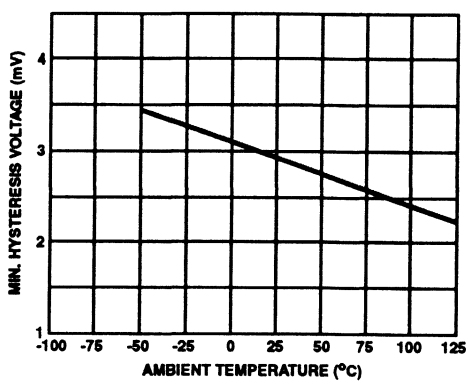


FIGURE 10. MINIMUM HYSTERESIS VOLTAGE vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

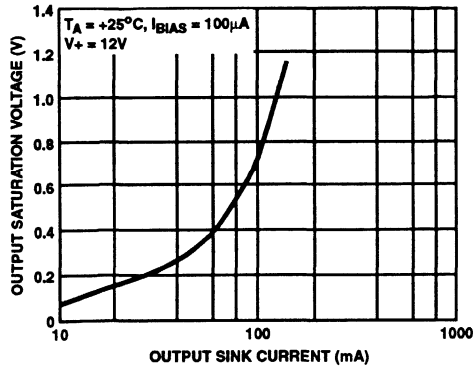


FIGURE 11. OUTPUT SATURATION VOLTAGE vs OUTPUT SINK CURRENT

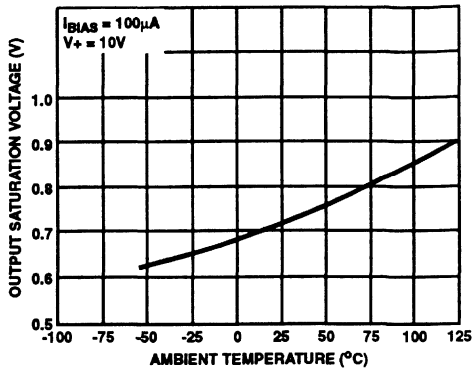
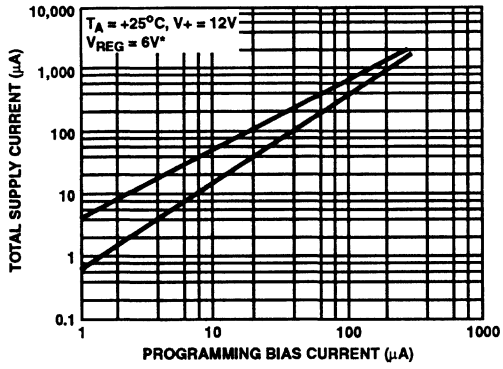


FIGURE 12. OUTPUT SATURATION VOLTAGE vs AMBIENT TEMPERATURE



* See Figure 3 for definition of V_{REG}

FIGURE 13. TOTAL SUPPLY CURRENT vs PROGRAMMING BIAS CURRENT

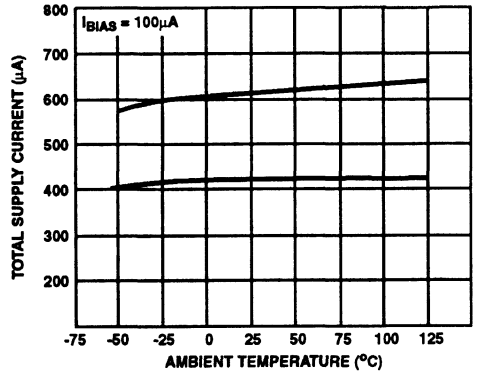
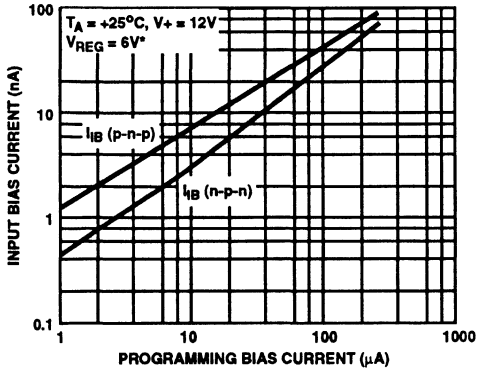


FIGURE 14. TOTAL SUPPLY CURRENT vs AMBIENT TEMPERATURE



* See Figure 3 for definition of V_{REG}

FIGURE 15. INPUT BIAS CURRENT vs PROGRAMMING BIAS CURRENT

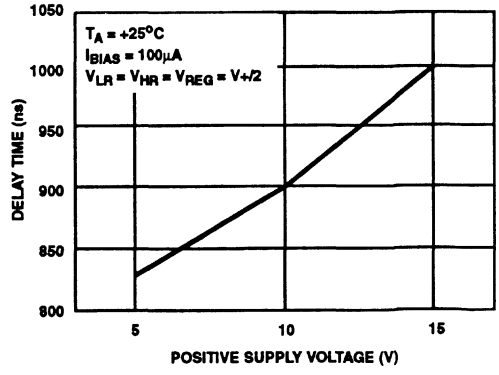


FIGURE 16. DELAY TIME vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

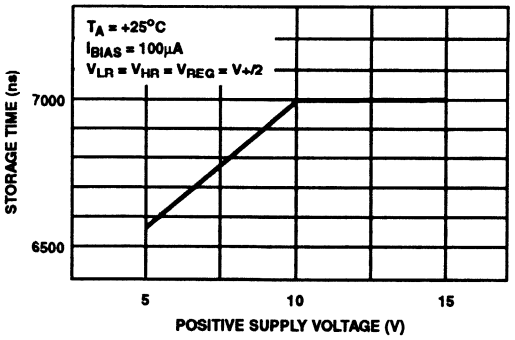


FIGURE 17. STORAGE TIME vs SUPPLY VOLTAGE

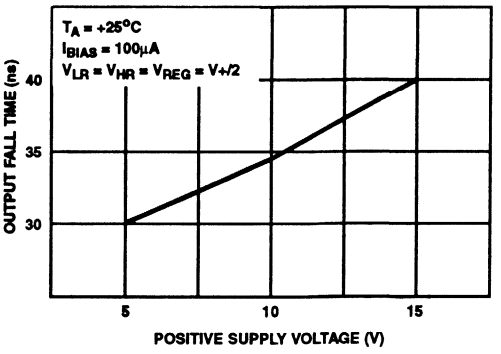


FIGURE 18. OUTPUT FALL TIME vs SUPPLY VOLTAGE

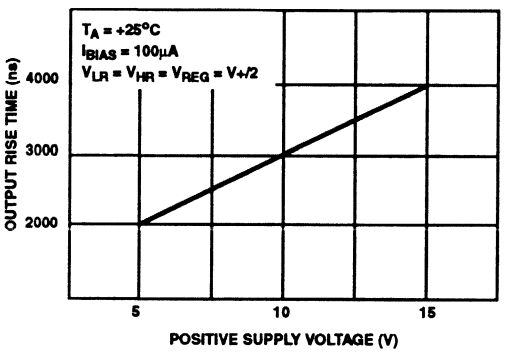


FIGURE 19. OUTPUT RISE TIME vs SUPPLY VOLTAGE

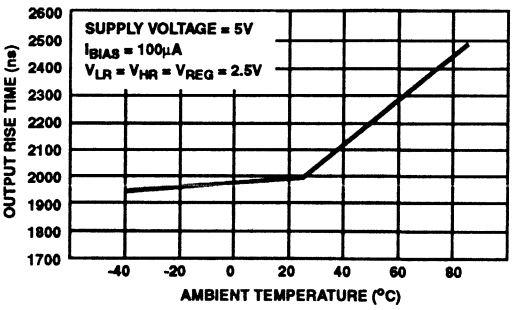


FIGURE 20. OUTPUT RISE TIME vs AMBIENT TEMPERATURE

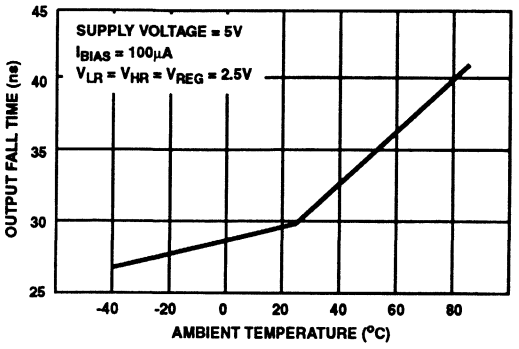


FIGURE 21. OUTPUT FALL TIME vs AMBIENT TEMPERATURE

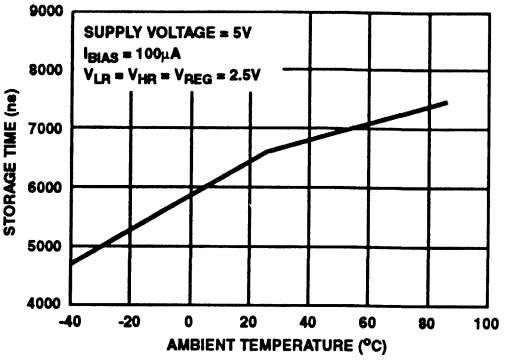


FIGURE 22. STORAGE TIME vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

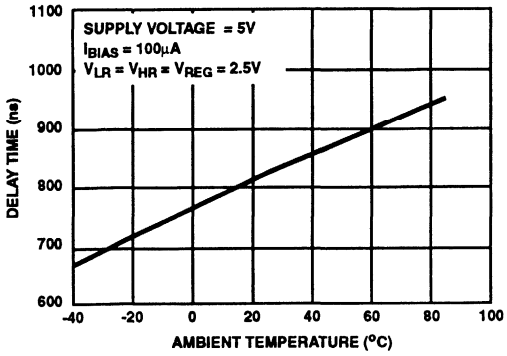


FIGURE 23. DELAY TIME vs AMBIENT TEMPERATURE

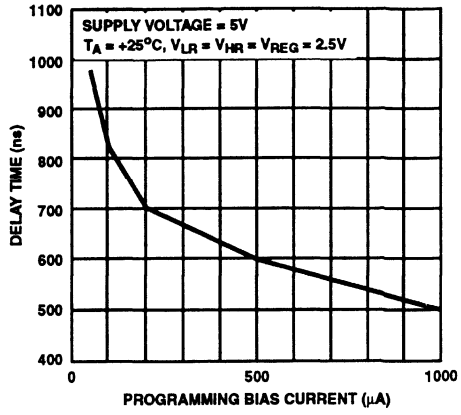


FIGURE 24. DELAY TIME vs PROGRAMMING BIAS CURRENT

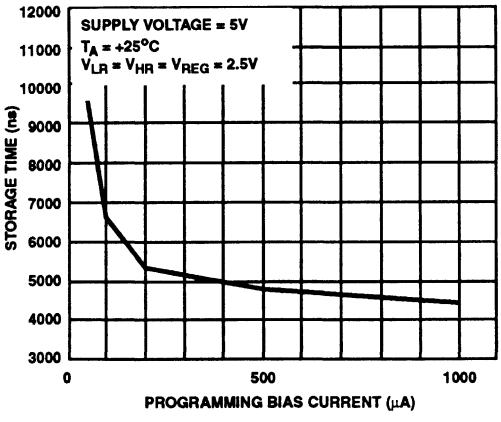


FIGURE 25. STORAGE TIME vs PROGRAMMING BIAS CURRENT

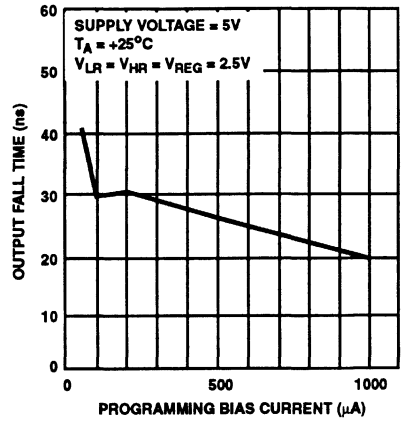


FIGURE 26. OUTPUT FALL TIME vs PROGRAMMING BIAS CURRENT

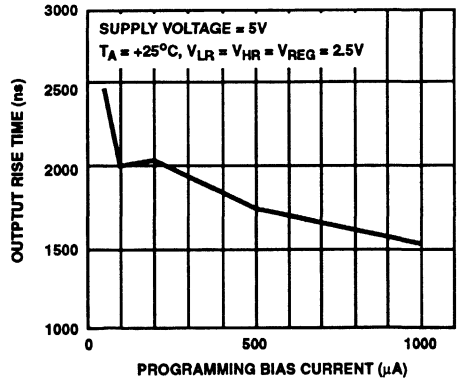


FIGURE 27. OUTPUT RISE TIME vs PROGRAMMING BIAS CURRENT

Typical Applications

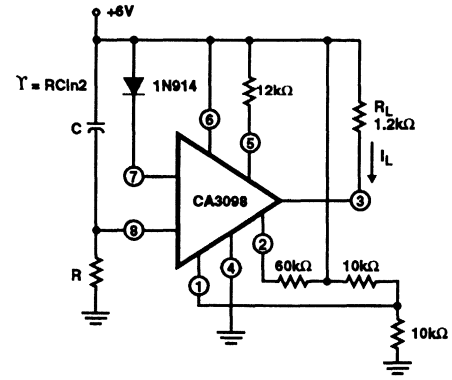


FIGURE 28. TIME DELAY CIRCUIT: TERMINAL 3 "SINKS" AFTER ϒ SECONDS

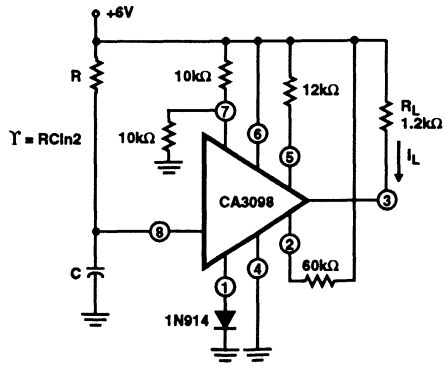


FIGURE 29. TIME DELAY CIRCUIT: "SINK" CURRENT INTERRUPTED AFTER ϒ SECONDS

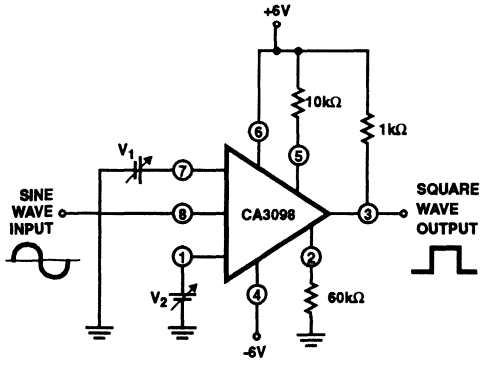
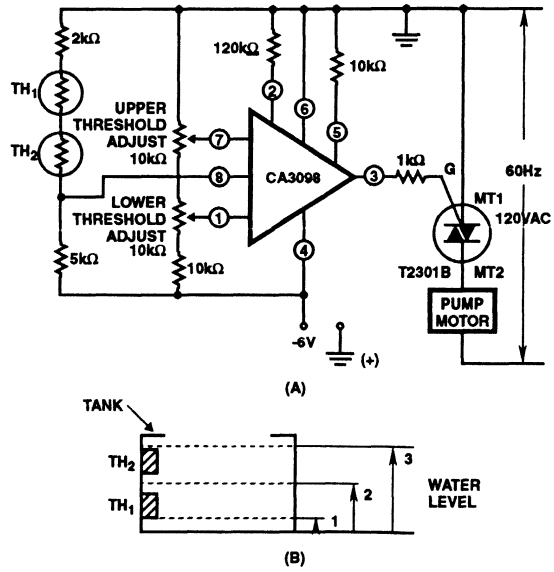


FIGURE 30. SINE WAVE TO SQUARE WAVE CONVERTER WITH DUTY CYCLE ADJUSTMENT (V_1 AND V_2)



NOTES:

1. Motor pump is "ON" when water level rises above thermistor TH_2.
2. Motor pump remains "ON" until water level falls below thermistor TH_1.
3. Thermistors, operate in self heating mode.

FIGURE 31. (A) WATER LEVEL CONTROL CIRCUIT (B) WATER LEVEL DIAGRAM FOR CIRCUIT

Typical Applications (Continued)

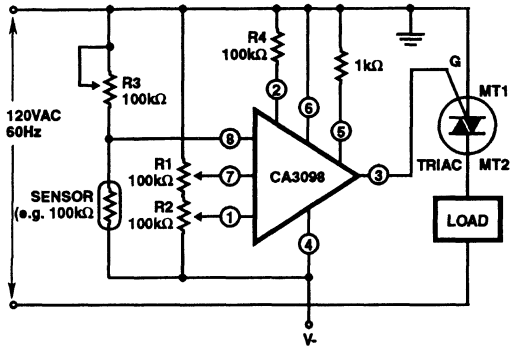
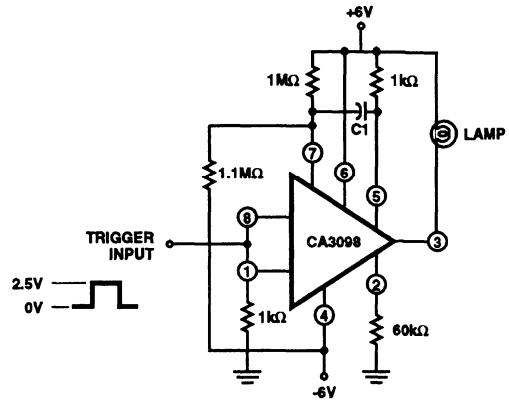


FIGURE 32. OFF/ON CONTROL OF TRIAC WITH PROGRAMMABLE HYSTERESIS



DESIRED t_{ON} (ms)	VALUE OF C1 (μF)
15	0.01
150	0.1
300	0.2

NOTE: Input pulse must be greater than 1ms but less than desired t_{ON}

FIGURE 33. ONE SHOT MULTIVIBRATOR

HARRIS SEMICONDUCTOR

CA3290

BiMOS Dual Voltage Comparator with MOSFET Input, Bipolar Output

March 1993

Features

- MOSFET Input Stage
  - Very High Input Impedance (Z_{IN}).....1.7TΩ (Typ.)
  - Very Low Input Current at V+ = 5V.....3.5pA (Typ.)
  - Wide Common Mode Input Voltage Range (V_{ICR}) can be swung 1.5V (Typ.) Below Negative Supply Voltage Rail
  - Virtually Eliminates Errors Due to Flow of Input Currents
- Output Voltage Compatible with TTL, DTL, ECL, MOS, and CMOS Logic Systems in Most Applications

Applications

- High Source Impedance Voltage Comparators
- Long Time Delay Circuits
- Square Wave Generators
- A/D Converters
- Window Comparators

Description

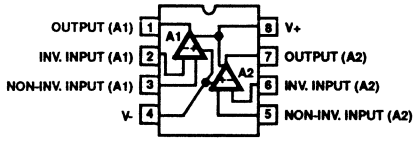
The CA3290A and CA3290 types consist of a dual voltage comparator on a single monolithic chip. The common mode input voltage range includes ground even when operated from a single supply. The low supply current drain makes these comparators suitable for battery operation; their extremely low input currents allow their use in applications that employ sensors with extremely high source impedances. Package options are shown in the table below.

Ordering Information

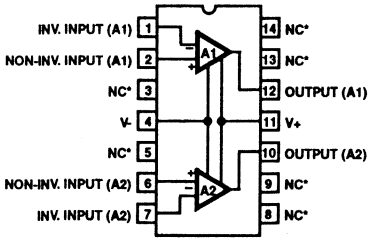
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3290AE	-55°C to +125°C	8 Lead Plastic DIP
CA3290AE1	-55°C to +125°C	14 Lead Plastic DIP
CA3290AT	-55°C to +125°C	8 Pin TO-5 Can
CA3290BT	-55°C to +125°C	8 Pin TO-5 Can
CA3290E	-55°C to +125°C	8 Lead Plastic DIP
CA3290E1	-55°C to +125°C	14 Lead Plastic DIP
CA3290T	-55°C to +125°C	8 Pin TO-5 Can

Pinouts

CA3290/A (PDIP)
TOP VIEW

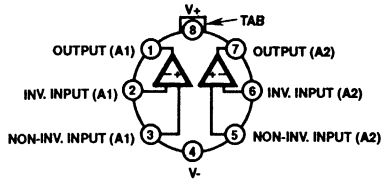


CA3290A, CA3290 (PDIP)
TOP VIEW



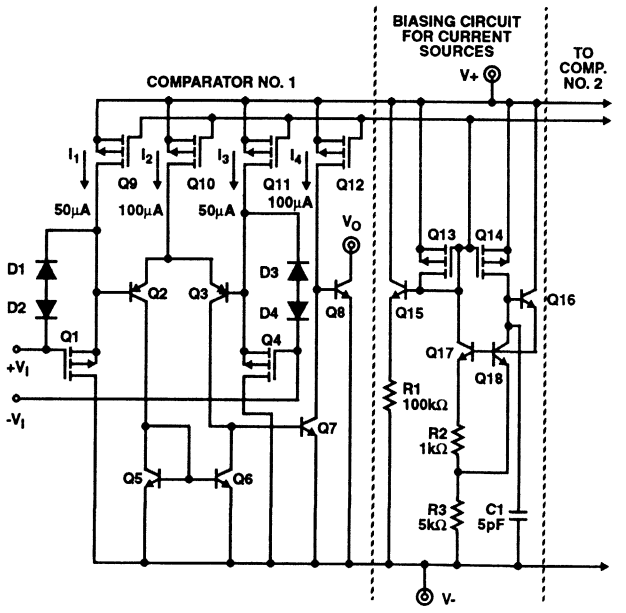
* Tie to GND or V+ for best Input/Output Isolation

CA3290A, CA3290, CA3290B (TO-5 CAN)
TOP VIEW



Schematic Diagram

(ONLY ONE IS SHOWN)



File Number 1049.1

Absolute Maximum Ratings

Supply Voltage
- Single Supply ..... +36V
- Dual Supply ..... ±18V

Differential Input Voltage ..... 36V or [(V+ - V-) +5V] (whichever is less)
DC Input Voltage ..... V+ +5V to V- -5V
Output to V- Short Circuit Duration (Note 1) ..... Continuous
Input Current 1mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... $-55°C \le T_A \le +125°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
8 Lead Plastic DIP Package	94	32
14 Lead Plastic DIP Package	107	38
TO-5 Can Package	114	35

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V- = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA3290A			CA3290			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	T_A = -55°C to +125°C, $V_{CM} = V_O$ = 1.4V, V+ = 5V	-	4.5	-	-	8.5	-	mV
		T_A = -55°C to +125°C, $V_{CM} = V_O$ = 0V, V+ = +15V, V- = -15V	-	8.5	-	-	8.5	-	mV
		T_A = +25°C, $V_{CM} = V_O$ = 1.4V, V+ = 5V	-	4.0	10	-	7.5	20	mV
		T_A = +25°C, $V_{CM} = V_O$ = 0V, V+ = +15V, V- = -15V	-	4.0	10	-	7.5	20	mV
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$		-	8	-	-	8	-	µV/°C
Input Offset Current	I_{IO}	T_A = -55°C to +125°C, V_{CM} = 1.4V, V+ = 5V	-	2	28	-	2	32	nA
		T_A = -55°C to +125°C, V_{CM} = 0V, V+ = +15V, V- = -15V	-	7	28	-	7	32	nA
		T_A = +25°C, V_{CM} = 1.4V, V+ = 5V	-	2	25	-	2	30	pA
		T_A = +25°C, V_{CM} = 0V, V+ = +15V, V- = -15V	-	7	25	-	7	30	pA
Input Current	I_I	T_A = +125°C, V_{CM} = 1.4V, V+ = 5V	-	2.8	45	-	2.8	55	nA
		T_A = +125°C, V_{CM} = 0V, V+ = +15V, V- = -15V	-	13	45	-	13	55	nA
		T_A = +25°C, V_{CM} = 1.4V, V+ = 5V	-	3.5	40	-	3.5	50	pA
		T_A = +25°C, V_{CM} = 0V, V+ = +15V, V- = -15V	-	12	40	-	12	50	pA
Supply Current	I+	T_A = -55°C, R_L = ∞, V+ = 5V	-	0.85	1.0	-	0.85	1.6	mA
		T_A = -55°C, R_L = ∞, V+ = 30V	-	1.62	3.0	-	1.62	3.5	mA
		T_A = +25°C, R_L = ∞, V+ = 5V	-	0.8	1.4	-	0.8	1.4	mA
		T_A = +25°C, R_L = ∞, V+ = 30V	-	1.35	3.0	-	1.35	3.0	mA

Electrical Specifications V- = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA3290A			CA3290			
			MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Gain	A_{OL}	T_A = -55°C to +125°C, R_L = 15kΩ, V+ = +15V, V- = -15V	-	150	-	-	150	-	V/mV
			-	103	-	-	103	-	dB
		T_A = +25°C, R_L = 15kΩ, V+ = +15V, V- = -15V	25	800	-	25	800	-	V/mV
			88	118	-	88	118	-	dB
Saturation Voltage	V_{SAT}	T_A = +125°C, I_{SINK} = 4mA, V+ = 5V, $+V_I$ = 0V, $-V_I$ = 1V	-	0.22	0.7	-	0.22	0.7	V
		T_A = -55°C, I_{SINK} = 4mA, V+ = 5V, $+V_I$ = 0V, $-V_I$ = 1V	-	0.1	-	-	0.1	-	V
		T_A = +25°C, I_{SINK} = 4mA, V+ = 5V, $+V_I$ = 0V, $-V_I$ = 1V	-	0.12	0.4	-	0.12	0.4	V
Output Leakage Current	I_{OL}	T_A = -55°C to +125°C, V+ = 15V	-	65	-	-	65	-	nA
		T_A = -55°C to +125°C, V+ = 36V	-	130	1k	-	130	1k	nA
		T_A = +25°C, V+ = 15V	-	100	-	-	100	-	pA
		T_A = +25°C, V+ = 36V	-	500	-	-	500	-	pA
Common Mode Input Voltage Range	V_{ICR}	T_A = +25°C, V_O = 1.4V, V+ = 5V	V+-3.5 V-	V+-3.1 V- -1.5	-	V+-3.5 V-	V+-3.1 V- -1.5	-	V
		T_A = +25°C, V_O = 0V, V+ = +15V, V- = -15V	V+-3.8 V-	V+-3.4 V- -1.6	-	V+-3.8 V-	V+-3.4 V- -1.6	-	V
Common Mode Rejection Ratio	CMRR	T_A = +25°C, V+ = +15V, V- = -15V	-	44	562	-	44	562	µV/V
		T_A = +25°C, V+ = 5V	-	100	562	-	100	562	µV/V
Power Supply Rejection Ratio	PSRR	T_A = +25°C, V+ = +15V, V- = -15V	-	15	316	-	15	316	µV/V
Output Sink Current		T_A = +25°C, V_O = 1.4V, V+ = 5V	6	30	-	6	30	-	mA
Response Time Rising Edge	T_R	T_A = +25°C, R_L = 5.1kΩ, V+ = 15V	-	1.2	-	-	1.2	-	µs
Response Time Falling Edge	T_F	T_A = +25°C, R_L = 5.1kΩ, V+ = 15V	-	200	-	-	200	-	ns
Large Signal Response Time		T_A = +25°C, R_L = 5.1kΩ, V+ = 15V	-	500	-	-	500	-	ns
		T_A = +25°C, R_L = 5.1kΩ, V+ = 5V	-	400	-	-	400	-	ns

NOTE:

1. Short circuits from the output to V+ can cause excessive heating and eventual destruction of the device.

Circuit Description

The Basic Comparator

Figure 1 shows the basic circuit diagram for one of the two comparators in the CA3290. It is generically similar to the industry type "139" comparators, with PMOS transistors replacing p-n-p transistors as input stage elements. Transistors Q1 through Q4 comprise the differential input stage, with Q5 and Q6 serving as a mirror connected active load and differential-to-single-ended converter. The differential input at Q1 and Q4 is amplified so as to toggle Q6 in accordance with the input signal polarity. For example, if $+V_{IN}$ is greater than $-V_{IN}$, Q1, Q2, and current mirror transistors Q5 and Q6 will be turned off; Transistors Q3, Q4, and Q7 will be turned on, causing Q8 to be turned off. The output is pulled positive when a load resistor is connected between the output and V+.

In essence, Q1 and Q4 function as source followers to drive Q2 and Q3, respectively, with zener diodes D1 through D4 providing gate oxide protection against input voltage transients (e.g., static electricity). The current flow in Q1 and Q4 is established at approximately 50μA by constant current sources I_1 and I_3, respectively. Since Q1 and Q4 are operated with a constant current load, their gate-to-source voltage drops will be effectively constant as long as the input voltages are within the common-mode range.

As a result, the input offset voltage ($V_{GS(Q1)} + V_{BE(Q2)} - V_{BE(Q3)} - V_{GS(Q4)}$) will not be degraded when a large differential dc voltage is applied to the device for extended periods of time at high temperatures.

Additional voltage gain following the first stage is provided by transistors Q7 and Q8. The collector of Q8 is open, offering the user a wide variety of options in applications. An additional discrete transistor can be added if it becomes necessary to boost the output sink current capability.

The detailed schematic diagram for one comparator and the common current source biasing is shown on the front page. PMOS transistors Q9 through Q12 are the current source elements identified in Figure 1 as I_1 through I_4, respectively. Their gate source potentials (V_{GS}) are supplied by a common bus from the biasing circuit shown in the right hand portion of the Schematic Diagram. The currents supplied by Q10 and Q12 are twice those supplied by Q9 and Q11. The transistor geometries are appropriately scaled to provide the requisite currents with common V_{GS} applied to Q9 through Q12.

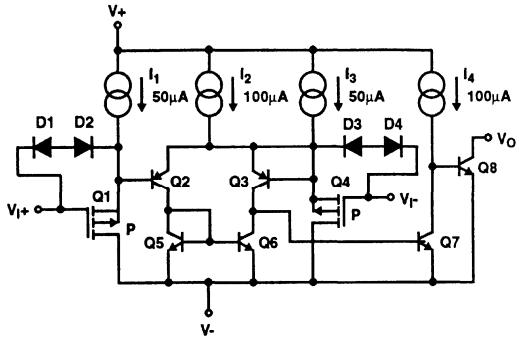
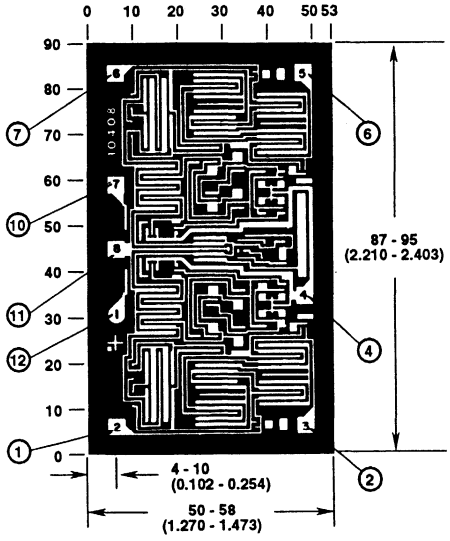


FIGURE 1. BASIC CIRCUIT DIAGRAM FOR ONE OF THE TWO COMPARATORS

Metallization Mask Layout

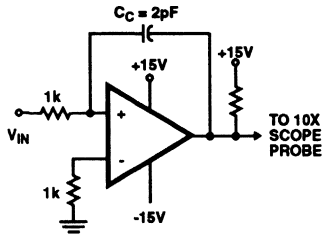


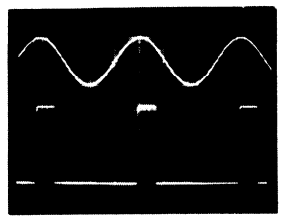
The photographs and dimensions of each chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

NOTE: Numbers in pads are for 8 lead DIP and TO-5 Can and numbers outside of chip are for 14 lead DIP

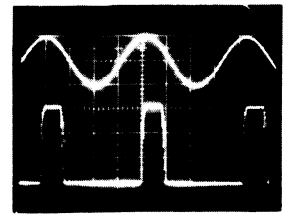
Test Circuits and Waveforms





WITH C_C

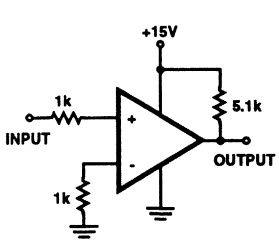
Top Trace = 4.5mV/Div = V_{IN}
Bottom Trace = 10V/Div = V_{OUT}
H = 5μs/Div

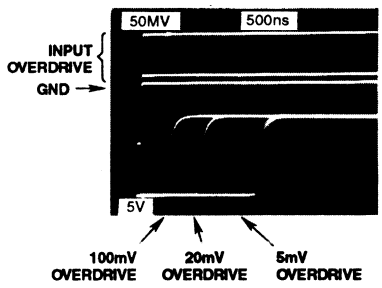


WITHOUT C_C

Top Trace = 4.5mV/Div
Bottom Trace = 10V/Div
H = 5μs/Div

FIGURE 2. PARASITIC OSCILLATIONS TEST CIRCUIT AND WAVEFORMS





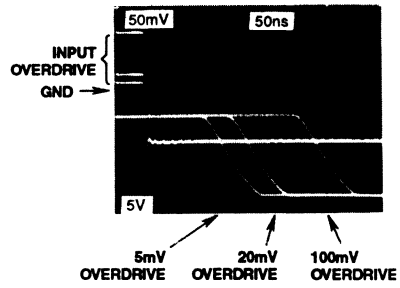
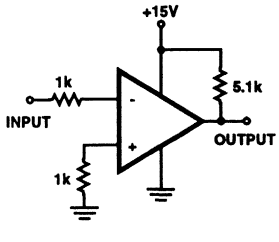
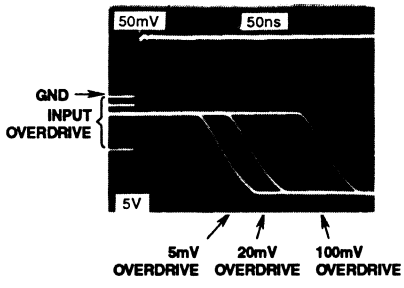


FIGURE 3. NON-INVERTING COMPARATOR RESPONSE TIME TEST CIRCUIT AND WAVEFORMS





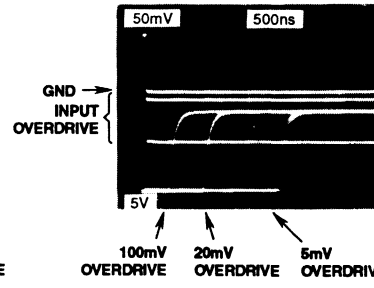


FIGURE 4. INVERTING COMPARATOR RESPONSE TIME TEST CIRCUIT AND WAVEFORMS

Typical Performance Curves

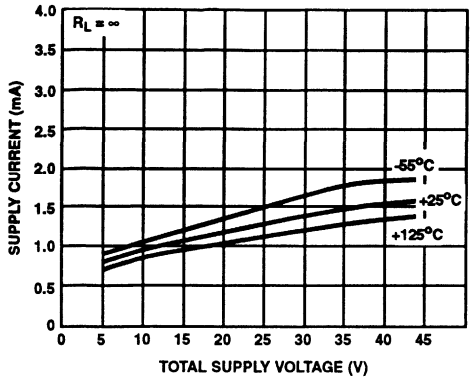


FIGURE 5. SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE (BOTH AMPLIFIERS)

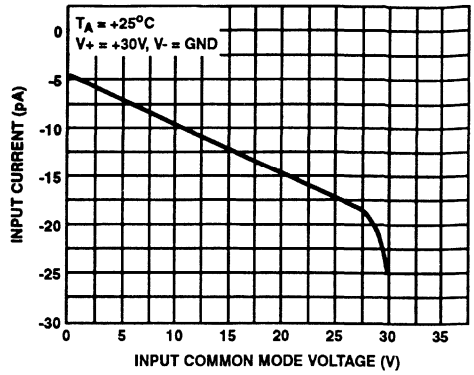


FIGURE 6. INPUT CURRENT AS A FUNCTION OF INPUT COMMON MODE VOLTAGE

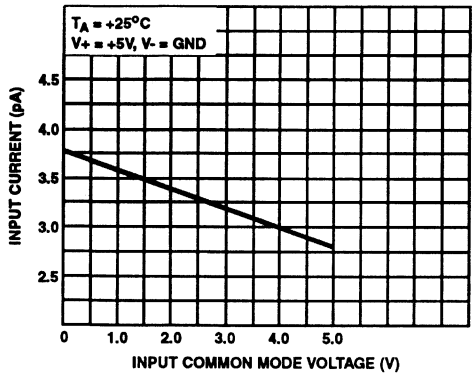


FIGURE 7. INPUT CURRENT AS A FUNCTION OF INPUT COMMON MODE VOLTAGE

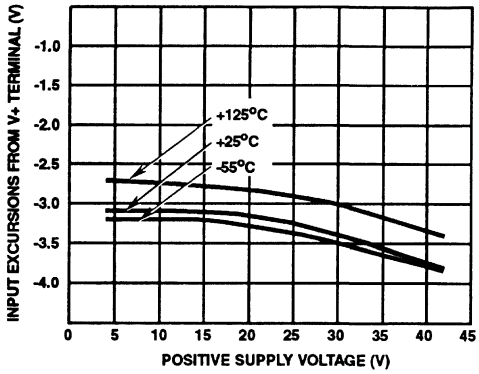


FIGURE 8. POSITIVE COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

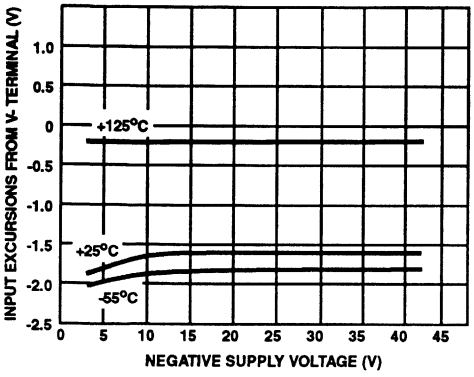


FIGURE 9. NEGATIVE COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

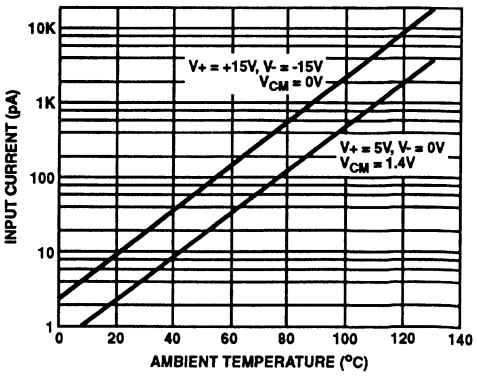


FIGURE 10. INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

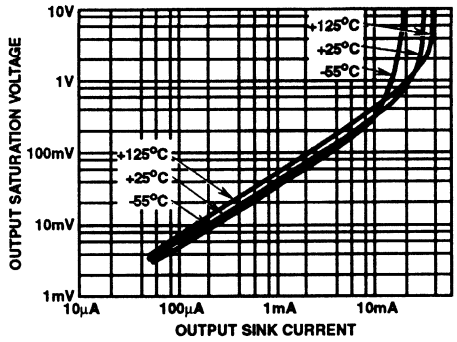


FIGURE 11. OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT

Operating Considerations

Input Circuit

The use of MOS transistors in the input stage of the CA3290 series circuits provides the user with the following features for comparator applications:

1. Ultra high input impedance (≅1.7TΩ);
2. The availability of common mode rejection for input signals at potentials below that of the negative power supply rail;
3. Retention of the in phase relationship of the input and output signals for input signals below the negative rail.

Although the CA3290 employs rugged bipolar (zener) diodes for protection of the input circuit, the input terminal currents should not exceed 1mA. Appropriate series connected limiting resistors should be used in circuits where greater current flows might exist, allowing the signal input voltage to be greater than the supply voltage without damaging the circuit.

Output Circuit

The output of the CA3290 is the open collector of an n-p-n transistor, a feature providing flexibility in a broad range of comparator applications. An output ORing function can be implemented by parallel connection of the open collectors. An output pull-up resistor can be connected to a power supply having a voltage range within the rating of the particular CA3290 in use; the magnitude of this voltage may be set at a value which is independent of that applied to the V+ terminal of the CA3290.

Parasitic Oscillations

The ideal comparator has, among other features, ultra high input impedance, high gain, and wide bandwidth. These desirable characteristics may, however, produce parasitic oscillations unless certain precautions are observed to minimize the stray capacitive coupling between the input and output terminals. Parasitic oscillations manifest themselves during the output voltage transition intervals as the comparator switches states. For high source impedances, stray capacitance can induce parasitic oscillations. The addition of a small amount (1mV to 10mV) of positive feedback (hysteresis) produces a faster transition, thereby reducing the likelihood of parasitic oscillations. Furthermore, if the input signal is a pulse waveform, with relatively rapid rise and fall times, parasitic tendencies are reduced.

When dual comparators, like the CA3290, are packaged in an 8 lead configuration, the output terminal of each comparator is adjacent to an input terminal. The lead-to-lead capacitance is approximately 1pF, which may be sufficient to cause undesirable feedback effects in certain applications. Circuit factors such as impedance levels, supply voltage, switching rate, etc., may increase the possibility of parasitic oscillations. To minimize this potential oscillatory condition, it is recommended that for source impedances greater than 1kΩ a capacitor (≥ 1pF - 2pF) be connected between the appropriate input terminal and the output terminal. (See Figure 2.)

The CA3290A and CA3290 are also supplied in a 14 lead dual-in-line plastic package. To minimize the possibility of parasitic oscillations the input and output terminals are positioned on opposite sides of the package. In addition, there are two leads between the output terminal of each comparator and its corresponding inverting input terminal, reducing the input/output coupling significantly. These leads (8, 9, 13, 14) should be tied to either the V+ or V- supply rail. If either comparator is unused, its input terminals should also be tied to either the V+ or V- supply rail.

Typical Applications

Light Controlled One-Shot Timer

In Figure 12 one comparator (A1) of the CA3290 is used to sense a change in photo diode current. The other comparator (A2) is configured as a one-shot timer and is triggered by the output of A1. The output of the circuit will switch to a low state for approximately 60 seconds after the light source to the photo diode has been interrupted. The circuit operates at normal room lighting levels. The sensitivity of the circuit may be adjusted by changing the values of R1 and R2. The ratio of R1 to R2 should be constant to insure constant reverse voltage bias on the photo diode.

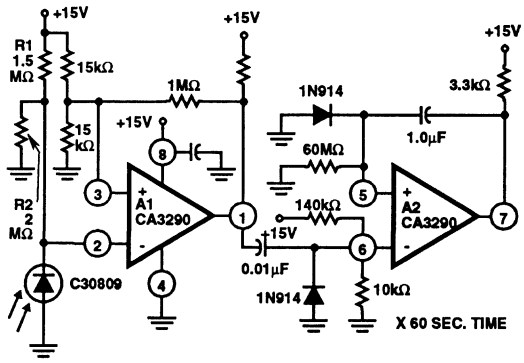


FIGURE 12. LIGHT CONTROLLED ONE-SHOT TIMER

Low-Frequency Multivibrator

In this application, one half of the CA3290 is used as a conventional multivibrator circuit. Because of the extremely high input impedance of this device, large values of timing resistor (R1) may be used for long time delays with relatively small leakage timing capacitors. The second half of the CA3290 is used as an output buffer to insure that the multivibrator frequency will not be affected by output loading. RP is the parallel combination of the two 1MΩ resistors connected between +15V and GND.

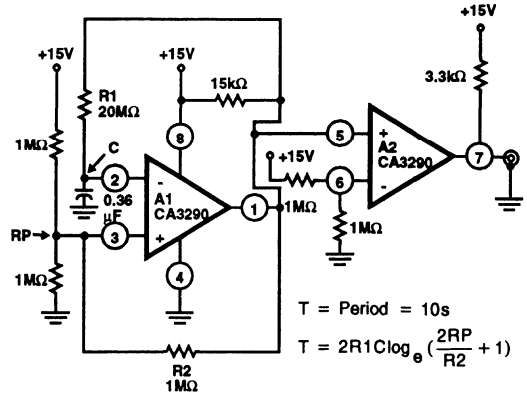


FIGURE 13. LOW FREQUENCY MULTIVIBRATOR

Window Comparator

Both halves of the CA3290 can be used in a high input impedance window comparator as shown in Figure 14. The LED will be turned "on" whenever the input signal is above the lower limit (V_L) but below the upper limit (V_U), as determined by the R1/R2/R3 resistor divider.

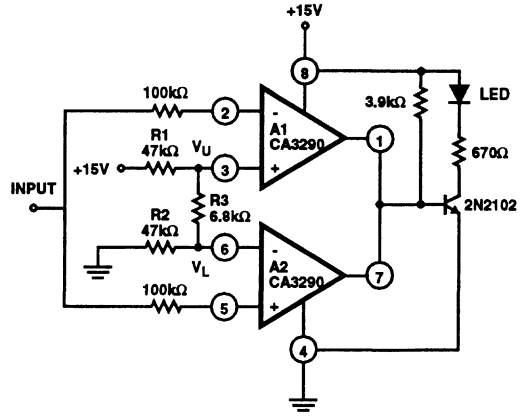


FIGURE 14. WINDOW COMPARATOR

HARRIS SEMICONDUCTOR

HA-4900, HA-4902 HA-4905

March 1993

Precision Quad Comparator

Features

- Fast Response Time 130ns
- Low Offset Voltage..... 2.0mV
- Low Offset Current 10nA
- Single or Dual Voltage Supply Operation
- Selectable Output Logic Levels
- Active Pull-Up/Pull-Down Output Circuit. No External Resistors Required

Applications

- Threshold Detector
- Zero Crossing Detector
- Window Detector
- Analog Interfaces for Microprocessors
- High Stability Oscillators
- Logic System Interfaces

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-4900-2	-55°C to +125°C	16 Lead Ceramic DIP
HA1-4902-2	-55°C to +125°C	16 Lead Ceramic DIP
HA1-4905-5	0°C to +75°C	16 Lead Ceramic DIP
HA3-4905-5	0°C to +75°C	16 Lead Plastic DIP
HA4P4905-5	0°C to +75°C	20 Lead PLCC
HA9P4905-5	0°C to +75°C	16 Lead Wide Body SOIC

Description

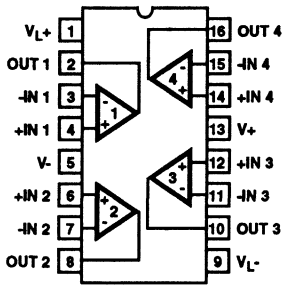
The HA-4900 series are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5V supply (digital systems) or from dual supplies (analog networks) up to ±15V. The HA-4900 series contains a unique current driven output stage which can be connected to logic system supplies (V_{LOGIC}+ and V_{LOGIC}-) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900 series input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

These comparators' combination of features make them ideal components for signal detection and processing in data acquisition systems, test equipment and microprocessor/analog signal interface networks.

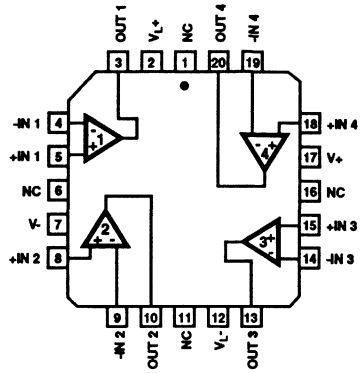
For military grade product, refer to the HA-4902/883 data sheet.

Pinout

HA-4900, HA-4902 (CDIP)
HA-4905 (PDIP, CDIP, 300 mil SOIC)
TOP VIEW



HA-4905
(PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2855.1**

Absolute Maximum Ratings (Note 1)

Supply Voltage (Between V+ and V- Terminals) 33V
Differential Input Voltage 15V
Voltage Between V_{Logic}+ and V_{Logic}- 18V
Output Current 50mA
Power Dissipation (Notes 7, 8)
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-4900-2 ..... $-55°C \le T_A \le +125°C$
HA-4902-2 ..... $-55°C \le T_A \le +125°C$
HA-4905-5 ..... $0°C \le T_A \le +75°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP Package	71	13
Plastic DIP Package	86	25
SOIC Package	96	26
PLCC Package	74	32

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = +15V, V- = -15V, V_{LOGIC}+ = 5V, V_{LOGIC}- = GND

PARAMETER	TEMP	HA-4900-2 -55°C to +125°C			HA-4902-2 -55°C to +125°C			HA-4905-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage (Note 2)	+25°C	-	2	3	-	2	5	-	4	7.5	mV
	Full	-	-	4	-	-	8	-	-	10	mV
Offset Current	+25°C	-	10	25	-	10	35	-	25	50	nA
	Full	-	-	35	-	-	45	-	-	70	nA
Bias Current (Note 3)	+25°C	-	50	75	-	50	150	-	100	150	nA
	Full	-	-	150	-	-	200	-	-	300	nA
Input Sensitivity (Note 4)	+25°C	-	-	V_{IO} + 0.3	-	-	V_{IO} + 0.5	-	-	V_{IO} + 0.5	mV
	Full	-	-	V_{IO} + 0.4	-	-	V_{IO} + 0.6	-	-	V_{IO} + 0.7	mV
Common Mode Range	Full	V-	-	(V+) - 2.4	V-	-	(V+) - 2.6	V-	-	(V+) - 2.4	V
Differential Input Resistance	+25°C	-	250	-	-	250	-	-	250	-	MΩ
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	+25°C	-	400	-	-	400	-	-	400	-	kV/V
Response Time ($T_{PD}0$) (Note 5)	+25°C	-	130	200	-	130	200	-	130	200	ns
Response Time ($T_{PD}1$) (Note 5)	+25°C	-	180	215	-	180	215	-	180	215	ns
OUTPUT CHARACTERISTICS											
Output Voltage Level											
Logic "Low State" (V_{OL}) (Note 6)	Full	-	0.2	0.4	-	0.2	0.4	-	0.2	0.4	V
Logic "High State" (V_{OH}) (Note 6)	Full	3.5	4.2	-	3.5	4.2	-	3.5	4.2	-	V
Output Current											
I_{SINK}	Full	3.0	-	-	3.0	-	-	3.0	-	-	mA
I_{SOURCE}	Full	3.0	-	-	3.0	-	-	3.0	-	-	mA

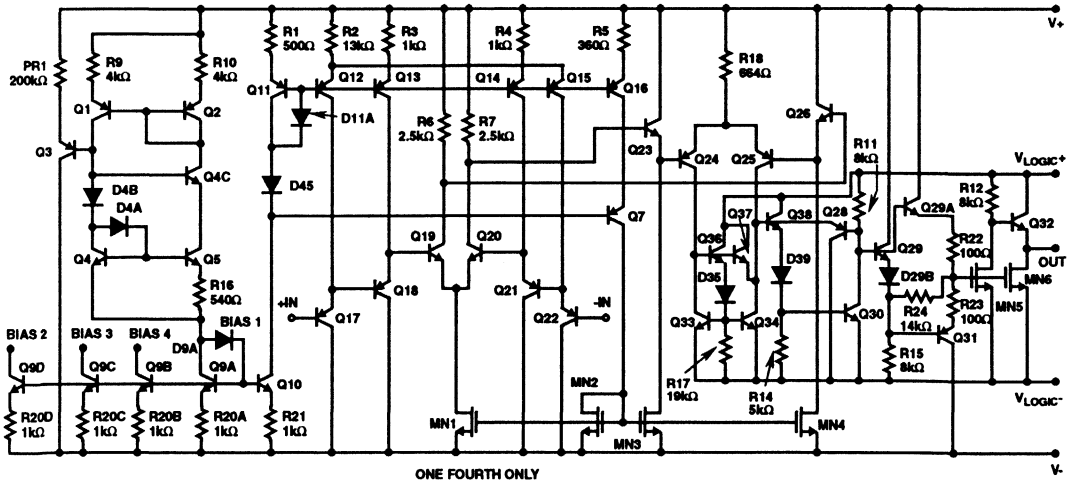
Electrical Specifications $V+ = +15V$, $V- = -15V$, $V_{LOGIC}+ = 5V$, $V_{LOGIC}- = GND$ **(Continued)**

PARAMETER	TEMP	HA-4900-2 -55°C to +125°C			HA-4902-2 -55°C to +125°C			HA-4905-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS											
Supply Current, I_{PS} (+)	+25°C	-	6.5	20	-	6.5	20	-	7	20	mA
Supply Current, I_{PS} (-)	+25°C	-	4	8	-	4	8	-	5	8	mA
Supply Current, I_{PS} (Logic)	+25°C	-	3.5	4	-	3.5	4	-	3.5	4	mA
Supply Voltage Range											
$V_{LOGIC}+$ (Note 8)	Full	0	-	+15.0	0	-	+15.0	0	-	+15.0	V
$V_{LOGIC}-$ (Note 8)	Full	-15.0	-	0	-15.0	-	0	-15.0	-	0	V

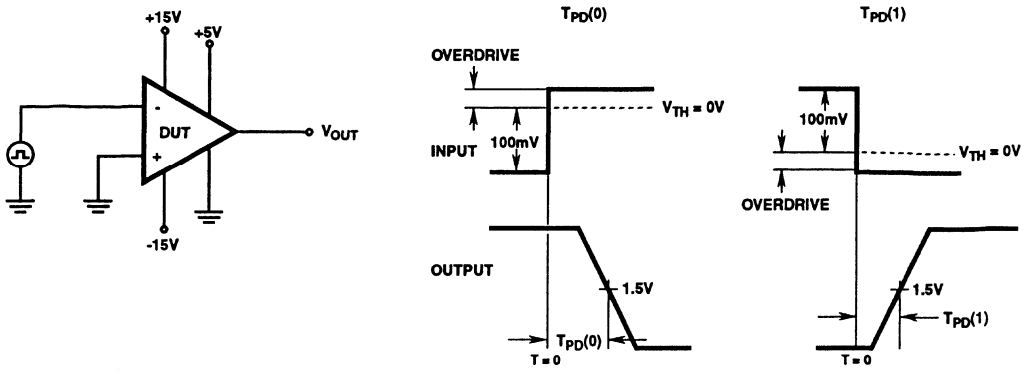
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Minimum differential input voltage required to ensure a defined output state.
3. Input bias currents are essentially constant with differential input voltages up to ±9V. With differential input voltages from ±9V to ±15V, bias current on the more negative input can rise to approximately 500µA. This will also cause higher supply currents.
4. $R_S \leq 200\Omega$ $V_{IN} \leq$ Common Mode Range. Input sensitivity is the worst case minimum differential input voltage required to guarantee a given output logic state. This parameter includes the effects of offset voltage, offset current, common mode rejection, and voltage gain.
5. For $T_{PD}(1)$; 100mV input step, -10mV overdrive. For $T_{PD}(0)$; -100mV input step, 10mV overdrive. Frequency ≈ 100Hz; Duty Cycle ≈ 50%; Inverting input driven. See Test Circuit on next page. All unused inverting inputs tied to +5V.
6. For V_{OH} and V_{OL}: $I_{SINK} = I_{SOURCE} = 3.0mA$. For other values of V_{LOGIC}; V_{OH} (min.) = $V_{LOGIC}+ -1.5V$.
7. Maximum power dissipation, including output load, must be designed to maintain the junction temperature below +175°C for ceramic packages, and below +150°C for plastic packages.
8. Total Power Dissipation (T.P.D.) is the sum of individual dissipation contributions of V+, V- and V_{LOGIC} shown in curves of Power Dissipation vs Supply Voltages (see Performance Curves). The calculated T.P.D. is then located on the graph of Maximum Allowable Package Dissipation vs Ambient Temperature to determine ambient temperature operating limits imposed by the calculated T.P.D. (See Performance Curves). For instance, the combination of +15V, -15V, +5V, 0V (V+, V-, $V_{LOGIC}+$, $V_{LOGIC}-$) gives a T.P.D. of 350mW, the combination +15V, -15V, +5V, 0V gives a T.P.D. of 450mW.

Schematic Diagram



Test Circuits



Typical Performance Curves T_A = +25°C, V_S = ±15V, V_{LOGIC}+ = 5V, V_{LOGIC}- = 0V, Unless Otherwise Specified

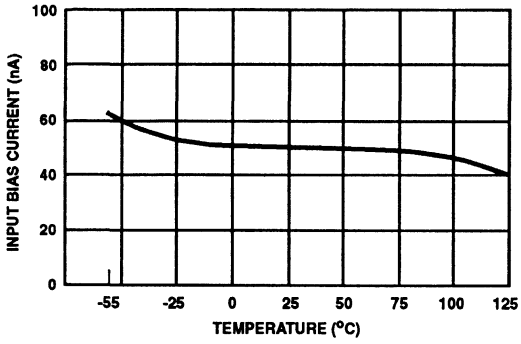


FIGURE 1. INPUT BIAS CURRENT vs TEMPERATURE

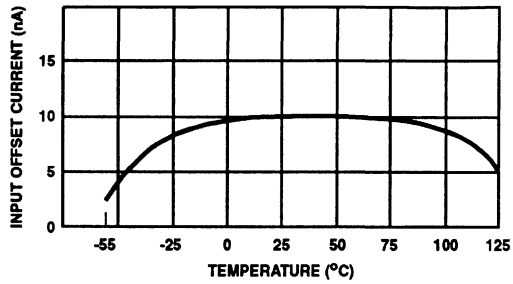


FIGURE 2. INPUT OFFSET CURRENT vs TEMPERATURE

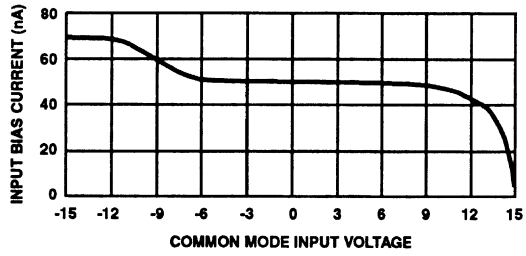


FIGURE 3. INPUT BIAS CURRENT vs COMMON MODE INPUT VOLTAGE (V_{DIFF} = 0V)

Typical Performance Curves T_A = +25°C, V_S = ±15V, V_{LOGIC}+ = 5V, V_{LOGIC}- = 0V, Unless Otherwise Specified (Continued)

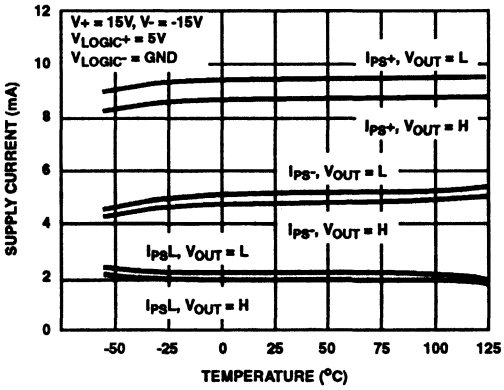


FIGURE 4. SUPPLY CURRENT vs TEMPERATURE (FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY)

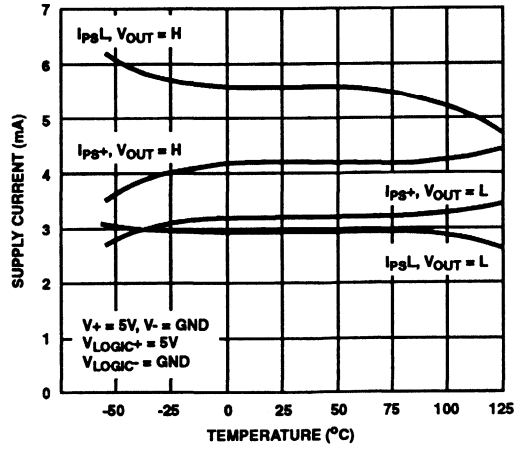


FIGURE 5. SUPPLY CURRENT vs TEMPERATURE (FOR SINGLE +5V OPERATION)

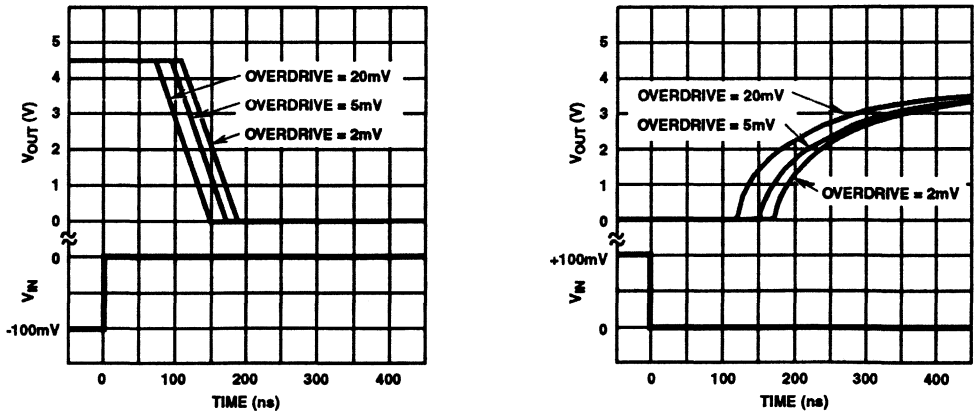


FIGURE 6. RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

Typical Performance Curves $T_A = +25°C$, $V_S = \pm15V$, $V_{LOGIC}+ = 5V$, $V_{LOGIC}- = 0V$, Unless Otherwise Specified (Continued)

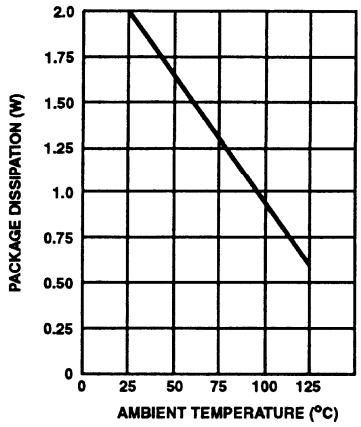


FIGURE 7. MAXIMUM PACKAGE DISSIPATION vs AMBIENT TEMPERATURE

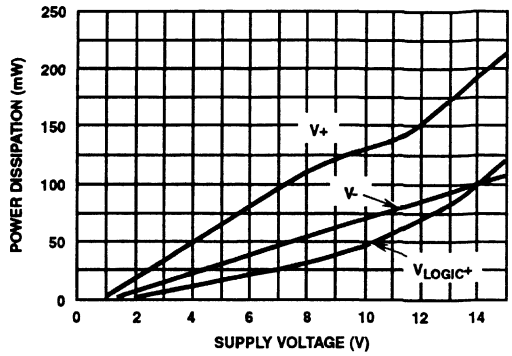


FIGURE 8. MAXIMUM POWER DISSIPATION vs SUPPLY VOLTAGE (NO LOAD CONDITION)

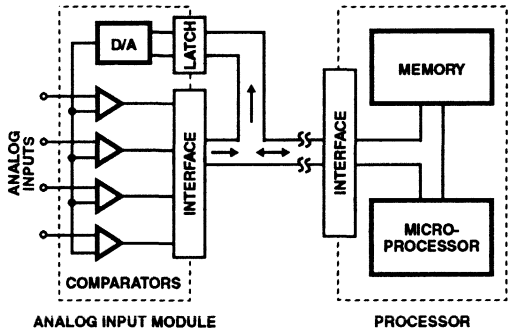
Applying the HA-4900 Series Comparators

1. SUPPLY CONNECTIONS: This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range; while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to $V_{LOGIC}+$ and $V_{LOGIC}-$. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings ($15V_{P-P}$, max.) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to 15V), V+ and $V_{LOGIC}+$ may be connected together to the positive supply while V- and $V_{LOGIC}-$ are grounded. If an input signal could swing negative with respect the V- terminal, a resistor should be connected in series with the input to limit input current to < 5mA since the C-B junction of the input transistor would be forward biased.
2. UNUSED INPUTS: Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter".
3. CROSSTALK: Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{OS}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.
4. POWER SUPPLY DECOUPLING: Decouple all power supply lines with 0.01µF ceramic capacitors to ground line located near the package to reduce coupling between channels or from external sources.
5. RESPONSE TIME: Fast rise time (< 200ns) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.

Typical Applications

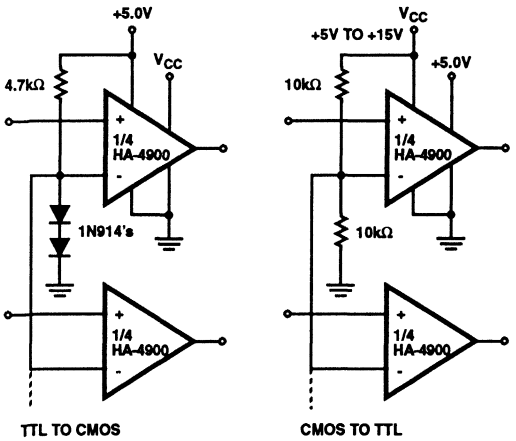
Data Acquisition System

In this circuit the HA-4900 series is used in conjunction with a D to A converter to form a simple, versatile, multi-channel analog input for a data acquisition system. In operation the processor first sends an address to the D to A, then the processor reads the digital word generated by the comparator outputs. To perform a simple comparision, the processor sets the D to A to a given reference level, then examines one or more comparator outputs to determine if their inputs are above or below the reference. A window comparison consists of two such cycles with 2 reference levels set by the D to A. One way to digitize the inputs would be for the processor to increment the D to A in steps. The D to A address, as each comparator switches, is the digitized level of the input. While stairstepping the D to A is slower than successive approximation, all channels are digitized during one staircase ramp.



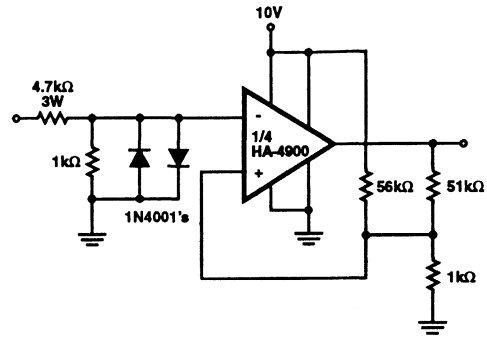
Logic Level Translators

The HA-4900 series comparators can be used as versatile logic interface devices as shown in the circuits above. Negative logic devices may also be interfaced with appropriate supply connections. If separate supplies are used for V- and V_{LOGIC}-, these logic level translators will tolerate several volts of ground line differential noise.



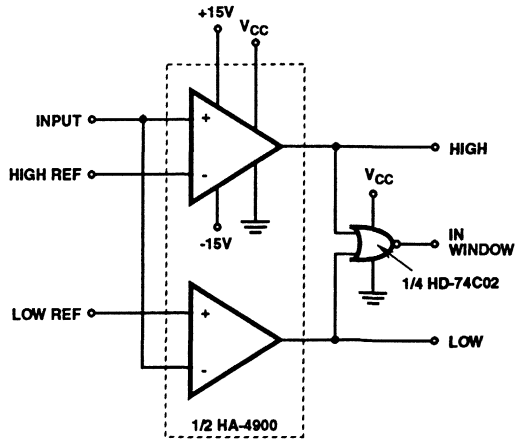
RS-232 To CMOS Line Receiver

This RS-232 type line receiver to drive CMOS logic uses a Schmitt trigger feedback network to give about 1V input hysteresis for added noise immunity. A possible problem in an interface which connects two equipments, each plugged into a different AC receptacle, is that the power line voltage may appear at the receiver input when the interface connection is made or broken. The two diodes and a 3W input resistor will protect the inputs under these conditions.



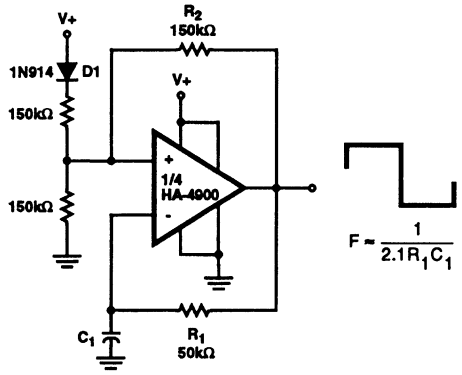
Window Detector

The high switching speed, low offset current and low offset voltage of the HA-4900 series makes this window detector circuit extremely well suited to applications requiring fast, accurate, decision-making. The circuit above is ideal for industrial process system feedback controllers or "out-of-limit" alarm indicators.



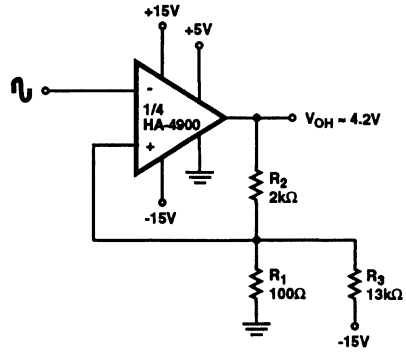
Oscillator/Clock Generator

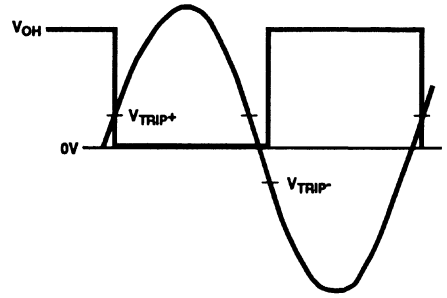
This self-starting fixed frequency oscillator circuit gives excellent frequency stability. R_1 and C_1 comprise the frequency determining network while R_2 provides the regenerative feedback. Diode D_1 enhances the stability by compensating for the difference between V_{OH} and V_{SUPPLY}. In applications where a precision clock generator up to 100kHz is required, such as in automatic test equipment, C_1 may be replaced by a crystal.



Schmitt Trigger (Zero Crossing Detector With Hysteresis)

This circuit has a 100mV hysteresis which can be used in applications where very fast transition times are required at the output even though the signal input is very slow. The hysteresis loop also reduces false triggering due to noise on the input. The waveforms below show the trip points developed by the hysteresis loop.





INPUT TO OUTPUT WAVEFORM SHOWING HYSTERESIS TRIP POINTS

HARRIS SEMICONDUCTOR

HFA-0003
HFA-0003L

PRELIMINARY

March 1993

Ultra High Speed Comparator

Features

- Low Propagation Delay (0003/0003L) 2.0/2.1ns
- Low Latch Set Up Time 0.8ns
- Low Offset Voltage, Drift Coefficient ..... 1.0mV, 4μV/°C
- Wide Common Mode Range ..... +5.2/-2.8V
- Low Power Dissipation 200mW
- Large Differential Input Resistance 1MΩ
- Complementary ECL Outputs; 50Ω Driving Capability
- Resistor Programmable Hysteresis with HFA-0003L
- Pin Compatible with MAX9690/9685 and AD96685
- Available in SOIC

Applications

- Window Detector
- High Speed Peak Detector
- High Speed Threshold Detector
- High Speed Data Acquisition Systems
- Fiber Optic Decision Circuits
- High Speed Phase Detector
- Frequency Counter

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1-0003L-5	0°C to +75°C	16 Lead Ceramic Sidebraze DIP
HFA1-0003L-9	-40°C to +85°C	16 Lead Ceramic Sidebraze DIP
HFA2-0003L-5	0°C to +75°C	10 Pin CAN
HFA2-0003L-9	-40°C to +85°C	10 Pin CAN
HFA3-0003-5	0°C to +75°C	8 Lead Plastic DIP
HFA3-0003-9	-40°C to +85°C	8 Lead Plastic DIP
HFA3-0003L-5	0°C to +75°C	16 Lead Plastic DIP
HFA3-0003L-9	-40°C to +85°C	16 Lead Plastic DIP
HFA7-0003-5	0°C to +75°C	8 Lead Ceramic Sidebraze DIP
HFA7-0003-9	-40°C to +85°C	8 Lead Ceramic Sidebraze DIP
HFA9P0003-5	0°C to +75°C	8 Lead SOIC
HFA9P0003L-5	0°C to +75°C	16 Lead Narrow Body SOIC
HFA9P0003L-9	-40°C to +85°C	16 Lead Narrow Body SOIC

Description

The HFA-0003/0003L are monolithic, ultra high speed, voltage comparators. These comparators combine a low input offset voltage (1.0mV) with a low propagation delay (2.0ns) to achieve a large dynamic input range. The low offset voltage also makes these comparators ideally suited for high speed, precision analog-to-digital processing applications. The circuits have differential analog inputs, and provide complementary, ECL compatible (10K and 100K) logic outputs. The outputs are capable of supplying the current required by terminated 50Ω transmission lines. Both outputs are open emitter structures, requiring external pull-down resistors. The recommended circuit is 50Ω connected to -2.0V, but any equivalent ECL termination circuit may be used.

The HFA-0003L is a latched version of the HFA-0003. The latch function allows the HFA-0003L to operate in sample-hold or track-hold modes, when synchronous detection is required. The Latch Enable (LE) input can be driven by a standard ECL gate. See the Applications section for more information on this feature.

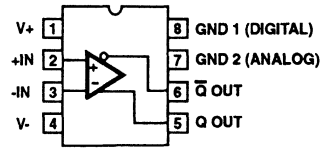
The HFA-0003L also has an additional feature, user programmable hysteresis. By connecting a resistor from the HYS pin to GND the user can select up to 20mV of input hysteresis. See the Applications section for more information on this feature.

The HFA-0003 is pin compatible with the MAX9690, and SP9680 while providing improved performance. The HFA-0003L is pin compatible with the MAX9685, AD96685, SP9685, HCMP96850, and the VC7695 while providing improved performance.

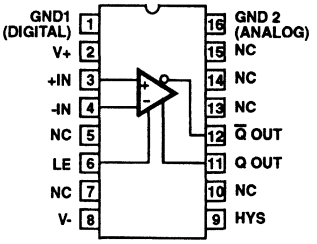
Refer to the /883 datasheets for military compliant product.

Pinouts

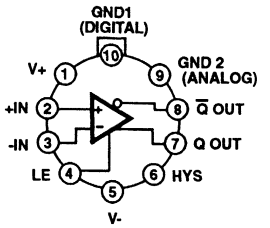
HFA-0003 (PDIP, CDIP, SOIC)
TOP VIEW



HFA-0003L (PDIP, CDIP, 150 mil SOIC)
TOP VIEW



HFA-0003L (TO-100 CAN)
TOP VIEW



3 COMPARATORS

File Number **2749.3**

Absolute Maximum Ratings (Note 1)

Supply Voltage (GND to V+) 8V
Supply Voltage (GND to V-) 18V
Voltage Between V+ and V- Terminals 20V
Differential Input Voltage 5.5V
Input Voltage ..... ±5V
Differential Ground Voltage (GND1 to GND2) ..... ±1V
Short Duration Output Current (Note 2) ..... -35mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HFA-0003/HFA-0003L-9 ..... $-40°C \le T_A \le +85°C$
HFA-0003/HFA-0003L-5 ..... $0°C \le T_A \le +75°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
8 Lead Ceramic Sidebrazed DIP	75	13
8 Lead Plastic DIP	96	34
8 Lead SOIC	157	43
16 Lead Ceramic Sidebrazed DIP	75	13
16 Lead Plastic DIP	92	32
16 Lead SOIC	114	35
TO-100 Metal CAN	108	32

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = 5V, V- = -5.2V, R_L = 50Ω to -2V, Unless Otherwise Specified

PARAMETER	TEMPERATURE	HFA-0003-5/-9			HFA-0003L-5/-9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Offset Voltage (V_{OS})	+25°C	-	1	3	-	1	3	mV
	Full	-	-	4	-	-	4	mV
Average Offset Voltage Drift (Note 8)	Full	-	-	4	-	-	4	µV/°C
Input Bias Current	+25°C	-	5	8	-	5	8	µA
	Full	-	8	13	-	8	13	µA
Input Offset Current	+25°C	-	0.15	0.2	-	0.15	0.2	µA
	Full	-	-	0.3	-	-	0.3	µA
Common Mode Range	Full	-2.8	-	+5.2	-2.8	-	+5.2	V
Differential Input Resistance	+25°C	-	1	-	-	1	-	MΩ
Common Mode Input Resistance	+25°C	-	9.5	-	-	9.5	-	MΩ
Input Capacitance	+25°C	-	1	-	-	1	-	pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain	+25°C	-	3100	-	-	3100	-	V/V
	Full	-	1200	-	-	1200	-	V/V
Common Mode Rejection Ratio (Note 3)	+25°C	70	75	-	70	75	-	dB
	Full	70	-	-	70	-	-	dB
Tracking Bandwidth (Note 4)	+25°C	-	270	-	-	270	-	MHz
SWITCHING CHARACTERISTICS								
Propagation Delay Input to Output (t_{PD})(Notes 5, 8, 9)	+25°C	-	2.0	2.4	-	2.1	2.6	ns
	Full	-	-	2.8	-	-	3.0	ns
Maximum Dispersion (Notes 6, 8)	Full	-	-	200	-	-	200	ps
OUTPUT CHARACTERISTICS								
Output Voltage Level:								
Logic Low (V_{OL})	+25°C	-	-1.83	-1.65	-	-1.83	-1.65	V
	Full	-	-1.83	-1.57	-	-1.83	-1.57	V
Logic High (V_{OH})	+25°C	-0.938	-0.85	-	-0.938	-0.85	-	V
	Full	-1.05	-0.96	-	-1.05	-0.96	-	V
Continuous Output Current (Note 2)	Full	-	-	-30	-	-	-30	mA

Electrical Specifications V+ = 5V, V- = -5.2V, R_L = 50Ω to -2V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMPERATURE	HFA-0003-5/-9			HFA-0003L-5/-9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
LATCH CHARACTERISTICS (HFA-0003L ONLY)								
LE Input Voltage Level:								
Logic Low (V_{IL})	Full	-	-	-	-	-	-1.475	V
Logic High (V_{IH})	Full	-	-	-	-1.105	-	-	V
LE Input Current Level:								
Logic Low (V_{IL} = -1.85V)	Full	-	-	-	-	0.06	0.5	µA
Logic High (V_{IH} = -0.81V)	Full	-	-	-	-	11	20	µA
Propagation Delay from LE to Output (t_{PDL}) (Notes 5, 8, 9)	+25°C	-	-	-	-	2.2	2.7	ns
	Full	-	-	-	-	2.6	3.1	ns
Minimum Set-Up Time (t_S) (Notes 8, 9)	+25°C	-	-	-	-	0.8	1.2	ns
	Full	-	-	-	-	-	1.5	ns
Minimum Hold Time (t_H) (Notes 8, 9)	Full	-	-	-	-	0.5	1.0	ns
Minimum LE Pulse Width (t_{PW}) (Notes 8, 9)	+25°C	-	-	-	-	0.9	0.95	ns
	Full	-	-	-	-	-	1.1	ns
POWER SUPPLY								
PSRR (Note 7)	+25°C	70	80	-	70	80	-	dB
	Full	65	-	-	65	-	-	dB
I_{CC}	Full	-	11	13	-	11	13	mA
I_{EE}	Full	-	19	22	-	19	22	mA
Power Dissipation	Full	-	-	200	-	-	200	mW

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the servicability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. Outputs have no sink current (+I) capability, since they are open emitter NPN transistors.
3. -2.0V ≤ V_{CM} ≤ +4.0V.
4. Tracking Bandwidth (TBW) is defined as the maximum input frequency at which the outputs still switch between V_{OL} and V_{OH}. V_{IN} = 15mVp-p sinewave centered on 0V.
5. V_{IN} = 100mV. V_{OD} is the amount of input overdrive.
6. Dispersion is defined as the change in propagation delay for input overdrives between 0.1V and 1.0V.
7. +4.5V ≤ V+ ≤ +5.5V or -6.2V ≤ V- ≤ -4.7V.
8. This parameter is not tested. It is guaranteed by design, and by device characterization.
9. V_{OD} = 10mV.

Applications Information

HFA-0003L Latch Functionality

The Latch Enable (LE) pin of the HFA-0003L controls the function of the on chip latch. When the LE input is at an ECL Logic 1, the latch is open (transparent) and the comparator functions normally. When the LE input switches to a Logic 0, the outputs are latched in unambiguous states dependant on the current input state, providing the set-up and hold times are met. If the latch function is not utilized, the LE input must be connected to an ECL Logic 1 (e.g. GND).

HFA-0003L Hysteresis Functionality

To improve performance in systems with slow transition times, and/or high noise levels, the HFA-0003L allows the user to easily set the amount of input hysteresis. The hysteresis level is set by the current flowing into the HYS input; the larger the current the larger the level of hysteresis. This current is provided by connecting a resistor (R_H) between the HYS pin and GND, and it is recommended that the input current not exceed 1mA. The input current can be approximated from the following formula:

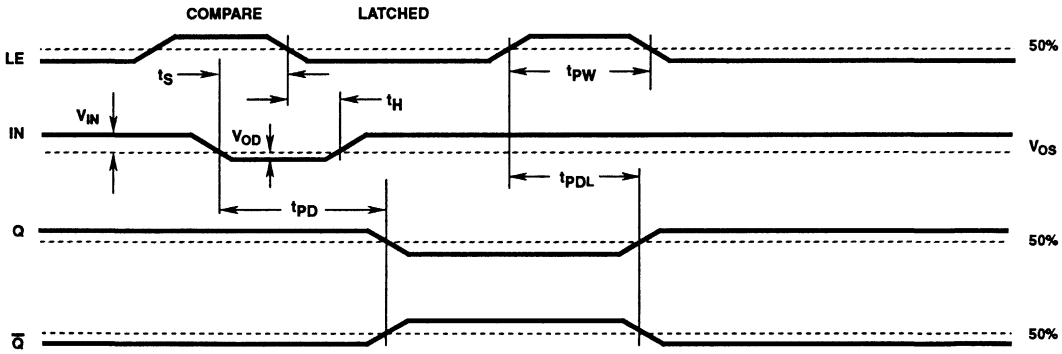
$$I_H = \frac{GND - (V-) - 0.7V}{R_H}$$

The table below gives approximate levels of hysteresis for some values of I_H, at $T_A = +25^oC$.

I_H (mA)	0.2	0.4	0.6	0.8	1.0
HYS (mV)	1	4	8	13	22

If the hysteresis function isn't used, the HYS input may be left floating, or may be connected to V-. The HYS input MUST NEVER BE CONNECTED directly to GND or V+, as device damage will occur. Before inserting an HFA-0003L into a competitor socket, the user must ensure that the corresponding socket pin is a true no connect (i.e. is floating).

Timing Diagram



LINEAR 4

SAMPLE AND HOLD AMPLIFIERS

NOTE: Bold Type Designates a New Product from Harris.

Selection Guide

SAMPLE AND HOLD AMPLIFIERS: Typical Values at +25°C, Unless Otherwise Specified.

TYPE	SAMPLE/HOLD TYPE	TEMPERATURE RANGE	PACKAGE*	ACQUISITION TIME (TO 0.01%)	HOLD STEP ERROR	APERTURE TIME	GAIN BANDWIDTH PRODUCT
HA1-2420-2	Low Droop Rate	-55°C to +125°C	14 Lead Ceramic DIP	3.2µs (C_H = 1,000pF)	10mV	30ns	2.5MHz
HA1-2420/883		-55°C to +125°C	14 Lead Ceramic DIP				
HA1-2425-5		0°C to +75°C	14 Lead Ceramic DIP				
HA3-2425-5		0°C to +75°C	14 Lead Plastic DIP				
HA4-2420/883		-55°C to +125°C	20 Lead LCC Ceramic				
HA4P2425-5		0°C to +75°C	20 Lead PLCC				
HA9P2425-5		0°C to +75°C	14 Lead SOIC				
HA1-5320-2	High Speed, Low Charge, Transfer Precision, Complete - Includes Hold Capacitor	-55°C to +125°C	14 Lead Ceramic DIP	1µs (C_H = Internal)	1mV	25ns	2.0MHz (C_H = 100pF)
HA1-5320-5		0°C to +75°C	14 Lead Ceramic DIP				
HA1-5320/883		-55°C to +125°C	14 Lead Ceramic DIP				
HA3-5320-5		0°C to +75°C	14 Lead Plastic DIP				
HA4-5320/883		-55°C to +125°C	20 Lead LCC Ceramic				
HA9P5320-5		0°C to +75°C	16 Lead 300 mil SOIC				
HA9P5320-9		-40°C to +85°C	16 Lead 300 mil SOIC				
HA1-5330-5	Very High Speed, Precision, Monolithic, Complete Includes Hold Capacitor	0°C to +75°C	14 Lead Ceramic DIP	650ns	0.5mV	20ns	4.5MHz
HA1-5330-4		-25°C to +85°C	14 Lead Ceramic DIP				
HA1-5330-2		-55°C to +125°C	14 Lead Ceramic DIP				
HA1-5330/883		-55°C to +125°C	14 Lead Ceramic DIP				
HA3-5330-5		0°C to +75°C	14 Lead Plastic DIP				
HA4-5330/883		-55°C to +125°C	20 Lead LCC Ceramic				
HA1-5340-5	High Speed, Low Distortion - Includes Hold Capacitor	0°C to +75°C	14 Lead Ceramic DIP	700ns	15mV	15ns	10MHz
HA1-5340-9		-40°C to +85°C	14 Lead Ceramic DIP				
HA1-5340/883		-55°C to +125°C	14 Lead Ceramic DIP				
HA3-5340-5		0°C to +75°C	14 Lead Plastic DIP				
HA3-5340-9		-40°C to +85°C	14 Lead Plastic DIP				
HA4-5340/883		-55°C to +125°C	20 Lead LCC Ceramic				
HA9P5340-5		0°C to +75°C	16 Lead 300 mil SOIC				
HA5350IP	Ultra High Speed and Low Power Includes Hold Capacitor, Full Featured	-40°C to +85°C	14 Lead Plastic DIP	85ns	1.25mV	±10ns	20MHz
HA5350IJ		-40°C to +85°C	14 Lead Ceramic DIP				
HA5350IB		-40°C to +85°C	14 Lead SOIC				
HA5351IP	Ultra High Speed and Low Power, Includes Hold Capacitor, Low Pin Count	-40°C to +85°C	8 Lead Plastic DIP	85ns	1.25mV	±10ns	20MHz
HA5351IJ		-40°C to +85°C	8 Lead Ceramic DIP				
HA5351IB		-40°C to +85°C	8 Lead SOIC				
HA5352IP	Dual, Ultra High Speed and Low Power, Includes Hold Capacitor	-40°C to +85°C	14 Lead Plastic DIP	85ns	1.25mV	±10ns	20MHz
HA5352IJ		-40°C to +85°C	14 Lead Ceramic DIP				
HA5352IB		-40°C to +85°C	16 Lead 300 mil SOIC				

* See Packaging Information in Section 11.

HA-2420, HA-2425

March 1993

Fast Sample and Hold Amplifiers

Features

- Maximum Acquisition Time
  - 10V Step to 0.1%..... 4µs
  - 10V Step to 0.01%..... 6µs
- Low Droop Rate (C_H = 1000pF)..... 5µV/ms (Typ)
- Gain Bandwidth Product ..... 2.5MHz (Typ)
- Low Effective Aperture Delay Time ..... 30ns (Typ)
- TTL Compatible Control Input
- ±12V to ±15V Operation

Applications

- 12 Bit Data Acquisition
- Digital to Analog Deglitcher
- Auto Zero Systems
- Peak Detector
- Gated Operational Amplifier

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-2420-2	-55°C to +125°C	14 Lead Ceramic DIP
HA1-2425-5	0°C to +75°C	14 Lead Ceramic DIP
HA3-2425-5	0°C to +75°C	14 Lead Plastic DIP
HA4P2425-5	0°C to +75°C	20 Lead PLCC
HA9P2425-5	0°C to +75°C	14 Lead SOIC

Description

The HA-2420 and HA-2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and JFET input unity gain amplifier.

With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

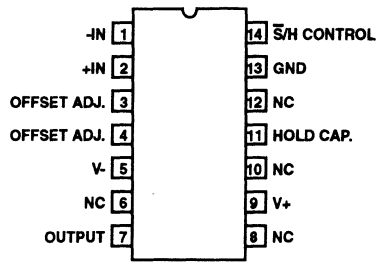
Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc. For more information, please see Application Note 517.

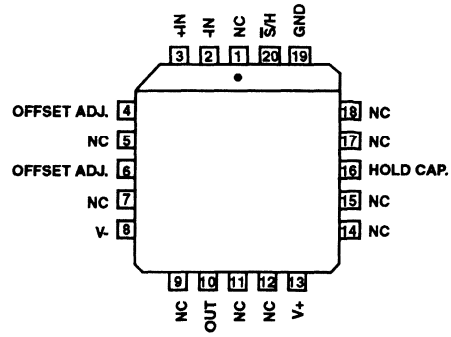
The MIL-STD-883 data sheet for this device is available on request.

Pinouts

HA-2420 (CDIP)
HA-2425 (CDIP, PDIP, AND SOIC)
TOP VIEW



HA-2425
(PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2856.1**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 24V
Digital Input Voltage (Sample and Hold Pin) ..... +8V, -15V
Output Current ..... Short Circuit Protected
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-2420-2 ..... $-55°C \le T_A \le +125°C$
HA-2425-5 ..... $0°C \le T_A \le +75°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$
Supply Voltage Range (TYP) ..... ±12V to ±15V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications Test Conditions (Unless Otherwise Specified) V_{SUPPLY} = 15.0V ; C_H = 1000pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold), Unity Gain Configuration (Output tied to Negative Input)

PARAMETER	TEMPERATURE	HA-2420-2			HA-2425-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10	-	-	±10	-	-	V
Offset Voltage	+25°C	-	2	4	-	3	6	mV
	Full	-	3	6	-	4	8	mV
Bias Current	+25°C	-	40	200	-	40	200	nA
	Full	-	-	400	-	-	400	nA
Offset Current	+25°C	-	10	50	-	10	50	nA
	Full	-	-	100	-	-	100	nA
Input Resistance	+25°C	5	10	-	5	10	-	MΩ
Common Mode Range	Full	±10	-	-	±10	-	-	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 1, 4)	Full	25	50	-	25	50	-	kV/V
Common Mode Rejection (Note 2)	Full	80	90	-	74	90	-	dB
Hold Mode Feedthrough Attenuation (Note 3)	Full	-	-76	-	-	-76	-	dB
Gain Bandwidth Product (Note 3)	+25°C	-	2.5	-	-	2.5	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10	-	-	±10	-	-	V
Output Current	+25°C	±15	-	-	±15	-	-	mA
Full Power Bandwidth (Notes 3, 4)	+25°C	-	100	-	-	100	-	kHz
Output Resistance (D.C.)	+25°C	-	0.15	-	-	0.15	-	Ω
TRANSIENT RESPONSE								
Rise Time (Notes 3, 5)	+25°C	-	75	100	-	75	100	ns
Overshoot (Notes 3, 5)	+25°C	-	25	40	-	25	40	%
Slew Rate (Notes 3, 6)	+25°C	3.5	5	-	3.5	5	-	V/µs
DIGITAL INPUT CHARACTERISTICS								
Digital Input Current (V_{IN} = 0V)	Full	-	-	-0.8	-	-	-0.8	mA
Digital Input Current (V_{IN} = +5.0V)	Full	-	-	20	-	-	20	µA
Digital Input Voltage (Low)	Full	-	-	0.8	-	-	0.8	V
Digital Input Voltage (High)	Full	2.0	-	-	2.0	-	-	V

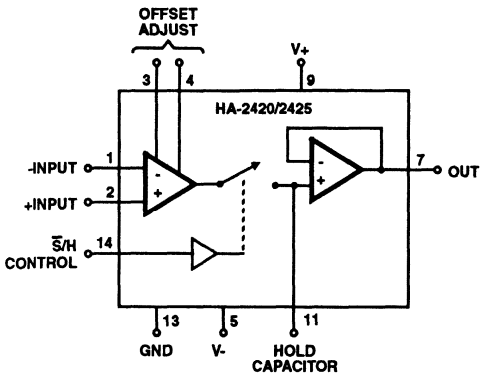
Electrical Specifications Test Conditions (Unless Otherwise Specified) V_{SUPPLY} = 15.0V ; C_H = 1000pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold), Unity Gain Configuration (Output tied to Negative Input) **(Continued)**

PARAMETER	TEMPERATURE	HA-2420-2			HA-2425-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SAMPLE AND HOLD CHARACTERISTICS								
Acquisition Time to 0.1% 10V Step (Note 3)	+25°C	-	2.3	4	-	2.3	4	µs
Acquisition Time to 0.01% 10V Step (Note 3)	+25°C	-	3.2	6	-	3.2	6	µs
Hold Step Error (Note 7)	+25°C	-	10	20	-	10	20	mV
Hold Mode Settling Time	+25°C	-	860	-	-	860	-	ns
Aperture Time (Note 9)	+25°C	-	30	-	-	30	-	ns
Effective Aperture Delay Time	+25°C	-	30	-	-	30	-	ns
Aperture Uncertainty	+25°C	-	5	-	-	5	-	ns
Drift Current (Notes 3, 7)	+25°C	-	5	-	-	5	-	pA
HA1-2420	Full	-	1.8	10	-	-	-	nA
HA1-2425	Full	-	-	-	-	0.1	1.0	nA
HA3-2425, HA4P2425	Full	-	-	-	-	7.5	10.0	nA
POWER SUPPLY CHARACTERISTICS								
Supply Current (+)	+25°C	-	3.5	5.5	-	3.5	5.5	mA
Supply Current (-)	+25°C	-	2.5	3.5	-	2.5	3.5	mA
Power Supply Rejection	Full	80	90	-	74	90	-	dB

NOTES:

1. R_L = 2kΩ
2. V_{CM} = ±10V_{DC}.
3. A_V = ±1, R_L = 2kΩ, C_L = 50pF.
4. V_{OUT} = 20V peak-to-peak.
5. V_{OUT} = 200mV peak-to-peak.
6. V_{OUT} = 10.0V peak-to-peak.
7. V_{IN} = 0V.
8. f_{IN} ≤ 100kHz.
9. Derived from computer simulation only; not tested.

Functional Diagram

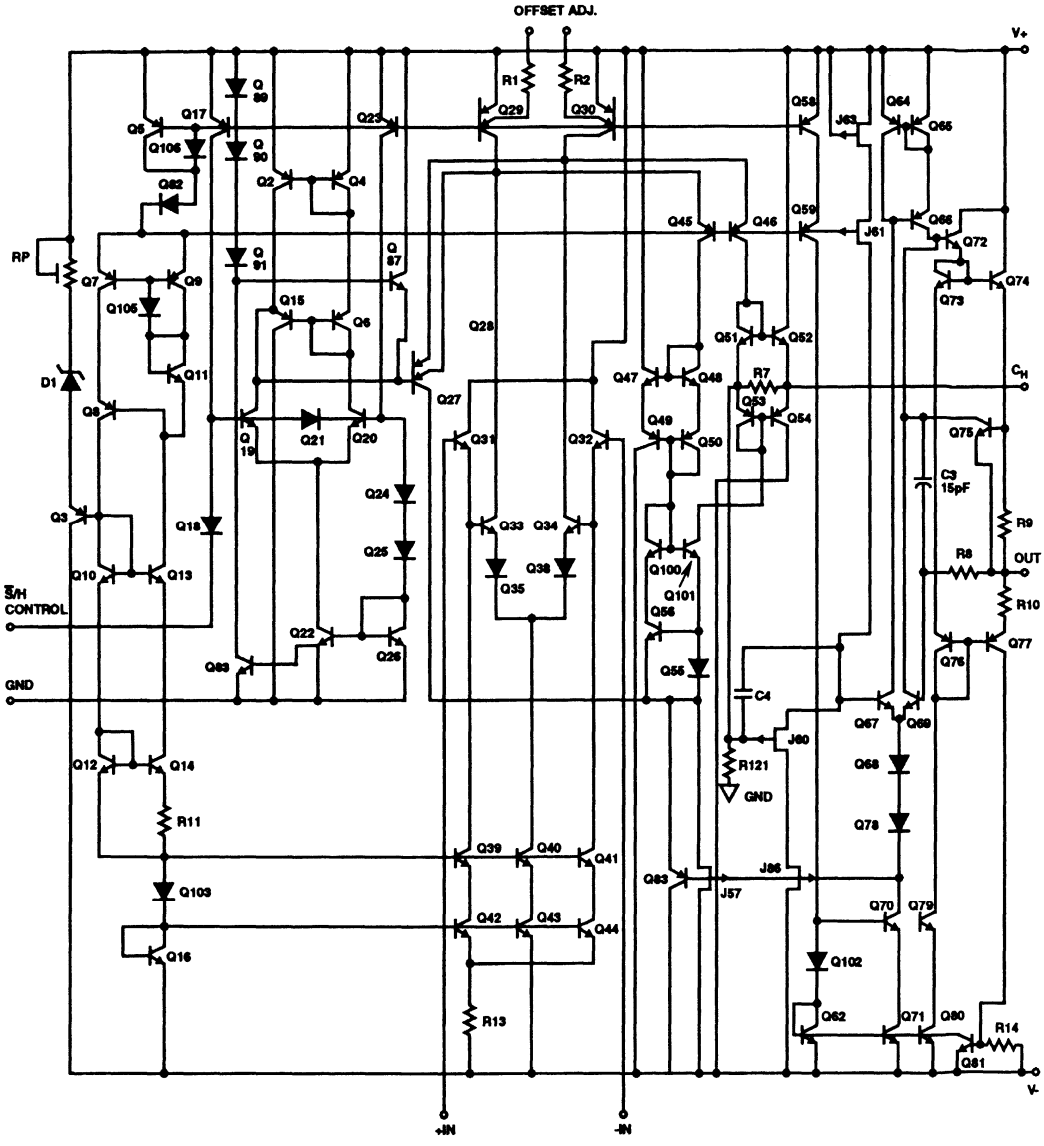


Die Characteristics

Transistor Count 85
Die Dimensions ..... 102 x 61 x 19 mils
Substrate Potential ..... $-V_{SUPPLY}$
Process ..... Bipolar DI

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	71	13
Plastic DIP	85	23
PLCC	74	33
SOIC	95	26

Schematic Diagram



Test Circuits

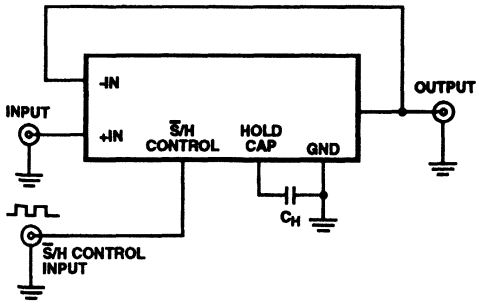
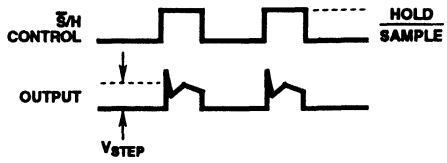
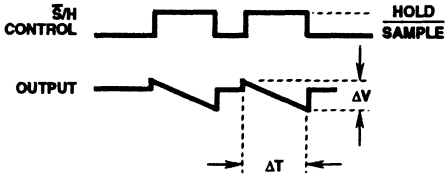


FIGURE 1. HOLD STEP ERROR AND DRIFT CURRENT



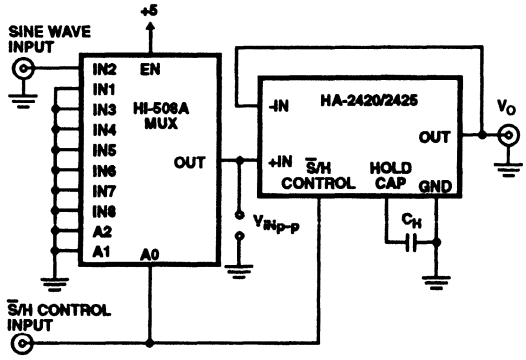
NOTE: Set rise/fall times of S/H Control to approximately 20ns.

FIGURE 2. HOLD STEP ERROR TEST



NOTE: Measure the slope of the output during hold, $\Delta V/\Delta t$, and compute drift current from : $I_D = C_H \Delta V/\Delta t$.

FIGURE 3. DRIFT CURRENT TEST



NOTE: Compute hold mode feedthrough attenuation from the formula:

$$\text{Feedthrough Attenuation} = 20\log\frac{V_{OUT}HOLD}{V_{IN}HOLD}$$

Where $V_{OUT}HOLD$ = Peak-to-Peak value of output sinewave during the hold mode.

FIGURE 4. HOLD MODE FEEDTHROUGH ATTENUATION

Typical Performance Curves

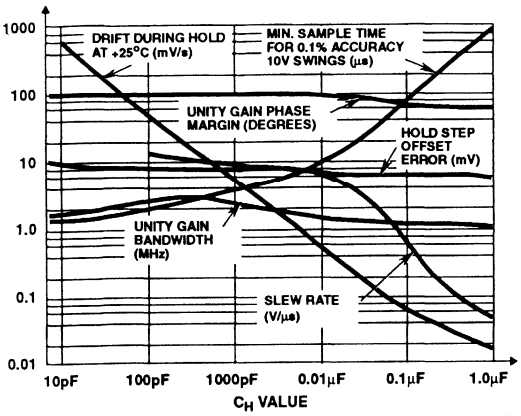


FIGURE 5. TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITOR

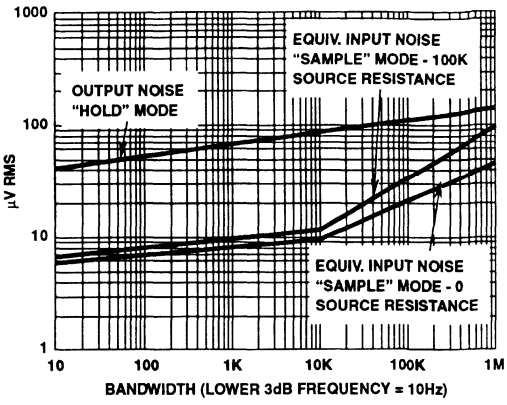


FIGURE 6. BROADBAND NOISE CHARACTERISTICS

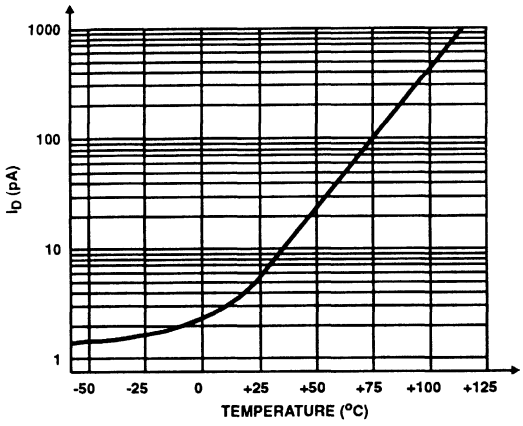


FIGURE 7. DRIFT CURRENT vs TEMPERATURE

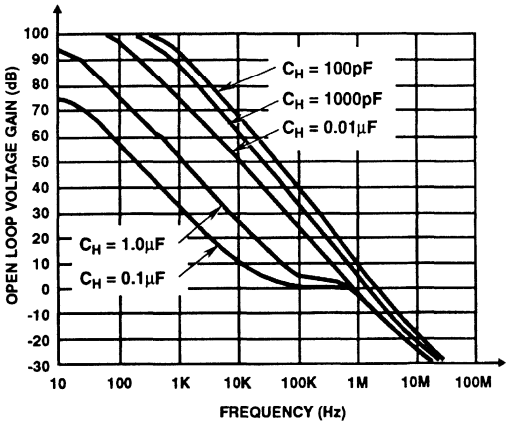


FIGURE 8. OPEN LOOP FREQUENCY RESPONSE

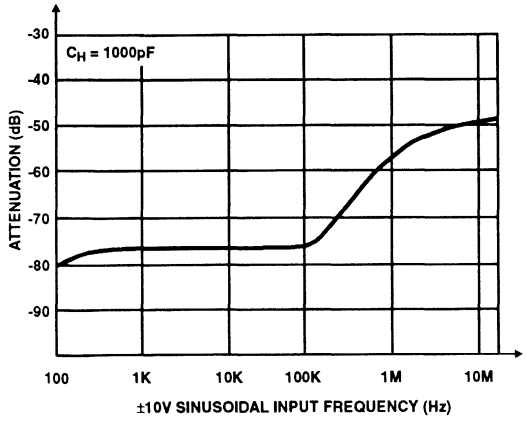


FIGURE 9. HOLD MODE FEED THROUGH ATTENUATION

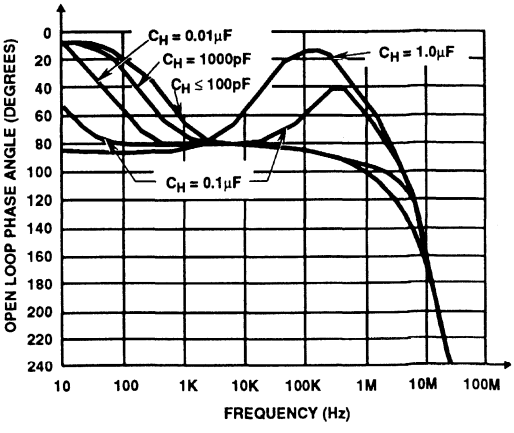


FIGURE 10. OPEN LOOP PHASE RESPONSE

Offset and Gain Adjustment

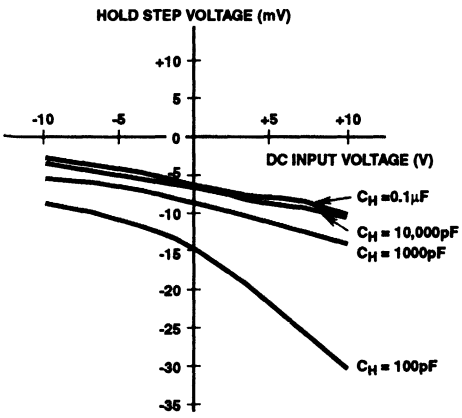


FIGURE 11. HOLD STEP vs INPUT VOLTAGE

Offset Adjustment

The offset voltage of the HA-2420and HA-2425 may be adjusted using a 100kΩ trim pot, as shown in Figure 20. The recommended adjustment procedure is:

Apply zero volts to the sample-and-hold input, and a square wave to the $\overline{S}$/H control.

Adjust the trim pot for zero volts output in the hold mode.

Gain Adjustment

The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.06% gain error (C_H = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage ($V_{-10NOMINAL}$). Adjust the trim pot for an output hold voltage of

$$\frac{(V_{-10NOMINAL}) + (-10V)}{2}$$

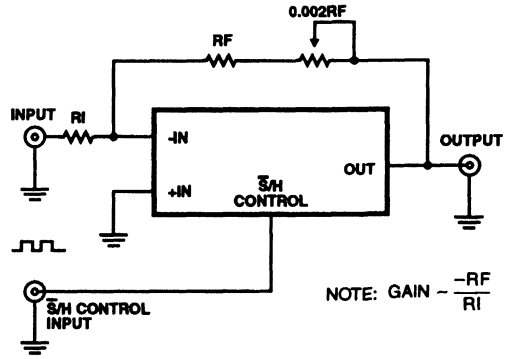


FIGURE 12. INVERTING CONFIGURATION

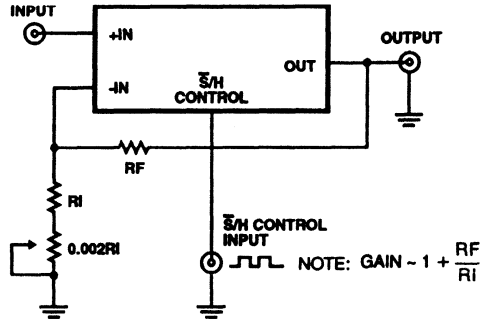


FIGURE 13. NON-INVERTING CONFIGURATION

Acquisition Times (C_H = 1000pF)

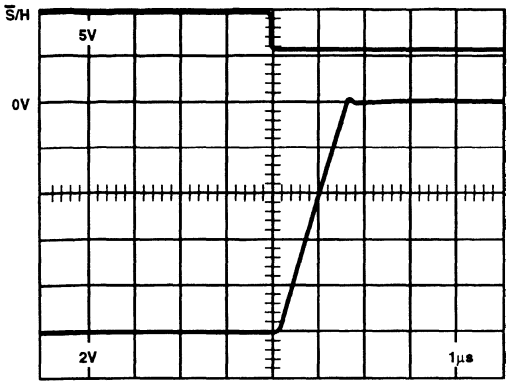


FIGURE 14. -10V TO 0V

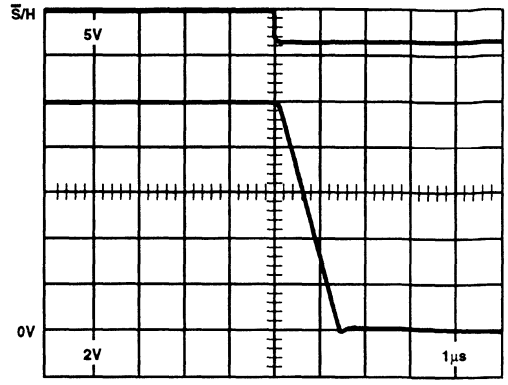


FIGURE 15. +10V TO 0V

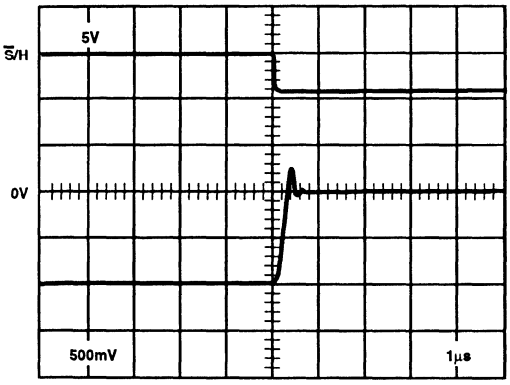


FIGURE 16. -1V TO 0V

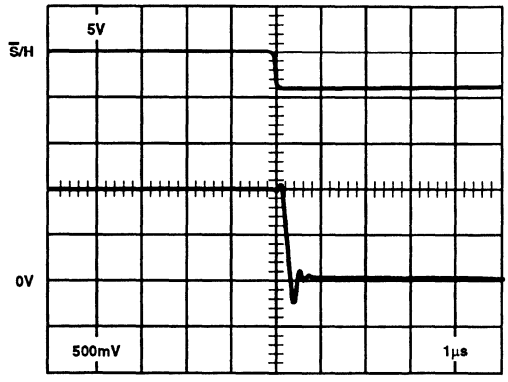


FIGURE 17. +1V TO 0V

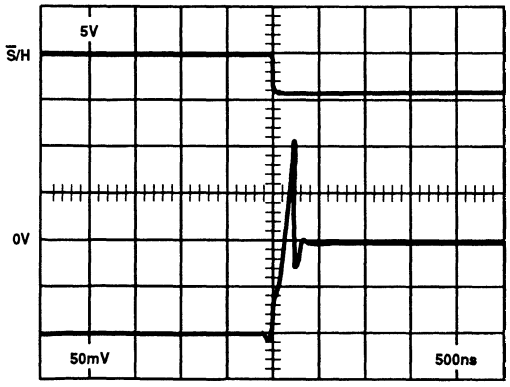


FIGURE 18. -100mV TO 0V

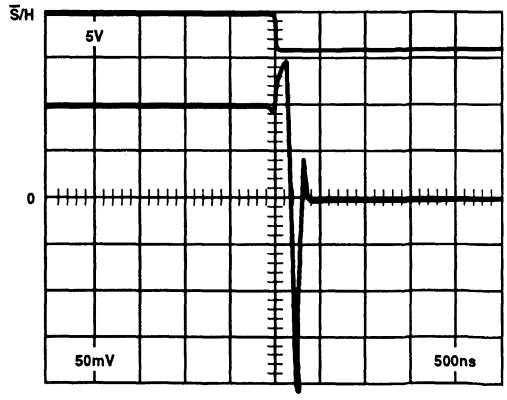


FIGURE 19. +100mV TO 0V

Applications

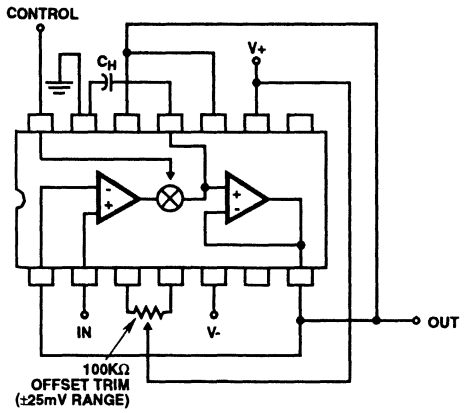


FIGURE 20. BASIC SAMPLE-AND-HOLD (TOP VIEW)

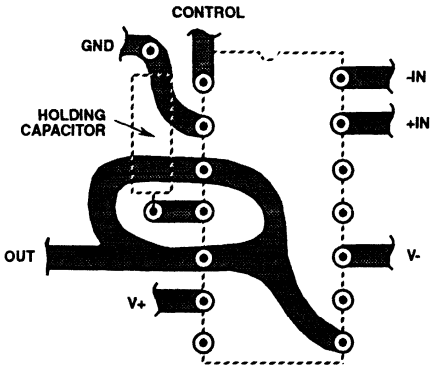


FIGURE 21. GUARD RING LAYOUT (BOTTOM VIEW)

NOTES:

1. Figure 20 shows a typical unity gain circuit, with Offset Zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420/2425. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.
2. The method used to reduce leakage paths on the P.C. board and the device package is shown in Figure 21. This guard ring is recommended to minimize the drift during hold mode.
3. The holding capacitor should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), Teflon, or Parlene types are recommended.

For more applications, consult Harris Application Note 517, or factory applications group.

Glossary of Terms

Acquisition Time

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Aperture Time

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Effective Aperture Delay Time (EADT)

The difference between the digital delay time from the Hold command to the opening of the S/H switch, and the propagation time from the analog input to the switch.

EADT may be positive, negative or zero. If zero, the $\overline{S}/H$ amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

Drift Current

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D\,(pA) = C_H\,(pF) \times \frac{\Delta V}{\Delta T}\,(V/s)$$

HARRIS SEMICONDUCTOR

HA-5320

High Speed Precision Monolithic Sample and Hold Amplifier

March 1993

Features

- Gain, DC ..... 2×10^6 V/V
- Aquisition Time 1.0µs (0.01%)
- Droop Rate ..... 0.08µV/µs (+25°C)
  17µV/µs (Full Temperature)
- Aperture Time 25ns
- Hold Step Error (See Glossary) 1.0mV
- Internal Hold Capacitor
- Fully Differential Input
- TTL Compatible

Applications

- Precision Data Acquisition Systems
- Digital to Analog Converter Deglitcher
- Auto Zero Circuits
- Peak Detector

Description

The HA-5320 was designed for use in precision, high speed data acquisition systems.

The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is required at the expense of acquisition time, additional hold capacitance may be added externally.

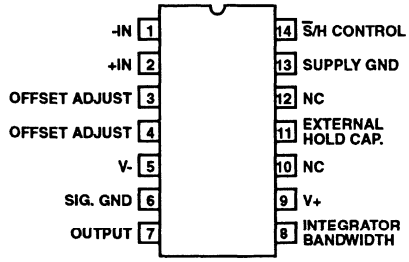
This monolithic device is manufactured using the Harris Dielectric Isolation Process, minimizing stray capacitance and eliminating SCR's. This allows higher speed and latch-free operation. For further information, please see Application Note 538. The Mil-Std-883 data sheet for this device is available on request.

Ordering Information

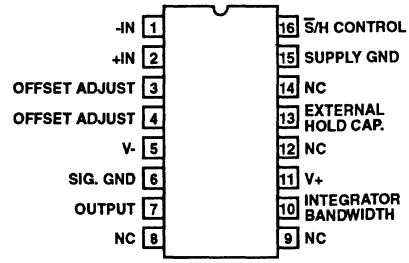
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-5320-2	-55°C to +125°C	14 Lead Ceramic DIP
HA1-5320-5	0°C to +75°C	14 Lead Ceramic DIP
HA3-5320-5	0°C to +75°C	14 Lead Plastic DIP
HA9P5320-5	0°C to +75°C	16 Lead Wide Body SOIC
HA9P5320-9	-40°C to +85°C	16 Lead Wide Body SOIC

Pinouts

HA-5320
(PDIP, CDIP)
TOP VIEW



HA-5320
(300 mil SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2857.1**

Absolute Maximum Ratings (Note 1)

Supply Voltage 40V
Differential Input Voltage 24V
Digital Input Voltage ..... +8V, -15V
Output Current, Continuous (Note 2) ..... ±20mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-5320-2 ..... $-55°C \le T_A \le +125°C$
HA-5320-5 ..... $0°C \le T_A \le +75°C$
HA-5320-9 ..... $-40°C \le T_A \le +85°C$
Recommended Supply Voltage Range (Note 13) ... ±13.5V to ±20V
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{SUPPLY} = ±15.0V; C_H = Internal; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold), Unity Gain Configuration (Output tied to -Input), Unless Otherwise Specified

PARAMETER	TEMPERATURE	HA-5320-2/-9			HA-5320-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10	-	-	±10	-	-	V
Input Resistance	+25°C	1	5	-	1	5	-	MΩ
Input Capacitance	+25°C	-	-	3	-	-	3	pF
Offset Voltage	+25°C	-	0.2	-	-	0.5	-	mV
	Full	-	-	2.0	-	-	1.5	mV
Bias Current	+25°C	-	70	200	-	100	300	nA
	Full	-	-	200	-	-	300	nA
Offset Current	+25°C	-	30	100	-	30	300	nA
	Full	-	-	100	-	-	300	nA
Common Mode Range	Full	±10	-	-	±10	-	-	V
CMRR (Note 3)	+25°C	80	90	-	72	90	-	dB
Offset Voltage T.C.	Full	-	5	15	-	5	20	µV/°C
TRANSFER CHARACTERISTICS								
Gain, D.C. (Note 12)	+25°C	10^6	2×10^6	-	3×10^5	2×10^6	-	V/V
Gain Bandwidth Product (A_V = +1) (Note 5)	+25°C							
C_H = 100pF	-	-	2.0	-	-	2.0	-	MHz
C_H = 1000pF	-	-	0.18	-	-	0.18	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage	Full	±10	-	-	±10	-	-	V
Output Current	+25°C	±10	-	-	±10	-	-	mA
Full Power Bandwidth (Note 4)	+25°C	-	600	-	-	600	-	kHz
Output Resistance (Hold Mode)	+25°C	-	1.0	-	-	1.0	-	Ω
Total Output Noise, D.C. to 10MHz								
Sample	+25°C	-	125	200	-	125	200	μV_{RMS}
Hold	+25°C	-	125	200	-	125	200	μV_{RMS}
TRANSIENT RESPONSE								
Rise Time (Note 5)	+25°C	-	100	-	-	100	-	ns
Overshoot (Note 5)	+25°C	-	15	-	-	15	-	%
Slew Rate (Note 6)	+25°C	-	45	-	-	45	-	V/µs

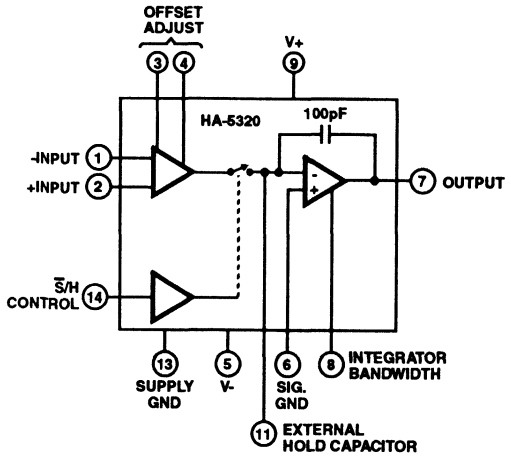
Electrical Specifications V_{SUPPLY} = ±15.0V; C_H = Internal; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold), Unity Gain Configuration (Output tied to -Input), Unless Otherwise Specified **(Continued)**

PARAMETER	TEMPERATURE	HA-5320-2/-9			HA-5320-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{IH}	Full	2.0	-	-	2.0	-	-	V
Input Voltage (Low), V_{IL}	Full	-	-	0.8	-	-	0.8	V
Input Current (V_{IL} = 0V)	+25°C	-	-	4	-	-	4	µA
	Full	-	-	10	-	-	10	µA
Input Current (V_{IH} = +5V)	Full	-	-	0.1	-	-	0.1	µA
SAMPLE AND HOLD CHARACTERISTICS								
Acquisition Time to 0.1% (Note 7)	+25°C	-	0.8	1.2	-	0.8	1.2	µs
Acquisition Time to 0.01% (Note 7)	+25°C	-	1.0	1.5	-	1.0	1.5	µs
Aperture Time (Note 8)	+25°C	-	25	-	-	25	-	ns
Effective Aperture Delay Time (See Glossary)	+25°C	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty	+25°C	-	0.3	-	-	0.3	-	ns
Droop Rate	+25°C	-	0.08	0.5	-	0.08	0.5	µV/µs
	Full	-	17	100	-	1.2	100	µV/µs
Drift Current (Note 9)	+25°C	-	8	50	-	8	50	pA
	Full	-	1.7	10	-	0.12	10	nA
Charge Transfer (Note 9)	+25°C	-	0.1	0.5	-	0.1	0.5	pC
Hold Step Error (Note 9)	+25°C	-	1	5	-	1	5	mV
Hold Mode Settling Time 0.01%	Full	-	165	350	-	165	350	ns
Hold Mode Feedthrough ($10V_{P-P}$, 100kHz)	Full	-	2	-	-	2	-	mV
POWER SUPPLY CHARACTERISTICS								
Positive Supply Current (Note 10)	+25°C	-	11	13	-	11	13	mA
Negative Supply Current (Note 10)	+25°C	-	-11	-13	-	-11	-13	mA
Supply Voltage Range (Note 13)		±13.5	–	±20	±13.5	-	±20	V
Power Supply Rejection (Note 11)								
V+	Full	80	-	-	80	-	-	dB
V-	Full	65	-	-	65	-	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Internal Power Dissipation may limit Output Current below 20mA.
3. V_{CM} = ±5VDC.
4. V_O = $20V_{P-P}$; R_L = 2kΩ; C_L = 50pF; unattenuated output.
5. V_O = $200mV_{P-P}$; R_L = 2kΩ; C_L = 50pF.
6. V_O = 20V Step; R_L = 2kΩ; C_L = 50pF.
7. V_O = 10V Step; R_L = 2kΩ; C_L = 50pF.
8. Derived from computer simulation only; not tested.
9. V_{IN} = 0V, V_{IH} = +3.5V, t_R < 20ns (V_{IL} to V_{IH}).
10. Specified for a zero differential input voltage between +IN and -IN. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ±46mA at 20V.
11. Based on a one volt delta in each supply, i.e. 15V ±0.5VDC.
12. R_L = 1kΩ, C_L = 30pF.
13. Specification based on a one time characterization. This parameter is not guaranteed.

Functional Diagram



Applying the HA-5320

The HA-5320 has the uncommitted differential inputs of an op amp, allowing the Sample and Hold function to be combined with many conventional op amp circuits. See the Harris Application Note 517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01 to 0.1µF, ceramic) should be provided from each power supply terminal to the Supply Ground terminal on pin 13.

The ideal ground connections are pin 6 (SIG. Ground) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

Hold Capacitor

The HA-5320 includes a 100pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on this internal capacitor).

Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

If an external hold capacitor C_{HEXT} is used, then a noise bandwidth capacitor of value $0.1C_{HEXT}$ should be connected from pin 8 to ground. Exact value and type are not critical.

The hold capacitor C_{HEXT} should have high insulation resistance and low dielectric absorption, to minimize droop errors. Polystyrene dielectric is a good choice for operating temperatures up to +85°C. Teflon® and glass dielectrics offer good performance to +125°C and above.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

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Applications

Figure 1 shows the HA-5320 connected as a unity gain noninverting amplifier - its most widely used configuration. As an input device for a fast successive - approximation A/D converter, it offers very high throughput rate for a monolithic IC sample/hold amplifier. Also, the HA-5320's hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12 bit accurate output from the converter.

The application may call for an external hold capacitor C_{HEXT} as shown. As mentioned earlier, $0.1C_{HEXT}$ is then recommended at pin 8 to reduce output noise in the Hold mode.

The HA-5320 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

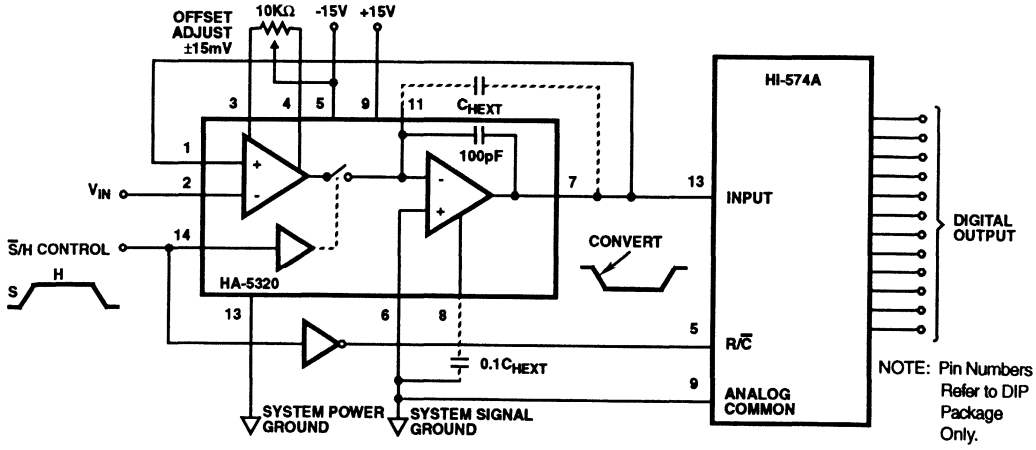


FIGURE 1. TYPICAL HA-5320 CONNECTIONS; NONINVERTING UNITY GAIN MODE

Test Circuits

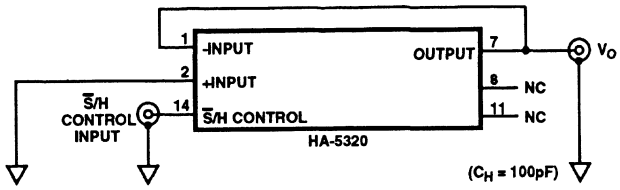
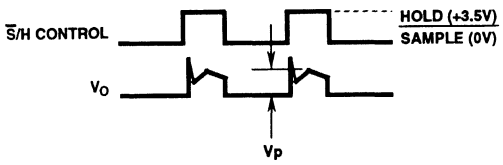


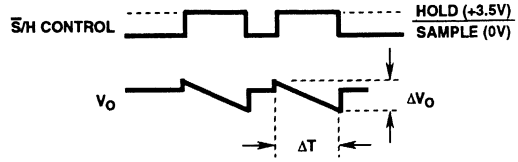
FIGURE 2. CHARGE TRANSFER AND DRIFT CURRENT



NOTES:

1. Observe the "hold step" voltage Vp
2. Compute charge transfer: $Q = VpC_H$

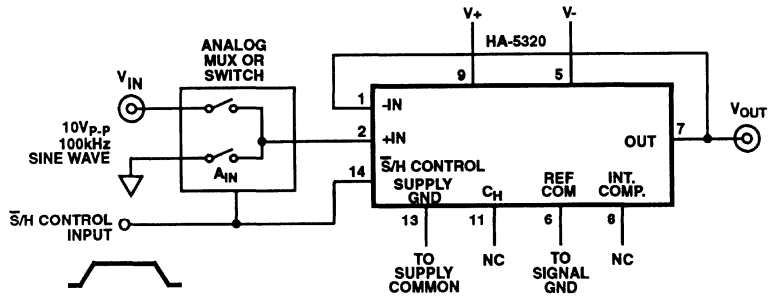
FIGURE 3. CHARGE TRANSFER TEST



NOTES:

1. Observe the voltage "droop", $\Delta V_O/\Delta T$
2. Measure the slope of the output during hold, $\Delta V_O/\Delta T$, and compute drift current: $I_D = C_H \Delta V_O/\Delta T$.

FIGURE 4. DRIFT CURRENT TEST



NOTE:

1. Feedthrough in

$$dB = 20\log\frac{V_{OUT}}{V_{IN}}$$ where:

V_{OUT} = $Volts_{P-P}$, Hold Mode,
V_{IN} = $Volts_{P-P}$

FIGURE 5. HOLD MODE FEED THROUGH ATTENUATION

Typical Performance Curves

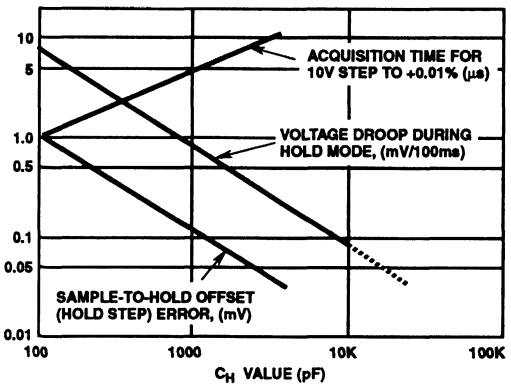


FIGURE 6. TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITOR

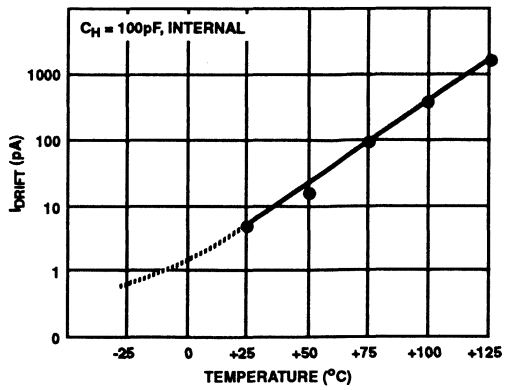


FIGURE 7. DRIFT CURRENT vs TEMPERATURE

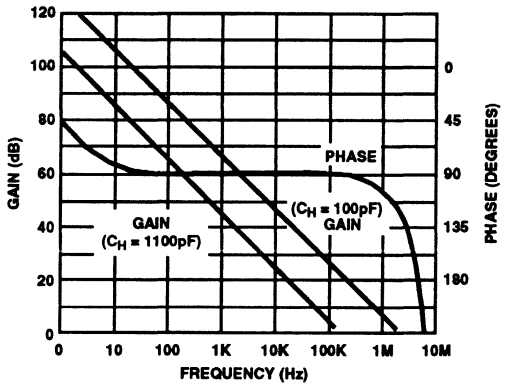
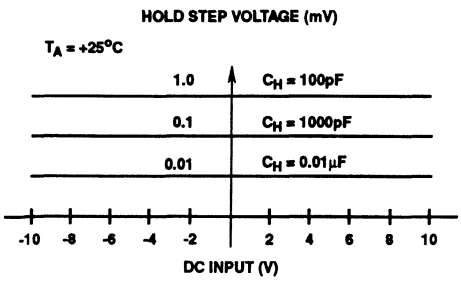
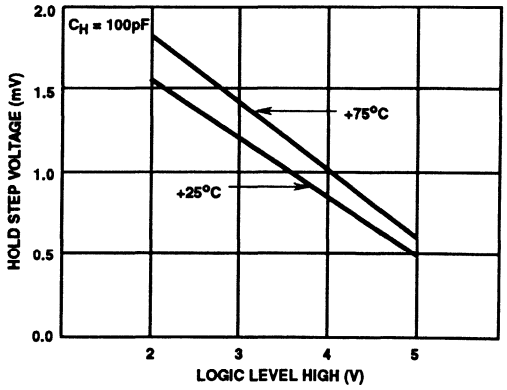


FIGURE 8. OPEN LOOP GAIN AND PHASE RESPONSE



9A. HOLD STEP vs INPUT VOLTAGE



9B. HOLD STEP vs LOGIC (V_{IH}) VOLTAGE

FIGURE 9. TYPICAL SAMPLE-TO-HOLD OFFSET (HOLD STEP) ERROR

Glossary of Terms

Acquisition Time

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Charge Transfer

The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the HOLD mode. Charge transfer is directly proportional to sample-to-hold offset pedestal error, where:

$$\text{Charge Transfer (pC)} = C_H \text{ (pF)} \times \text{Hold Step Error (V)}$$

Aperture Time

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is the interval between the conditions of 10% open and 90% open.

Hold Step Error

Hold Step Error is the output error due to Charge Transfer (see above). It may be calculated from the specified parameter, Charge Transfer, using the following relationship:

$$\text{Hold Step (V)} = \frac{\text{Charge Transfer (pC)}}{\text{Hold Capacitance (pF)}}$$

See Performance Curves.

Effective Aperture Delay Time (EADT)

The difference between the digital delay time from the Hold command to the opening of the S/H switch, and the propagation time from the analog input to the switch.

EADT may be positive, negative or zero. If zero, the $\overline{S}$/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

Drift Current

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D \text{ (pA)} = C_H \text{ (pF)} \times \frac{\Delta V}{\Delta T} \text{ (V/s)}$$

Die Characteristics

Transistor Count	175
Die Dimensions	90.2 x 143.7 x 19 mils
Substrate Potential	$-V_{SUPPLY}$
Process	Bipolar DI

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	70	13
Plastic DIP	85	23
SOIC	95	26

HARRIS SEMICONDUCTOR

HA-5330

Very High Speed Precision Monolithic Sample and Hold Amplifier

March 1993

Features

- Very Fast Acquisition 500ns (0.1%) 650ns (0.01%)
- Low Droop Rate 0.01μV/μs
- Very Low Offset 0.2mV
- High Slew Rate..... 90V/μs
- Wide Supply Range..... ±10V to ±20V
- Internal Hold Capacitor
- Fully Differential Input
- TTL/CMOS Compatible

Applications

- Precision Data Acquisition Systems
- D/A Converter Deglitching
- Auto-Zero Circuits
- Peak Detectors

Description

The HA-5330 is a very fast sample and hold amplifier designed primarily for use with high speed A/D converters. It utilizes the Harris Dielectric Isolation process to achieve a 650ns acquisition time to 12 bit accuracy and a droop rate of 0.01μV/μs. The circuit consists of an input transconductance amplifier capable of producing large amounts of charging current, a low leakage analog switch, and an integrating output stage which includes a 90pF hold capacitor.

The analog switch operates into a virtual ground, so charge injection on the hold capacitor is constant and independent of V_{IN}. Charge injection is held to a low value by compensation circuits and, if necessary, the resulting 0.5mV hold step error can be adjusted to zero via the Offset Adjust terminals. Compensation is also used to minimize leakage currents which cause voltage droop in the Hold mode.

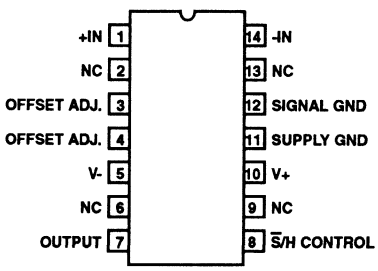
The HA-5330 will operate at reduced supply voltages (to ±10V) with a reduced signal range. The MIL-STD-883 data sheet for this device is available on request.

Ordering Information

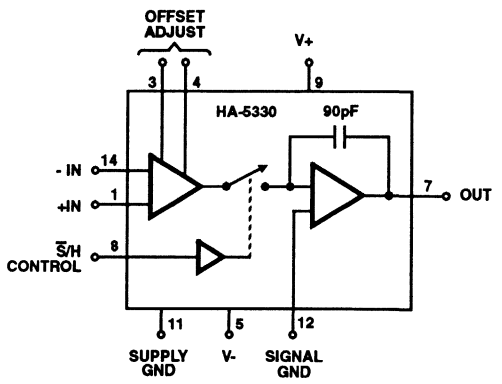
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-5330-2	-55°C to +125°C	14 Lead Ceramic DIP
HA1-5330-4	-25°C to +85°C	14 Lead Ceramic DIP
HA1-5330-5	0°C to +75°C	14 Lead Ceramic DIP
HA3-5330-5	0°C to +75°C	14 Lead Plastic DIP

Pinout

HA-5330
(PDIP, CDIP)
TOP VIEW



Functional Diagram



4 SAMPLE AND HOLD AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2858.1**

Absolute Maximum Ratings (Note 1)

Voltage between V+ and SUPPLY/SIG GND ..... +20V
Voltage between V- and SUPPLY/SIG GND ..... -20V
Voltage between SUPPLY GND and SIG GND ..... ±2.0V
Voltage between $\overline{S}$/H Control and SUPPLY/SIG GND ..... +8V, -6V
Differential Input Voltage 24V
Output Current, Continuous (Note 2) ..... ±17mA
Junction Temperature (Note 13) ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-5330-2 ..... $-55°C \le T_A \le +125°C$
HA-5330-4 ..... $-25°C \le T_A \le +85°C$
HA-5330-5 ..... $0°C \le T_A \le +75°C$
Storage Temperature Range ..... $-65°C \le T_A \le 150°C$
Supply Voltage Range (TYP) ..... ±10V to ±20V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{SUPPLY} = ±15V; $\overline{S}$/H Control V_{IL} = +0.8V (Sample): V_{IH} = +2.0V (Hold); SIG GND = SUPPLY GND, Unity Gain Configuration (Output tied to -Input), Unless Otherwise Specified

PARAMETER	TEMPERATURE	HA-5330-2, -4			HA-5330-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10	-	-	±10	-	-	V
Input Resistance (Note 3)	+25°C	5	15	-	5	15	-	MΩ
Input Capacitance	+25°C	-	3	-	-	3	-	pF
Offset Voltage	+25°C	-	0.2	-	-	0.2	-	mV
	Full	-	-	2.0	-	-	1.5	mV
Offset Voltage Temperature Coefficient	Full	-	1	10	-	1	10	µV/°C
Bias Current	+25°C	-	±20	-	-	±20	-	nA
	Full	-	-	±500	-	-	±300	nA
Offset Current	+25°C	-	20	-	-	20	-	nA
	Full	-	-	500	-	-	300	nA
Common Mode Range	Full	±10	-	-	±10	-	-	V
CMRR (Note 4)	Full	86	100	-	86	100	-	dB
TRANSFER CHARACTERISTICS								
Gain, DC	Full	2×10^6	2×10^7	-	2×10^6	2×10^7	-	V/V
Gain Bandwidth Product (Note 12)	+25°C	-	4.5	-	-	4.5	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage	Full	±10	-	-	±10	-	-	V
Output Current	Full	±10	-	-	±10	-	-	mA
Full Power Bandwidth (Note 6)	+25°C	-	1.4	-	-	1.4	-	MHz
Output Resistance								
Hold Mode	+25°C	-	0.2	-	-	0.2	-	Ω
Sample Mode	+25°C	-	10^{-5}	0.001	-	10^{-5}	0.001	Ω
Total Output Noise, DC to 4.0MHz								
Sample Mode	+25°C	-	230	-	-	230	-	μV_{RMS}
Hold Mode	+25°C	-	190	-	-	190	-	μV_{RMS}
TRANSIENT RESPONSE								
Rise Time (Note 5)	+25°C	-	70	-	-	70	-	ns
Overshoot (Note 5)	+25°C	-	10	-	-	10	-	%
Slew Rate (Note 7)	+25°C	-	90	-	-	90	-	V/µs

Electrical Specifications V_{SUPPLY} = ±15V; $\overline{S}$/H Control V_{IL} = +0.8V (Sample): V_{IH} = +2.0V (Hold); SIG GND = SUPPLY GND, Unity Gain Configuration (Output tied to -Input), Unless Otherwise Specified **(Continued)**

PARAMETER	TEMPERATURE	HA-5330-2, -4			HA-5330-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{IH}	Full	2.0	-	-	2.0	-	-	V
Input Voltage (Low), V_{IL}	Full	-	-	0.8	-	-	0.8	V
Input Current (V_{IL} = 0V)	Full	-	10	40	-	10	40	µA
Input Current (V_{IH} = +5V)	Full	-	10	40	-	10	40	µA
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time (Note 8)								
(0.1%)	+25°C	-	500	-	-	500	-	ns
	Full	-	-	700	-	-	700	ns
(0.01%)	+25°C	-	650	-	-	650	-	ns
	Full	-	-	900	-	-	900	ns
Aperture Time (Note 3)	+25°C	-	20	-	-	20	-	ns
Effective Aperture Delay Time (See Glossary)	+25°C	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty	+25°C	-	0.1	-	-	0.1	-	ns
Droop Rate (Note 9)	+25°C	-	0.01	-	-	0.01	-	µV/µs
	Full	-	-	100	-	-	10	µV/µs
Hold Step Error (Note 10)	+25°C	-	0.5	-	-	0.5	-	mV
Hold Mode Settling Time (0.01%)	+25°C	-	100	200	-	100	200	ns
Hold Mode Feedthru 20V_{P-P}, 100kHz	Full	-	-88	-	-	-88	-	dB
POWER SUPPLY CHARACTERISTICS								
Positive Supply Current	Full	-	18	22	-	18	24	mA
Negative Supply Current	Full	-	19	23	-	19	25	mA
Power Supply Rejection, V+, V- (Note 11)	Full	86	100	-	86	100	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Internal Power Dissipation may limit Output Current below ±17mA.
3. Derived from computer simulation only; not tested.
4. $+V_{CM}$ = ±10V DC.
5. V_I = 200mV Step; R_L = 2K; C_L = 50pF .
6. Full power bandwidth based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$. Distortion of wave shape occurs beyond 100KHz due to slew rate enhancement circuitry.
7. V_O = 20V Step; R_L = 2kΩ; C_L = 50pF.
8. V_O = 10V Step; R_L = 2kΩ; C_L = 50pF.
9. This parameter is measured at ambient temperature extremes in a high speed test environment. Consequently, steady state heating effects from internal power dissipation are not included.
10. V_{IN} = 0V; V_{IH} = +3.5V; t_R = 22ns (V_{IL} to V_{IH}). See graph.
11. Based on a three volt delta in each supply, i.e. 15V = ±1.5V DC.
12. V_{OUT} = 200mV_{P-P}, R_L = 2kΩ, C_L = 50pF.
13. Maximum power dissipation, including output load, must be designed to maintain the junction temperature below +175°C for the ceramic package, and below +150°C for the plastic package

Applying the HA-5330

The HA-5330 has the uncommitted differential inputs of an op amp, allowing the Sample/Hold function to be combined with many conventional op amp circuit ideas. See the Harris Application Note 517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01µF to 0.1µF, ceramic) should be provided from each power supply terminal to the Supply GND Terminal on pin 11.

Applications

The HA-5330 is configured as a unity gain noninverting amplifier by simply connecting the output (pin 7) to the inverting input (pin 14). As an input device for a fast successive - approximation A/D converter, it offers an extremely high throughput rate. Also, the HA-5330's pedestal error is adjustable to zero by using an Offset Adjust potentiometer (10K to 50K) center tapped to V-.

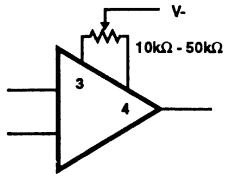


FIGURE 1. HA-5330 OFFSET ADJUST

The ideal ground connections are pin 11 (Supply Ground) directly to the system Supply Common, and pin 12 (Signal Ground) directly to the system Signal Ground (Analog Ground).

Hold Capacitor

The HA-5330 includes a 90pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on the internal capacitor).

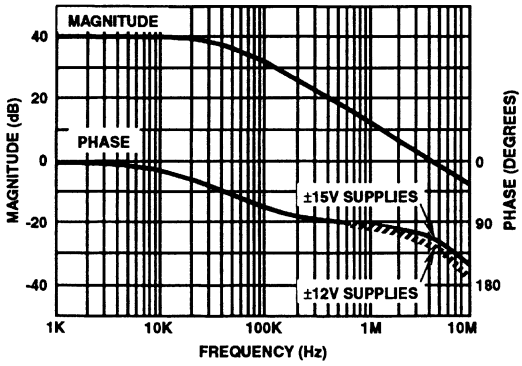


FIGURE 2. MAGNITUDE AND PHASE RESPONSE (CLOSED LOOP GAIN = 100)

Output Stage

The HA-5330 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the $\overline{S}$/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

Glossary of Terms

Acquisition Time

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Aperture Time

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Hold Step Error

Hold step error is the output shift due to charge transfer from the sample to the hold mode. It is also referred to as "offset step" or "pedestal error".

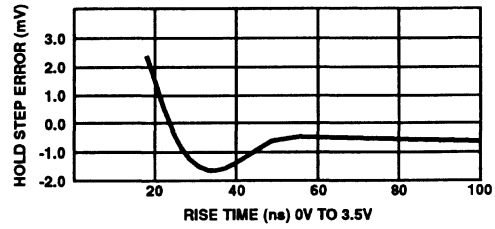


FIGURE 3. HOLD STEP ERROR vs $\overline{S}$/H CONTROL RISE TIME

Effective Aperture Delay Time (EADT)

The difference between the digital delay time from the Hold command to the opening of the $\overline{S}$/H switch, and the propagation time from the analog input to the switch.

EADT may be positive, negative or zero. If zero, the $\overline{S}$/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

Die Characteristics

Transistor Count 205
Die Dimensions..... 99 x 166 x 19 mils
Substrate Potential ..... SIG GND
Process..... Bipolar DI

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	70	13
Plastic DIP	85	23

HARRIS SEMICONDUCTOR

HA-5340

High Speed, Low Distortion, Precision Monolithic Sample and Hold Amplifier

March 1993

Features

- Fast Acquisition Time (0.01%) 700ns
- Fast Hold Mode Settling Time (0.01%) 200ns
- Low Distortion (Hold Mode) . . . . . -72dBc (V_{IN} = 200kHz, Fs = 450kHz, $5V_{P-P}$)
- Bandwidth Minimally Affected By External C_H
- Fully Differential Analog Inputs
- Built-in 135pF Hold Capacitor
- Pin Compatible with HA-5320

Applications

- High Bandwidth Precision Data Acquisition Systems
- Inertial Navigation and Guidance Systems
- Ultrasonics
- SONAR
- RADAR

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-5340-5	0°C to +75°C	14 Lead Ceramic DIP
HA1-5340-9	-40°C to +85°C	14 Lead Ceramic DIP
HA3-5340-5	0°C to +75°C	14 Lead Plastic DIP
HA3-5340-9	-40°C to +85°C	14 Lead Plastic DIP
HA9P5340-5	0°C to +75°C	16 Lead Wide Body SOIC

Description

The HA-5340 combines the advantages of two sample/ hold architectures to create a new generation of monolithic sample/hold. High amplitude, high frequency signals can be sampled with very low distortion being introduced. The combination of exceptionally fast acquisition time and specified/characterized hold mode distortion is an industry first. Additionally, the AC performance is only minimally affected by additional hold capacitance.

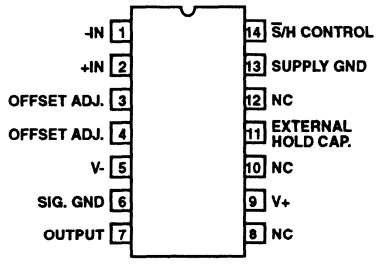
To achieve this level of performance, the benefits of an integrating output stage have been combined with the advantages of a buffered hold capacitor. To the user this translates to a front-end stage that has high bandwidth due to charging only a small capacitive load and an output stage with constant pedestal error which can be nulled out using the offset adjust pins. Since the performance penalty for additional hold capacitance is low, the designer can further minimize pedestal error and droop rate without sacrificing speed.

Low distortion, fast acquisition, and low droop rate are the result, making the HA-5340 the obvious choice for high speed, high accuracy sampling systems.

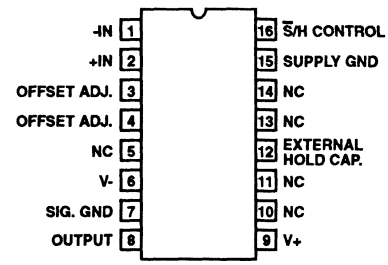
For a Military temperature range version request the HA-5340/883 data sheet.

Pinouts

HA-5340
(PDIP, CDIP)
TOP VIEW



HA-5340
(300 mil SOIC)
TOP VIEW



4 SAMPLE AND HOLD AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2859.1

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 36V
Differential Input Voltage. 24V
Digital Input Voltage . . . . . +8V, -6V
Output Current, Continuous . . . . . ±20mA
Junction Temperature (Note 5) . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.). . . . . +300°C

Operating Conditions

Operating Temperature Range
HA-5340-9 . . . . . $-40°C \leq T_A \leq +85°C$
HA-5340-5 . . . . . $0°C \leq T_A \leq +75°C$
Storage Temperature Range . . . . . $-65°C \leq T_A \leq +150°C$
Supply Voltage Range (TYP) . . . . . ±12V to ±18V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{SUPPLY} = ±15.0V; C_H = Internal = 135pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold). Non-Inverting Unity Gain Configuration (Output tied to -Input), R_L = 2kΩ, C_L = 60pF, Unless Otherwise Specified

PARAMETER		TEMPERATURE	HA-5340-9 HA-5340-5 MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Voltage Range		Full	-10	-	+10	V
Input Resistance (Note 2)		+25°C	-	1	-	MΩ
Input Capacitance		+25°C	-	-	3	pF
Input Offset Voltage		+25°C	-	-	1.5	mV
		Full	-	-	3.0	mV
Offset Voltage Temperature Coefficient		Full	-	-	30	µV/°C
Bias Current		+25°C	-	±70	-	nA
		Full	-	-	±350	nA
Offset Current		+25°C	-	±50	-	nA
		Full	-	-	±350	nA
Common Mode Range		Full	-10	-	+10	V
CMRR (±10 Vdc) (Note 3)		+25°C	-	83	-	dB
		Full	72	-	-	dB
TRANSFER CHARACTERISTICS						
Gain, DC		+25°C	110	140	-	dB
Gain Bandwidth Product	C_H External = 0pF	Full	-	10	-	MHz
	C_H External = 100pF	Full	-	9.6	-	MHz
	C_H External = 1000pF	Full	-	6.7	-	MHz
TRANSIENT RESPONSE						
Rise Time (200mV step)		+25°C	-	20	30	ns
Overshoot (200mV step)		+25°C	-	35	50	%
Slew Rate (10V step)		+25°C	40	60	-	V/µs
DIGITAL INPUT CHARACTERISTICS						
Input Voltage (High), V_{IH}		Full	2.0	-	-	V
Input Voltage (Low), V_{IL}		Full	-	-	0.8	V
Input Current V_{IL} = 0V, I_{IL}		Full	-	7	40	µA
Input Current V_{IH} = 5V, I_{IH}		Full	-	4	40	µA

Electrical Specifications V_{SUPPLY} = ±15.0V; C_H = Internal = 135pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold). Non-Inverting Unity Gain Configuration (Output tied to -Input), R_L = 2kΩ, C_L = 60pF, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMPERATURE	HA-5340-9 HA-5340-5 MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS						
Output Voltage		Full	-10	-	+10	V
Output Current		Full	-10	-	+10	mA
Full Power Bandwidth (Slew Rate Limited) (Note 4)		Full	0.6	0.9	-	MHz
Output Resistance - Hold Mode		+25°C	-	0.05	0.1	Ω
		Full	-	0.07	0.15	Ω
TOTAL OUTPUT NOISE, D.C. TO 10MHz						
Sample Mode		+25°C	-	325	400	μV_{RMS}
Hold Mode		+25°C	-	325	400	μV_{RMS}
DISTORTION CHARACTERISTICS						
SAMPLE MODE						
Signal to Noise Ratio (RMS Signal to RMS noise)	V_{IN} = 200kHz ($20V_{P-P}$)	Full	-	115	-	dB
Total Harmonic Distortion	V_{IN} = 200kHz, $5V_{P-P}$	Full	-90	-100	-	dBc
	V_{IN} = 200kHz, $10V_{P-P}$	Full	-76	-82	-	dBc
	V_{IN} = 200kHz, $20V_{P-P}$	Full	-70	-74	-	dBc
	V_{IN} = 500kHz, $5V_{P-P}$	Full	-66	-75	-	dBc
Intermodulation Distortion V_{IN} = $10V_{P-P}$	(f1 = 20kHz, f2 = 21kHz)	Full	-78	-83	-	dBc
HOLD MODE (50% Duty Cycle S/H) Signal to Noise Ratio (RMS Signal to RMS noise)						
Fs = 450kHz	V_{IN} = 200kHz, $5V_{P-P}$	+25°C	-	76	-	dB
	V_{IN} = 200kHz, $10V_{P-P}$	+25°C	-	76	-	dB
Total Harmonic Distortion						
Fs = 450kHz	V_{IN} = 200kHz, $5V_{P-P}$	+25°C	-	-72	-	dBc
	V_{IN} = 200kHz, $10V_{P-P}$	+25°C	-	-66	-	dBc
	V_{IN} = 200kHz, $20V_{P-P}$	+25°C	-	-56	-	dBc
Fs = 450kHz	V_{IN} = 100kHz, $5V_{P-P}$	+25°C	-	-84	-	dBc
	V_{IN} = 100kHz, $10V_{P-P}$	+25°C	-	-71	-	dBc
	V_{IN} = 100kHz, $20V_{P-P}$	+25°C	-	-61	-	dBc
Fs = $2f_{IN}$(Nyquist)	V_{IN} = 20kHz, $5V_{P-P}$	+25°C	-	-95	-	dBc
	V_{IN} = 50kHz, $5V_{P-P}$	+25°C	-	-91	-	dBc
	V_{IN} = 100kHz, $5V_{P-P}$	+25°C	-	-82	-	dBc
Intermodulation Distortion Fs = 450kHz	V_{IN} = $10V_{P-P}$ (f1 = 20kHz, f2 = 21kHz)	+25°C	-	-79	-	dBc

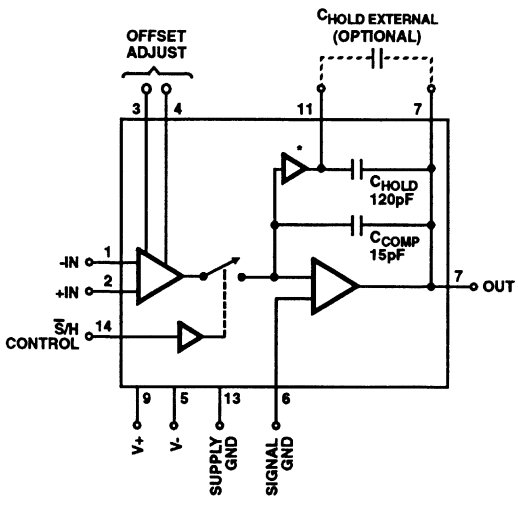
Electrical Specifications V_{SUPPLY} = ±15.0V; C_H = Internal = 135pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold). Non-Inverting Unity Gain Configuration (Output tied to -Input), R_L = 2kΩ, C_L = 60pF, Unless Otherwise Specified (Continued)

PARAMETER		TEMPERATURE	HA-5340-9 HA-5340-5 MIN	TYP	MAX	UNITS
SAMPLE/HOLD CHARACTERISTICS						
Acquisition Time	10V Step to 0.01%	+25°C	-	700	-	ns
		Full	-	-	900	ns
	10V Step to 0.1%	+25°C	-	430	600	ns
Droop Rate (C_H = Internal)		+25°C	-	0.1	-	µV/µs
		Full	-	-	95	µV/µs
Hold Step Error (V_{IL} = 0V, V_{IH} = 4.0V, t_R = 5ns)		+25°C	-	15	-	mV
Hold Mode Settling Time (to ±1mV)		Full	-	200	300	ns
Hold Mode Feedthrough ($20V_{P-P}$, 200kHz, sine)		Full	-	-76	-	dB
EADT (Effective Aperture Delay Time)		+25°C	-	-15	-	ns
Aperture Uncertainty		+25°C	-	0.2	-	ns
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current		Full	-	19	25	mA
Negative Supply Current		Full	-	19	25	mA
PSRR (V or -V, 10% delta)		Full	75	82	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Derived from Computer Simulation only, not tested.
3. +CMRR is measured from 0V to +10V, -CMRR is measured from 0V to -10V
4. Based on the calculation FPBW = Slew Rate/$2\pi V_{PEAK}$ (V_{PEAK} = 10V).
5. See Thermal Impedances in "Die Characteristics" section. Maximum power dissipation must be designed to maintain the junction temperature below +175°C for the ceramic package, and below +150°C for the plastic packages.

Functional Diagram



Die Characteristics

Transistor Count 196

Die Dimensions. . . . . 139 x 84 x 19 mils

Tie Substrate To . . . . . V-

Process. . . . . Bipolar DI

Thermal Constants (°C/W)	θ_{JA}	θ_{Jc}
Ceramic DIP	70	13
Plastic DIP	85	23
SOIC	95	26

Applying the HA-5340

The HA-5340 has the uncommitted differential inputs of an op amp, allowing the Sample and Hold function to be combined with many conventional op amp circuits. See the Harris Application Note 517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01µF to 0.1µF, ceramic) should be provided from each power supply terminal to the Supply Ground terminal on pin 13.

The ideal ground connections are pin 6 (SIG. GND) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

Hold Capacitor

The HA-5340 includes a 135pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on this internal capacitor). Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

The hold capacitor C_H should have high insulation resistance and low dielectric absorption, to minimize droop errors. Teflon®, polystyrene and polypropylene dielectric capacitor types offer good performance over the specified operating temperature range.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

®Teflon is a registered Trademark of Dupont Corporation.

Applications

Figure 1 shows the HA-5340 connected as a unity gain non-inverting amplifier - its most widely used configuration. As an input device for a fast successive - approximation A/D converter, it offers very high throughput rate for a monolithic IC sample/hold amplifier. Also, the HA-5340's hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12 bit accurate output from the converter.

The HA-5340 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

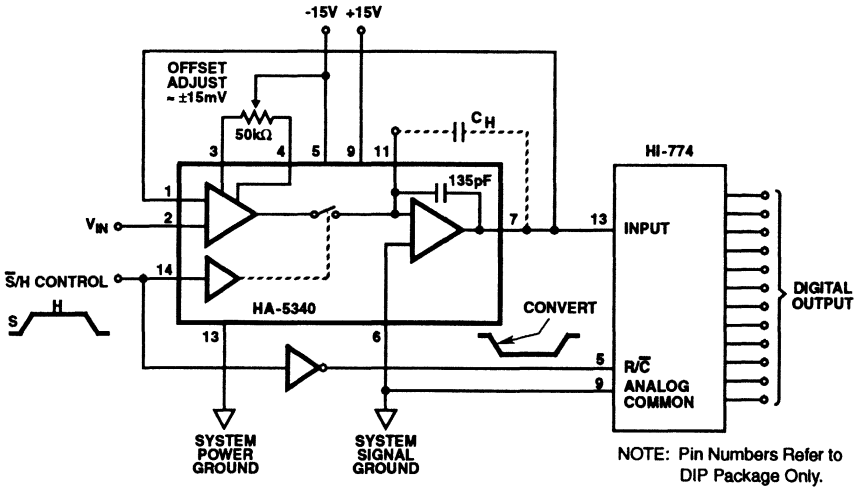


FIGURE 1. TYPICAL HA-5340 CONNECTIONS; NONINVERTING UNITY GAIN MODE

Test Circuits

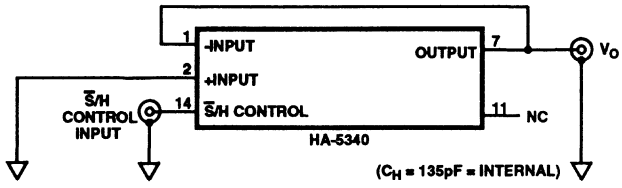
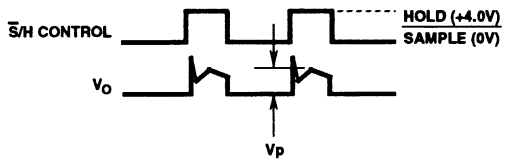


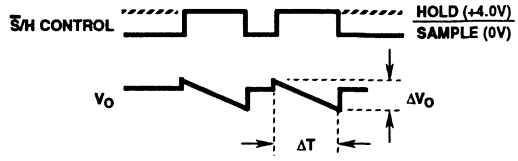
FIGURE 2. HOLD STEP ERROR AND DROOP RATE



NOTE:

1. Observe the "hold step" voltage Vp

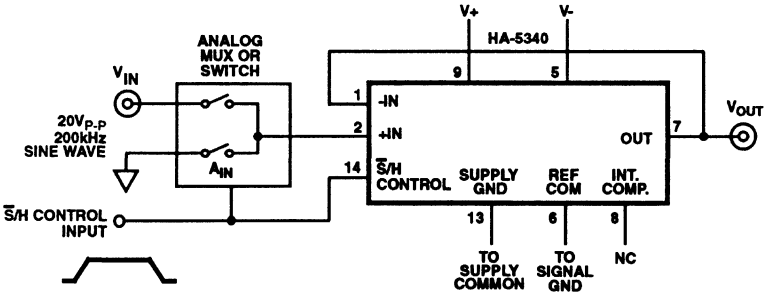
FIGURE 3. HOLD STEP ERROR



NOTES:

1. Observe the voltage "droop", $\Delta V_O/\Delta T$
2. Measure the slope of the output during hold, $\Delta V_O/\Delta T$
3. Droop can be positive or negative - usually to one rail or the other not to GND

FIGURE 4. DROOP RATE TEST



NOTE:

1. Feedthrough in

$$dB = 20\log\frac{V_{OUT}}{V_{IN}}$$ where:

V_{OUT} = $Volts_{P-P}$, Hold Mode,
V_{IN} = $Volts_{P-P}$

FIGURE 5. HOLD MODE FEED THROUGH ATTENUATION

Typical Performance Curves $T_A = +25°C, V_S = \pm15V$, Unless Otherwise Specified

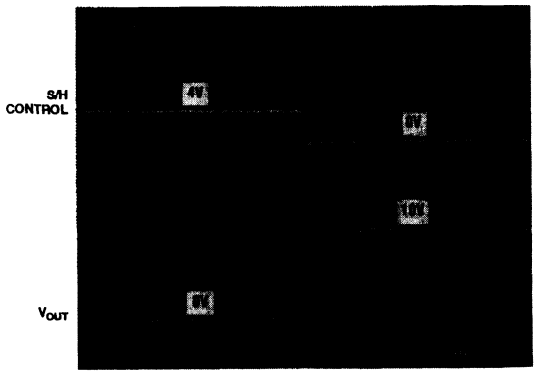


FIGURE 6. T_{ACQ} POS 0 TO +10 STEP

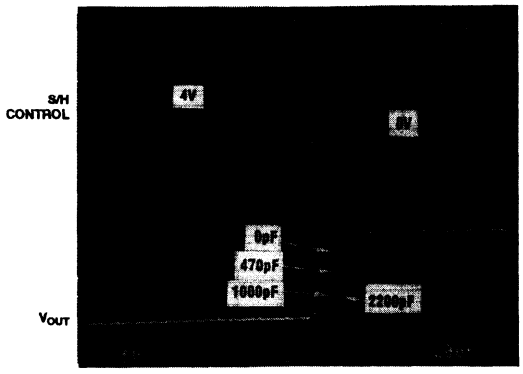


FIGURE 7. T_{ACQ} vs ADDITIONAL C_H

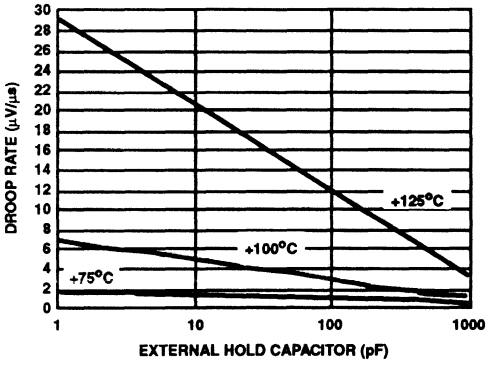


FIGURE 8. DROOP RATE vs HOLD CAPACITOR SIZE

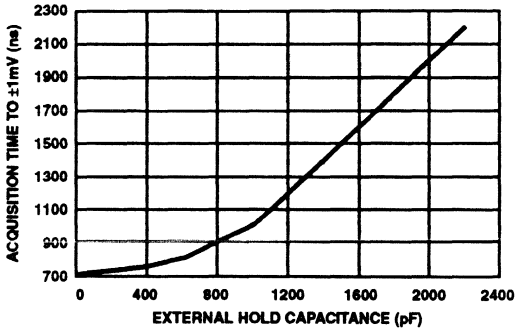


FIGURE 9. ACQUISITION TIME (0.01%) vs HOLD CAPACITANCE

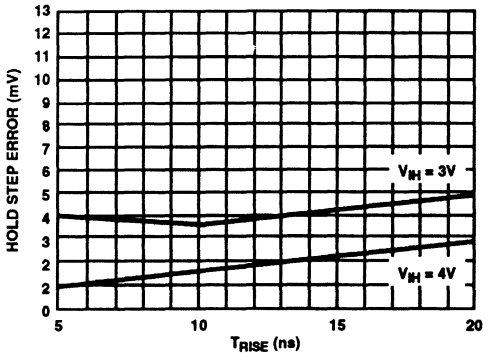


FIGURE 10. HOLD STEP ERROR vs T_{RISE}
C_H = Internal, Temperature = +25°C

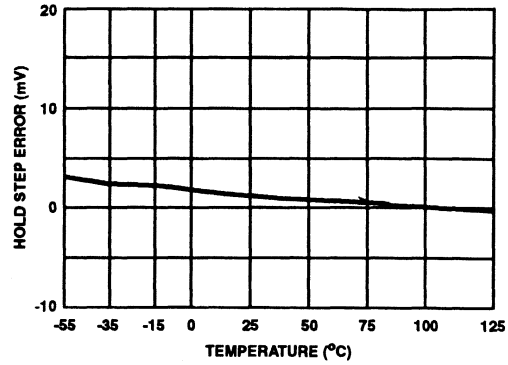


FIGURE 11. HOLD STEP ERROR vs TEMPERATURE
V_{IH} = 4V, C_H = 470pF

Typical Performance Curves $T_A = +25°C, V_S = \pm15V$, Unless Otherwise Specified (Continued)

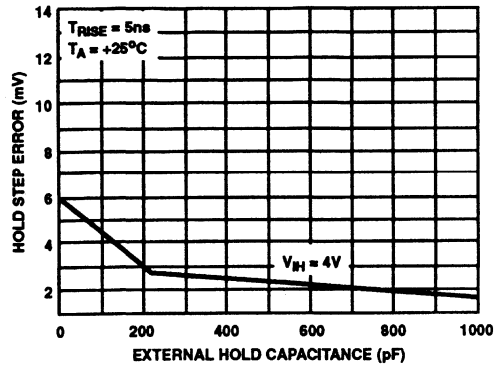


FIGURE 12. HOLD STEP ERROR vs HOLD CAPACITANCE

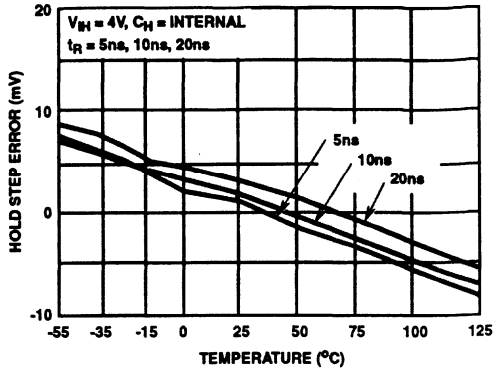


FIGURE 13. HOLD STEP ERROR vs TEMPERATURE

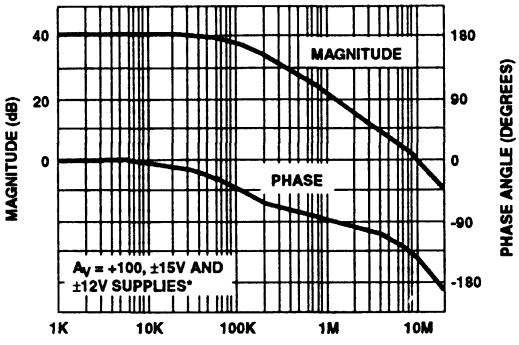


FIGURE 14. CLOSED LOOP PHASE/GAIN

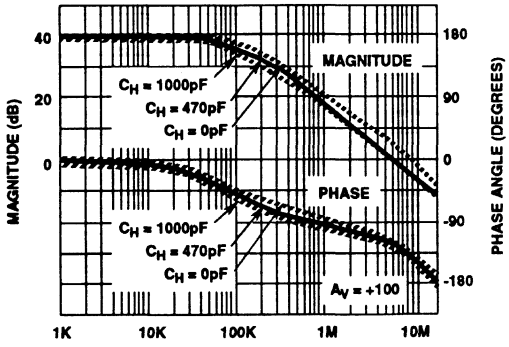


FIGURE 15. CLOSED LOOP PHASE/GAIN

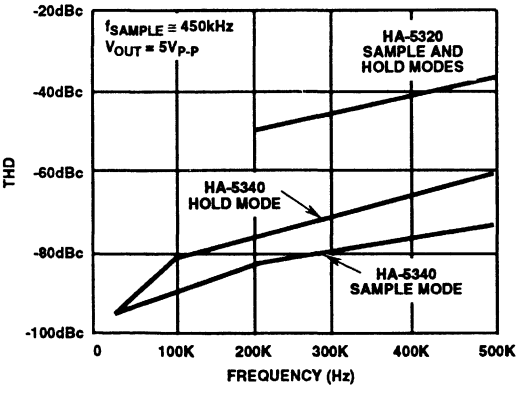


FIGURE 16. THD vs FREQUENCY

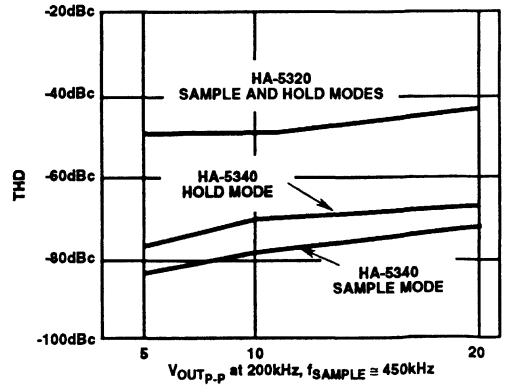


FIGURE 17. THD vs V_{OUT}

* ±15V and ±12V supplies trace the same line within the width of the line, therefore only one line is shown.

HARRIS SEMICONDUCTOR

HA5350, HA5351

PRELIMINARY

March 1993

Ultra Fast (50ns) Sample and Hold Amplifiers

Features

- Ultra Fast Acquisition 50ns
- Very Low Offset Error 0.5mV
- Very Low Hold Step Error 1.25mV
- On Chip Hold Capacitor
- Fast Hold Mode Settling Time..... 30ns
- Low Power Dissipation 200mW
- Total Harmonic Distortion (Hold Mode)..... -68dBc
- Fully Differential Inputs
- Embedded Track/Peak Function (HA5350)

Applications

- Synchronous Sampling
- Instrumentation
- A/D Conversion
- Peak Detectors

Description

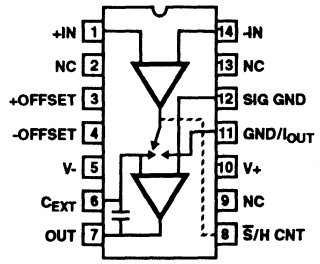
The HA5350/51 are ultra-fast sample/hold amplifiers designed for a wide range of applications including A/D conversion, synchronous sampling, and peak detection. Built with the Harris HBC-10 BiCMOS process, these sample/hold amplifiers also feature extremely low power dissipation, making them ideal for use in systems that sample multiple signals and require low power. The HA5350 features fully differential inputs, offset adjustment and an external hold capacitor pin to reduce droop rate if required. In addition, it can be configured as a dedicated peak detector with the addition of an external diode. The HA5351 is an 8 lead version designed for minimum board space. Both HA5350 and HA5351 are available in PDIP, CERDIP, and SOIC packages as indicated below.

Ordering Information

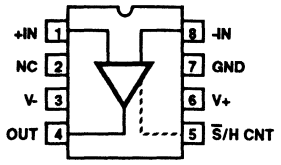
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA5350IP	-40°C to +85°C	14 Lead Plastic DIP
HA5350IJ	-40°C to +85°C	14 Lead Ceramic DIP
HA5350IB	-40°C to +85°C	14 Lead SOIC
HA5351IP	-40°C to +85°C	8 Lead Plastic DIP
HA5351IJ	-40°C to +85°C	8 Lead Ceramic DIP
HA5351IB	-40°C to +85°C	8 Lead SOIC

Pinouts

HA5350
(PDIP, CDIP, SOIC)
TOP VIEW



HA5351
(PDIP, CDIP, SOIC)
TOP VIEW



4 SAMPLE AND HOLD AMPLIFIERS

File Number 3379

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals ..... +11V
Differential Input Voltage 6V
Voltage Between $\overline{S}$/H Control and Ground ..... +5.5V
Output Current, Continuous ..... ±30mA
Junction Temperature (Ceramic Package) ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA5350I ..... $-40°C \le T_A \le +85°C$
HA5351I ..... $-40°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions (Unless Otherwise Specified) $V_{SUPPLY} = \pm5V$; C_H = Internal = 15pF, Digital Input: $V_{IL} = +0.0V$ (Sample), $V_{IH} = 4.0V$ (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), $R_L = 500\Omega$, $C_L = 50pF$

PARAMETERS		TEMP	HA5350I, HA5351I LIMITS MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Voltage Range		Full	-2.5	-	+2.5	V
Input Resistance (Note 2)		+25°C	100	500	-	kΩ
Input Capacitance		+25°C	-	-	5	pF
Input Offset Voltage		+25°C	0.5	-	0.5	mV
		Full	-2	-	2	mV
Offset Voltage Temperature Coefficient		Full	-	-	20	µV/°C
Bias Current		+25°C	-	2.5	5	µA
		Full	-	-	15	µA
Offset Current		+25°C	-1.5	-	+1.5	µA
		Full	-3	-	3	µA
Common Mode Range		Full	-2.5	-	+2.5	V
CMRR ($\pm2.5V_{DC}$) (Note 3)		+25°C	72	-	-	dB
		Full	-	-	-	dB
TRANSFER CHARACTERISTICS						
Gain, DC		+25°C	-	115	-	dB
Gain Bandwidth Product	C_H External = 0pF	+25°C	20	-	-	MHz
	C_H External = 5pF	+25°C	-	-	-	MHz
	C_H External = 10pF	+25°C	-	-	-	MHz
TRANSIENT RESPONSE						
Rise Time	(200mV Step)	+25°C	-	-	15	ns
Overshoot	(200mV Step)	+25°C	-	-	30	%
Slew Rate	(2.5V Step)	+25°C	100	130	-	V/µs
DIGITAL INPUT CHARACTERISTICS						
Input Voltage (High)	V_{IH}	Full	2.0	-	-	V
Input Voltage (Low)	V_{IL}	Full	-	-	0.8	V
Input Current $V_{IL} = 0V$	I_{IL}	Full	-10	-	10	µA
Input Current ($V_{IH} = 5V$)	I_{IH}	Full	-10	-	10	µA

Electrical Specifications Test Conditions (Unless Otherwise Specified) V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), R_L = 500Ω, C_L = 50pF **(Continued)**

PARAMETERS		TEMP	HA5350I, HA5351I LIMITS MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS						
Output Voltage		Full	-2.5	-	+2.5	V
Output Current Drive (100Ω to ±2.0V)		Full	-20	-	+20	mA
Full Power Bandwidth (Slew Rate Limited) (Note 4)		Full	-	8.5	-	MHz
Output Resistance - Hold Mode		+25°C	-	0.02	-	Ω
		Full	-	-	-	Ω
TOTAL OUTPUT NOISE, D.C. TO 10MHz						
Sample Mode		+25°C	-	325	-	μV_{RMS}
Hold Mode		+25°C	-	325	-	μV_{RMS}
DISTORTION CHARACTERISTICS						
SAMPLE MODE Signal to Noise Ratio (RMS Signal to RMS Noise)	V_{IN} = $5V_{P-P}$, F_{IN} = 1MHz	+25°C	-	-	-	dB
Total Harmonic Distortion	V_{IN} = $5V_{P-P}$, F_{IN} = 1MHz	+25°C	-70	-	-	dBc
	V_{IN} = $5V_{P-P}$, F_{IN} = 5MHz	+25°C	-	-	-	dBc
Intermodulation Distortion V_{IN} = $5V_{P-P}$	F1 = 200kHz, F2 = 201kHz	+25°C	-	-	-	dBc
HOLD MODE (50% Duty Cycle $\overline{S}$/H) Signal to Noise Ratio (RMS Signal to RMS Noise) Fs = 5MHz	V_{IN} = $5V_{P-P}$, F_{IN} = 1MHz	+25°C	-	-	-	dB
Total Harmonic Distortion Fs = 5MHz	V_{IN} = $5V_{P-P}$, F_{IN} = 1MHz	+25°C	-68	-	-	dBc
Fs = 5MHz	V_{IN} = $5V_{P-P}$, F_{IN} = 500kHz	+25°C	-	-	-	dBc
Fs = $2F_{IN}$(Nyquist)	V_{IN} = $5V_{P-P}$, F_{IN} = 200kHz	+25°C	-	-	-	dBc
	V_{IN} = $5V_{P-P}$, F_{IN} = 500kHz	+25°C	-	-	-	dBc
	V_{IN} = $5V_{P-P}$, F_{IN} = 1MHz	+25°C	-	-	-	dBc
Intermodulation Distortion Fs = 5MHz	V_{IN} = $5V_{P-P}$ (F1 = 200kHz, F2 = 201kHz)	+25°C	-	-	-	dBc
SAMPLE AND HOLD CHARACTERISTICS						
Acquisition Time	2.5V Step to ±1mV	+25°C	-	50	-	ns
		Full	-	-	-	ns
	2.5V Step to 0.01%	+25°C	-	85	100	ns
Droop Rate (C_H = Internal)		+25°C	-	0.1	-	V/ms
		Full	-1	-	1	V/ms
Hold Step Error (V_{IL} = 0V, V_{IH} = 4.0V, t_R = 5ns)		+25°C	-1.25	-	+1.25	mV
Hold Mode Settling Time (to ±1mV)		+25°C	-	30	-	ns

Electrical Specifications Test Conditions (Unless Otherwise Specified) V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), R_L = 500Ω, C_L = 50pF **(Continued)**

PARAMETERS	TEMP	HA5350I, HA5351I LIMITS			UNITS
		MIN	TYP	MAX	
SAMPLE AND HOLD CHARACTERISTICS (Continued)					
Hold Mode Feedthrough ($5V_{P-P}$, 500kHz, Sine)	+25°C	68	-	-	dB
EADT (Effective Aperture Delay Time)	+25°C	-	10	-	ns
Aperture Uncertainty	+25°C	-	10	-	ps
POWER SUPPLY CHARACTERISTICS					
Positive Supply Current	Full	-	20	22	mA
Negative Supply Current	Full	-	20	22	mA
PSRR (V+ or V-, 10% Delta)	Full	65	-	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Derived from Computer Simulation only, not tested.
3. +CMRR is measured from 0V to +2.5V, -CMRR is measured from 0V to -2.5V.
4. Based on the calculation FPBW = Slew Rate/$2\pi V_{PEAK}$ (V_{PEAK} = 2.5V).

Die Characteristics

DIE DIMENSIONS:
70 x 90 x 19 ± 1mils

METALLIZATION:
Metal 1: AlCu (1%)/TiW, Thickness: 6kÅ ± 0.75kÅ
Metal 2: AlCu (1%), Thickness: 16kÅ ± 1.1kÅ

GLASSIVATION:
Type: Sandwich Passivation (Nitride + Oxide)
Thickness: Silox - 8kÅ ± 0.8kÅ; Nitride - 4.2kÅ ± 0.4kÅ

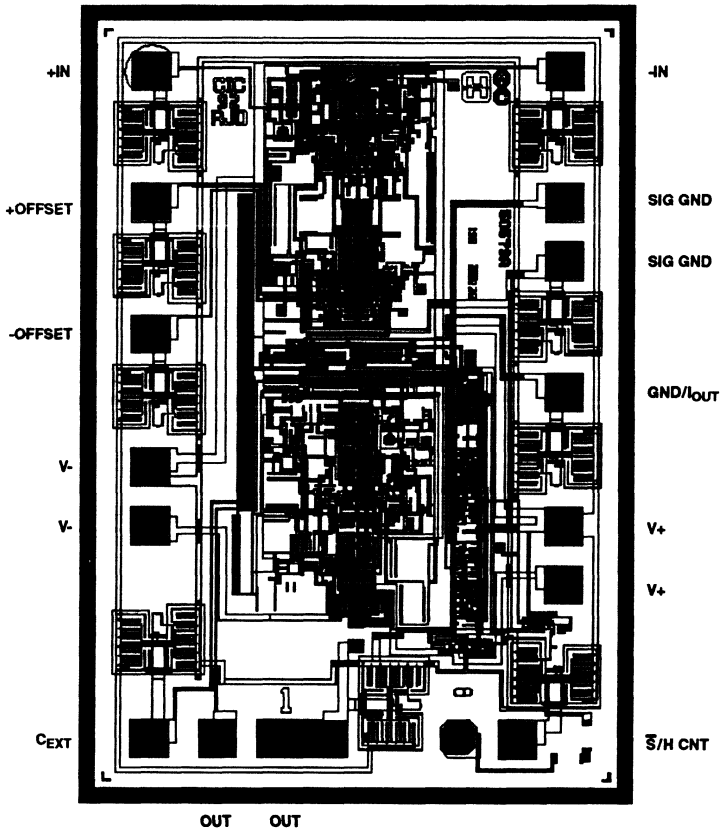
DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC
Eutectic - Ceramic DIP

TRANSISTOR COUNT: 165

SUBSTRATE POTENTIAL (Powered Up): V-

Metallization Mask Layout

HA5350, HA5351



NOTE: Adjacent pads with the same names (e.g. V-) must both be bonded to the same point.

HARRIS SEMICONDUCTOR

HA5352

PRELIMINARY

March 1993

Ultra Fast (50ns) Dual Sample and Hold Amplifier

Features

- Ultra Fast Acquisition 50ns
- Very Low Offset Error 0.5mV
- Very Low Hold Step Error 1.25mV
- On Chip Hold Capacitor
- Fast Hold Mode Settling Time..... 30ns
- Low Power Dissipation 200mW
- Total Harmonic Distortion (Hold Mode)..... -68dBc
- Fully Differential Inputs

Applications

- Synchronous Sampling
- Instrumentation
- A/D Conversion
- Peak Detectors

Description

The HA5352 is an ultra-fast dual sample/hold amplifier designed for a wide range of applications including A/D conversion, synchronous sampling, and peak detection. Built with the Harris HBC-10 BiCMOS process, this sample/hold amplifier also features extremely low power dissipation, making it ideal for use in systems that sample multiple signals and require low power.

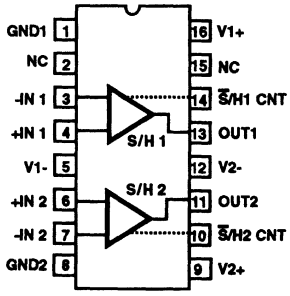
The HA5352 is available in PDIP, CERDIP, and SOIC packages as indicated below.

Ordering Information

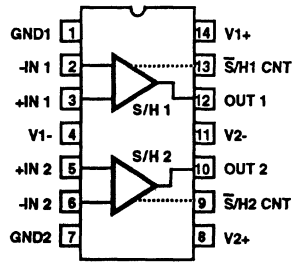
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA5352IP	-40°C to +85°C	14 Lead Plastic DIP
HA5352IJ	-40°C to +85°C	14 Lead Ceramic DIP
HA5352IB	-40°C to +85°C	16 Lead Wide Body SOIC

Pinouts

HA5352
(300 mil SOIC)
TOP VIEW



HA5352
(PDIP, CDIP)
TOP VIEW



File Number 3394

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals ..... +11V
Differential Input Voltage 6V
Voltage Between $\overline{S}$/H Control and Ground ..... +5.5V
Output Current, Continuous ..... ±30mA
Junction Temperature (Ceramic Package) ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA5352I ..... -40°C ≤ T_A ≤ +85°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions (Unless Otherwise Specified) V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), R_L = 500Ω, C_L = 50pF

PARAMETERS		TEMP	HA5352I LIMITS MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Voltage Range		Full	-2.5	-	+2.5	V
Input Resistance (Note 2)		+25°C	100	500	-	kΩ
Input Capacitance		+25°C	-	-	5	pF
Input Offset Voltage		+25°C	0.5	-	0.5	mV
		Full	-2	-	2	mV
Offset Voltage Temperature Coefficient (Note 2)		Full	-	-	20	µV/°C
Bias Current		+25°C	-	2.5	5	µA
		Full	-	-	15	µA
Offset Current		+25°C	-1.5	-	+1.5	µA
		Full	-3	-	3	µA
Common Mode Range		Full	-2.5	-	+2.5	V
CMRR (±2.5V_{DC}) (Note 3)		+25°C	72	-	-	dB
		Full	-	-	-	dB
TRANSFER CHARACTERISTICS						
Gain, DC		+25°C	-	115	-	dB
Gain Bandwidth Product	C_H External = 0pF	+25°C	20	-	-	MHz
	C_H External = 5pF	+25°C	-	-	-	MHz
	C_H External = 10pF	+25°C	-	-	-	MHz
TRANSIENT RESPONSE						
Rise Time	(200mV Step)	+25°C	-	-	15	ns
Overshoot	(200mV Step)	+25°C	-	-	30	%
Slew Rate	(2.5V Step)	+25°C	100	130	-	V/µs
DIGITAL INPUT CHARACTERISTICS						
Input Voltage (High)	V_{IH}	Full	2.0	-	-	V
Input Voltage (Low)	V_{IL}	Full	-	-	0.8	V
Input Current V_{IL} = 0V	I_{IL}	Full	-10	-	10	µA
Input Current V_{IH} = 5V	I_{IH}	Full	-10	-	10	µA

Electrical Specifications Test Conditions (Unless Otherwise Specified) V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), R_L = 500Ω, C_L = 50pF **(Continued)**

PARAMETERS		TEMP	HA5352I LIMITS MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS						
Output Voltage		Full	-2.5	-	+2.5	V
Output Current Drive (100Ω to ±2.0V)		Full	-20	-	+20	mA
Full Power Bandwidth (Slew Rate Limited) (Note 4)		Full	-	8.5	-	MHz
Output Resistance - Hold Mode		+25°C	-	0.02	-	Ω
		Full	-	-	-	Ω
TOTAL OUTPUT NOISE, DC TO 10MHz						
Sample Mode		+25°C	-	325	-	μV_{RMS}
Hold Mode		+25°C	-	325	-	μV_{RMS}
DISTORTION CHARACTERISTICS						
SAMPLE MODE						
Signal to Noise Ratio (RMS Signal to RMS Noise)	V_{IN} = $5V_{P-P}$, F_{IN} = 1MHz	+25°C	-	-	-	dB
Total Harmonic Distortion	V_{IN} = $5V_{P-P}$, F_{IN} = 1MHz	+25°C	-70	-	-	dBc
	V_{IN} = $5V_{P-P}$, F_{IN} = 5MHz	+25°C	-	-	-	dBc
Intermodulation Distortion V_{IN} = $5V_{P-P}$	F1 = 200kHz, F2 = 201kHz	+25°C	-	-	-	dBc
HOLD MODE (50% Duty Cycle $\overline{S}$/H)						
Signal to Noise Ratio (RMS Signal to RMS Noise) Fs = 5MHz	V_{IN} = $5V_{P-P}$, F_{IN} = 1MHz	+25°C	-	-	-	dB
Total Harmonic Distortion Fs = 5MHz	V_{IN} = $5V_{P-P}$, F_{IN} = 1MHz	+25°C	-68	-	-	dBc
Fs = 5MHz	V_{IN} = $5V_{P-P}$, F_{IN} = 500kHz	+25°C	-	-	-	dBc
Fs = $2F_{IN}$(Nyquist)	V_{IN} = $5V_{P-P}$, F_{IN} = 200kHz	+25°C	-	-	-	dBc
	V_{IN} = $5V_{P-P}$, F_{IN} = 500kHz	+25°C	-	-	-	dBc
	V_{IN} = $5V_{P-P}$, F_{IN} = 1MHz	+25°C	-	-	-	dBc
Intermodulation Distortion Fs = 5MHz	V_{IN} = $5V_{P-P}$ (F1 = 200kHz, F2 = 201kHz)	+25°C	-	-	-	dBc
SAMPLE AND HOLD CHARACTERISTICS						
Acquisition Time	2.5V Step to ±1mV	+25°C	-	50	-	ns
		Full	-	-	-	ns
	2.5V Step to 0.01%	+25°C	-	85	100	ns
Droop Rate (C_H = Internal)		+25°C	-	0.1	-	V/ms
		Full	-1	-	1	V/ms
Hold Step Error (V_{IL} = 0V, V_{IH} = 4.0V, t_R = 5ns)		+25°C	-1.25	-	+1.25	mV

Electrical Specifications Test Conditions (Unless Otherwise Specified) V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), R_L = 500Ω, C_L = 50pF **(Continued)**

PARAMETERS	TEMP	HA5352I LIMITS			UNITS
		MIN	TYP	MAX	
SAMPLE AND HOLD CHARACTERISTICS (Continued)					
Hold Mode Settling Time (to ±1mV)	+25°C	-	30	-	ns
Hold Mode Feedthrough ($5V_{P-P}$, 500kHz, Sine)	+25°C	68	-	-	dB
EADT (Effective Aperture Delay Time)	+25°C	-	10	-	ns
Aperture Uncertainty	+25°C	-	10	-	ps
POWER SUPPLY CHARACTERISTICS					
Positive Supply Current (per Amp)	Full	-	20	22	mA
Negative Supply Current (per Amp)	Full	-	20	22	mA
PSRR (V+ or V-, 10% Delta)	Full	65	-	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Derived from Computer Simulation only, not tested.
3. +CMRR is measured from 0V to +2.5V, -CMRR is measured from 0V to -2.5V.
4. Based on the calculation FPBW = Slew Rate/$2\pi V_{PEAK}$ (V_{PEAK} = 2.5V).

LINEAR 5

DIFFERENTIAL AMPLIFIERS

Selection Guide

DIFFERENTIAL AMPLIFIERS: Typical Values, Unless Otherwise Specified.

TYPE	DESCRIPTION	FEATURES (NOTE 4)	FREQ. RANGE DC TO (MHz)	A (dB)	BW (3dB POINT) (MHz)	1/F NF (dB)	AGC RANGE (dB)	LEAD CT AND PKG TYPE*
CA3028A	Differential /Cascode Amplifiers	• Balanced differential amplifier configuration with controlled constant current source • RF, IF and video frequency capability • Balanced AGC capability • Operation from DC to 500MHz • CA3028B is controlled for input offset voltage, current, and input bias current, and is intended for "balance" requirements • Push-Pull inputs and outputs • CA3028 and CA3053 are identical except for 100MHz noise specification	120	40 (Note 1)	-	7.2	62	8E, 8M, 8S, 8T
CA3028B			120	40	8	7.2	62	
CA3049	Dual High Frequency		500	22	1.35 (Note 2)	53	75	12T
CA3053	Differential/Cascode Amplifier		120	40	Recommended for IF Amplifier Applications			8E, 8M, 8S, 8T
CA3054	Dual Independent		120	32	550 (Note 3)	3.25	75	14E, 14M
CA3102	Dual High Frequency		500	22	1.35 (Note 2)	1.5	7.5	14E, 14M

* See Packaging Information in Section 11.

NOTES:

1. G_P Min. at 100MHz; Cascode = 16dB; Differential Amplifier = 14dB.
2. GHz
3. f_T (MHz)
4. T_A Range: -55°C to +125°C except for type CA3054 (0°C to +85°C)

HARRIS SEMICONDUCTOR

CA3028, CA3053

Differential/Cascode Amplifiers for Commercial and Industrial Equipment from DC to 120MHz

March 1993

Features

- Controlled for Input Offset Voltage, Input Offset Current and Input Bias Current (CA3028 Series Only)
- Balanced Differential Amplifier Configuration with Controlled Constant Current Source
- Single-Ended and Dual-Ended Operation

Applications

- RF and IF Amplifiers (Differential or Cascode)
- DC, Audio and Sense Amplifiers
- Converter in the Commercial FM Band
- Oscillator
- Mixer
- Limiter
- Companion Application Note AN5337 "Application of the CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges." This note covers characteristics of different operating modes, noise performance, mixer, limiter, and amplifier design considerations

Description

The CA3028A and CA3028B are differential/cascode amplifiers designed for use in communications and industrial equipment operating at frequencies from DC to 120MHz.

The CA3028B is like the CA3028A but is capable of premium performance particularly in critical DC and differential amplifier applications requiring tight controls for input offset voltage, input offset current, and input bias current.

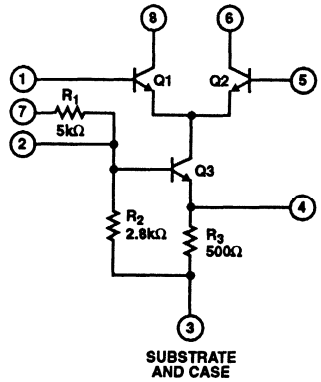
The CA3053 is similar to the CA3028A and CA3028B but is recommended for IF amplifier applications.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3028A	-55°C to +125°C	8 Pin CAN
CA3028AE	-55°C to +125°C	8 Lead Plastic DIP
CA3028AM	-55°C to +125°C	8 Lead SOIC
CA3028AM96	-55°C to +125°C	8 Lead SOIC*
CA3028B	-55°C to +125°C	8 Pin CAN
CA3028BE	-55°C to +125°C	8 Lead Plastic DIP
CA3028BM	-55°C to +125°C	8 Lead SOIC
CA3028BM96	-55°C to +125°C	8 Lead SOIC*
CA3053	-55°C to +125°C	8 Pin CAN
CA3053E	-55°C to +125°C	8 Lead Plastic DIP
CA3053M	-55°C to +125°C	8 Lead SOIC
CA3053M96	-55°C to +125°C	8 Lead SOIC*

* Denotes Tape and Reel

Schematic Diagram



5 DIFFERENTIAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 382.2

Absolute Maximum Ratings (T_A = +25°C)

Power Dissipation
- Up to T_A = +85°C 450mW
- Above T_A = +85°C ..... Derate Linearly 5mW/°C

Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -55°C ≤ T_A ≤ +125°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Maximum Voltage Ratings T_A = +25°C

The following chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal Terminal 4 with respect to Terminal 2 is -1V to +5V.

TERM NO.	1	2	3	4	5	6	7	8
1		0 to -15 (Note 3)	0 to -15 (Note 3)	0 to -15 (Note 3)	+5 to -5	Note 2	Note 2	+20 to 0 (Note 4)
2			+5 to -11	+5 to -1	+15 to 0 (Note 5)	Note 2	+15 to 0 (Note 5)	Note 2
3 (Note 1)				+10 to 0	+15 to 0 (Note 5)	+30 to 0 (Note 6)	+15 to 0 (Note 5)	+30 to 0 (Note 6)
4					+15 to 0 (Note 5)	Note 2	Note 2	Note 2
5						+20 to 0 (Note 4)	Note 2	Note 2
6							Note 2	Note 2
7								Note 2
8								

Maximum Current Ratings

TERM NO.	I_{IN} mA	I_{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

NOTES:
1. Terminal No. 3 is connected to the substrate and case.
2. Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.
3. Limit is -12V for CA3053.
4. Limit is +15V for CA3053.
5. Limit is +12V for CA3053.
6. Limit is +24V for CA3028A and +18V for CA3053.

Electrical Specifications T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS									UNIT
			CA3028A			CA3028B			CA3053			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
STATIC CHARACTERISTICS												
Input Offset Voltage (Figures 1, 14)	V_{IO}	V_{CC} = 6V, V_{EE} = -6V	-	-	-	-	0.98	5.0	-	-	-	mV
		V_{CC} = 12V, V_{EE} = -12V	-	-	-	-	0.89	5.0	-	-	-	mV
Input Offset Current (Figures 2, 14)	I_{IO}	V_{CC} = 6V, V_{EE} = -6V	-	-	-	-	0.56	5.0	-	-	-	µA
		V_{CC} = 12V, V_{EE} = -12V	-	-	-	-	1.06	6.0	-	-	-	µA
Input Bias Current (Figures 2, 3, 15, 16)	I_I	V_{CC} = 6V, V_{EE} = -6V	-	16.6	70	-	16.6	40	-	-	-	µA
		V_{CC} = 12V, V_{EE} = -12V	-	36	106	-	36	80	-	-	-	µA
		V_{CC} = 9V		-	-	-	-	-	-	29	85	µA
		V_{CC} = 12V	-	-	-	-	-	-	-	36	125	µA

Electrical Specifications T_A = +25°C **(Continued)**

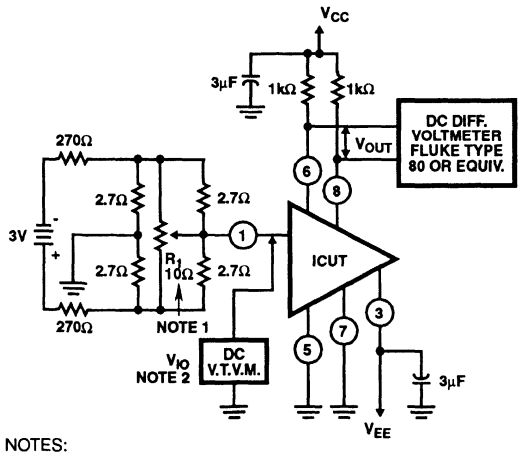
PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS CA3028A MIN	CA3028A TYP	CA3028A MAX	CA3028B MIN	CA3028B TYP	CA3028B MAX	CA3053 MIN	CA3053 TYP	CA3053 MAX	UNIT
STATIC CHARACTERISTICS (Continued)													
Quiescent Operating Current (Figures 2, 3, 17, 18, 19)	I_6, I_8	V_{CC} = 6V, V_{EE} = -6V		0.8	1.25	2.0	1.0	1.25	1.5	-	-	-	mA
		V_{CC} = 12V, V_{EE} = -12V		2.0	3.3	5.0	2.5	3.3	4.0	-	-	-	mA
		V_{CC} = 9V		-	-	-	-	-	-	1.2	2.2	3.5	mA
		V_{CC} = 12V		-	-	-	-	-	-	2.0	3.3	5.0	mA
AGC Bias Current (Into Constant Current Source Terminal 7) (Figures 4, 20)	I_7	V_{CC} = 12V, V_{AGC} = 9V		-	1.28	-	-	1.28	-	-	-	-	mA
		V_{CC} = 12V, V_{AGC} = 12V		-	1.65	-	-	1.65	-	-	-	-	mA
		V_{CC} = 9V		-	-	-	-	-	-	-	1.15	-	mA
		V_{CC} = 12V		-	-	-	-	-	-	-	1.55	-	mA
Input Current (Terminal 7)	I_7	V_{CC} = 6V, V_{EE} = -6V		0.5	0.85	1.0	0.5	0.85	1.0	-	-	-	mA
		V_{CC} = 12V, V_{EE} = -12V		1.0	1.65	2.1	1.0	1.65	2.1	-	-	-	mA
Power Dissipation (Figures 2, 3, 21)	P_T	V_{CC} = 6V, V_{EE} = -6V		24	36	54	24	36	42	-	-	-	mW
		V_{CC} = 12V, V_{EE} = -12V		120	175	260	120	175	220	-	-	-	mW
		V_{CC} = 9V		-	-	-	-	-	-	-	50	80	mW
		V_{CC} = 12V		-	-	-	-	-	-	-	100	150	mW
DYNAMIC CHARACTERISTICS													
Power Gain (Figures 5, 6, 7, 22, 24, 26)	G_P	f = 100MHz	Cascode	16	20	-	16	20	-	-	-	-	dB
		V_{CC} = 9V	Diff. Amp.	14	17	-	14	17	-	-	-	-	dB
		f = 10.7MHz	Cascode (Note 1)	35	39	-	35	39	-	35	39	-	dB
		V_{CC} = 9V	Diff. Amp. (Note 1)	28	32	-	28	32	-	28	32	-	dB
Noise Figure (Figures 5, 6, 7, 23, 25, 26)	NF	f = 100MHz, V_{CC} = 9V	Cascode	-	7.2	9.0	-	7.2	9.0	-	-	-	dB
			Diff. Amp.	-	6.7	9.0	-	6.7	9.0	-	-	-	dB
Input Admittance (Figures 27, 28)	Y_{11}	f = 10.7MHz, V_{CC} = 9V	Cascode	-	0.6 + j1.6	-	-	0.6 + j1.6	-	-	0.6 + j1.6	-	mmho
			Diff. Amp.	-	0.5 + j0.5	-	-	0.5 + j0.5	-	-	0.5 + j0.5	-	mmho
Reverse Transfer Admittance (Figures 29, 30)	Y_{12}	f = 10.7MHz, V_{CC} = 9V	Cascode	-	0.0003 - j0	-	-	0.0003 - j0	-	-	0.0003 - j0	-	mmho
			Diff. Amp.	-	0.01 - j0.0002	-	-	0.01 - j0.0002	-	-	0.01 - j0.0002	-	mmho
Forward Transfer Admittance (Figures 31, 32)	Y_{21}	f = 10.7MHz, V_{CC} = 9V	Cascode	-	99 - j18	-	-	99 - j18	-	-	99 - j18	-	mmho
			Diff. Amp.	-	-37 + j0.5	-	-	-37 + j0.5	-	-	-37 + j0.5	-	mmho
Output Admittance (Figures 33, 34)	Y_{22}	f = 10.7MHz, V_{CC} = 9V	Cascode	-	0 + j0.08	-	-	0 + j0.08	-	-	0 + j0.08	-	mmho
			Diff. Amp.	-	0.04 + j0.23	-	-	0.04 + j0.23	-	-	0.04 + j0.23	-	mmho
Output Power (Untuned) (Figures 8, 35)	P_O	f = 10.7MHz, V_{CC} = 9V	Diff. Amp., 50Ω Input-Output	-	5.7	-	-	5.7	-	-	-	-	µW
AGC Range (Maximum Power Gain to Full Cut-off) (Figures 9, 36)	AGC	f = 10.7MHz, V_{CC} = 9V	Diff. Amp.	-	62	-	-	62	-	-	-	-	dB
Voltage Gain (Figures 10, 11, 37, 38)	A	f = 10.7MHz, V_{CC} = 90V, R_L = 1kΩ	Cascode	-	40	-	-	40	-	-	40	-	dB
			Diff. Amp.	-	30	-	-	30	-	-	30	-	dB

Electrical Specifications T_A = +25°C **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS CA3028A MIN	CA3028A TYP	CA3028A MAX	CA3028B MIN	CA3028B TYP	CA3028B MAX	CA3053 MIN	CA3053 TYP	CA3053 MAX	UNIT
DYNAMIC CHARACTERISTICS (Continued)													
Differential Voltage Gain at f = 1kHz (Figure 12)	A	V_{CC} = 6V, V_{EE} = -6V, R_L = 2kΩ		-	-	-	35	38	42	-	-	-	dB
		V_{CC} = 12V, V_{EE} = -12V, R_L = 1.6kΩ		-	-	-	40	42.5	45	-	-	-	dB
Max. Peak-to-Peak Output Voltage at f = 1kHz (Figure 12)	V_O(P-P)	V_{CC} = 6V, V_{EE} = -6V, R_L = 2kΩ		-	-	-	7.0	11.5	-	-	-	-	V_{P-P}
		V_{CC} = 12V, V_{EE} = -12V, R_L = 1.6kΩ		-	-	-	15	23	-	-	-	-	V_{P-P}
Bandwidth at -3dB Point (Figure 12)	BW	V_{CC} = 6V, V_{EE} = -6V, R_L = 2kΩ		-	-	-	-	7.3	-	-	-	-	MHz
		V_{CC} = 12V, V_{EE} = -12V, R_L = 1.6kΩ		-	-	-	-	8.0	-	-	-	-	MHz
Common Mode Input Voltage Range (Figure 13)	V_{CMR}	V_{CC} = 6V, V_{EE} = -6V		-	-	-	-2.5	-3.2 to -4.5	4	-	-	-	V
		V_{CC} = 12V, V_{EE} = -12V		-	-	-	-5.0	-7 to -9	7	-	-	-	V
Common Mode Rejection Ratio (Figure 13)	CMRR	V_{CC} = 6V, V_{EE} = -6V		-	-	-	60	110	-	-	-	-	dB
		V_{CC} = 12V, V_{EE} = -12V		-	-	-	60	90	-	-	-	-	dB
Input Impedance at f = 1kHz	Z_{IN}	V_{CC} = 6V, V_{EE} = -6V		-	-	-	-	5.5	-	-	-	-	kΩ
		V_{CC} = 12V, V_{EE} = -12V		-	-	-	-	3.0	-	-	-	-	kΩ
Peak-to-Peak Output Current	I_{P-P}	f = 10.7MHz, e_{IN} = 400mV, Diff. Amp.	V_{CC} = 9V	2.0	4.0	7.0	2.5	4.0	6.0	2.0	4.0	7.0	mA
			V_{CC} = 12V	3.5	6.0	10	4.5	6.0	8.0	3.5	6.0	10	mA

NOTE: 1. Does not apply to CA3053.

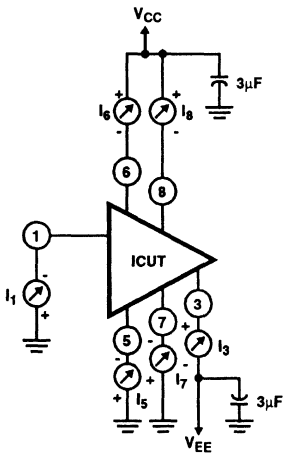
Test Circuits



NOTES:

1. Adjust R_1 for V_{OUT} = 0V ± 0.1V.
2. Record Input Offset Voltage.

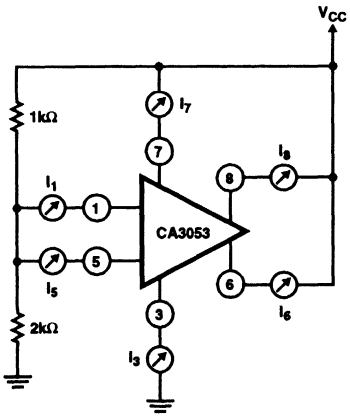
FIGURE 1. INPUT OFFSET VOLTAGE TEST CIRCUIT FOR CA3028B



NOTE: POWER DISSIPATION = $I_3V_{EE} + (I_6 + I_8)V_{CC}$

FIGURE 2. INPUT OFFSET CURRENT, INPUT BIAS CURRENT, POWER DISSIPATION, AND QUIESCENT OPERATING CURRENT TEST CIRCUIT FOR CA3028A AND CA3028B

Test Circuits (Continued)



NOTE: POWER DISSIPATION = $V_{CC} I_3$

FIGURE 3. INPUT BIAS CURRENT, POWER DISSIPATION AND QUIESCENT OPERATING CURRENT TEST CIRCUIT FOR CA3053

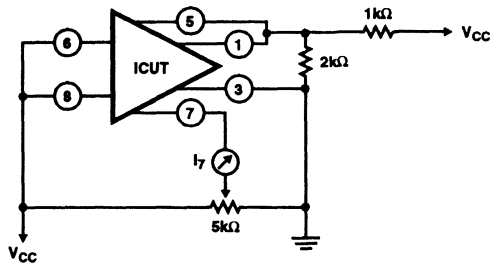
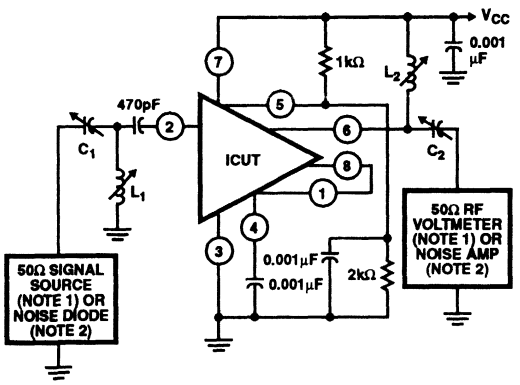


FIGURE 4. AGC BIAS CURRENT TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

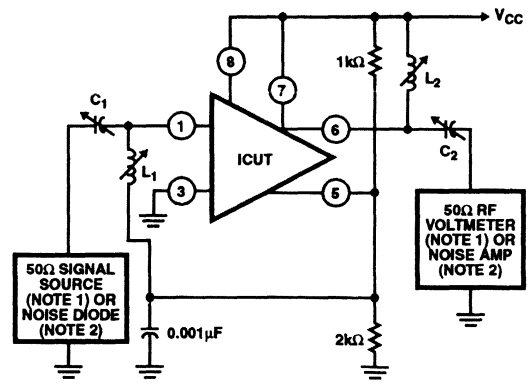


NOTES:

1. For Power Gain Test
2. For Noise Figure Test

f (MHz)	C_1 (pF)	C_2 (pF)	L_1 (µH)	L_2 (µH)
10.7	20 - 60	20 - 60	3 - 5	3 - 5
100	3 - 30	3 - 30	0.1 - 0.25	0.15 - 0.3

FIGURE 5. POWER GAIN AND NOISE FIGURE TEST CIRCUIT (CASCODE CONFIGURATION) FOR CA3028A, CA3028B AND CA3053*



NOTES:

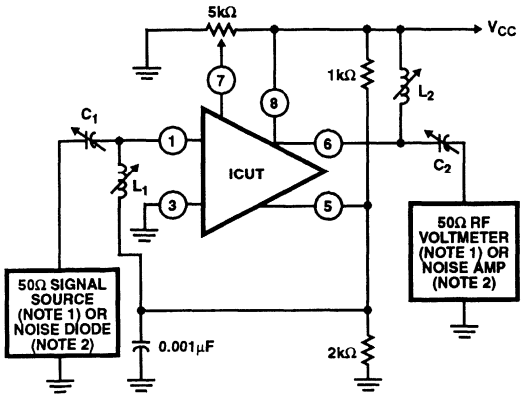
1. For Power Gain Test
2. For Noise Figure Test

f (MHz)	C_1 (pF)	C_2 (pF)	L_1 (µH)	L_2 (µH)
10.7	30 - 60	20 - 50	3 - 6	3 - 6
100	2 - 15	2 - 15	0.2 - 0.5	0.2 - 0.5

FIGURE 6. POWER GAIN AND NOISE FIGURE TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION AND TERMINAL 7 CONNECTED TO VCC) FOR CA3028A, CA3028B AND CA3053*

* 10.7MHz Power Gain Test Only

Test Circuits (Continued)



NOTES:

1. For Power Gain Test
2. For Noise Figure Test

f (MHz)	C_1 (pF)	C_2 (pF)	L_1 (μH)	L_2 (μH)
10.7	30 - 60	20 - 50	3 - 6	3 - 6
100	2 - 15	2 - 15	0.2 - 0.5	0.2 - 0.5

FIGURE 7. POWER GAIN AND NOISE FIGURE TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

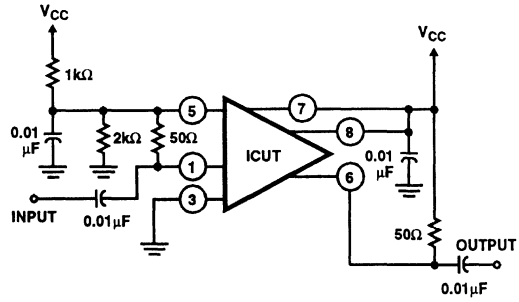
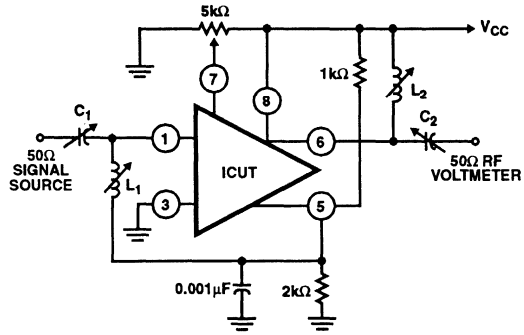


FIGURE 8. OUTPUT POWER TEST CIRCUIT FOR CA3028A AND CA3028B



f (MHz)	C_1 (pF)	C_2 (pF)	L_1 (μH)	L_2 (μH)
10.7	30 - 60	20 - 50	3 - 6	3 - 6
100	2 - 15	2 - 15	0.2 - 0.5	0.2 - 0.5

FIGURE 9. AGC RANGE TEST CIRCUIT (DIFFERENTIAL AMPLIFIER) FOR CA3028A AND CA3028B

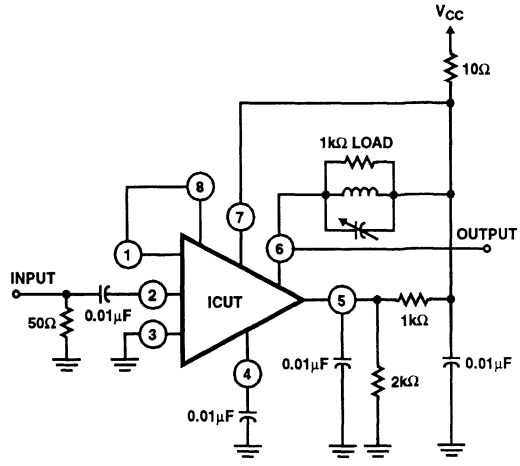


FIGURE 10. TRANSFER CHARACTERISTIC (VOLTAGE GAIN) TEST CIRCUIT (10.7MHz) CASCODE CONFIGURATION FOR CA3028A, CA3028B AND CA3053

Test Circuits (Continued)

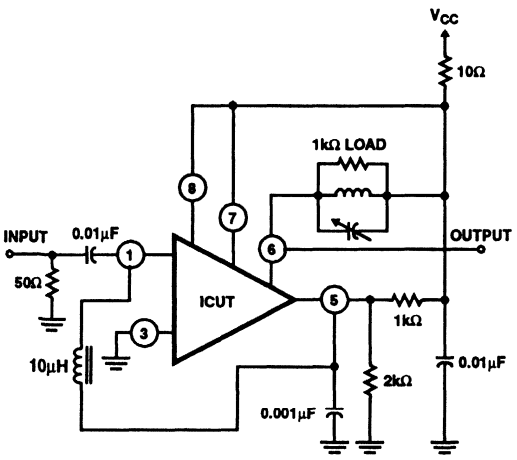
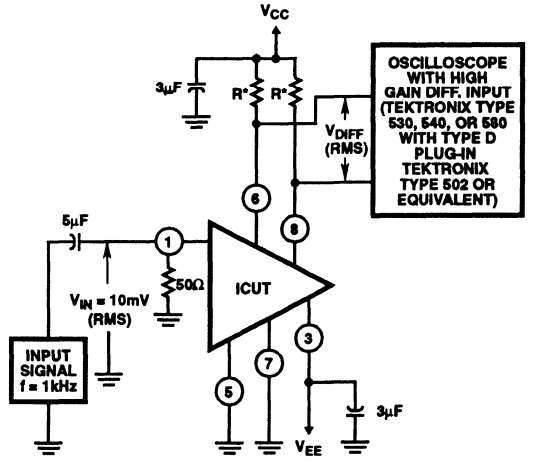
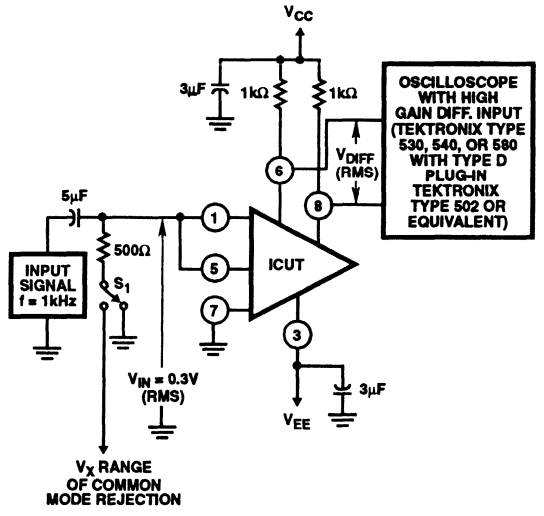


FIGURE 11. TRANSFER CHARACTERISTIC (VOLTAGE GAIN) TEST CIRCUIT (10.7MHz) DIFFERENTIAL AMPLIFIER CONFIGURATION FOR CA3028A, CA3028B AND CA3053



* For R = 1.6kΩ: V_{CC} = 12V, V_{EE} = -12V
For R = 2.0kΩ: V_{CC} = 6V, V_{EE} = -6V

FIGURE 12. DIFFERENTIAL VOLTAGE GAIN, MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AND BANDWIDTH TEST CIRCUIT FOR CA3028B



NOTES:

1. For CMR test: S_1 to GND.
2. For Input Common Mode Voltage Range Test: S_1 to V_X.
3. Common Mode Rejection Ratio $= 20\log_{10}\frac{(A^*)\ (2)\ (0.3)}{V_{DIFF}\ (RMS)}$

* A = Single-Ended Voltage Gain.

FIGURE 13. COMMON MODE REJECTION RATIO AND COMMON MODE INPUT VOLTAGE RANGE TEST CIRCUIT FOR CA3028B

Typical Performance Curves

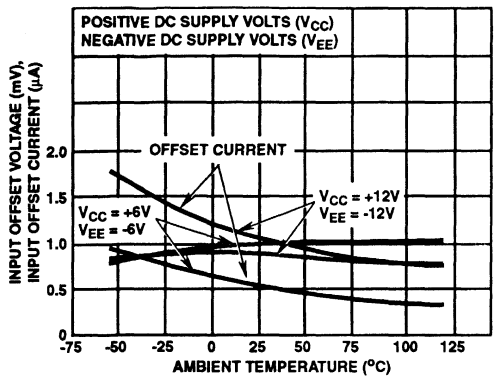


FIGURE 14. INPUT OFFSET VOLTAGE AND INPUT OFFSET CURRENT FOR CA3028B vs TEMPERATURE

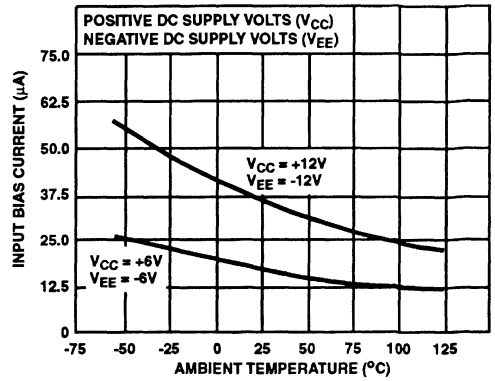


FIGURE 15. INPUT BIAS CURRENT vs TEMPERATURE FOR CA3028A AND CA3028B

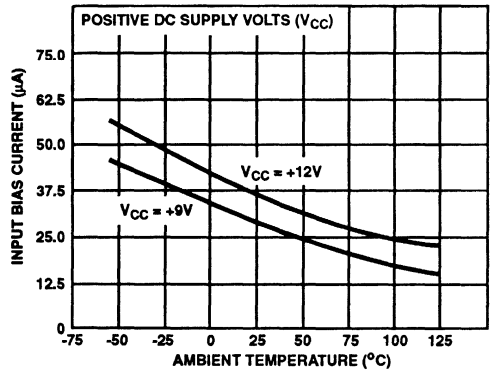


FIGURE 16. INPUT BIAS CURRENT vs TEMPERATURE FOR CA3053

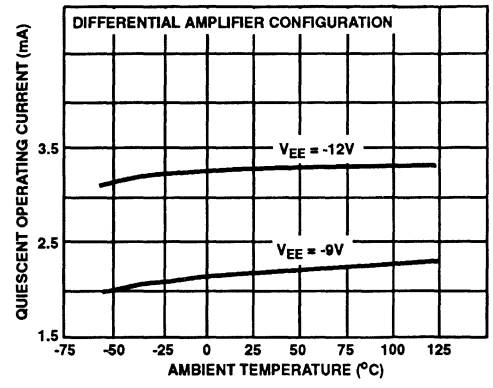


FIGURE 17. QUIESCENT OPERATING CURRENT vs TEMPERATURE FOR CA3028A AND CA3028B

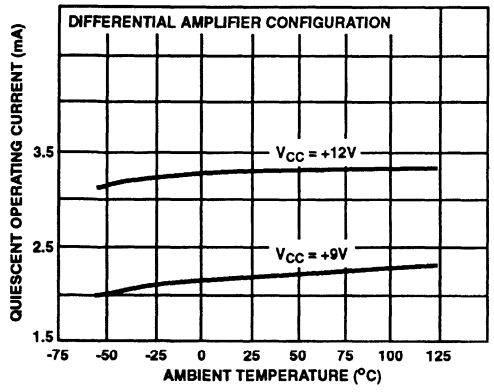


FIGURE 18. QUIESCENT OPERATING CURRENT vs TEMPERATURE FOR CA3053

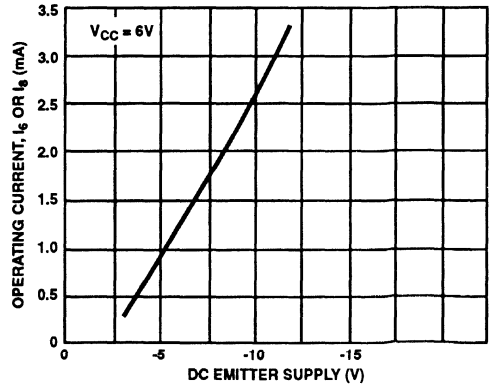


FIGURE 19. OPERATING CURRENT vs V_{EE} VOLTAGE FOR CA3028A AND CA3028B

Typical Performance Curves (Continued)

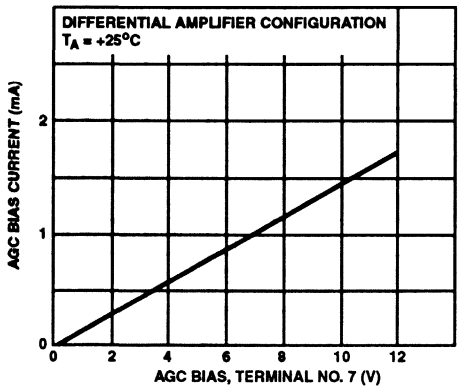


FIGURE 20. AGC BIAS CURRENT vs BIAS VOLTAGE (TERMINAL 7) FOR CA3028A AND CA3028B

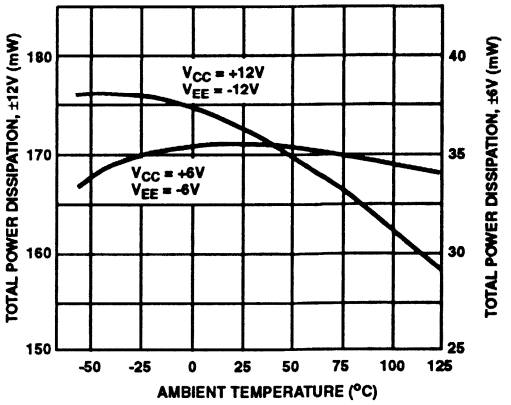


FIGURE 21. POWER DISSIPATION vs TEMPERATURE FOR CA3028A AND CA3028B

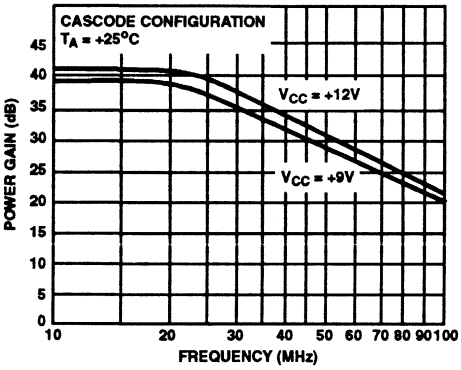


FIGURE 22. POWER GAIN vs FREQUENCY (CASCODE CONFIGURATION) FOR CA3028A AND CA3028B

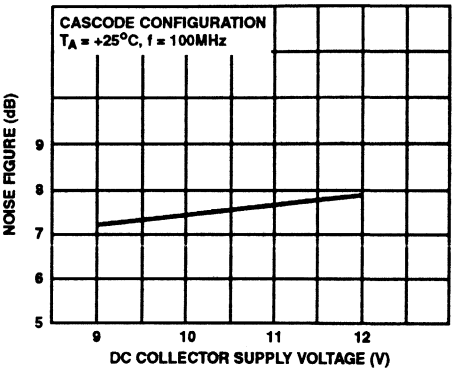


FIGURE 23. 100MHz NOISE FIGURE vs COLLECTOR SUPPLY VOLTAGE (CASCODE CONFIGURATION) FOR CA3028A AND CA3028B

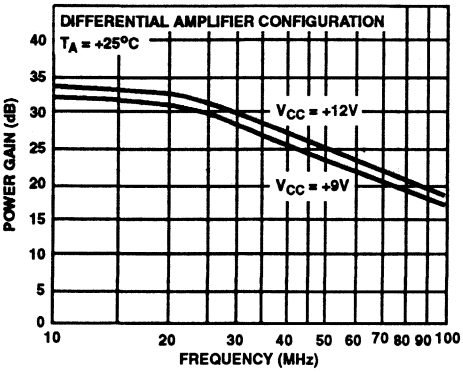


FIGURE 24. POWER GAIN vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

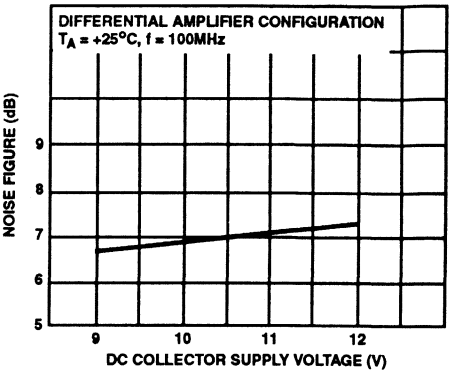


FIGURE 25. 100MHz NOISE FIGURE vs COLLECTOR SUPPLY VOLTAGE (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

Typical Performance Curves (Continued)

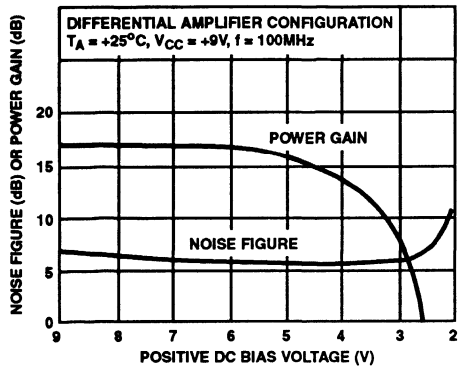


FIGURE 26. 100MHz NOISE FIGURE AND POWER GAIN vs BASE-TO-EMITTER BIAS VOLTAGE (TERMINAL 7) FOR CA3028A AND CA3028B

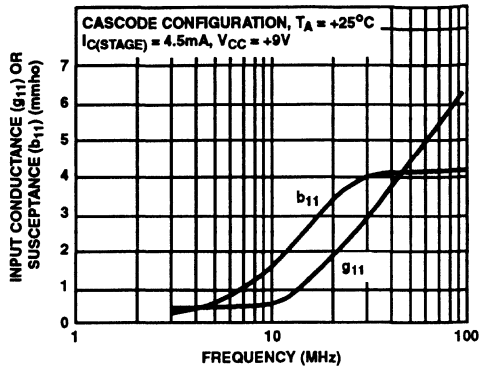


FIGURE 27. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY (CASCODE CONFIGURATION)

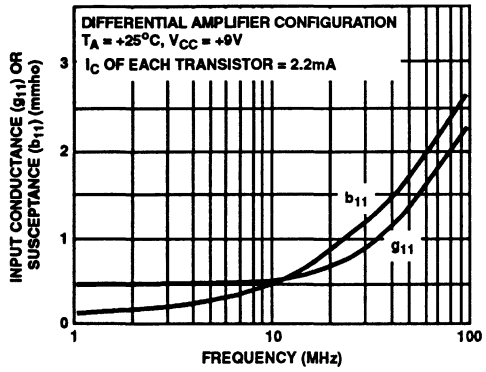


FIGURE 28. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION)

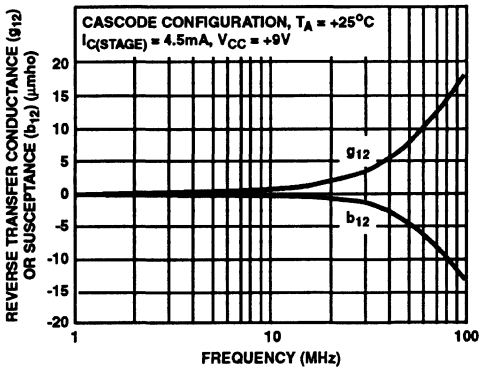


FIGURE 29. REVERSE TRANSADMITTANCE (Y_{12}) vs FREQUENCY (CASCODE CONFIGURATION)

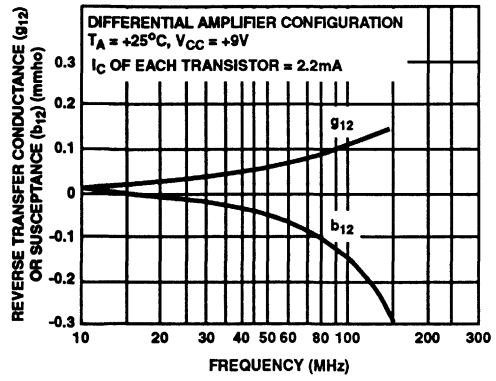


FIGURE 30. REVERSE TRANSADMITTANCE (Y_{12}) vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION)

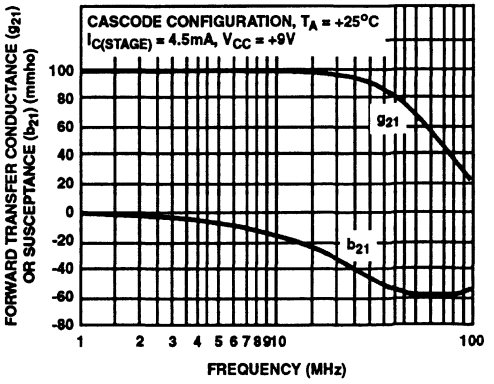


FIGURE 31. FORWARD TRANSADMITTANCE (Y_{21}) vs FREQUENCY (CASCODE CONFIGURATION)

Typical Performance Curves (Continued)

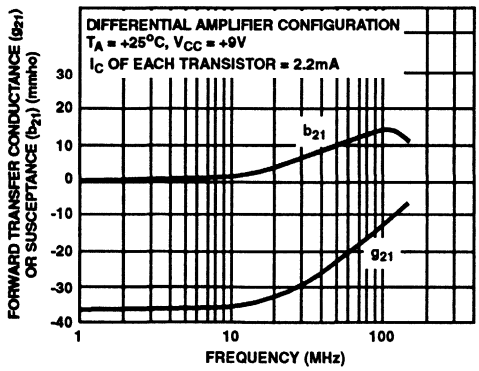


FIGURE 32. FORWARD TRANSADMITTANCE (Y_{21}) vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION)

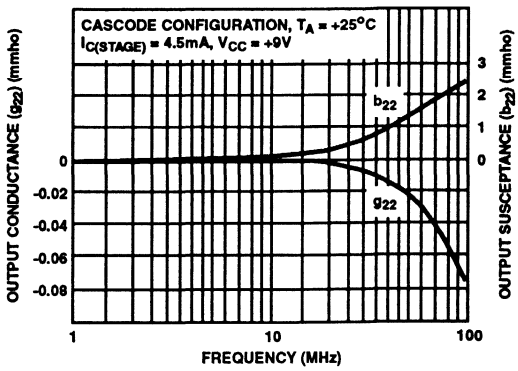


FIGURE 33. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY (CASCODE CONFIGURATION)

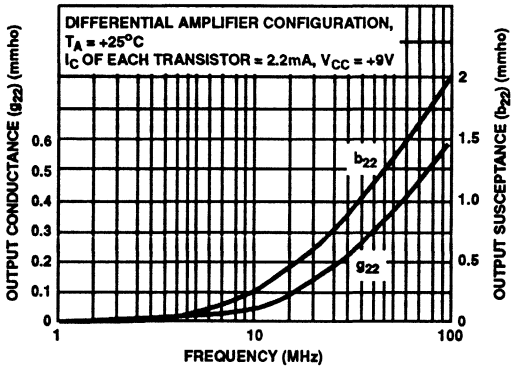


FIGURE 34. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION)

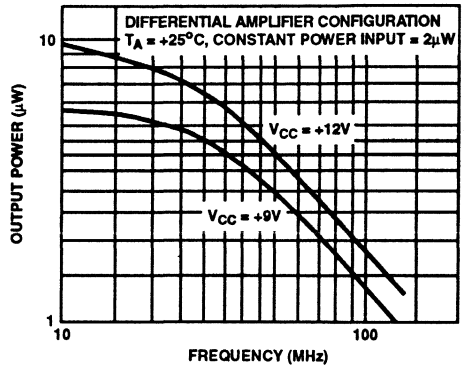


FIGURE 35. OUTPUT POWER vs FREQUENCY - 50Ω INPUT AND 50Ω OUTPUT (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

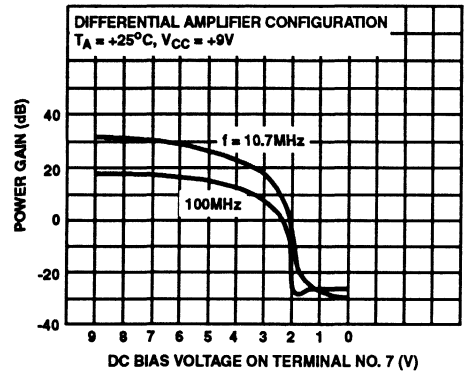


FIGURE 36. AGC CHARACTERISTICS FOR CA3028A AND CA3028B

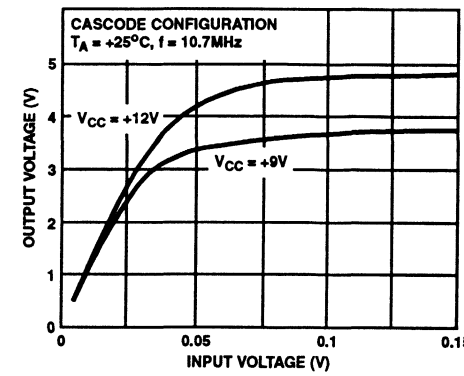


FIGURE 37. TRANSFER CHARACTERISTICS (CASCODE CONFIGURATION)

Typical Performance Curves (Continued)

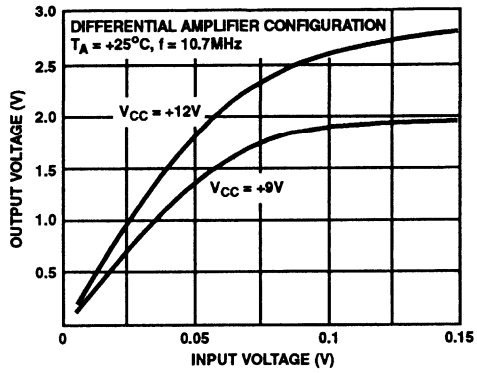


FIGURE 38. TRANSFER CHARACTERISTICS (DIFFERENTIAL AMPLIFIER CONFIGURATION)

Glossary of Terms

AGC Bias Current

The current drawn by the device from the AGC voltage source, at maximum AGC voltage.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device.

Common Mode Rejection Ratio

The ratio of the full differential voltage gain to the common mode voltage gain.

Power Dissipation

The total power drain of the device with no signal applied and no external load current.

Input Bias Current

The average value (one half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Offset Current

The difference in the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Offset Voltage

The difference in the dc voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

Noise Figure

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

Power Gain

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

Quiescent Operating Current

The average (dc) value of the current in either output terminal.

Voltage Gain

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at ac ground.

HARRIS SEMICONDUCTOR

CA3049, CA3102

Dual High Frequency Differential Amplifiers For Low Power Applications Up to 500MHz

March 1993

Features

- Power Gain 23dB (Typ) 200MHz
- Noise Figure 4.6dB (Typ)..... 200MHz
- Two Differential Amplifiers on a Common Substrate
- Independently Accessible Inputs and Outputs
- Full Military Temperature Range .... -55°C to +125°C

Applications

- VHF Amplifiers
- VHF Mixers
- Multifunction Combinations - RF/Mixer/Oscillator; Converter/IF
- IF Amplifiers (Differential and/or Cascode)
- Product Detectors
- Doubly Balanced Modulators and Demodulators
- Balanced Quadrature Detectors
- Cascade Limiters
- Synchronous Detectors
- Balanced Mixers
- Synthesizers
- Balanced (Push-Pull) Cascode Amplifiers
- Sense Amplifiers

Description

The CA3049T and CA3102* consist of two independent differential amplifiers with associated constant current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general purpose devices which exhibit low 1/F noise and a value of f_T in excess of 1GHz. These feature make the CA3049T and CA3102 useful from DC to 500MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3049T and CA3102 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual channel applications where matched performance of the two channels is required.

The CA3102 is like the CA3049T except that it has a separate substrate connection for greater design flexibility.

* Formerly Developmental No. TA6228.

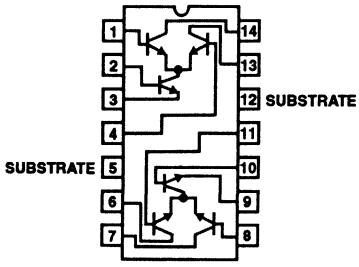
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3049T	-55°C to +125°C	12 Pin CAN
CA3102E	-55°C to +125°C	14 Lead Plastic DIP
CA3102E5	-55°C to +125°C	14 Lead Plastic DIP
CA3102M	-55°C to +125°C	14 Lead SOIC
CA3102M96	-55°C to +125°C	14 Lead SOIC*

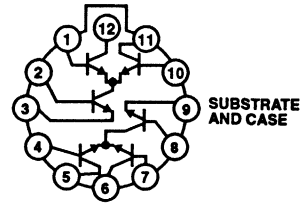
* Denotes Tape and Reel

Pinouts

CA3102
(PDIP, SOIC)
TOP VIEW



CA3049
(TO-5 CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 611.2

Absolute Maximum Ratings (T_A = +25°C)

Collector-to-Emitter Voltage, V_{CEO} 15V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
Emitter-to-Base Voltage, V_{EBO} 5V
Collector Current, I_C 50mA
Power Dissipation
  Any One Transistor (CA3049T and CA3102) 300mW
  Total Package
    CA3049T 600mW
    CA3102E 750mW
  For T_A > +55°C
    CA3049T ..... Derate Linearly 5.0mW/°C
    CA3102E ..... Derate Linearly 6.67mW/°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -55°C ≤ T_A ≤ +125°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS CA3102			LIMITS CA3049			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC CHARACTERISTICS									
For Each Differential Amplifier									
Input Offset Voltage (Figures 1, 4)	V_{IO}		-	0.25	5.0	-	0.25	-	mV
Input Offset Current (Figure 1)	I_{IO}	$I_3 = I_9$ = 2mA	-	0.3	3.0	-	0.3	-	µA
Input Bias Current (Figures 1, 5)	I_B		-	13.5	33	-	13.5	33	µA
Temperature Coefficient Magnitude of Input Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		-	1.1	-	-	1.1	-	µV/°C
For Each Transistor									
DC Forward Base-to-Emitter Voltage (Figure 6)	VBE	V_{CE} = 6V, I_C = 1mA	674	774	874	-	774	-	mV
Temperature Coefficient of Base-to-Emitter Voltage (Figure 6)	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 6V, I_C = 1mA	-	-0.9	-	-	-0.9	-	mV/°C
Collector Cutoff Current (Figure 7)	I_{CBO}	V_{CB} = 10V, I_E = 0	-	0.0013	100	-	0.0013	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	15	24	-	15	24	-	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10µA, I_E = 0	20	60	-	20	60	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10µA, $I_B = I_E$ = 0	20	60	-	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10µA, I_C = 0	5	7	-	5	7	-	V
DYNAMIC CHARACTERISTICS									
1/f Noise Figure (For Single Transistor) (Figure 12)	NF	f = 100kHz, R_S = 500Ω, I_C = 1mA	-	1.5	-	-	1.5	-	dB
Gain Bandwidth Product (For Single Transistor) (Figure 11)	f_T	V_{CE} = 6V, I_C = 5mA	-	1.35	-	-	1.35	-	GHz
Collector-Base Capacitance (Figure 8)	C_{CB}	I_C = 0, V_{CB} = 5V, Note 2	-	0.28	-	-	0.28	-	pF
		I_C = 0, V_{CB} = 5V, Note 3	-	0.15	-	-	0.28	-	pF
Collector-Substrate Capacitance (Figure 8)	C_{CI}	I_C = 0, V_{CI} = 5V	-	1.65	-	-	1.65	-	pF

Electrical Specifications T_A = +25°C **(Continued)**

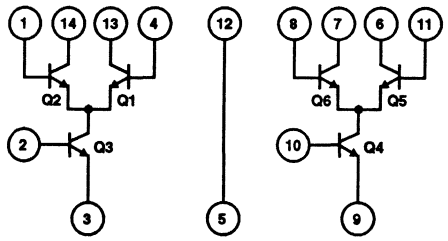
PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS CA3102 MIN	LIMITS CA3102 TYP	LIMITS CA3102 MAX	LIMITS CA3049 MIN	LIMITS CA3049 TYP	LIMITS CA3049 MAX	UNIT
DYNAMIC CHARACTERISTICS (Continued)										
For Each Differential Amplifier										
Common Mode Rejection Ratio	CMRR	$I_3 = I_9$ = 2mA		-	100	-	-	100	-	dB
AGC Range, One Stage (Figure 2)	AGC	Bias Voltage = -6V		-	75	-	-	75	-	dB
Voltage Gain, Single-Ended Output (Figures 2, 9, 10)	A	Bias Voltage = -4.2V, f = 10MHz		18	22	-	-	22	-	dB
Insertion Power Gain (Figure 3)	G_P	V_{CC} = 12V, For Cascode Configuration $I_3 = I_9$ = 2mA. For Diff. Amp. Confiugration $I_3 = I_9$ = 4mA (each collector $I_C \cong$ 2mA) f = 200MHz	Cascode	-	23	-	-	23	-	dB
Noise Figure (Figure 3)	NF		Cascode	-	4.6	-	-	4.6	-	dB
Input Admittance	Y_{11}		Cascode (Figures 14, 16, 18)	-	1.5 + j2.45	-	-	1.5 + j2.45	-	mmho
			Diff. Amp. (Figures 15, 17, 19)	-	0.878 + j1.3	-	-	0.878 + j1.3	-	mmho
Reverse Transfer Admittance	Y_{12}		Cascode	-	0.0 - j0.008	-	-	0.0 - j0.008	-	mmho
			Diff. Amp.	-	0.0 - j0.013	-	-	0.0 - j0.013	-	mmho
Forward Transfer Admittance	Y_{21}		Cascode (Figures 26, 28, 30)	-	17.9 - j30.7	-	-	17.9 - j30.7	-	mmho
			Diff. Amp. (Figures 27, 29, 31)	-	-10.5 + j13	-	-	-10.5 + j13	-	mmho
Output Admittance	Y_{22}		Cascode (Figures 20, 22, 24)	-	-0.503 - j15	-	-	-0.503 - j15	-	mmho
			Diff. Amp. (Figures 21, 23, 25)	-	0.071 + j0.62	-	-	0.071 + j0.62	-	mmho

NOTES:

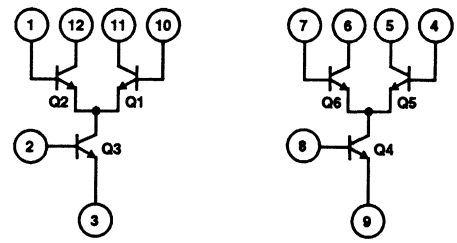
1. The collector of each transistor of the CA3049T and CA3102 is isolated from the substrate by an integral diode. The substrate (Terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. Terminals 1 and 14 or 7 and 8 (CA3102). Terminals 1 and 12 or 6 and 7 (CA3049T)
3. Terminals 13 and 4 or 6 and 11 (CA3102). Terminals 10 and 11 or 4 and 5 (CA3049T)

Schematic Diagrams

CA3102E, CA3102M



CA3049T



Test Circuits

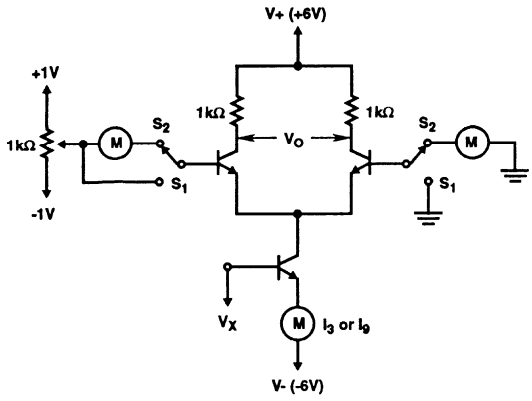


FIGURE 1. STATIC CHARACTERISTICS TEST CIRCUIT FOR CA3102

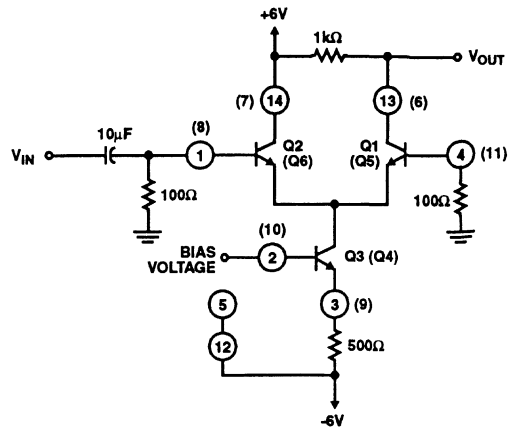
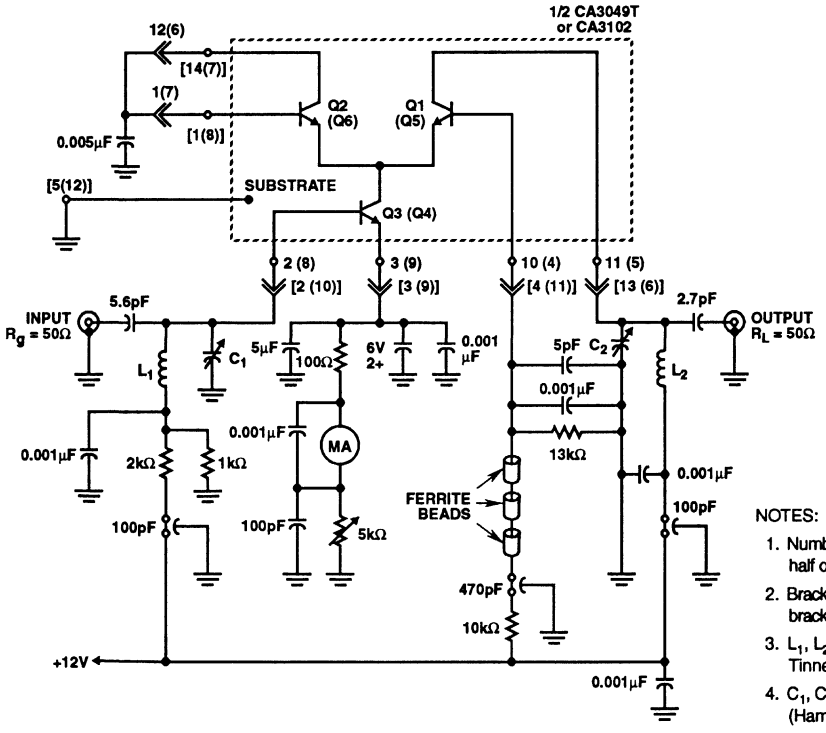


FIGURE 2. AGC RANGE AND VOLTAGE GAIN TEST CIRCUIT FOR CA3102



NOTES:

1. Numbers in parentheses refer to other half of the CA3049T or CA3102
2. Bracketed numbers refer to CA3102, unbracketed numbers refer to CA3049T
3. L_1, L_2 - Approximately $^1/_2$ Turn #18 Tinned Copper Wire, 5/8" Diameter
4. C_1, C_2 - 15pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent)

FIGURE 3. 200MHz CASCODE POWER GAIN AND NOISE FIGURE TEST CIRCUIT

Typical Performance Curves

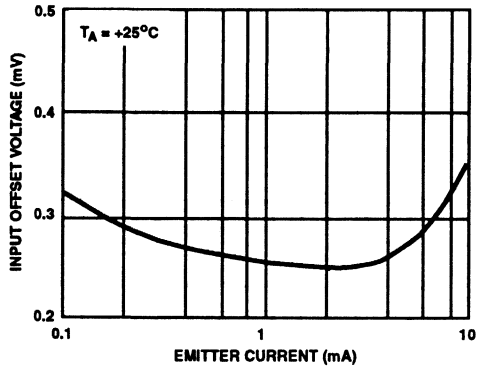


FIGURE 4. INPUT OFFSET VOLTAGE vs EMITTER CURRENT

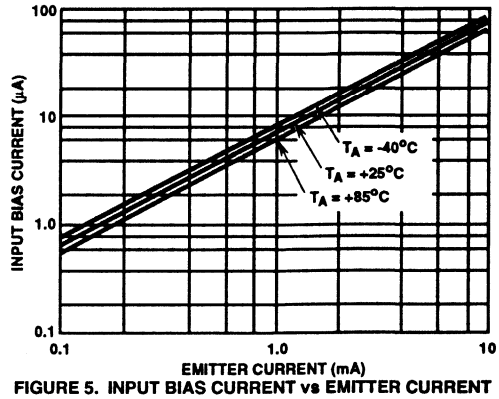


FIGURE 5. INPUT BIAS CURRENT vs EMITTER CURRENT

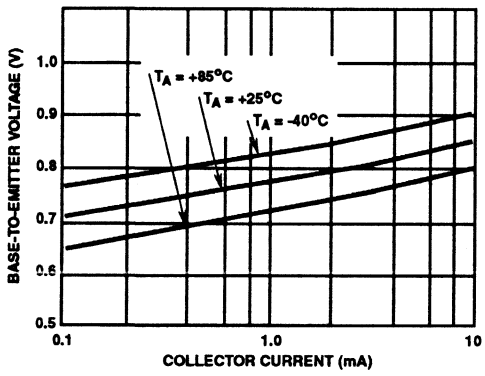


FIGURE 6. BASE-TO-EMITTER VOLTAGE vs COLLECTOR CURRENT

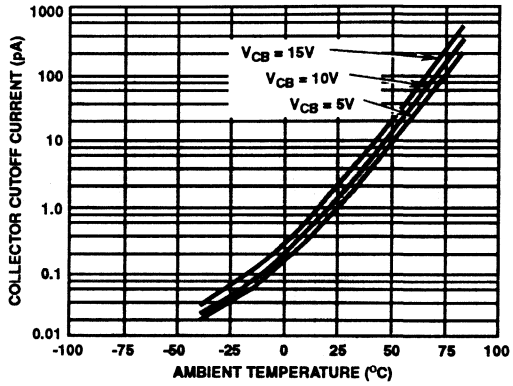


FIGURE 7. COLLECTOR CUTOFF CURRENT vs TEMPERATURE

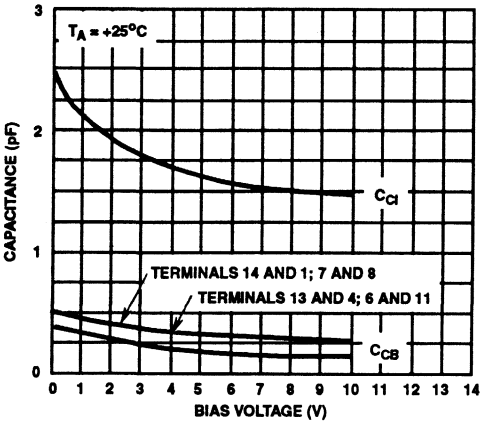


FIGURE 8. CAPACITANCE vs DC BIAS VOLTAGE

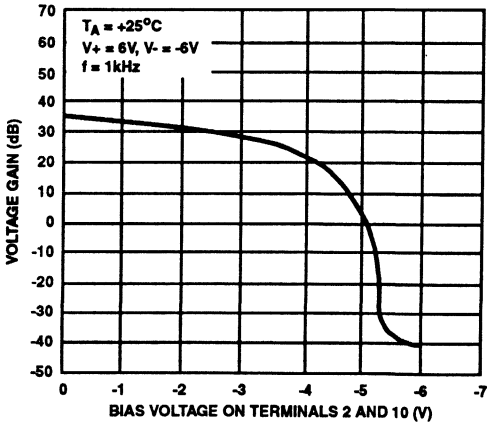


FIGURE 9. VOLTAGE GAIN vs DC BIAS VOLTAGE

Typical Performance Curves (Continued)

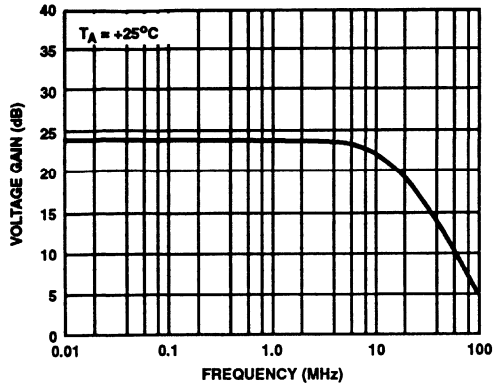


FIGURE 10. VOLTAGE GAIN vs FREQUENCY

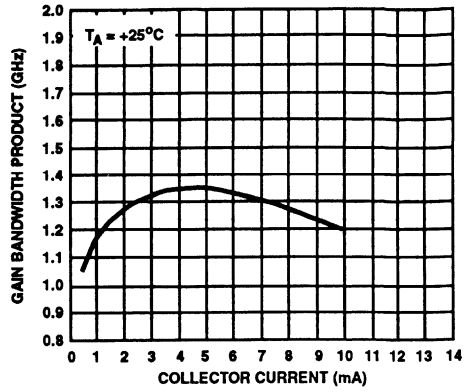


FIGURE 11. GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT

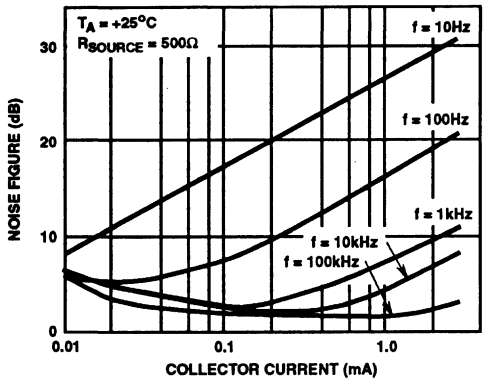


FIGURE 12. 1/f NOISE FIGURE vs COLLECTOR CURRENT

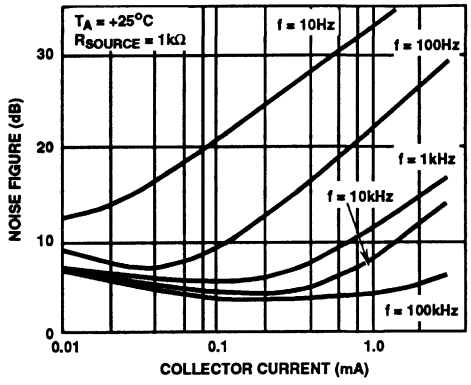


FIGURE 13. 1/f NOISE FIGURE vs COLLECTOR CURRENT

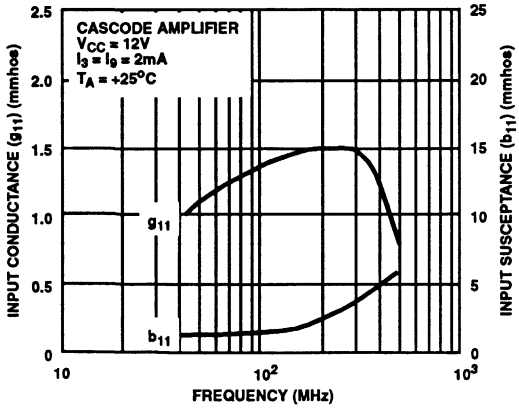


FIGURE 14. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY

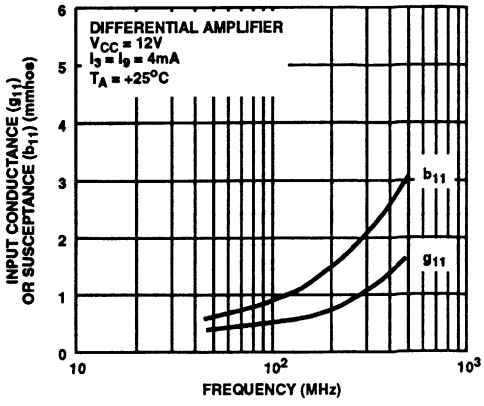


FIGURE 15. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY

Typical Performance Curves (Continued)

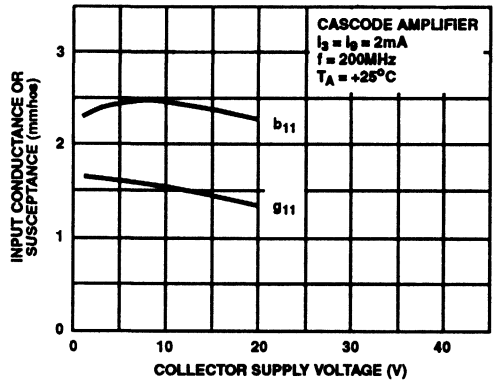


FIGURE 16. INPUT ADMITTANCE (Y_{11}) vs COLLECTOR SUPPLY VOLTAGE

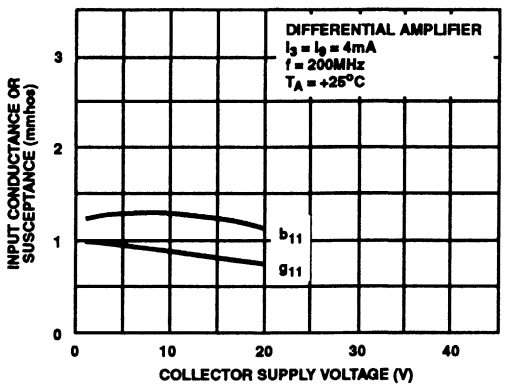


FIGURE 17. INPUT ADMITTANCE (Y_{11}) vs COLLECTOR SUPPLY VOLTAGE

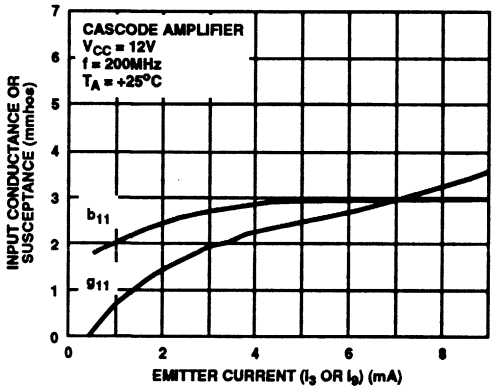


FIGURE 18. INPUT ADMITTANCE (Y_{11}) vs EMITTER CURRENT

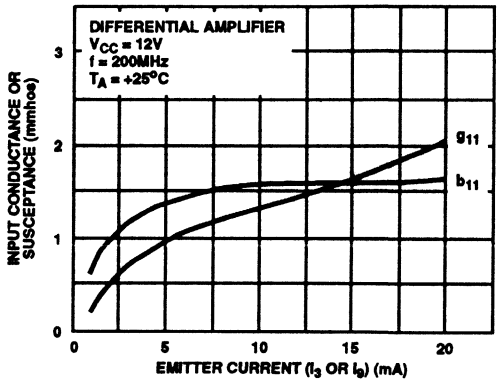


FIGURE 19. INPUT ADMITTANCE (Y_{11}) vs EMITTER CURRENT

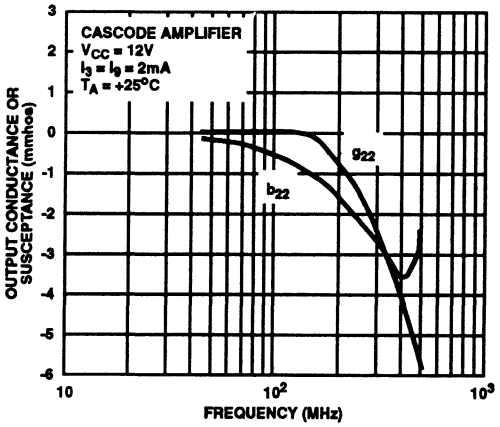


FIGURE 20. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

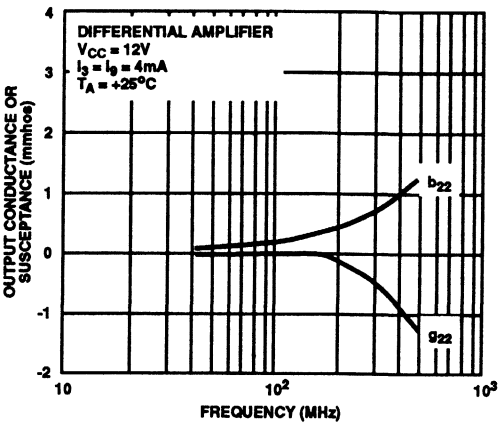


FIGURE 21. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

Typical Performance Curves (Continued)

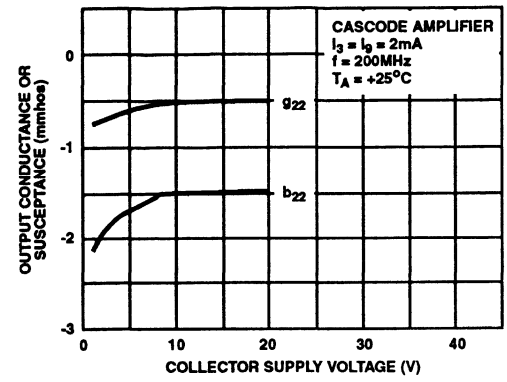


FIGURE 22. OUTPUT ADMITTANCE (Y_{22}) vs COLLECTOR SUPPLY VOLTAGE

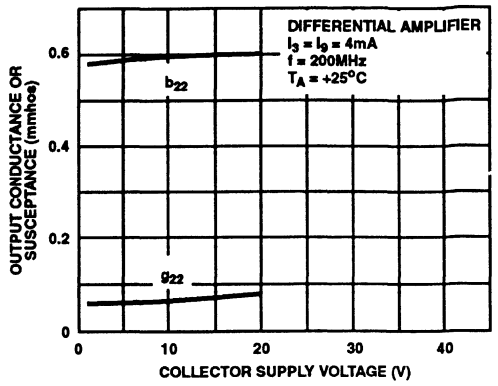


FIGURE 23. OUTPUT ADMITTANCE (Y_{22}) vs COLLECTOR SUPPLY VOLTAGE

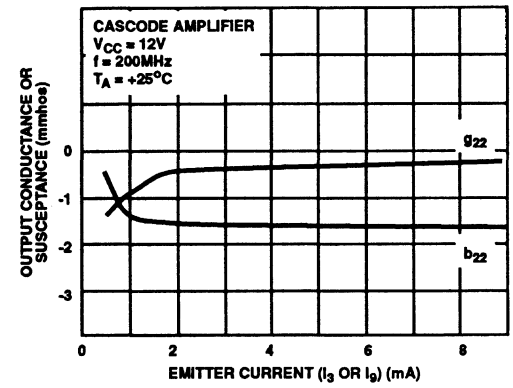


FIGURE 24. OUTPUT ADMITTANCE (Y_{22}) vs EMITTER CURRENT

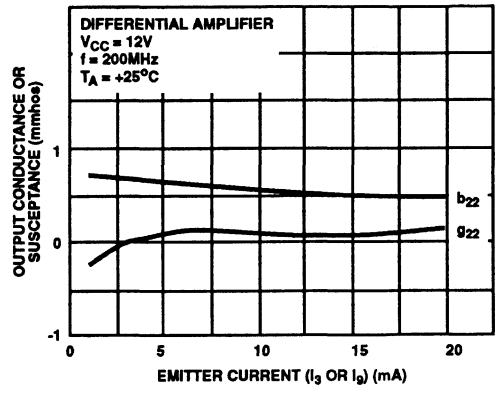


FIGURE 25. OUTPUT ADMITTANCE (Y_{22}) vs EMITTER CURRENT

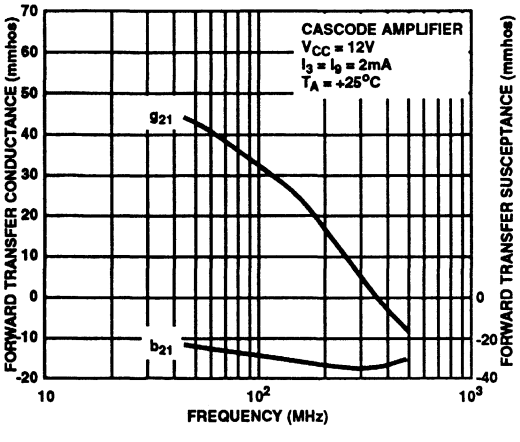


FIGURE 26. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs FREQUENCY

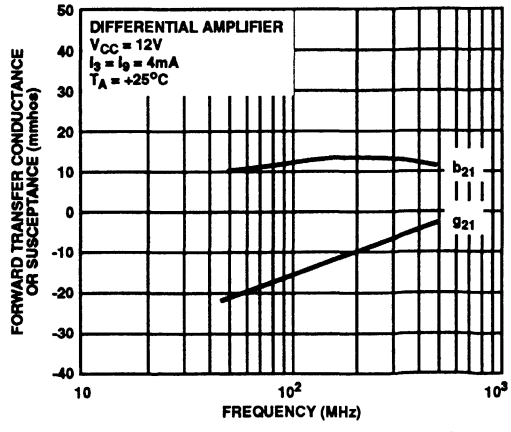


FIGURE 27. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs FREQUENCY

Typical Performance Curves (Continued)

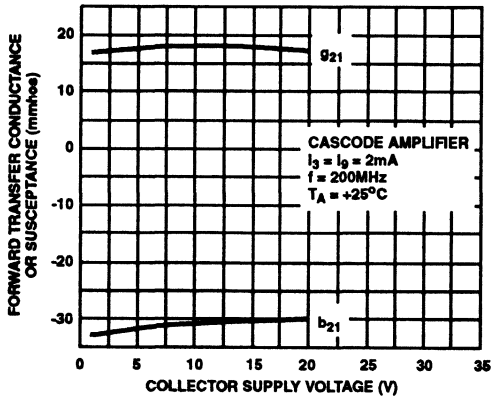


FIGURE 28. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs COLLECTOR SUPPLY VOLTAGE

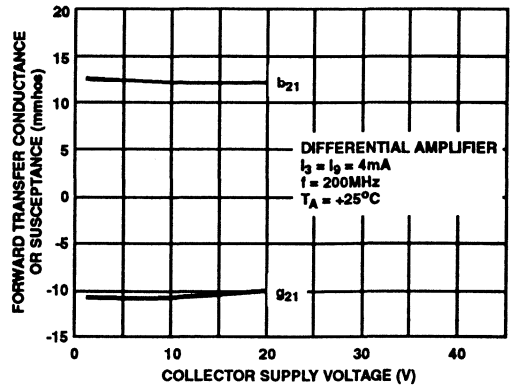


FIGURE 29. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs COLLECTOR SUPPLY VOLTAGE

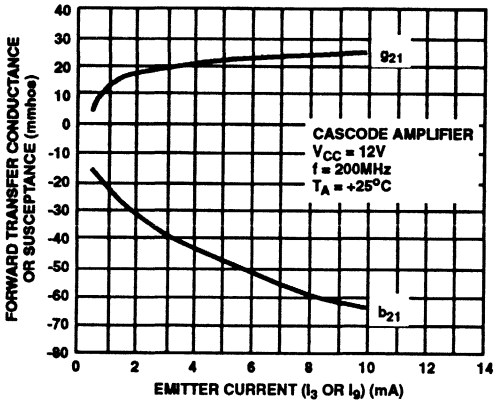


FIGURE 30. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs EMITTER CURRENT

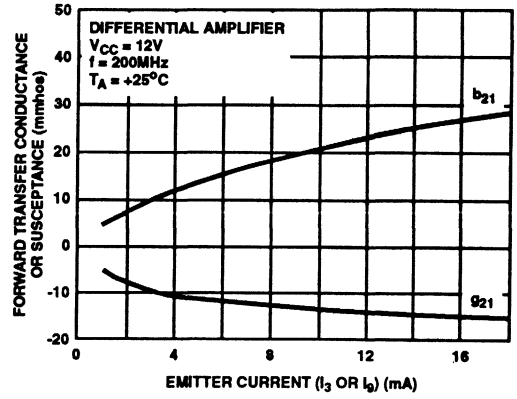


FIGURE 31. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs EMITTER CURRENT

HARRIS SEMICONDUCTOR

CA3054

Transistor Array - Dual Independent Differential Amp for Low Power Applications from DC to 120MHz

March 1993

Features

- Two Differential Amplifiers on a Common Substrate
- Independently Accessible Inputs and Outputs
- Maximum Input Offset Voltage..... ±5mV
- Temperature Range..... 0°C to +85°C

Applications

- Dual Sense Amplifiers
- Dual Schmitt Triggers
- Multifunction Combinations
  - RF/Mixer/Oscillator; Converter/IF
- IF Amplifiers (Differential and/or Cascode)
- Product Detectors
- Doubly Balanced Modulators and Demodulators
- Balanced Quadrature Detectors
- Cascade Limiters
- Synchronous Detectors
- Pairs of Balanced Mixers
- Synthesizer Mixers
- Balanced (Push-Pull) Cascode Amplifiers

Description

The CA3054 consists of two independent differential amplifiers with associated constant current transistors on a common monolithic substrate. The six n-p-n transistors which comprise the amplifiers are general purpose devices which exhibit low 1/f noise and a value of f_T in excess of 300MHz. These feature make the CA3054 useful from DC to 120MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual channel applications where matched performance of the two channels is required.

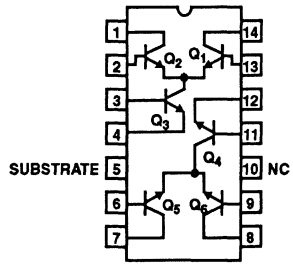
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3054	0°C to +85°C	14 Lead Plastic DIP
CA3054M	0°C to +85°C	14 Lead SOIC
CA3054M96	0°C to +85°C	14 Lead SOIC*

* Denotes Tape and Reel

Pinout

CA3054
(PDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Collector-to-Emitter Voltage, V_{CEO} 15V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
Emitter-to-Base Voltage, V_{EBO} 5V
Collector Current, I_C 50mA
Power Dissipation
Any One Transistor 300mW
Total Package 750mW
For T_A = +55°C ..... Derate Linearly 6.67mW/°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... $0°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

NOTE:

1. The collector of each transistor of the CA3054 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical Terminal 2 with respect to Terminal 4 is +15V to -5V.

TERM NO.*	13	14	1	2	3	4	6	7	8	9	11	12	5
13		0, -20	Note 1	+5, -5	Note 1	+15, -5	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1
14			Note 1	Note 1	Note 1	+20, 0	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	+20, 0
1				+20, 0	Note 1	+20, 0	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	+20, 0
2					Note 1	+15, -5	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1
3						+1, -5	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1
4							Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1
6								0, -20	Note 1	+5, -5	Note 1	+15, -5	Note 1
7									Note 1	Note 1	Note 1	Note 1	+20, 0
8										+20, 0	Note 1	Note 1	+20, 0
9											Note 1	+15, -5	Note 1
11												-1, -5	Note 1
12													Note 1
5													Ref. Sub-strate

NOTES:

1. Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Maximum Current Ratings

TERM NO.*	I_{IN} mA	I_{OUT} mA
13	5	0.1
14	50	0.1
1	50	0.1
2	5	0.1
3	5	0.1
4	0.1	50
6	5	0.1
7	50	0.1
8	50	0.1
9	5	0.1
11	5	0.1
12	0.1	50

* Terminal No. 10 of CA3054 is not used.

Electrical Specifications T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC CHARACTERISTICS						
For Each Differential Amplifier						
Input Offset Voltage (Figure 8)	V_{IO}	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	0.45	5	mV
Input Offset Current (Figure 9)	I_{IO}	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	0.3	2	µA
Input Bias Current (Figure 5)	I_I	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	10	24	µA
Quiescent Operating Current Ratio (Figure 5)	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$ or $\frac{I_{C(Q5)}}{I_{C(Q6)}}$	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	0.98 to 1.02	-	-
Temperature Coefficient Magnitude of Input Offset Voltage (Figure 7)	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	1.1	-	µV/°C

Electrical Specifications T_A = +25°C **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
For Each Transistor							
DC Forward Base-to-Emitter Voltage (Figure 8)	V_{BE}	V_{CB} = 3V	I_C = 50µA	-	0.630	0.700	V
			I_C = 1mA	-	0.715	0.800	V
			I_C = 3mA	-	0.750	0.850	V
			I_C = 10mA	-	0.800	0.900	V
Temperature Coefficient of Base-to-Emitter Voltage (Figure 6)	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3V, I_C = 1mA		-	-1.9	-	µV/°C
Collector Cutoff Current (Figure 4)	I_{CBO}	V_{CB} = 10V, I_E = 0		-	0.002	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		15	24	-	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10µA, I_E = 0		20	60	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10µA, I_{CI} = 0		20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10µA, I_C = 0		5	7	-	V
DYNAMIC CHARACTERISTICS							
Common Mode Rejection Ratio for each Amplifier (Figures 1, 10)	CMRR	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	100	-	dB
AGC Range, One Stage (Figures 2, 11)	AGC	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	75	-	dB
Voltage Gain, Single Stage Double-Ended Output (Figures 2, 11)	A	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	32	-	dB
AGC Range, Two Stage (Figures 3, 12)	AGC	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	105	-	dB
Voltage Gain, Two Stage Double-Ended Output (Figures 3, 12)	A	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	60	-	dB
Low Frequency, Small Signal Equivalent Circuit Characteristics (for single transistor)							
Forward Current Transfer Ratio (Figure 13)	h_{FE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	110	-	-
Short Circuit Input Impedance (Figure 13)	h_{IE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	3.5	-	kΩ
Open Circuit Output Impedance (Figure 13)	h_{OE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	15.6	-	µmho
Open Circuit Reverse Voltage Transfer Ratio (Figure 13)	h_{RE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	1.8×10^{-4}	-	-
1/f Noise Figure for Single Transistor	NF	f = 1kHz, V_{CE} = 3V		-	3.25	-	dB
Gain Bandwidth Product for Single Transistor (Figure 14)	f_T	V_{CE} = 3V, I_C = 3mA		-	550	-	MHz
Admittance Characteristics; Differential Circuit Configuration (for each amplifier)							
Forward Transfer Admittance (Figure 15)	Y_{21}	V_{CB} = 3V, f = 1MHz Each Collector I_C ≈ 1.25mA		-	-20 + j0	-	mmho
Input Admittance (Figure 16)	Y_{11}	V_{CB} = 3V, f = 1MHz Each Collector I_C ≈ 1.25mA		-	0.22 + j0.1	-	mmho
Output Admittance (Figure 17)	Y_{22}	V_{CB} = 3V, f = 1MHz Each Collector I_C ≈ 1.25mA		-	0.01 + j0	-	mmho
Reverse Transfer Admittance (Figure 18)	Y_{12}	V_{CB} = 3V, f = 1MHz Each Collector I_C ≈ 1.25mA		-	-0.003 + j0	-	mmho

Electrical Specifications T_A = +25°C **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Admittance Characteristics; Cascode Circuit Configuration (for each amplifier)						
Forward Transfer Admittance (Figure 19)	Y_{21}	V_{CB} = 3V, f = 1MHz Total Stage I_C ≈ 2.5 mA	-	68 - j0	-	mmho
Input Admittance (Figure 20)	Y_{11}	V_{CB} = 3V, f = 1MHz Total Stage I_C ≈ 2.5 mA	-	0.55 + j0	-	mmho
Output Admittance (Figure 21)	Y_{22}	V_{CB} = 3V, f = 1MHz Total Stage I_C ≈ 2.5 mA	-	0 + j0.02	-	mmho
Reverse Transfer Admittance (Figure 22)	Y_{12}	V_{CB} = 3V, f = 1MHz Total Stage I_C ≈ 2.5 mA	-	0.004 - j0.005	-	µmho
Noise Figure	NF	f = 100MHz	-	8	-	dB

Test Circuits

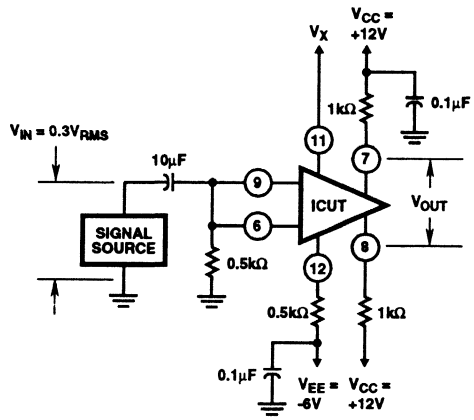


FIGURE 1. COMMON MODE REJECTION RATIO TEST SETUP

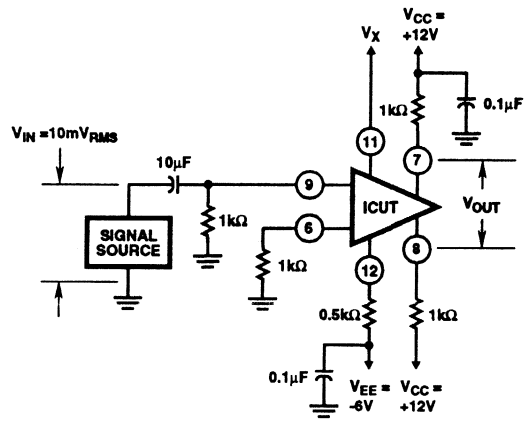


FIGURE 2. SINGLE STAGE VOLTAGE GAIN TEST SETUP

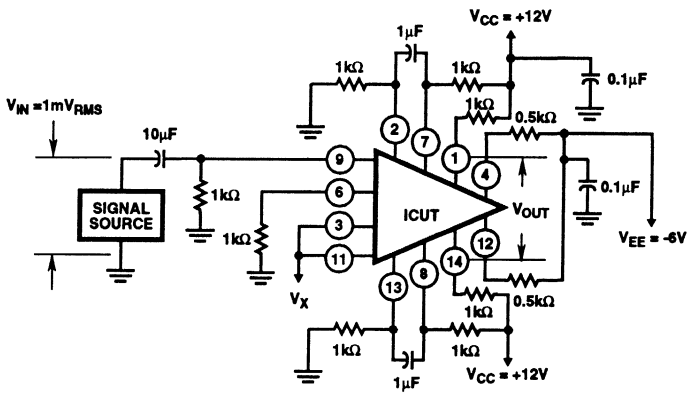
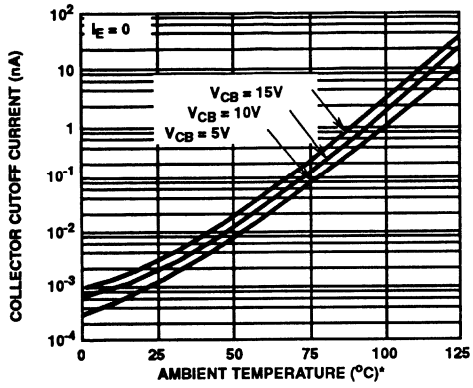


FIGURE 3. TWO STAGE VOLTAGE GAIN TEST SETUP

Typical Performance Curves



* For CA3054 use data from 0°C to +85°C only

FIGURE 4. COLLECTOR-TO-BASE CUTOFF CURRENT vs TEMPERATURE FOR EACH TRANSISTOR

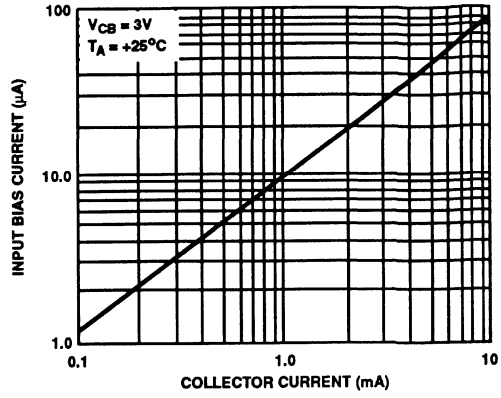
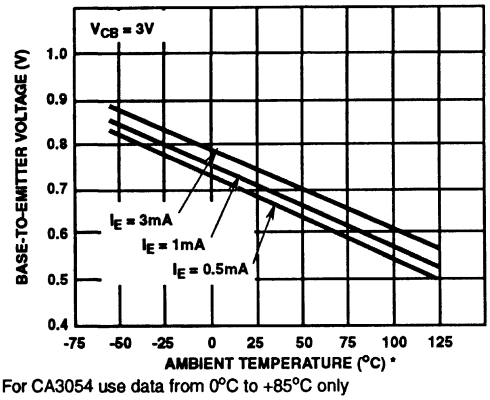
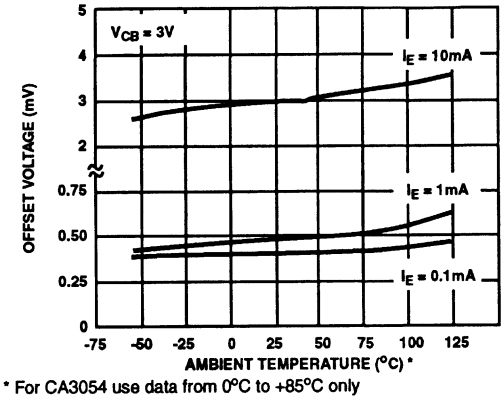


FIGURE 5. INPUT BIAS CURRENT vs COLLECTOR CURRENT FOR EACH TRANSISTOR



* For CA3054 use data from 0°C to +85°C only

FIGURE 6. BASE-TO-EMITTER VOLTAGE FOR EACH TRANSISTOR vs TEMPERATURE



* For CA3054 use data from 0°C to +85°C only

FIGURE 7. OFFSET VOLTAGE vs TEMPERATURE FOR DIFFERENTIAL PAIRS

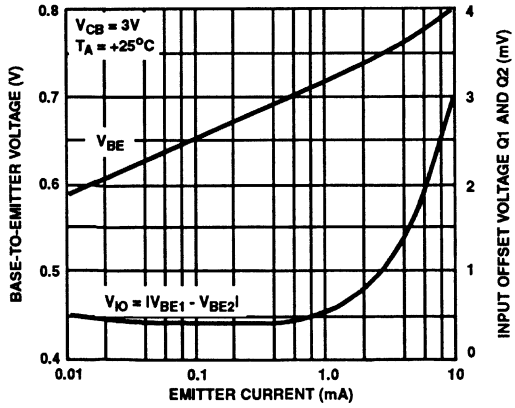


FIGURE 8. STATIC BASE-TO-EMITTER VOLTAGE AND INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIRS vs EMITTER CURRENT

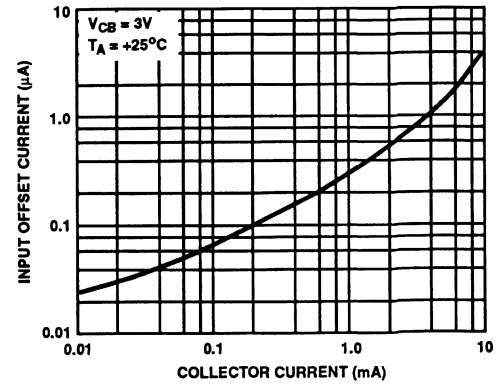


FIGURE 9. INPUT OFFSET CURRENT FOR MATCHED DIFFERENTIAL PAIRS vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

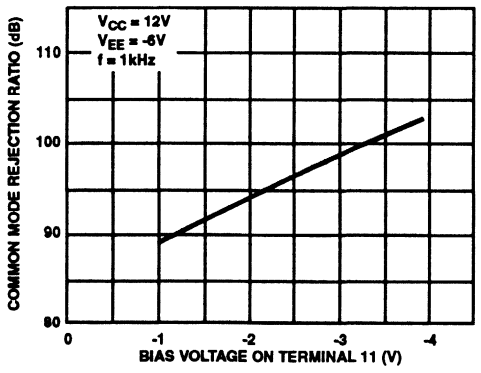


FIGURE 10. COMMON MODE REJECTION RATIO CHARACTERISTIC

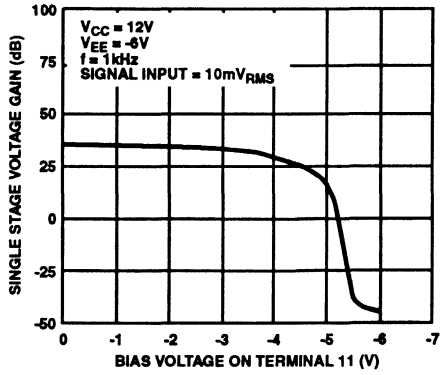


FIGURE 11. SINGLE STAGE VOLTAGE GAIN CHARACTERISTIC

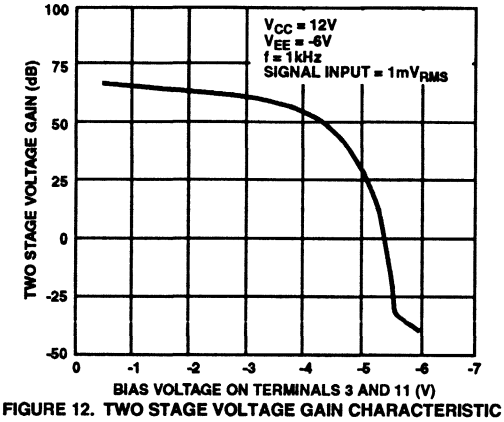


FIGURE 12. TWO STAGE VOLTAGE GAIN CHARACTERISTIC

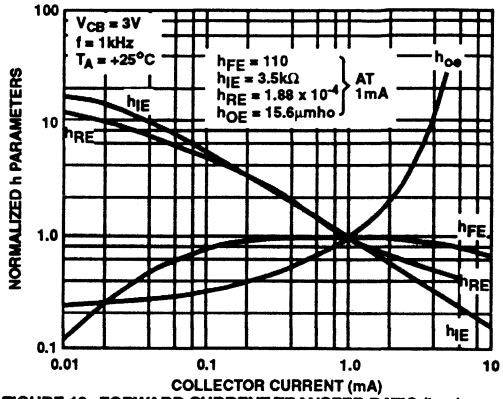


FIGURE 13. FORWARD CURRENT TRANSFER RATIO (h_{FE}), SHORT CIRCUIT INPUT IMPEDANCE (h_{IE}), OPEN CIRCUIT OUTPUT IMPEDANCE (h_{OE}), AND OPEN CIRCUIT REVERSE VOLTAGE TRANSFER RATIO (h_{RE}) vs COLLECTOR CURRENT FOR EACH TRANSISTOR

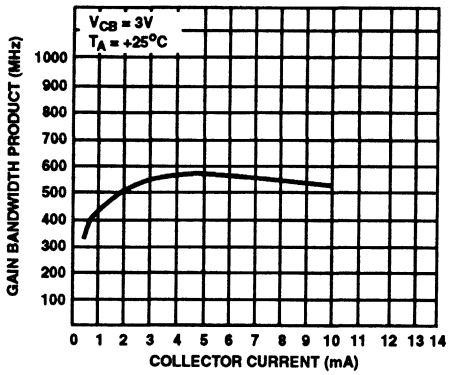


FIGURE 14. GAIN BANDWIDTH PRODUCT (f_T) vs COLLECTOR CURRENT

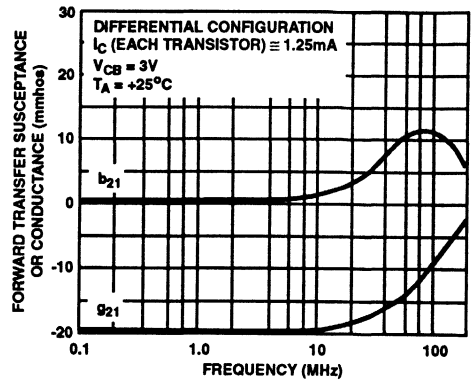


FIGURE 15. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs FREQUENCY

Typical Performance Curves (Continued)

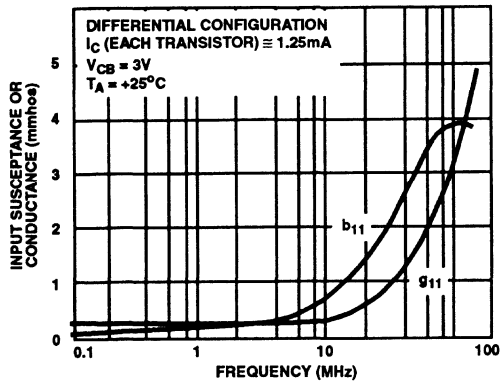


FIGURE 16. INPUT ADMITTANCE (Y_{11})

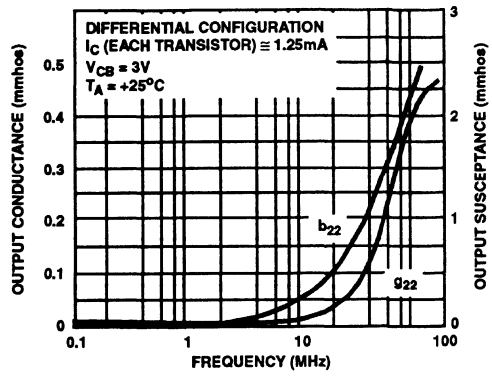


FIGURE 17. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

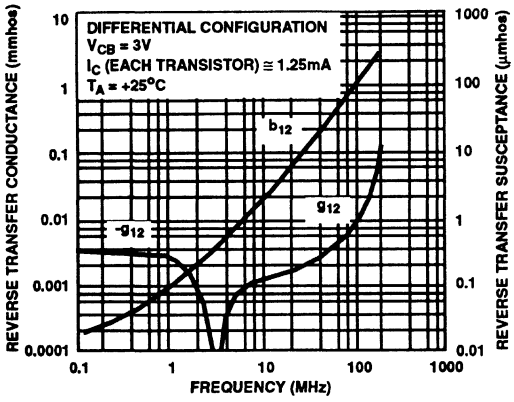


FIGURE 18. REVERSE TRANSFER ADMITTANCE (Y_{12}) vs FREQUENCY

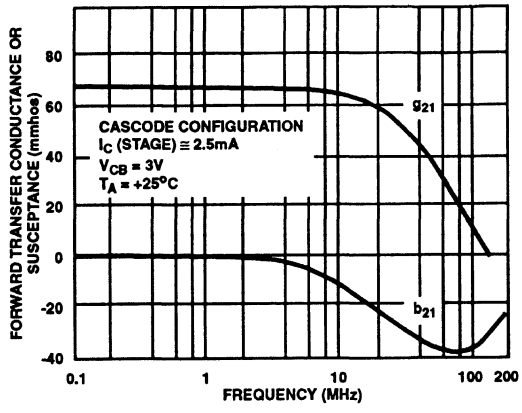


FIGURE 19. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs FREQUENCY

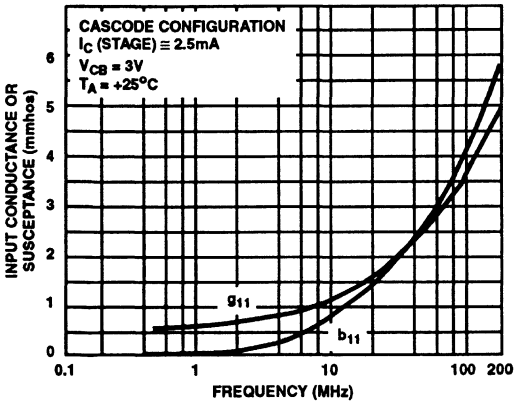


FIGURE 20. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY

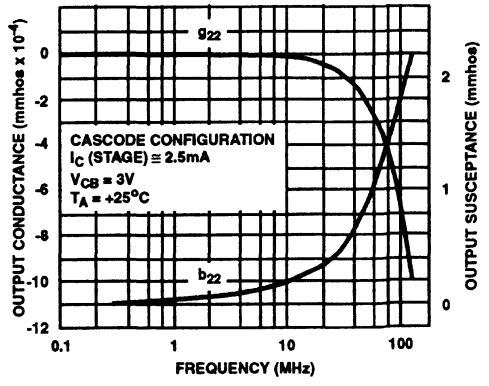


FIGURE 21. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

Typical Performance Curves (Continued)

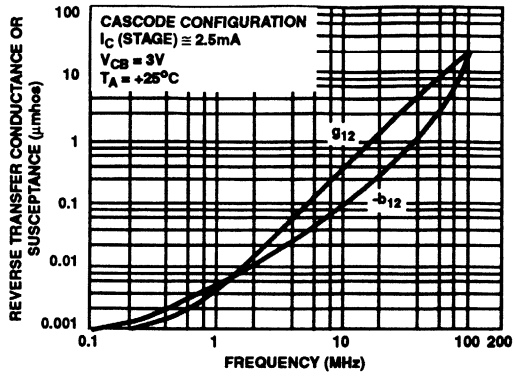


FIGURE 22. REVERSE TRANSFER ADMITTANCE (Y_{12}) vs FREQUENCY

LINEAR 6

TRANSISTOR AND DIODE ARRAYS

NOTE: Bold Type Designates a New Product from Harris.

Selection Guide

TRANSISTOR ARRAYS

Electrical Characteristics $T_A = +25°C$

TYPE	DESCRIPTION	$V_{(BR)\ CEO}$ (MIN) V	$V_{(BR)\ CBO}$ (MIN) V	h_{FE} (MIN)	I_C (MAX) mA	(NOTE 1) LEAD COUNT & PACKAGE TYPE
CA3018	Two Isolated Transistors Plus a Darlington Pair	15	20	30	50	12T
CA3018A		15	30	60	50	
		h_{FE} matched ±10%. V_{BE} matched ±2mV and ±5mV max. Operation from DC to 120MHz				
CA3045	Three Transistors Plus a Differential Pair	15	20	40	50	14D, 14F
CA3046		15	20	40	50	14E,14M
		f_T > 300MHz. 2 matched pairs ±5mV				
CA3081	General-Purpose n-p-n High-Current Transistors	16	20	40	100	16E, 16F, 16M
		Seven Common-Emitter				
CA3082		16	20	40	100	16E,16F, 16M
		Seven Common-Collector				
CA3083		15	20	40	100	16E, 16F, 16M
		Five independent transistors. Q_1 and Q_2 matched; I_{IO} (at 1mA) 2.5µA Maximum				
CA3086	Three Isolated Transistors plus a Differential Pair	15	20	40	50	14E, 14F, 14M
		f_T > 550MHz Typ. Operation from DC to 120MHz				
CA3127	Five Independent Transistors	15	20	40	20	16E, 16F, 16M
		f_T > 1GHz. Operation from DC to 500MHz.				
CA3146	Three Transistors Plus a Differential Pair	30	40	30	50	14E, 14M
CA3146A		40	50	30	50	
		f_T > 500MHz Typ. Operation from DC to 120MHz.				
CA3183	Five High-Current Transistors	30	40	40	75	16E, 16M
CA3183A		40	50	40	75	
		High-voltage versions of CA3083 Transistors Q_1 and Q_2 matched at 1mA.				
CA3227	Five Independent Transistors	8	12	40	20	16E, 16M
		f_T = 3GHz Typ. Operation from DC to 1.5GHz.				
CA3246	Three Independent Transistors Plus a Differential Pair	8	12	40	20	14E, 14M
		f_T = 3GHz Typ. Operation from DC to 1.5GHz.				

NOTE:

1. See Packaging Information Section of this catalog.

Selection Guide

TRANSISTOR ARRAYS (Continued)

Electrical Characteristics T_A = +25°C

TYPE	DESCRIPTION	$V_{(BR)\ CEO}$ (MIN) V n-p-n/p-n-p	$V_{(BR)\ CBO}$ (MIN) V n-p-n/p-n-p	h_{FE} (MIN) n-p-n/p-n-p	I_C (MAX) n-p-n/p-n-p	(NOTE 1) LEAD COUNT & PACKAGE TYPE
CA3096	Five Independent Transistors, 3 n-p-n, 2 p-n-p	35/-40	45/-40	150/20	50/-10	16E, 16M
CA3096A		35/-40	45/-40	150/20	50/-10	
CA3096C		24/-24	30/-24	100/15	50/-10	
		n-p-n		p-n-p		
		$\lvert V_{IO}\rvert$ = 5mV Max		5mV Max		
		$\lvert I_{IO}\rvert$ = 0.6µA Max		0.25µA Max		
HFA3046	Three 8GHz NPN Transistors Plus an NPN Differential Pair	8	12	40	40	14B
		$\lvert V_{IO}\rvert$ = 5mV Max				
HFA3096	Three 8GHz NPN Transistors Plus Two 5.5GHz PNP Transistors	8	12/10	40/25	40	16B
		NF = 1.7dB at 1GHz				
HFA3127	Five Independent 8GHz NPN Transistors	8	12	40	40	16B
		NF = 1.7dB at 1GHz				
HFA3128	Five Independent 5.5GHz PNP Transistors	8	10	25	40	16B
		NF = 1.7dB at 1GHz				

NOTE: Bold Type Designates a New Product from Harris

DIODE ARRAYS

Electrical Characteristics T_A = +25°C. Apply for Each Diode

TYPE	DESCRIPTION	$V_{(BR)\ R}$ (MIN) V	I_R (MAX) µA	C_D (TYP) pF	$V_{F1} - V_{F2}$ (MAX) mV	(NOTE 1) PIN COUNT & PACKAGE TYPE
CA3039	6 Individual	5	0.1	0.65	5 (I_F =1mA)	12T,14M
		Ultra-fast low-capacitance matched diodes				
CA3141	10 High Reverse Breakdown Voltage Diodes (Note 2)	30	0.1	0.3	0.55 (typ. each diode pr.)	16E
		• Low-Noise Performance • Low-Leakage Current				

NOTE:

1. See Packaging Information Section of this catalog.
2. Six connected to form 3 common-cathode pairs. Four connected to form 2 common-anode diode pairs.

HARRIS SEMICONDUCTOR

CA3018

March 1993

General Purpose Transistor Arrays

Features

- Matched Monolithic General Purpose Transistors
- h_{FE} Matched ..... ±10%
- V_{BE} Matched
  - CA3018A ..... ±2mV
  - CA3018 ..... ±5mV
- Operation From DC to 120MHz
- Wide Operating Current Range
- CA3018A Performance Characteristics Controlled from 10μA to 10mA
- Low Noise Figure.....3.2dB Typical at 1kHz
- Full Military Temperature Range .... -55°C to +125°C

Applications

- Two Isolated Transistors and a Darlington Connected Transistor Pair for Low Power Applications at Frequencies from DC through the VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- See Application Note, AN5296 "Application of the CA3018 Integrated Circuit Transistor Array" for Suggested Applications

Description

The CA3018 and CA3018A consist of four general purpose silicon n-p-n transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

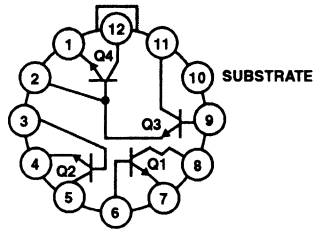
The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3018	-55°C to +125°C	12 Pin CAN
CA3018A	-55°C to +125°C	12 Pin CAN

Pinout

CA3018, CA3018A
(TO-5 CAN)
TOP VIEW



6 TRANSISTOR AND DIODE ARRAYS

File Number 338.2

Absolute Maximum Ratings (T_A = +25°C)

	CA3018	CA3018A
Collector-to-Emitter Voltage, V_{CEO}	15V	15V
Collector-to-Base Voltage, V_{CBO}	20V	30V
Collector-to-Substrate Voltage, V_{CIO} (Note 1)	20V	40V
Emitter-to-Base Voltage, V_{EBO}	5V	5V
Collector Current, I_C	50mA	50mA
Power Dissipation		
Any One Transistor	300mW	
Total Package	450mW	
T_A > +85°C	Derate at 5mW/°C	
Junction Temperature	+175°C	
Lead Temperature (Soldering 10 Sec.)	+300°C	

Operating Conditions

Operating Temperature Range . . . . . -55°C ≤ T_A ≤ +125°C
Storage Temperature Range . . . . . -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS CA3018 MIN	CA3018 TYP	CA3018 MAX	CA3018A MIN	CA3018A TYP	CA3018A MAX	UNITS
STATIC CHARACTERISTICS										
Collector Cutoff Current (Figure 1)	I_{CBO}	V_{CB} = 10V, I_E = 0		-	0.002	100	-	0.002	40	nA
Collector Cutoff Current (Figure 2)	I_{CEO}	V_{CE} = 10V, I_B = 0		-	See Fig. 2	5	-	See Fig. 2	0.5	µA
Collector Cutoff Current Darlington Pair	I_{CEOD}	V_{CE} = 10V, I_B = 0		-	-	-	-	-	5	µA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		15	24	-	15	24	-	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10µA, I_E = 0		20	60	-	30	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10µA, I_C = 0		5	7	-	5	7	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10µA, I_{CI} = 0		20	60	-	40	60	-	V
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1mA, I_C = 10mA		-	0.23	-	-	0.23	0.5	V
Static Forward Current Transfer Ratio (Note 2) (Figure 3)	h_{FE}	V_{CE} = 3V	I_C = 10mA	-	100	-	50	100	-	-
			I_C = 1mA	30	100	200	60	100	200	-
			I_C = 10µA	-	54	-	30	54	-	-
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2) (Figure 3)		V_{CE} = 3V, I_{C1} = I_{C2} = 1mA		0.9	0.97	-	0.9	0.97	-	-
Static Forward Current Transfer Ratio Darlington Pair (Q3 and Q4) (Figure 4)	h_{FED}	V_{CE} = 3V	I_C = 1mA	1500	5400	-	2000	5400	-	-
			I_C = 100µA	-	-	-	1000	2800	-	-
Base-to-Emitter Voltage (Figure 5)	V_{BE}	V_{CE} = 3V	I_E = 1mA	-	0.715	-	0.600	0.715	0.800	V
			I_E = 10mA	-	0.800	-	-	0.800	0.900	V
Input Offset Voltage (Figures 5, 7)	$\lvert V_{BE1} \rvert$ $\lvert -V_{BE2} \rvert$	V_{CE} = 3V, I_E = 1mA		-	0.48	5	-	0.48	2	mV

Electrical Specifications T_A = +25°C **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA3018			CA3018A			
			MIN	TYP	MAX	MIN	TYP	MAX	
Temperature Coefficient: Base-to-Emitter Voltage Q_1, Q_2 (Figure 6)	$\frac{\lvert\Delta V_{BE}\rvert}{\Delta T}$	V_{CE} = 3V, I_E = 1mA	-	-1.9	-	-	-1.9	-	mV/°C
Base (Q3)-to-Emitter (Q4) Voltage Darlington Pair (Figure 8)	V_{BED} (V_{9-1})	V_{CE} = 3V, I_E = 10mA	-	1.46	-	-	1.46	1.60	V
		I_E = 1mA	-	1.32	-	1.10	1.32	1.50	V
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair (Q3 and Q4) (Figure 9)	$\frac{\lvert\Delta V_{BED}\rvert}{\Delta T}$	V_{CE} = 3V, I_E = 1mA	-	4.4	-	-	4.4	-	mV/°C
Temperature Coefficient: Magnitude of Input Offset Voltage	$\frac{\lvert V_{BE1} - V_{BE2}\rvert}{\Delta T}$	V_{CC} = 6V, V_{EE} = -6V, $I_{C1} = I_{C2}$ = 1mA	-	10	-	-	10	-	µV/°C
DYNAMIC CHARACTERISTICS									
Low Frequency Noise Figure (Figures 10 - 12)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100µA, Source Resistance = 1kΩ	-	3.25	-	-	3.25	-	dB
Low Frequency, Small Signal Equivalent Circuit Characteristics									
Forward Current Transfer Ratio (Figure 13)	h_{FE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	110	-	-	110	-	-
Short Circuit Input Impedance (Figure 13)	h_{IE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	3.5	-	-	3.5	-	kΩ
Open Circuit Output Impedance (Figure 13)	h_{OE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	15.6	-	-	15.6	-	µmho
Open Circuit Reverse Voltage Transfer Ratio (Figure 13)	h_{RE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	1.8×10^{-4}	-	-	1.8×10^{-4}	-	-
Admittance Characteristics									
Forward Transfer Admittance (Figure 14)	Y_{FE}	f = 1MHz, V_{CE} = 3V, I_C = 1mA	-	31 - j1.5	-	-	31 - j1.5	-	mmho
Input Admittance (Figure 15)	Y_{IE}	f = 1MHz, V_{CE} = 3V, I_C = 1mA	-	0.3 + j0.04	-	-	0.3 + j0.04	-	mmho
Output Admittance (Figure 16)	Y_{OE}	f = 1MHz, V_{CE} = 3V, I_C = 1mA	-	0.001 + j0.03	-	-	0.001 + j0.03	-	mmho
Reverse Transfer Admittance (Figure 17)	Y_{RE}	f = 1MHz, V_{CE} = 3V, I_C = 1mA	See Figure 17						mmho
Gain Bandwidth Product (Figure 18)	f_T	V_{CE} = 3V, I_C = 3mA	300	500	-	300	500	-	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3V, I_E = 0	-	0.6	-	-	0.6	-	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3V, I_C = 0	-	0.58	-	-	0.58	-	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 3V, I_C = 0	-	2.8	-	-	2.8	-	pF

NOTE:

1. The collector of each transistor of the CA3018 and CA3018A is isolated from the substrate by an integral diode. The substrate (Terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. Actual forcing current is via the emitter for this test.

Typical Performance Curves

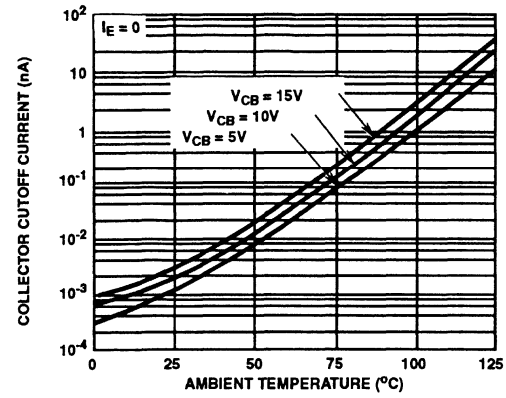


FIGURE 1. TYPICAL COLLECTOR-TO-BASE CUTOFF CURRENT vs TEMPERATURE

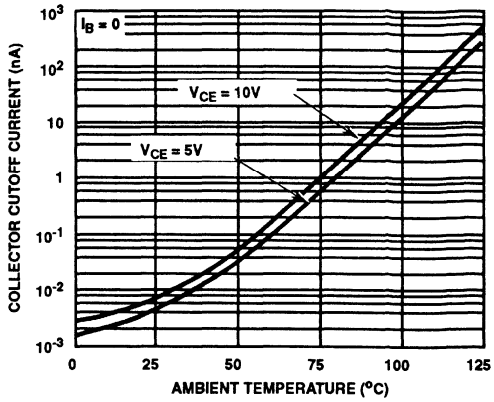


FIGURE 2. TYPICAL COLLECTOR-TO-EMITTER CUTOFF CURRENT vs TEMPERATURE

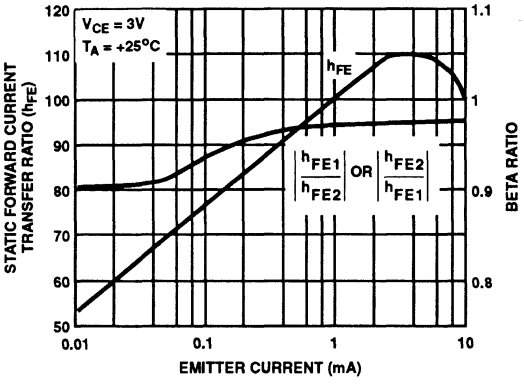


FIGURE 3. TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO AND BETA RATIO FOR TRANSISTORS Q_1 AND Q_2 vs EMITTER CURRENT

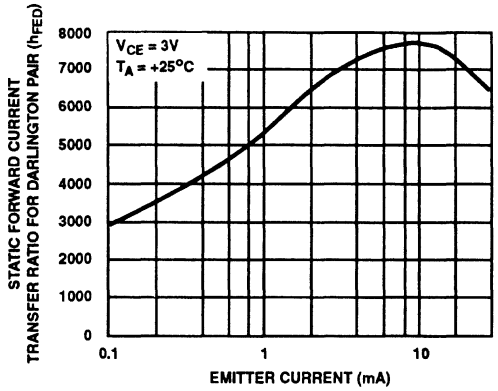


FIGURE 4. TYPICAL STATIC FORWARD CURRENT-TRANSFER RATIO FOR DARLINGTON CONNECTED TRANSISTORS Q_3 AND Q_4 vs EMITTER CURRENT

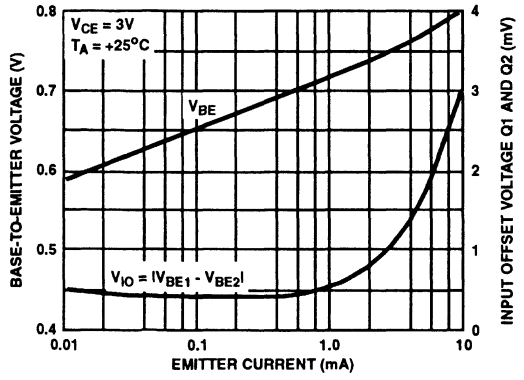


FIGURE 5. TYPICAL STATIC BASE-TO-EMITTER VOLTAGE CHARACTERISTIC AND INPUT OFFSET VOLTAGE FOR Q_1 AND Q_2 vs EMITTER CURRENT

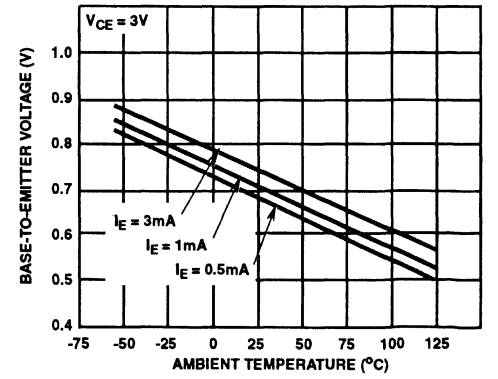


FIGURE 6. TYPICAL BASE-TO-EMITTER VOLTAGE CHARACTERISTIC FOR EACH TRANSISTOR vs TEMPERATURE

Typical Performance Curves (Continued)

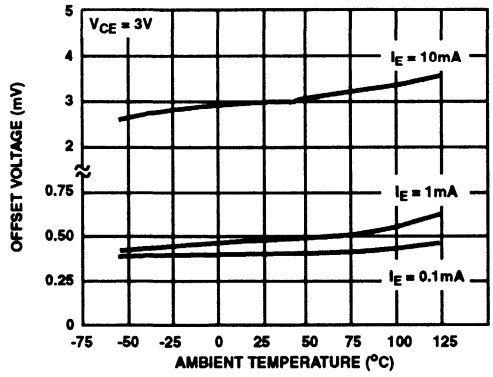


FIGURE 7. TYPICAL OFFSET VOLTAGE CHARACTERISTIC vs TEMPERATURE

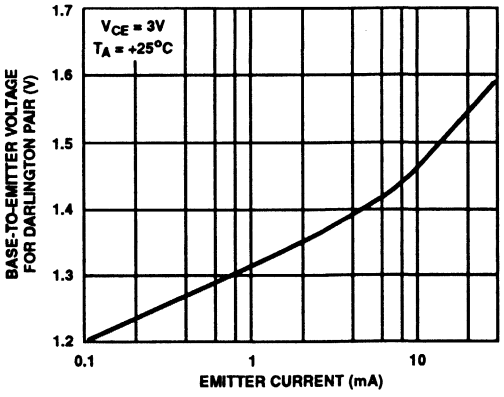


FIGURE 8. TYPICAL STATIC INPUT VOLTAGE CHARACTERISTIC FOR DARLINGTON PAIR (Q_3 AND Q_4) vs EMITTER CURRENT

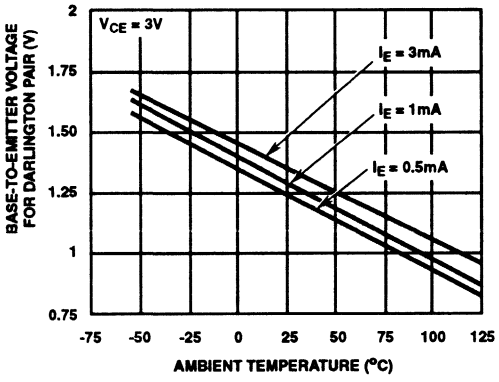


FIGURE 9. TYPICAL STATIC INPUT VOLTAGE CHARACTERISTIC FOR DARLINGTON PAIR (Q_3 AND Q_4) vs TEMPERATURE

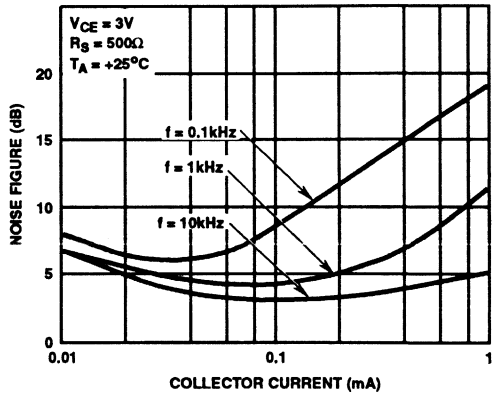


FIGURE 10. NOISE FIGURE vs COLLECTOR CURRENT, R_S = 500Ω

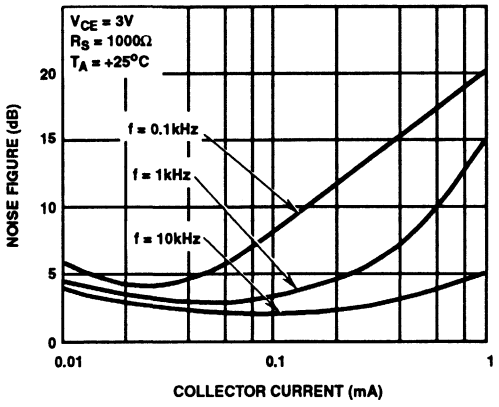


FIGURE 11. NOISE FIGURE vs COLLECTOR CURRENT, R_S = 1kΩ

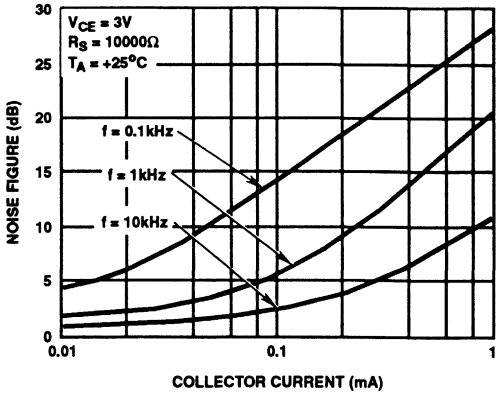


FIGURE 12. NOISE FIGURE vs COLLECTOR CURRENT, R_S = 10kΩ

Typical Performance Curves (Continued)

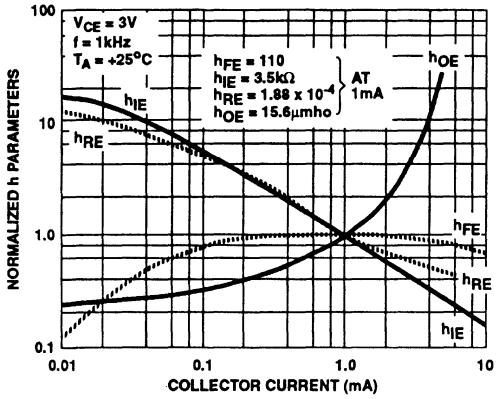


FIGURE 13. h PARAMETERS vs COLLECTOR CURRENT

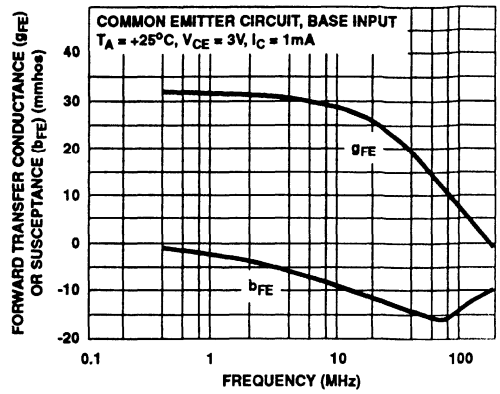


FIGURE 14. FORWARD TRANSFER ADMITTANCE (Y_{FE})

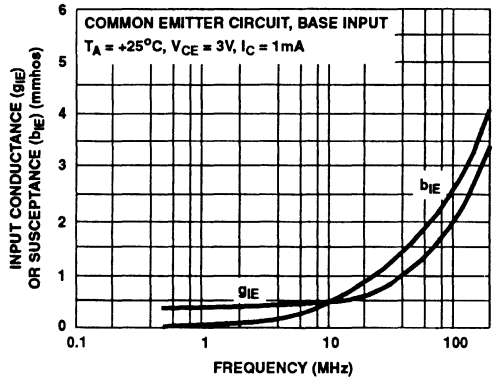


FIGURE 15. INPUT ADMITTANCE (Y_{IE})

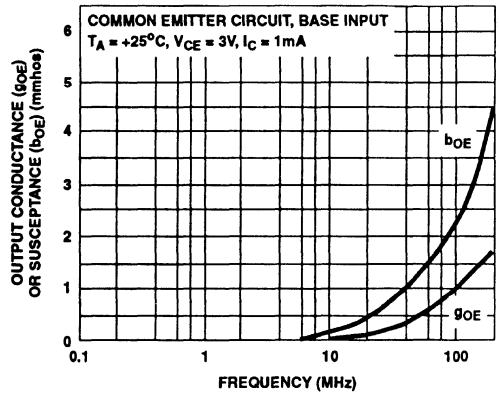


FIGURE 16. OUTPUT ADMITTANCE (Y_{OE})

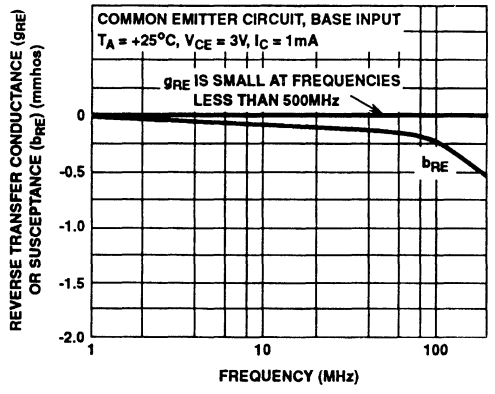


FIGURE 17. REVERSE TRANSFER ADMITTANCE (Y_{RE})

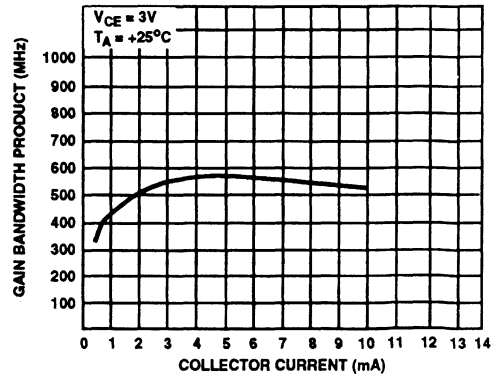


FIGURE 18. TYPICAL GAIN BANDWIDTH PRODUCT (f_T) vs COLLECTOR CURRENT

HARRIS SEMICONDUCTOR

CA3039

March 1993

Diode Array

Features

- Six Matched Diodes on a Common Substrate
- Excellent Reverse Recovery Time 1ns Typical
- Matched Monolithic Construction
  - V_F Matched Within 5mV
- Low Diode Capacitance
  - C_D = 0.65pF Typical at V_R = -2V

Applications

- Ultra-Fast Low Capacitance Matched Diodes for Applications in Communications and Switching Systems
- Balanced Modulators or Demodulators
- Ring Modulators
- High Speed Diode Gates
- Analog Switches

Description

The CA3039 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

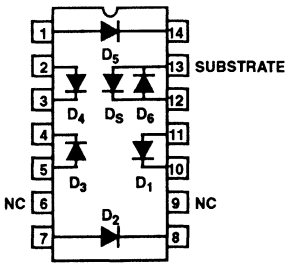
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3039	-55°C to +125°C	12 Pin CAN
CA3039M	-55°C to +125°C	14 Lead SOIC
CA3039M96	-55°C to +125°C	14 Lead SOIC*

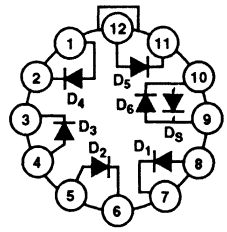
* Denotes Tape and Reel

Pinouts

CA3039
(SOIC)
TOP VIEW



CA3039
(TO-5 CAN)
TOP VIEW



6 TRANSISTOR AND DIODE ARRAYS

File Number 343.2

Absolute Maximum Ratings

Inverse Voltage (PIV) for: D_1 - D_5 ..... 5V
D_6 ..... 0.5V
Diode-to-Substrate Voltage (V_{DI}) for D_1 - D_5 ..... +20V, -1V
(Terminal 1, 4, 5, 8 or 12 to Terminal 10)
DC Forward Current (I_F) 25mA
Recurrent Forward Current (I_F) 100mA
Forward Surge Current ($I_{F(SURGE)}$) 100mA
Power Dissipation
Any One Diode Unit 100mW
Total for Device 600mW
For T_A > +55°C ..... Derate Linearly 5.7mW/°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -55°C ≤ T_A ≤ +125°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C. Characteristics apply for each diode unit, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DC Forward Voltage Drop (Figure 1)	V_F	I_F = 50µA	-	0.65	0.69	V
		I_F = 1mA	-	0.73	0.78	V
		I_F = 3mA	-	0.76	0.80	V
		I_F = 10mA	-	0.81	0.90	V
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = -10µA	5	7	-	V
DC Reverse Breakdown Voltage Between Any Diode Unit and Substrate	$V_{(BR)R}$	I_R = -10µA	20	-	-	V
DC Reverse (Leakage) Current (Figure 2)	I_R	V_R = -4V	-	0.016	100	nA
DC Reverse (Leakage) Current Between Any Diode Unit and Substrate (Figure 3)	I_R	V_R = -10V	-	0.022	100	nA
Magnitude of Diode Offset Voltage (Note 1) (Figure 1)	$\lvert V_{F1} - V_{F2} \rvert$	I_F = 1mA	-	0.5	5.0	mV
Temperature Coefficient of $\lvert V_{F1} - V_{F2} \rvert$ (Figure 4)	$\frac{\Delta \lvert V_{F1} - V_{F2} \rvert}{\Delta T}$	I_F = 1mA	-	1.0	-	µV/°C
Temperature Coefficient of Forward Drop (Figure 5)	$\frac{\Delta V_F}{\Delta T}$	I_F = 1mA	-	-1.9	-	mV/°C
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1mA	-	0.65	-	V
Reverse Recovery Time	t_{RR}	I_F = 10mA, I_R = -10mA	-	1.0	-	ns
Diode Resistance (Figure 6)	R_D	f = 1kHz, I_F = 1mA	25	30	45	Ω
Diode Capacitance (Figure 7)	C_D	V_R = -2V, I_F = 0	-	0.65	-	pF
Diode-to-Substrate Capacitance (Figure 8)	C_{DI}	V_{DI} = 4V, I_F = 0	-	3.2	-	pF

NOTE:

1. Magnitude of Diode Offset Voltage is the difference in DC Forward Voltage Drops of any two diode units.

Typical Performance Curves

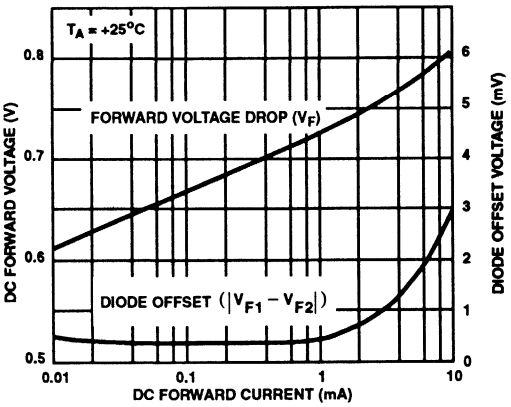


FIGURE 1. DC FORWARD VOLTAGE DROP (ANY DIODE) AND DIODE OFFSET VOLTAGE vs DC FORWARD CURRENT

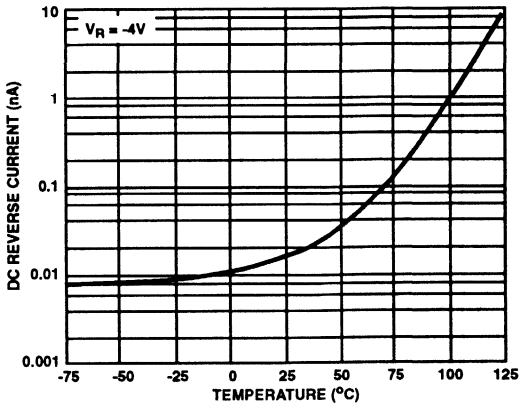


FIGURE 2. DC REVERSE (LEAKAGE) CURRENT (D_1 - D_5) vs TEMPERATURE

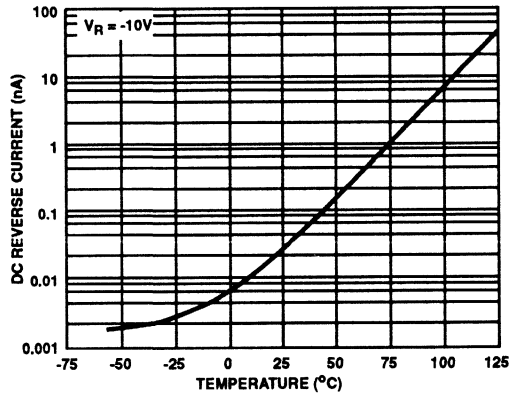


FIGURE 3. DC REVERSE (LEAKAGE) CURRENT BETWEEN D_1, D_2, D_3, D_4, D_5 AND SUBSTRATE vs TEMPERATURE

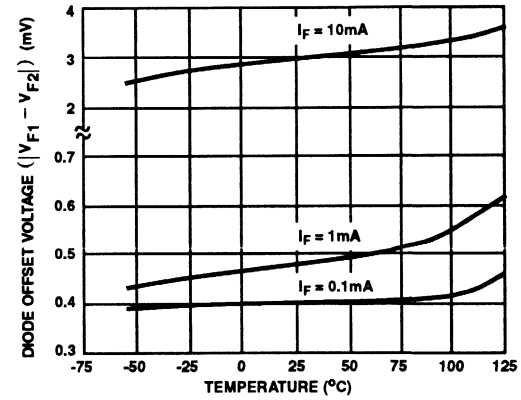


FIGURE 4. DIODE OFFSET VOLTAGE (ANY DIODE) vs TEMPERATURE

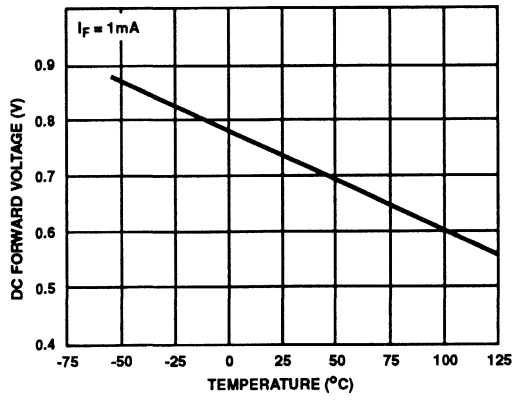


FIGURE 5. DC FORWARD VOLTAGE DROP (ANY DIODE) vs TEMPERATURE

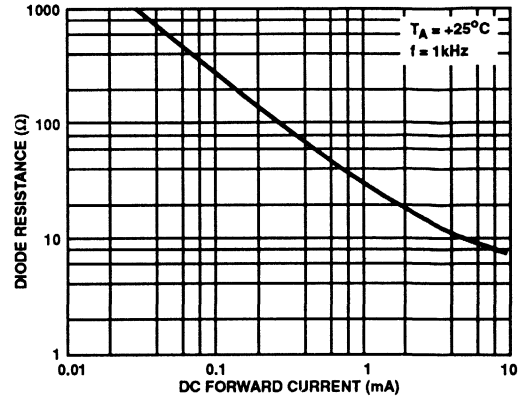


FIGURE 6. DIODE RESISTANCE (ANY DIODE) vs DC FORWARD CURRENT

Typical Performance Curves (Continued)

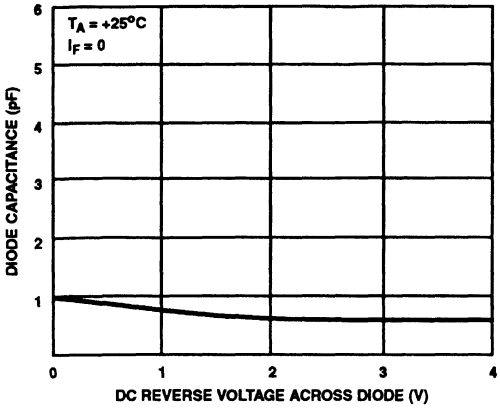


FIGURE 7. DIODE CAPACITANCE (D_1 - D_5) vs REVERSE VOLTAGE

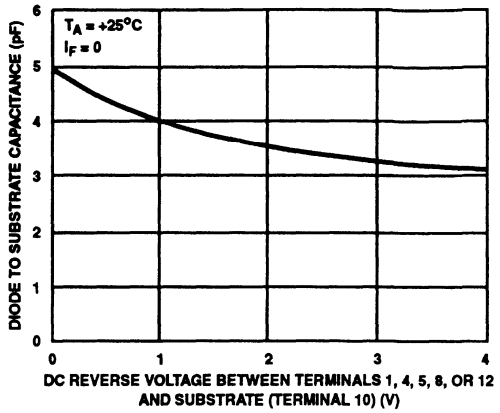


FIGURE 8. DIODE-TO-SUBSTRATE CAPACITANCE vs REVERSE VOLTAGE

HARRIS SEMICONDUCTOR

CA3045, CA3046

General Purpose N-P-N Transistor Arrays

March 1993

Features

- Two Matched Transistors: V_{BE} Matched ±5mV; Input Offset Current 2μA Max at I_C = 1mA
- 5 General Purpose Monolithic Transistors
- Operation From DC to 120MHz
- Wide Operating Current Range
- Low Noise Figure 3.2dB Typical at 1kHz
- Full Military Temperature Range -55°C to +125°C

Applications

- Three Isolated Transistors and One Differentially Connected Transistor Pair for Low Power Applications at Frequencies from DC Through the VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- See Application Note, AN5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for Suggested Applications

Description

The CA3045 and CA3046 each consist of five general purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

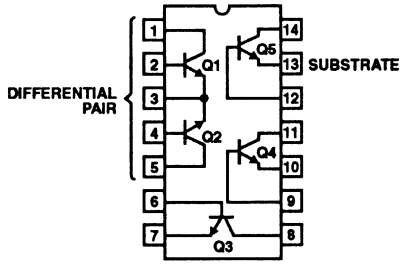
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3045	-55°C to +125°C	14 Lead Ceramic Sidebraze DIP
CA3045F	-55°C to +125°C	14 Lead Ceramic DIP
CA3046	-55°C to +125°C	14 Lead Plastic DIP
CA3046M	-55°C to +125°C	14 Lead SOIC
CA3046M96	-55°C to +125°C	14 Lead SOIC*

* Denotes Tape and Reel

Pinout

CA3045, CA3046
(PDIP, CDIP, SOIC)
TOP VIEW



6 TRANSISTOR AND DIODE ARRAYS

Absolute Maximum Ratings (T_A = +25°C)

Collector-to-Emitter Voltage (V_{CEO}) 15V
Collector-to-Base Voltage (V_{CBO}) 20V
Collector-to-Substrate Voltage (V_{CIO}) (Note 1) 20V
Emitter-to-Base Voltage (V_{EBO}) 5V
Collector Current (I_C) 50mA
Power Dissipation

	Each Transistor	Total Pkg.
CA3045		
Up to T_A = +75°C	300mW	750mW
Above T_A = +75°C	Derate Linearly 8mW/°C	
CA3046, CA3045F		
Up to T_A = +55°C	300mW	750mW
Above T_A = +55°C	Derate Linearly 6.67mW/°C	

Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -55°C ≤ T_A ≤ +125°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ 150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C, Characteristics apply for each transistor in CA3045 & CA3046 as specified.

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
STATIC CHARACTERISTICS							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10μA, I_E = 0		20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10μA, I_{CI} = 0		20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0		5	7	-	V
Collector Cutoff Current (Figure 1)	I_{CBO}	V_{CB} = 10V, I_E = 0		-	0.002	40	nA
Collector Cutoff Current (Figure 2)	I_{CEO}	V_{CE} = 10V, I_B = 0		-	See Fig. 2	0.5	μA
Static Forward Current Transfer Ratio (Static Beta) (Note 2) (Figure 3)	h_{FE}	V_{CE} = 3V	I_C = 10mA	-	100	-	-
			I_C = 1mA	40	100	-	-
			I_C = 10μA	-	54	-	-
Input Offset Current for Matched Pair Q_1 and Q_2. $\|I_{IO1} - I_{IO2}\|$ (Note 2) (Figure 4)		V_{CE} = 3V, I_C = 1mA		-	0.3	2	μA
Base-to-Emitter Voltage (Note 2) (Figure 5)	V_{BE}	V_{CE} = 3V	I_E = 1mA	-	0.715	-	V
			I_E = 10mA	-	0.800	-	V
Magnitude of Input Offet Voltage for Differential Pair $\|V_{BE1} - V_{BE2}\|$ (Note 2) (Figures 5, 7)		V_{CE} = 3V, I_C = 1mA		-	0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors $\|V_{BE3} - V_{BE4}\|$, $\|V_{BE4} - V_{BE5}\|$, $\|V_{BE5} - V_{BE3}\|$ (Note 2) (Figures 5, 7)		V_{CE} = 3V, I_C = 1mA		-	0.45	5	mV
Temperature Coefficient of Base-to-Emitter Voltage (Figure 6)	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3V, I_C = 1mA		-	-1.9	-	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1mA, I_C = 10mA		-	0.23	-	V
Temperature Coefficient: Magnitude of Input Offset Voltage (Figure 7)	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$	V_{CE} = 3V, I_C = 1mA		-	1.1	-	μV/°C

Electrical Specifications T_A = +25°C, Characteristics apply for each transistor in CA3045 & CA3046 as specified. **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
DYNAMIC CHARACTERISTICS						
Low Frequency Noise Figure (Figure 9)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100µA, Source Resistance = 1kΩ	-	3.25	-	dB
Low Frequency, Small Signal Equivalent Circuit Characteristics						
Forward Current Transfer Ratio (Figure 11)	h_{FE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	110	-	-
Short Circuit Input Impedance (Figure 11)	h_{IE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	3.5	-	kΩ
Open Circuit Output Impedance (Figure 11)	h_{OE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	15.6	-	µmho
Open Circuit Reverse Voltage Transfer Ratio (Figure 11)	h_{RE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	1.8×10^{-4}	-	-
Admittance Characteristics						
Forward Transfer Admittance (Figure 12)	Y_{FE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	31 - j1.5	-	-
Input Admittance (Figure 13)	Y_{IE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	0.3 + j0.04	-	-
Output Admittance (Figure 14)	Y_{OE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	0.001 + j0.03	-	-
Reverse Transfer Admittance (Figure 15)	Y_{RE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	See Fig. 14	-	-
Gain Bandwidth Product (Figure 16)	f_T	V_{CE} = 3V, I_C = 3mA	300	550	-	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3V, I_E = 0	-	0.6	-	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3V, I_C = 0	-	0.58	-	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3V, I_C = 0	-	2.8	-	pF

NOTE:

1. The collector of each transistor of the CA3045 and CA3046 is isolated from the substrate by an integral diode. The substrate (Terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. Actual forcing current is via the emitter for this test.

Typical Performance Curves

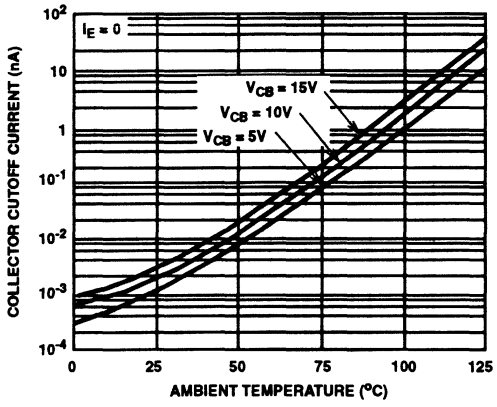


FIGURE 1. TYPICAL COLLECTOR-TO-BASE CUTOFF CURRENT vs TEMPERATURE FOR EACH TRANSISTOR

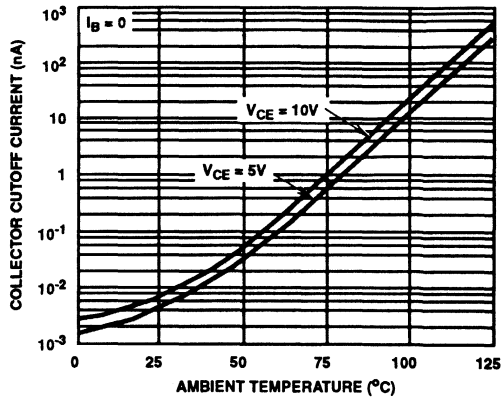


FIGURE 2. TYPICAL COLLECTOR-TO-EMITTER CUTOFF CURRENT vs TEMPERATURE FOR EACH TRANSISTOR

Typical Performance Curves (Continued)

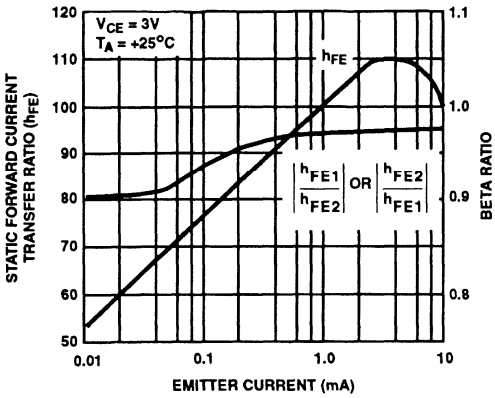


FIGURE 3. TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO AND BETA RATIO FOR Q_1 AND Q_2 vs EMITTER CURRENT

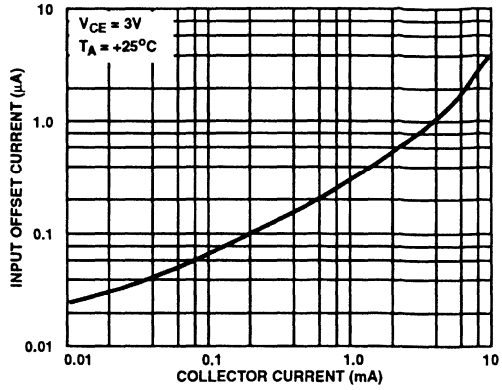


FIGURE 4. TYPICAL INPUT OFFSET CURRENT FOR MATCHED TRANSISTOR PAIR Q_1Q_2 vs COLLECTOR CURRENT

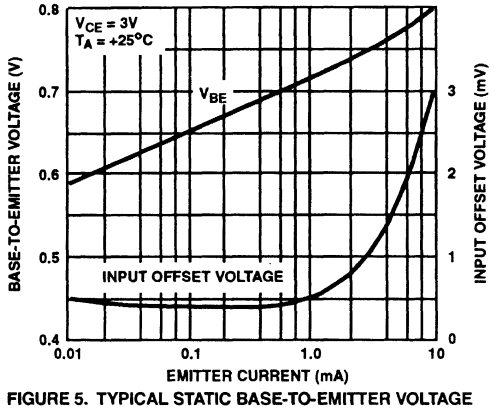


FIGURE 5. TYPICAL STATIC BASE-TO-EMITTER VOLTAGE CHARACTERISTICS AND INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS vs EMITTER CURRENT

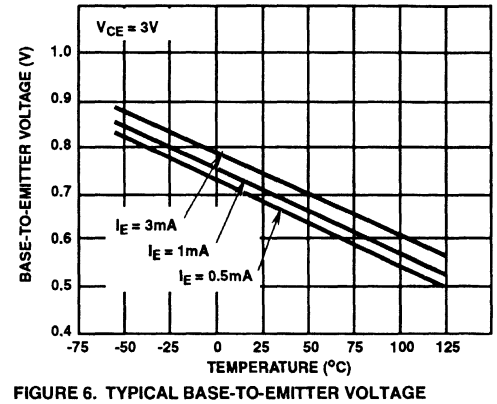


FIGURE 6. TYPICAL BASE-TO-EMITTER VOLTAGE CHARACTERISTIC vs TEMPERATURE FOR EACH TRANSISTOR

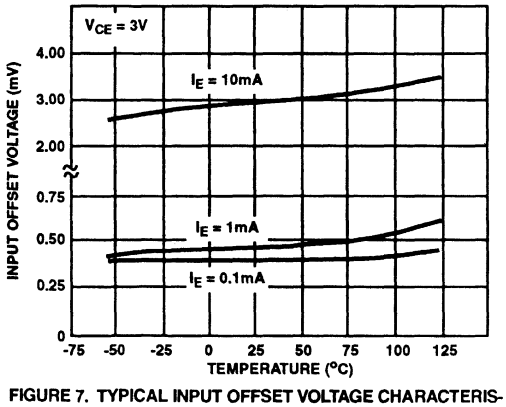


FIGURE 7. TYPICAL INPUT OFFSET VOLTAGE CHARACTERISTICS FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS vs TEMPERATURE

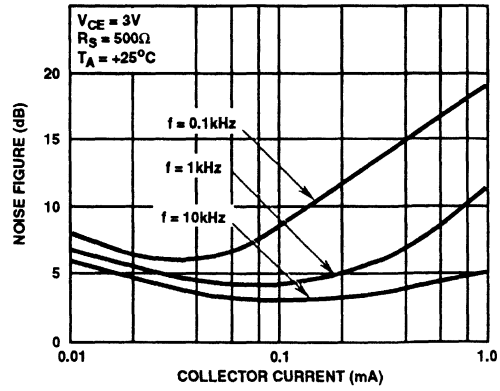


FIGURE 8. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

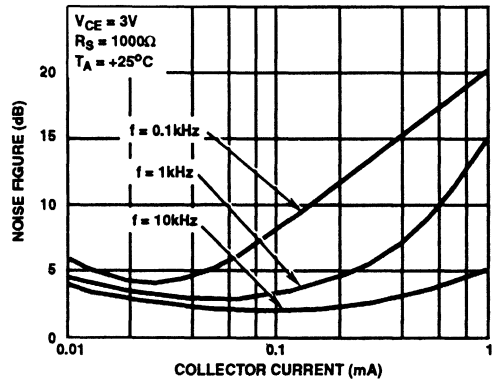


FIGURE 9. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

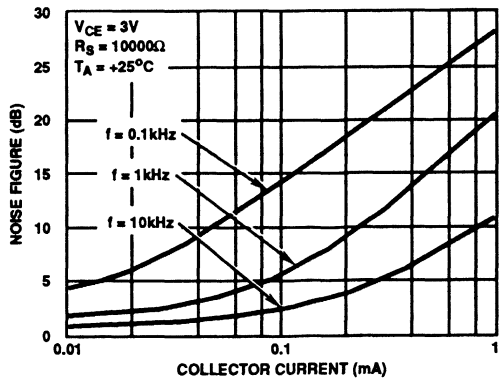


FIGURE 10. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

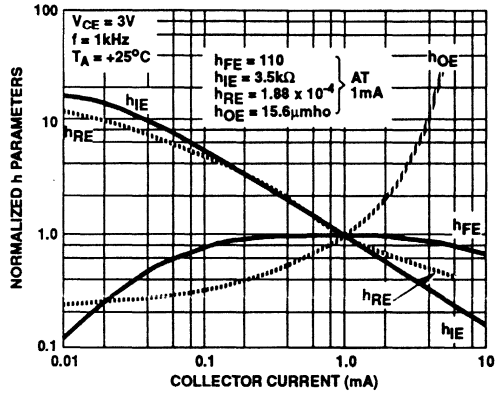


FIGURE 11. TYPICAL NORMALIZED FORWARD CURRENT TRANSFER RATIO, SHORT CIRCUIT INPUT IMPEDANCE, OPEN CIRCUIT OUTPUT IMPEDANCE, AND OPEN CIRCUIT REVERSE VOLTAGE TRANSFER RATIO vs COLLECTOR CURRENT

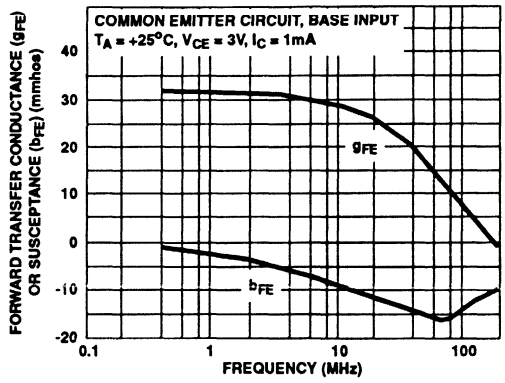


FIGURE 12. TYPICAL FORWARD TRANSFER ADMITTANCE vs FREQUENCY

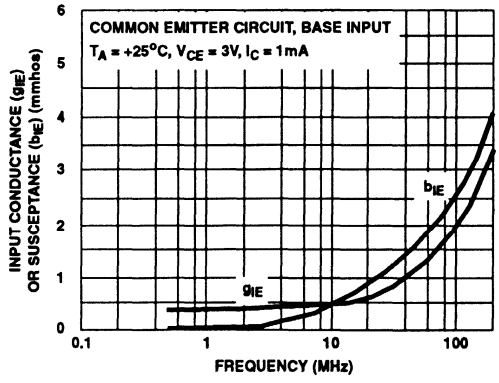


FIGURE 13. TYPICAL INPUT ADMITTANCE vs FREQUENCY

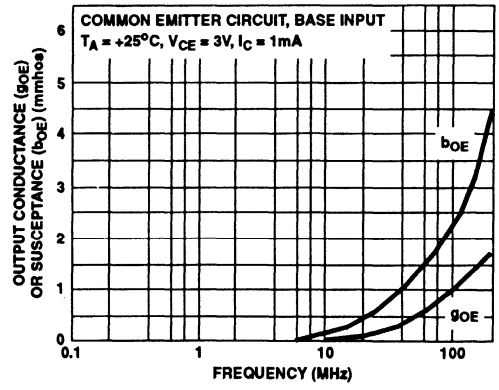


FIGURE 14. TYPICAL OUTPUT ADMITTANCE vs FREQUENCY

Typical Performance Curves (Continued)

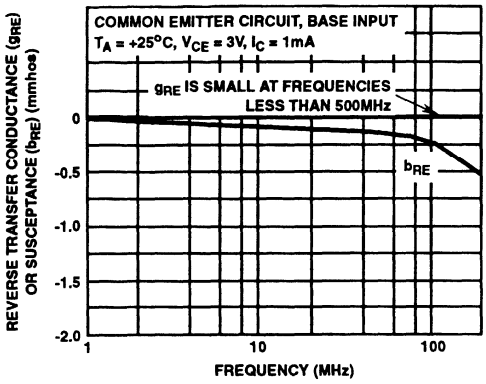


FIGURE 15. TYPICAL REVERSE TRANSFER ADMITTANCE vs FREQUENCY

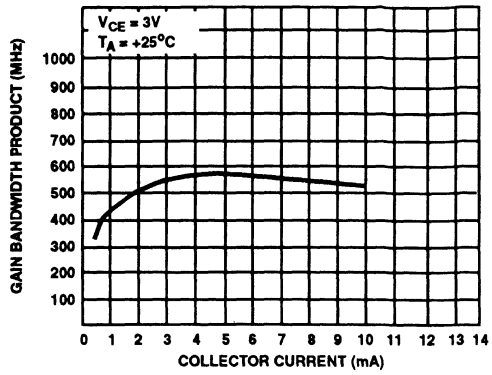


FIGURE 16. TYPICAL GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT

HARRIS SEMICONDUCTOR

CA3081, CA3082

General Purpose High Current N-P-N Transistor Arrays

March 1993

Features

- CA3081 - Common Emitter Array
- CA3082 - Common Collector Array
- Directly Drive Seven Segment Incandescent Displays and Light Emitting Diode (LED) Display
- 7 Transistors Permit a Wide Range of Applications in Either a Common Emitter (CA3081) or Common Collector (CA3082) Configuration
- High I_C 100mA Max
- Low V_{CESAT} (at 50mA) 0.4 Typ

Applications

- Drivers for
  - Incandescent Display Devices
  - LED Displays
  - Relay Control
  - Thyristor Firing

Description

CA3081 and CA3082 consist of seven high current (to 100mA) silicon n-p-n transistors on a common monolithic substrate. The CA3081 is connected in a common emitter configuration and the CA3082 is connected in a common collector configuration.

The CA3081 and CA3082 are capable of directly driving seven segment displays, and light emitting diode (LED) displays. These types are also well suited for a variety of other drive applications, including relay control and thyristor firing.

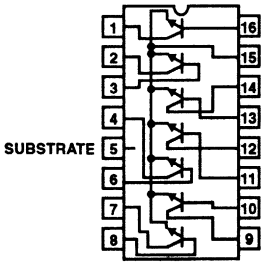
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3081	-55°C to +125°C	16 Lead Plastic DIP
CA3081F	-55°C to +125°C	16 Lead Ceramic DIP
CA3081M	-55°C to +125°C	16 Lead Narrow Body SOIC
CA3081M96	-55°C to +125°C	16 Lead Narrow Body SOIC*
CA3082	-55°C to +125°C	16 Lead Plastic DIP
CA3082F	-55°C to +125°C	16 Lead Ceramic DIP
CA3082M	-55°C to +125°C	16 Lead Narrow Body SOIC
CA3082M96	-55°C to +125°C	16 Lead Narrow Body SOIC*

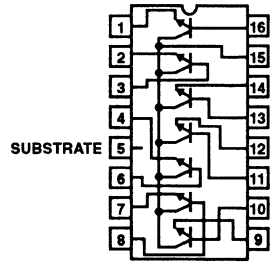
* Denotes Tape and Reel

Pinouts

CA3081
COMMON EMITTER CONFIGURATION
(PDIP, CDIP, 150 mil SOIC)
TOP VIEW



CA3082
COMMON COLLECTOR CONFIGURATION
(PDIP, CDIP, 150 mil SOIC)
TOP VIEW



6 TRANSISTOR AND DIODE ARRAYS

Absolute Maximum Ratings (T_A = +25°C)

Collector-to-Emitter Voltage (V_{CEO}) 16V
Collector-to-Base Voltage (V_{CBO}) 20V
Collector-to-Substrate Voltage (V_{CIO}) (Note 1) 20V
Emitter-to-Base Voltage (V_{EBO}) 5V
Collector Current (I_C) 100mA
Base Current (I_B) 20mA
Power Dissipation
  Any One Transistor 500mW
  Total Package 750mW
  Above T_A = +55°C ..... Derate Linearly 6.67mW/°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -55°C ≤ T_A ≤ +125°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications For Equipment Design T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 500µA, I_E = 0	20	60	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 500µA, I_B = 0	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	16	24	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_C = 500µA	5.0	6.9	-	V
DC Forward Current Transfer Ratio	h_{FE}	V_{CE} = 0.5V, I_C = 30mA	30	68	-	-
		V_{CE} = 0.8V, I_C = 50mA	40	70	-	-
Base-to-Emitter Saturation Voltage (Figure 2)	V_{BESAT}	I_C = 30mA, I_B = 1mA	-	0.87	1.2	V
Collector-to-Emitter Saturation Voltage	V_{CESAT}					
CA3081, CA3082		I_C = 30mA, I_B = 1mA	-	0.27	0.5	V
CA3081 (Figure 3)		I_C = 50mA, I_B = 5mA	-	0.4	0.7	V
CA3082 (Figure 3)		I_C = 50mA, I_B = 5mA	-	0.4	0.8	V
Collector Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	-	-	10	µA
Collector Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	-	-	1.0	µA

NOTE:

1. The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

Typical Performance Curves

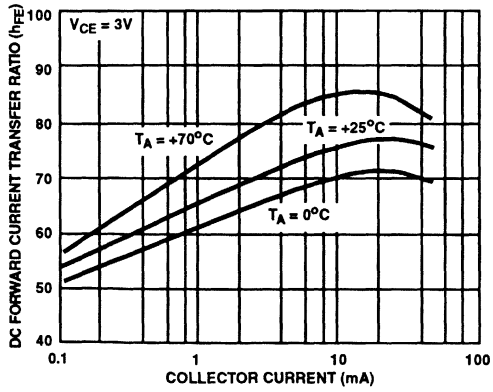


FIGURE 1. DC FORWARD CURRENT TRANSFER RATIO vs COLLECTOR CURRENT

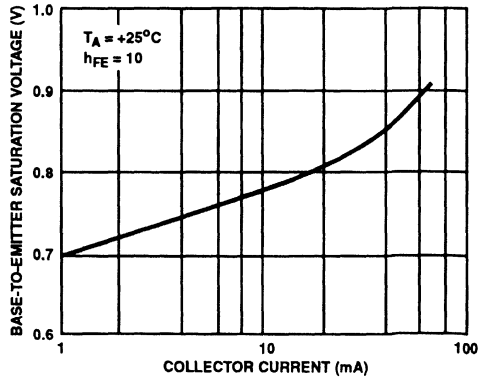


FIGURE 2. BASE-TO-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

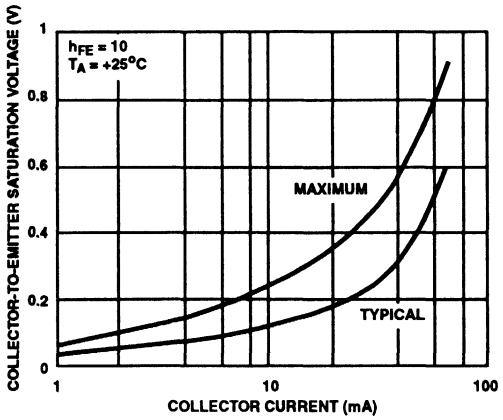


FIGURE 3. COLLECTOR-TO-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT AT T_A = +25°C

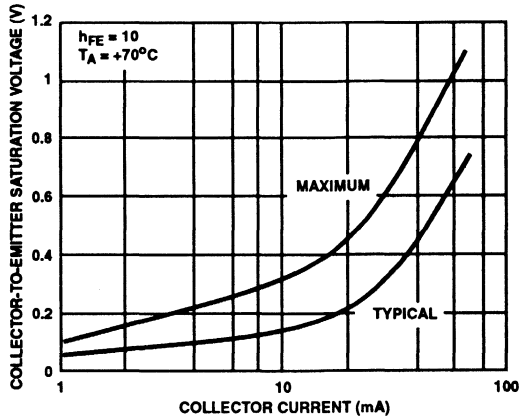


FIGURE 4. COLLECTOR-TO-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT AT T_A = +70°C

Typical Read - Out Driver Applications

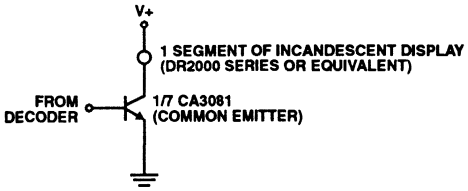
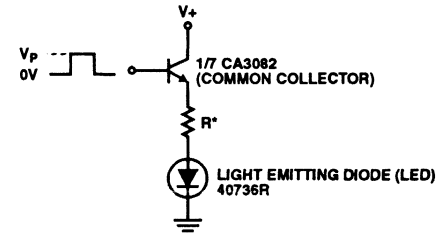


FIGURE 5. SCHEMATIC DIAGRAM SHOWING ONE TRANSISTOR OF THE CA3081 DRIVING ONE SEGMENT OF AN INCANDESCENT DISPLAY



* The Resistance for R is determined by the relationship:

$$R = \frac{V_P - V_{BE} - V_F(LED)}{I(LED)}$$

$$R = 0 \text{ for } V_P = V_{BE} + V_F(LED)$$

Where: V_P = Input Pulse Voltage
V_F = Forward Voltage Drop Across the Diode

FIGURE 6. SCHEMATIC DIAGRAM SHOWING ONE TRANSISTOR OF THE CA3082 DRIVING A LIGHT EMITTING DIODE (LED)

HARRIS SEMICONDUCTOR

CA3083

General Purpose High Current N-P-N Transistor Array

March 1993

Features

- High I_C ..... 100mA Max
- Low $V_{CE\ sat}$ (at 50mA) ..... 0.7V Max
- Matched Pair (Q_1 and Q_2)
  - V_{IO} (V_{BE} Matched) ..... ±5mV Max
  - I_{IO} (at 1mA) ..... 2.5μA Max
- 5 Independent Transistors Plus Separate Substrate Connection

Applications

- Signal Processing and Switching Systems Operating from DC to VHF
- Lamp and Relay Driver
- Differential Amplifier
- Temperature Compensated Amplifier
- Thyristor Firing
- See Application Note AN5296 "Applications of the CA3018 Circuit Transistor Array" for Suggested Applications

Description

The CA3083 is a versatile array of five high current (to 100mA) n-p-n transistors on a common monolithic substrate. In addition, two of these transistors (Q_1 and Q_2) are matched at low current (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design.

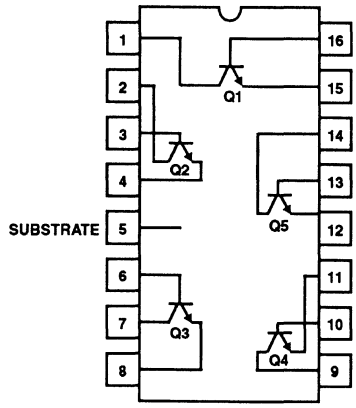
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3083	-55°C to +125°C	16 Lead Plastic DIP
CA3083F	-55°C to +125°C	16 Lead Ceramic DIP
CA3083M	-55°C to +125°C	16 Lead Narrow Body SOIC
CA3083M96	-55°C to +125°C	16 Lead Narrow Body SOIC*

* Denotes Tape and Reel

Pinout

CA3083
(PDIP, CDIP 150mil SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 481.2

Absolute Maximum Ratings (T_A = +25°C)

The following ratings apply for each transistor in the device:
Collector-to-Emitter Voltage, V_{CEO} 15V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
Emitter-to-Base Voltage, V_{EBO} 5V
Collector Current (I_C) 100mA
Base Current (I_B) 20mA
Power Dissipation
Any One Transistor 500mW
Total Package 750mW
T_A > +55°C ..... Derate at 6.67mW/°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -55°C ≤ T_A ≤ +125°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C. For Equipment Design

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
FOR EACH TRANSISTOR						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100µA, I_E = 0	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100µA, I_B = 0, I_E = 0	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500µA, I_C = 0	5	6.9	-	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	-	-	10	µA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	-	-	1	µA
DC Forward-Current Transfer Ratio (Note 2) (Figure 1)	h_{FE}	V_{CE} = 3V, I_C = 10mA	40	76	-	
		I_C = 50mA	40	75	-	
Base-to-Emitter Voltage (Figure 2)	V_{BE}	V_{CE} = 3V, I_C = 10mA	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage (Figures 3, 4)	$V_{CE\ SAT}$	I_C = 50mA, I_B = 5mA	-	0.40	0.70	V
Gain Bandwidth Product	f_T	V_{CE} = 3V, I_C = 10mA	-	450	-	MHz
FOR TRANSISTORS Q1 AND Q2 (As a Differential Amplifier)						
Absolute Input Offset Voltage (Figure 6)	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	-	1.2	5	mV
Absolute Input Offset Current (Figure 7)	$\lvert I_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	-	0.7	2.5	µA

NOTE:

1. The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.
2. Actual forcing current is via the emitter for this test.

Typical Performance Curves

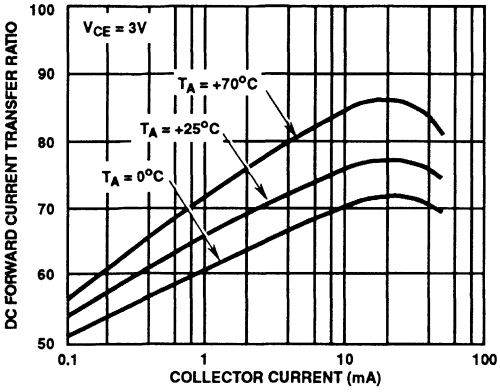


FIGURE 1. h_{FE} vs I_C

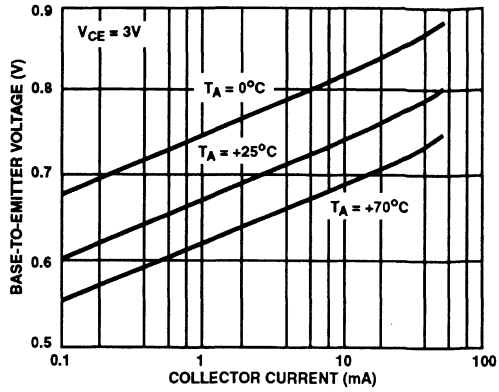


FIGURE 2. V_{BE} vs I_C

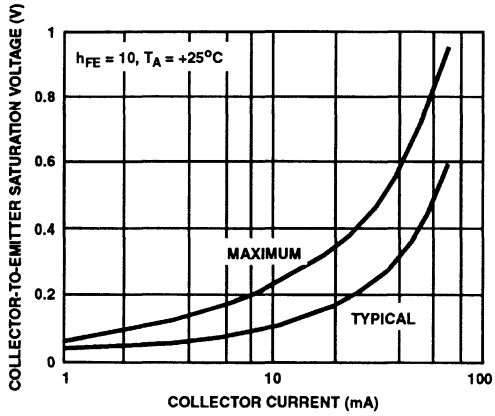


FIGURE 3. $V_{CE\ SAT}$ vs I_C AT +25°C

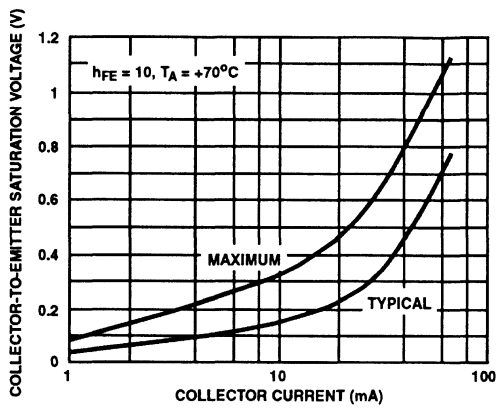


FIGURE 4. $V_{CE\ SAT}$ vs I_C AT +70°C

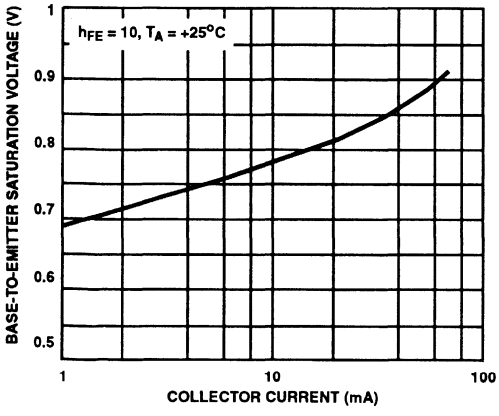


FIGURE 5. $V_{BE\ SAT}$ vs I_C

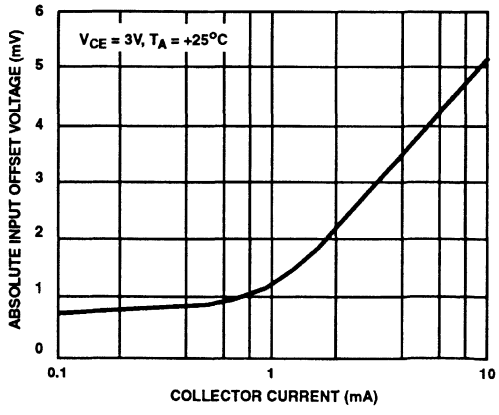


FIGURE 6. V_{IO} vs I_C (TRANSISTORS Q1 AND Q2 AS A DIFFERENTIAL AMPLIFIER)

Typical Performance Curves (Continued)

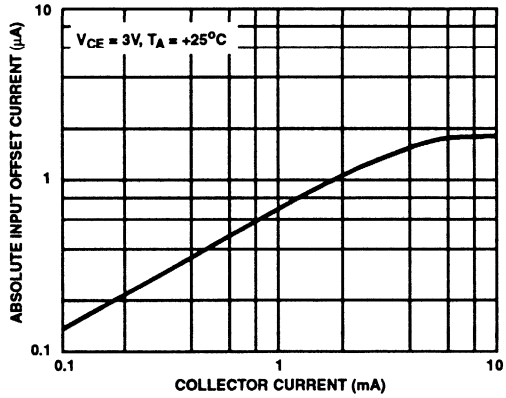


FIGURE 7. I_{IO} vs I_C (TRANSISTORS Q1 AND Q2 AS A DIFFERENTIAL AMPLIFIER)

HARRIS SEMICONDUCTOR

CA3086

General Purpose N-P-N Transistor Array

March 1993

Applications

- **Three Isolated Transistors and One Differentially Connected Transistor Pair For Low-Power Applications from DC to 120 MHz**
- **General-Purpose Use In Signal Processing Systems Operating in the DC to 190MHz Range**
- **Temperature Compensated Amplifiers**
- **See Application Note, AN5296 "Application of the CA3018 Integrated-Circuit Transistor Array"' for Suggested Applications**

Description

The CA3086 consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching.

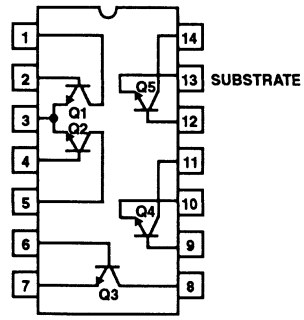
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3086	-55°C to +125°C	14 Lead Plastic DIP
CA3086M	-55°C to +125°C	14 Lead SOIC
CA3086M96	-55°C to +125°C	14 Lead SOIC*
CA3086F	-55°C to +125°C	14 Lead Ceramic DIP

* Denotes Tape and Reel

Pinout

CA3086
(PDIP, CDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **483.2**

Absolute Maximum Ratings

Power Dissipation
- Any one transistor 300mW
- Total package up to T_A = +55°C 750mW
- Above T_A = +55°C ..... Derate linearly 6.67 mW/°C

Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C
The following ratings apply for each transistor in the device:
- Collector-to-Emitter Voltage, V_{CEO} 15V
- Collector-to-Base Voltage, V_{CBO} 20V
- Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
- Emitter-to-Base Voltage, V_{EBO} 5V
- Collector Current, I_C 50mA

Operating Conditions

Ambient Temperature Range
- Operating ..... -55°C to +125°C
- Storage ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C, For Equipment Design

PARAMETERS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10μA, I_E = 0	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10μA, I_{CI} = 0	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0	5	7	-	V
Collector-Cutoff Current (Figure 1)	I_{CBO}	V_{CB} = 10V, I_E = 0,	-	0.002	100	nA
Collector-Cutoff Current (Figure 2)	I_{CEO}	V_{CE} = 10V, I_B = 0,	-	(Figure 2)	5	μA
DC Forward-Current Transfer Ratio (Figure 3)	h_{FE}	V_{CE} = 3V, I_C = 1mA	40	100	-	

NOTE:

1. The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

Electrical Specifications T_A = +25°C, Typical Values Intended Only for Design Guidance

PARAMETERS	SYMBOLS	TEST CONDITIONS		TYPICAL VALUES	UNITS
DC Forward-Current Transfer Ratio (Figure 3)	h_{FE}	V_{CE} = 3V	I_C = 10mA	100	
			I_C = 10μA	54	
Base-to-Emitter Voltage (Figure 4)	V_{BE}	V_{CE} = 3V	I_E = 1 mA	0.715	V
			I_E = 10mA	0.800	V
V_{BE} Temperature Coefficient (Figure 5)	$\Delta V_{BE}/\Delta T$	V_{CE} = 3V, I_C = 1 mA		-1.9	mV/°C
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	I_B = 1mA, I_C = 10mA		0.23	V
Noise Figure (Low Frequency)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100μA, R_S = 1kΩ		3.25	dB

Electrical Specifications T_A = +25°C, Typical Values Intended Only for Design Guidance **(Continued)**

PARAMETERS	SYMBOLS	TEST CONDITIONS	TYPICAL VALUES	UNITS
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:		f = 1kHz, V_{CE} = 3V, I_C = 1mA		
Forward Current-Transfer Ratio (Figure 6)	h_{FE}		100	-
Short-Circuit Input Impedance (Figure 6)	h_{IE}		3.5	kΩ
Open-Circuit Output Impedance (Figure 6)	h_{OE}		15.6	μmho
Open-Circuit Reverse-Voltage Transfer Ratio (Figure 6)	h_{RE}		1.8×10^{-4}	-
Admittance Characteristics:		f = 1MHz, V_{CE} = 3V, I_C = 1mA		
Forward Transfer Admittance (Figure 7)	y_{FE}		31 - j1.5	mmho
Input Admittance (Figure 8)	y_{IE}		0.3 + j0.04	mmho
Output Admittance (Figure 9)	y_{OE}		0.001 + j0.03	mmho
Reverse Transfer Admittance (Figure 10)	y_{RE}		See Figure 10	-
Gain-Bandwidth Product (Figure 11)	f_T	V_{CE} = 3V, I_C = 3mA	550	MHz
Emitter-to-Base Capacitance	C_{EBO}	V_{EB} = 3V, I_E = 0	0.6	pF
Collector-to-Base Capacitance	C_{CBO}	V_{CB} = 3V, I_C = 0	0.58	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 3V, I_C = 0	2.8	pF

Typical Static Characteristics for Each Transistor

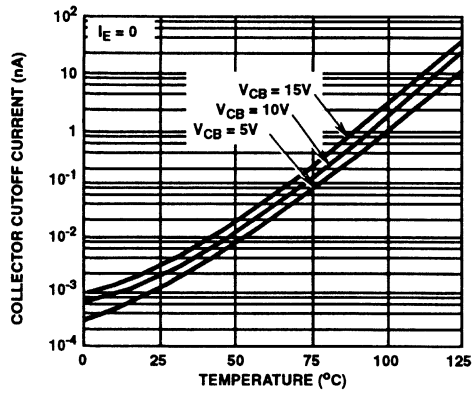


FIGURE 1. I_{CBO} vs TEMPERATURE

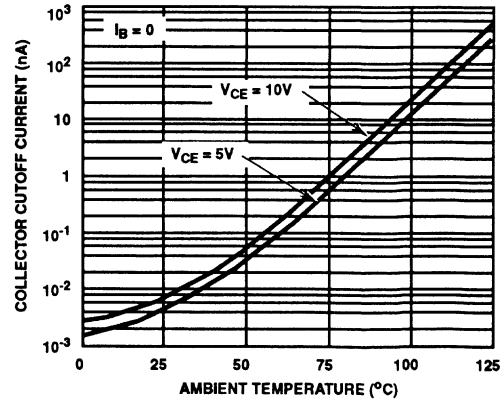


FIGURE 2. I_{CEO} vs TEMPERATURE

Typical Static Characteristics for Each Transistor (Continued)

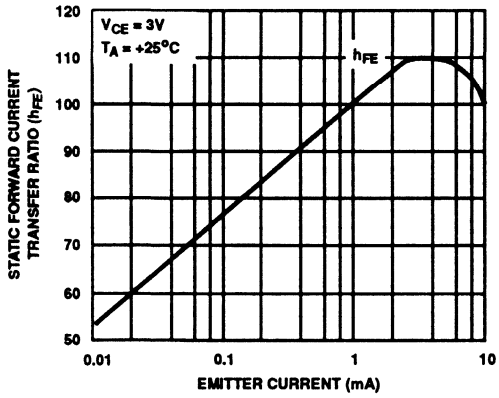


FIGURE 3. h_{FE} vs I_E

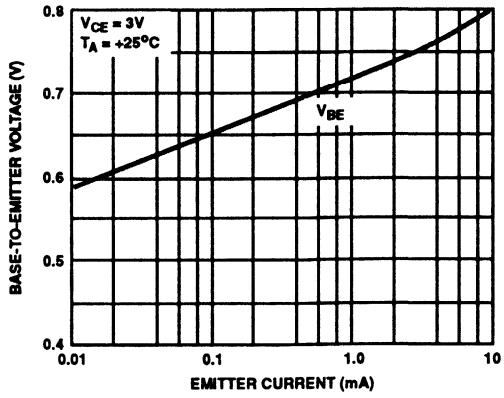


FIGURE 4. V_{BE} vs I_E

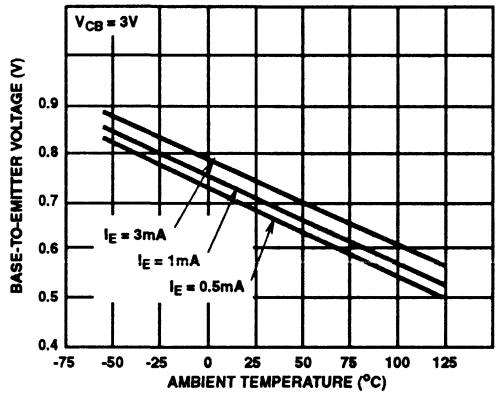


FIGURE 5. V_{BE} vs TEMPERATURE

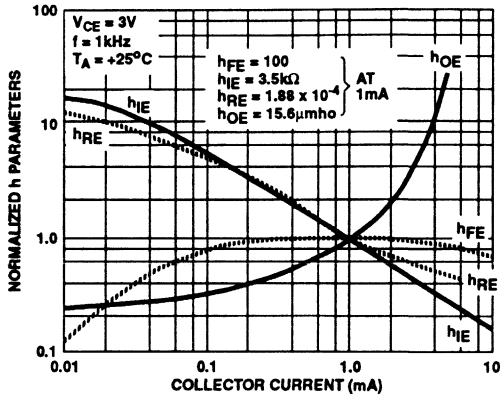


FIGURE 6. NORMALIZED h_{FE}, h_{IE}, h_{RE}, h_{OE} vs I_C

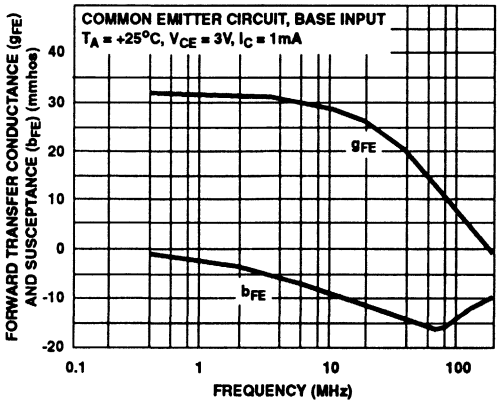


FIGURE 7. y_{FE} vs FREQUENCY

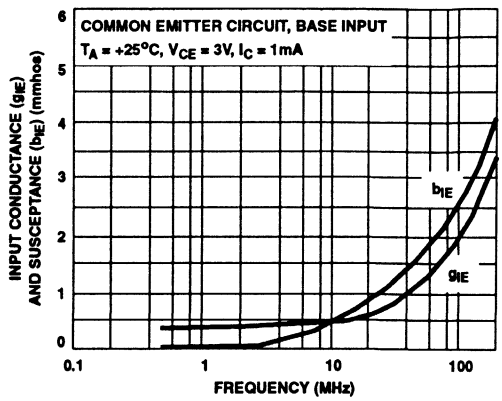


FIGURE 8. y_{IE} vs FREQUENCY

Typical Static Characteristics for Each Transistor (Continued)

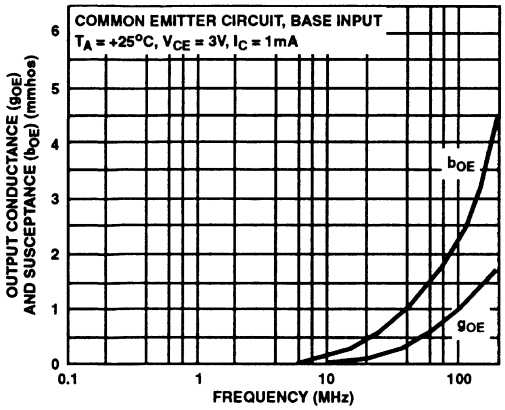


FIGURE 9. y_{OE} vs FREQUENCY

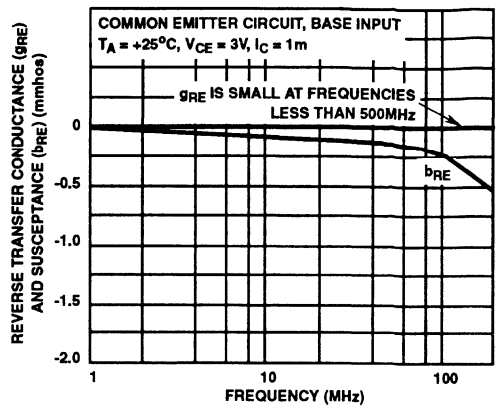


FIGURE 10. y_{RE} vs FREQUENCY

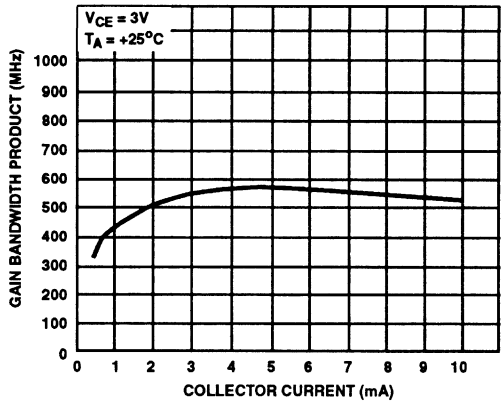


FIGURE 11. f_T vs I_C

HARRIS SEMICONDUCTOR

CA3096

March 1993

N-P-N/P-N-P Transistor Array

Applications

- **Five-Independent Transistors**
  - **Three N-P-N and**
  - **Two P-N-P**
- **Differential Amplifiers**
- **DC Amplifiers**
- **Sense Amplifiers**
- **Level Shifters**
- **Timers**
- **Lamp and Relay Drivers**
- **Thyristor Firing Circuits**
- **Temperature Compensated Amplifiers**
- **Operational Amplifiers**

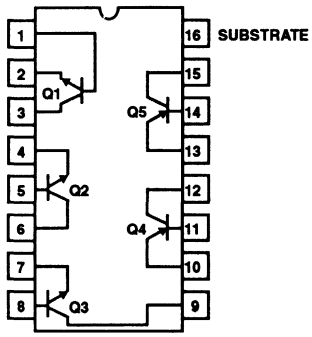
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3096AE	-55°C to +125°C	16 Lead Plastic DIP
CA3096AM	-55°C to +125°C	16 Lead Narrow Body SOIC
CA3096AM96	-55°C to +125°C	16 Lead Narrow Body SOIC*
CA3096CE	-55°C to +125°C	16 Lead Plastic DIP
CA3096E	-55°C to +125°C	16 Lead Plastic DIP
CA3096M	-55°C to +125°C	16 Lead Narrow Body SOIC
CA3096M96	-55°C to +125°C	16 Lead Narrow Body SOIC*

* Denotes Tape and Reel

Pinout

CA3096, CA3096A, CA3096C
(PDIP, 150 mil SOIC)
TOP VIEW



Description

The CA3096C, CA3096, and CA3096A are general purpose high voltage silicon transistor arrays. Each array consists of five independent transistors (two p-n-p and three n-p-n types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096A, CA3096, and CA3096C are identical, except that the CA3096A specifications include parameter matching and greater stringency in I_{CBO}, I_{CEO}, and V_{CE}(SAT). The CA3096C is a relaxed version of the CA3096.

CA3096A, CA3096, CA3096C Essential Differences

CHARACTERISTIC		CA3096A	CA3096	CA3096C
$V_{(BR)CEO}$ (V) Min				
	n-p-n	35	35	24
	p-n-p	-40	-40	-24
$V_{(BR)CBO}$ (V) Min.				
	n-p-n	45	45	30
	p-n-p	-40	-40	-24
h_{FE} at 1mA				
	n-p-n	150-500	150-500	100-670
	p-n-p	20-200	20-200	15-200
h_{FE} at 100μA				
	p-n-p	40-250	40-250	30-300
I_{CBO} (nA) Max.				
	n-p-n	40	100	100
	p-n-p	-40	-100	-100
I_{CEO} (nA) Max.				
	n-p-n	100	1000	1000
	p-n-p	-100	-1000	-1000
$V_{CE\ SAT}$ (V) Max.				
	n-p-n	0.5	0.7	0.7
$\|V_{IO}\|$ (mV)Max.				
	n-p-n	5	-	-
	p-n-p	5	-	-
$\|I_{IO}\|$ (μA) Max.				
	n-p-n	0.6	-	-
	p-n-p	0.25	-	-

6 TRANSISTOR AND DIODE ARRAYS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **595.2**

Absolute Maximum Ratings

	N-P-N	P-N-P
Collector-to-Emitter Voltage, V_{CEO}		
CA3096, CA3096A	35V	-40V
CA3096C	24V	-24V
Collector-to-Base Voltage, V_{CBO}		
CA3096, CA3096A	45V	-40V
CA3096C	30V	-24V
Collector-to-Substrate Voltage, V_{CIO} (Note 1)		
CA3096, CA3096A	45V	-
CA3096C	30V	-
Emitter-to-Substrate Voltage, V_{EIO}		
CA3096, CA3096A	-	-40V
CA3096C	-	-24V
Emitter-to-Base Voltage, V_{EBO}		
CA3096, CA3096A	6V	-40V
CA3096C	6V	-24V
Collector Current, I_C (All Types)	50mA	-10mA
Power Dissipation, P_D (Up to T_A = +55°C)		
Device (Total)	750mW	
Each Transistor	200mW	
Above T_A = +55°C	Derate Linearly at 6.67mW/°C	
Junction Temperature (Plastic Packages)	+150°C	
Lead Temperature (Soldering 10 Sec.)	+300°C	

Operating Conditions

Operating Temperature Range . . . . . -55°C ≤ T_A ≤ +125°C
Storage Temperature Range . . . . . -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications T_A = +25°C

For Equipment Design

PARAMETERS	TEST CONDITIONS	LIMITS									UNITS
		CA3096A			CA3096			CA3096C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
FOR EACH N-P-N TRANSISTOR											
I_{CBO}	V_{CB} = 10V, I_E = 0	-	0.001	40	-	0.001	100	-	0.001	100	nA
I_{CEO}	V_{CE} =10V, I_B = 0	-	0.006	100	-	0.006	1000	-	0.006	1000	nA
$V_{(BR)CEO}$	I_C =1mA, I_B = 0	35	50	-	35	50	-	24	35	-	V
$V_{(BR)CBO}$	I_C =10μA, I_E = 0	45	100	-	45	100	-	30	80	-	V
$V_{(BR)CIO}$	I_{CI} = 10μA, I_B = I_E = 0	45	100	-	45	100	-	30	80	-	V
$V_{(BR)EBO}$	I_E = 10μA, I_C = 0	6	8	-	6	8	-	6	8	-	V
V_Z	I_Z = 10μA	6	7.9	9.8	6	7.9	9.8	6	7.9	9.8	V
$V_{CE\ SAT}$	I_C =10mA, I_B = 1mA	-	0.24	0.5	-	0.24	0.7	-	0.24	0.7	V
V_{BE} (Note 2)	I_C =1mA, V_{CE} = 5V	0.6	0.69	0.78	0.6	0.69	0.78	0.6	0.69	0.78	V
h_{FE} (Note 2)		150	390	500	150	390	500	100	390	670	

Static Electrical Specifications T_A = +25°C **(Continued)**

For Equipment Design

PARAMETERS	TEST CONDITIONS	LIMITS									UNITS
		CA3096A			CA3096			CA3096C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\lvert\Delta V_{BE}/\Delta T\rvert$ (Note 2)	I_C = 1mA, V_{CE} = 5V	-	1.9	-	-	1.9	-	-	1.9	-	mV/°C
FOR EACH P-N-P TRANSISTOR											
I_{CBO}	V_{CB} = -10V, I_E = 0	-	-0.006	-40	-	-0.06	-100	-	-0.06	-100	nA
I_{CEO}	V_{CE} = -10V, I_B = 0	-	-0.12	-100	-	-0.12	-1000	-	-0.12	-1000	nA
$V_{(BR)CEO}$	I_C = -100µA, I_B = 0	-40	-75	-	-40	-75	-	-24	-30	-	V
$V_{(BR)CBO}$	I_C = -10µA, I_E = 0	-40	-80	-	-40	-80	-	-24	-60	-	V
$V_{(BR)EBO}$	I_E = -10µA, I_C = 0	-40	-100	-	-40	-100	-	-24	-80	-	V
$V_{(BR)EIO}$	I_{EI} = 10µA, $I_B = I_C$ = 0	40	100	-	40	100	-	24	80	-	V
$V_{CE\ SAT}$	I_C = -1mA, I_B = -100µA	-	-0.16	-0.4	-	-0.16	-0.4	-	-0.16	-0.4	V
V_{BE} (Note 2)	I_C = -100µA, V_{CE} = -5V	-0.5	-0.6	-0.7	-0.5	-0.6	-0.7	-0.5	-0.6	-0.7	V
h_{FE} (Note 2)	I_C = -100µA, V_{CE} = -5V	40	85	250	40	85	250	30	85	300	
	I_C = -1mA, V_{CE} = -5V	20	47	200	20	47	200	15	47	200	
$\lvert\Delta V_{BE}/\Delta T\rvert$ (Note 2)	I_C = -100µA, V_{CE} = -5V	-	2.2	-	-	2.2	-	-	2.2	-	mV/°C

I_{CBO}	Collector-Cutoff Current	V_Z	Emitter-to-Base Zener Voltage
I_{CEO}	Collector-Cutoff Current	$V_{CE\ SAT}$	Collector-to-Emitter Saturation Voltage
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	V_{BE}	Base-to-Emitter Voltage
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	h_{FE}	DC Forward-Current Transfer Ratio
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	$\lvert\Delta V_{BE}/\Delta T\rvert$	Magnitude of Temperature Coefficient: (for each transistor)
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage		

NOTE:

1. The collector of each transistor of the CA3096 is isolated from the substrate by an integral diode. The substrate (terminal 16) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. Actual forcing current is via the emitter for this test.

Static Electrical Specifications T_A = +25°C (CA3096A Only)

For Equipment Design

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS CA3096A MIN	TYP	MAX	UNITS
FOR TRANSISTORS Q1 AND Q2 (AS A DIFFERENTIAL AMPLIFIER)						
Absolute Input Offset Voltage	$\|V_{IO}\|$	V_{CE} = 5V, I_C = 1mA	-	0.3	5	mV
Absolute Input Offset Current	$\|I_{IO}\|$		-	0.07	0.6	µA
Absolute Input Offset Voltage Temperature Coefficient	$\frac{\|\Delta V_{IO}\|}{\Delta T}$		-	1.1	-	µV/°C
FOR TRANSISTORS Q4 AND Q5 (AS A DIFFERENTIAL AMPLIFIER)						
Absolute Input Offset Voltage	$\|V_{IO}\|$	V_{CE} = -5V, I_C = -100µA, R_S = 0	-	0.15	5	mV
Absolute Input Offset Current	$\|I_{IO}\|$		-	2	250	nA
Absolute Input Offset Voltage Temperature Coefficient	$\frac{\|\Delta V_{IO}\|}{\Delta T}$		-	0.54	-	µV/°C

Dynamic Electrical Specifications T_A = +25°C

Typical Values Intended Only for Design Guidance

PARAMETERS	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
FOR EACH N-P-N TRANSISTOR				
Noise Figure (Low Frequency)	NF	f = 1kHz, V_{CE} = 5V, I_C = 1mA, R_S = 1kΩ	2.2	dB
Low-Frequency, Input Resistance	R_I	f = 1.0kHz, V_{CE} = 5V I_C = 1 mA	10	kΩ
Low-Frequency Output Resistance	R_O	f = 1.0kHz, V_{CE} = 5V I_C = 1 mA	80	kΩ
Admittance Characteristics				
Forward Transfer Admittance	y_{FE} g_{FE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	7.5	mmho
	y_{FE} b_{FE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	-j13	mmho
Input Admittance	y_{IE} g_{IE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	2.2	mmho
	y_{IE} b_{IE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	j3.1	mmho
Output Admittance	y_{OE} g_{OE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	0.76	mmho
	y_{OE} b_{OE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	j2.4	mmho
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 1.0mA	280	MHz
		V_{CE} = 5V, I_C = 5mA	335	MHz
Emitter-To-Base Capacitance	C_{EB}	V_{EB} = 3V	0.75	pF
Collector-To-Base Capacitance	C_{CB}	V_{CB} = 3V	0.46	pF
Collector-To-Substrate Capacitance	C_{CI}	V_{CI} = 3V	3.2	pF

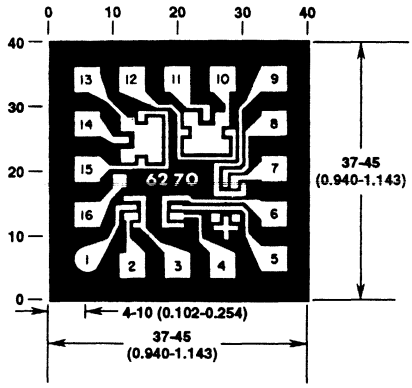
Dynamic Electrical Specifications T_A = +25°C

Typical Values Intended Only for Design Guidance

PARAMETERS	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
FOR EACH P-N-P TRANSISTOR				
Noise Figure (Low Frequency)	NF	f = 1kHz, I_C = 100μA, R_S = 1kΩ	3	dB
Low-Frequency Input Resistance	R_I	f = 1kHz, V_{CE} = 5V, I_C = 100μA	27	kΩ
Low-Frequency Output Resistance	R_O	f = 1kHz, V_{CE} = 5V, I_C = 100μA	680	kΩ
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 100μA	6.8	MHz
Emitter-To-Base Capacitance	C_{EB}	V_{EB} = -3V	0.85	pF
Collector-To-Base Capacitance	C_{CB}	V_{CB} = -3V	2.25	pF
Base-To-Substrate Capacitance	C_{BI}	V_{BI} = 3V	3.05	pF

Metallization Mask Layout

CA3096H



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

Typical Performance Curves

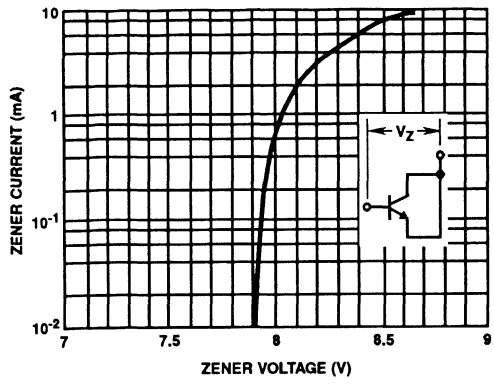


FIGURE 1. BASE-TO-EMITTER ZENER CHARACTERISTIC (N-P-N)

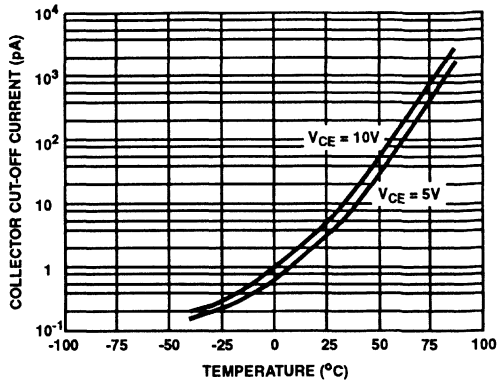


FIGURE 2. COLLECTOR CUT-OFF CURRENT (I_{CEO}) vs TEMPERATURE (N-P-N)

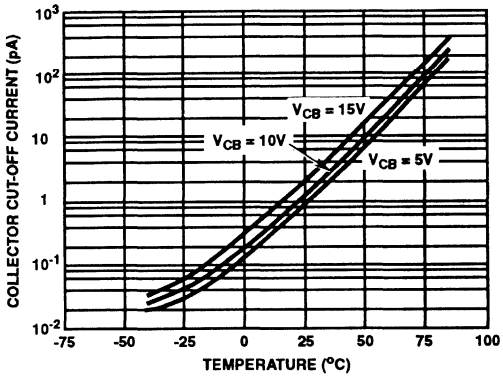


FIGURE 3. COLLECTOR CUT-OFF CURRENT (I_{CBO}) vs TEMPERATURE (N-P-N)

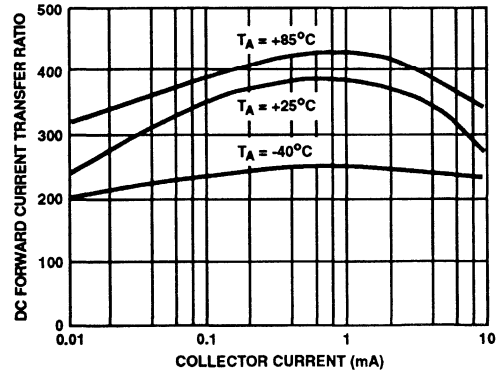


FIGURE 4. TRANSISTOR (N-P-N) h_{FE} vs COLLECTOR CURRENT

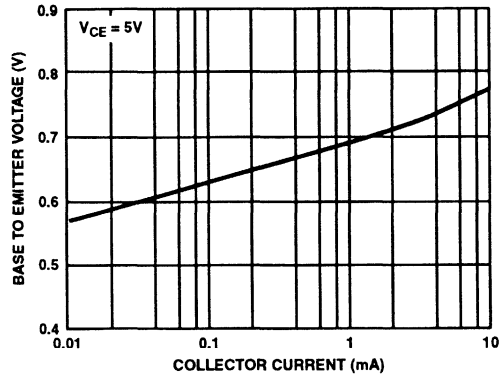


FIGURE 5. V_{BE} (N-P-N) vs COLLECTOR CURRENT

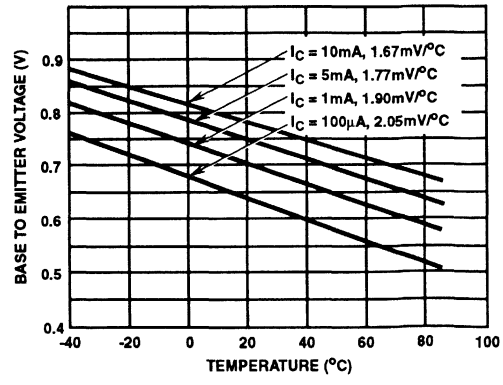


FIGURE 6. V_{BE} (N-P-N) vs TEMPERATURE

Typical Performance Curves (Continued)

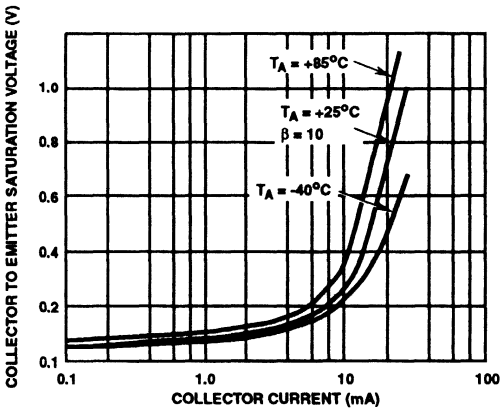


FIGURE 7. $V_{CE\ SAT}$ (N-P-N) vs COLLECTOR CURRENT

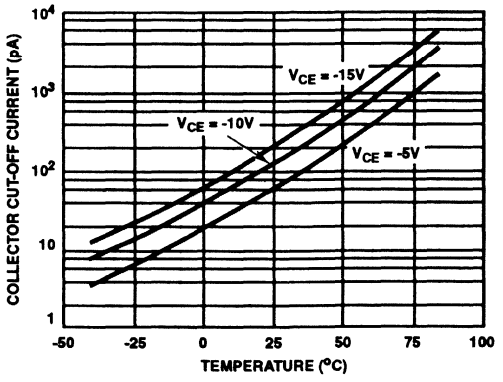


FIGURE 8. COLLECTOR CUT-OFF CURRENT (I_{CEO}) vs TEMPERATURE (P-N-P)

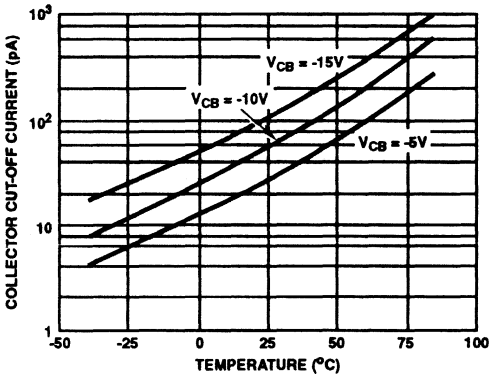


FIGURE 9. COLLECTOR CUT-OFF CURRENT (I_{CBO}) vs TEMPERATURE (P-N-P)

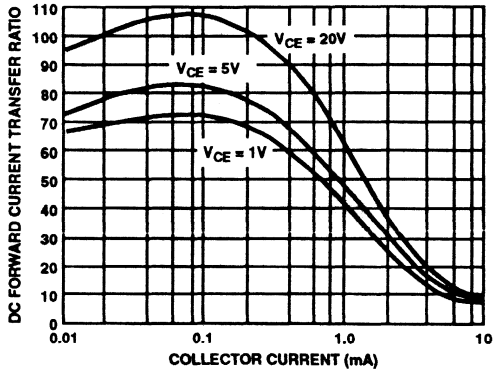


FIGURE 10. TRANSISTOR (P-N-P) h_{FE} vs COLLECTOR CURRENT

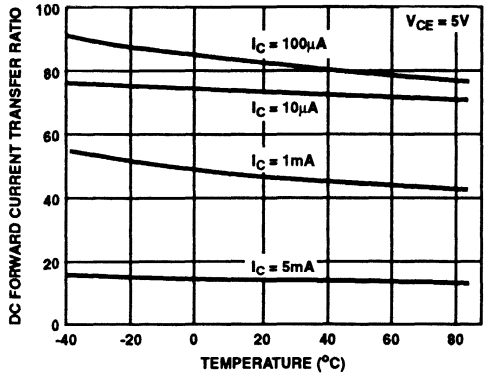


FIGURE 11. TRANSISTOR (P-N-P) h_{FE} vs TEMPERATURE

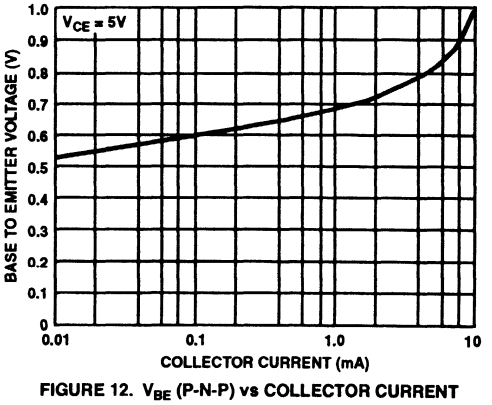


FIGURE 12. V_{BE} (P-N-P) vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

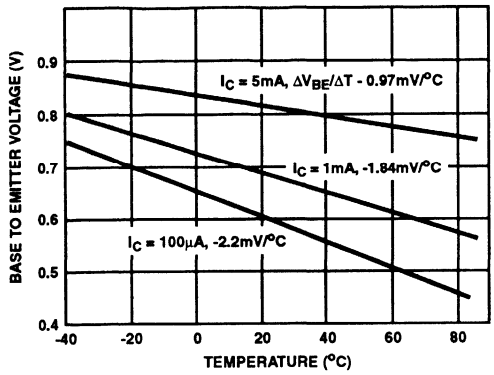


FIGURE 13. V_{BE} (P-N-P) vs TEMPERATURE

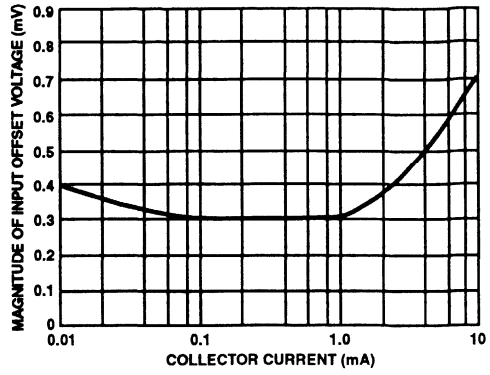


FIGURE 14. MAGNITUDE OF INPUT OFFSET VOLTAGE $|V_{IO}|$ vs COLLECTOR CURRENT FOR N-P-N TRANSISTOR Q1 - Q2

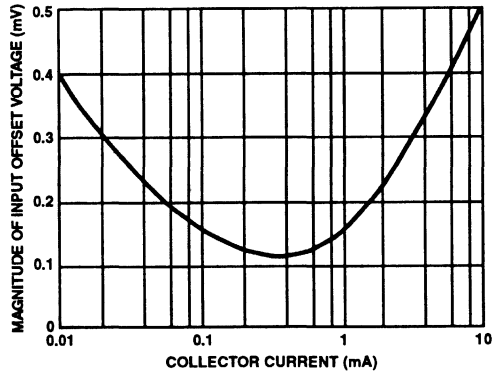


FIGURE 15. MAGNITUDE OF INPUT OFFSET VOLTAGE $|V_{IO}|$ vs COLLECTOR CURRENT FOR P-N-P TRANSISTOR Q4 - Q5

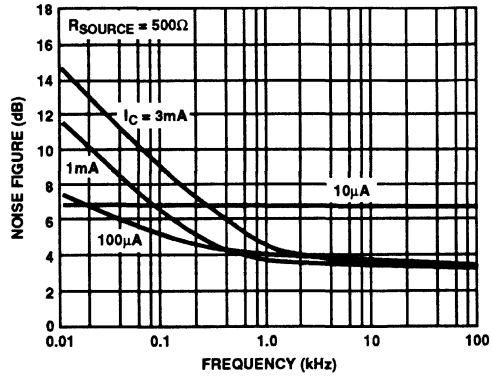


FIGURE 16. NOISE FIGURE vs FREQUENCY FOR N-P-N TRANSISTORS

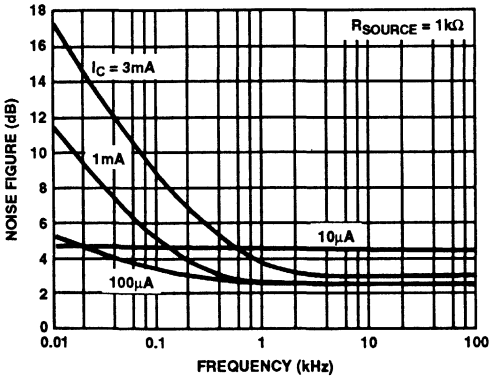


FIGURE 17. NOISE FIGURE vs FREQUENCY FOR N-P-N TRANSISTORS

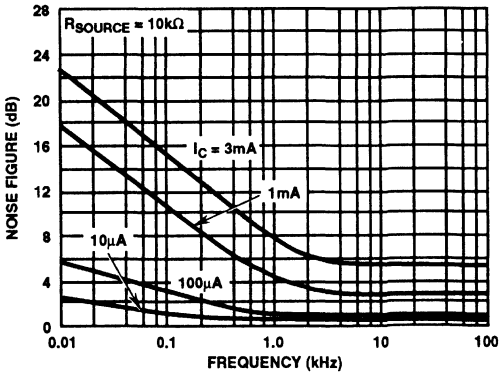


FIGURE 18. NOISE FIGURE vs FREQUENCY FOR N-P-N TRANSISTORS

Typical Performance Curves (Continued)

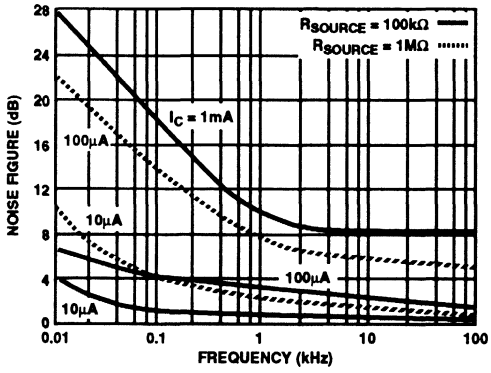


FIGURE 19. NOISE FIGURE vs FREQUENCY FOR N-P-N TRANSISTORS

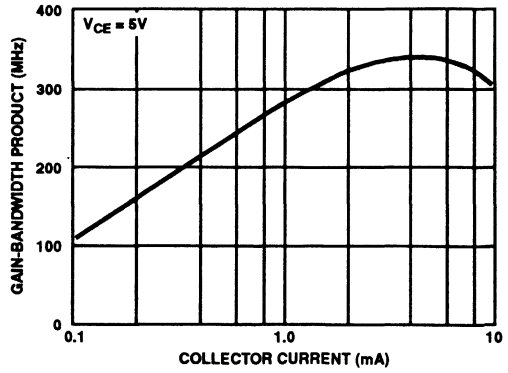


FIGURE 20. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT (N-P-N)

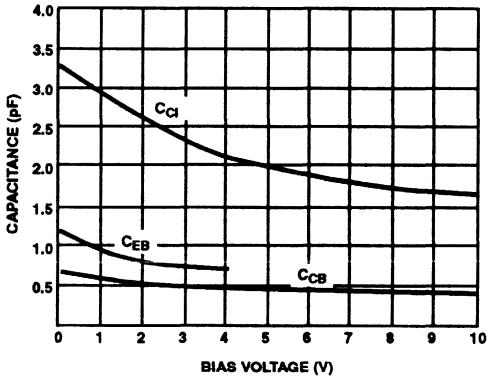


FIGURE 21. CAPACITANCE vs BIAS VOLTAGE (N-P-N)

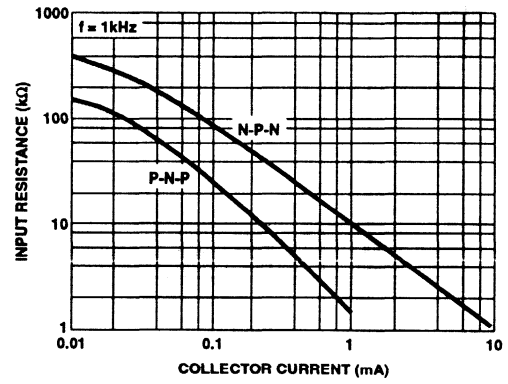


FIGURE 22. INPUT RESISTANCE vs COLLECTOR CURRENT

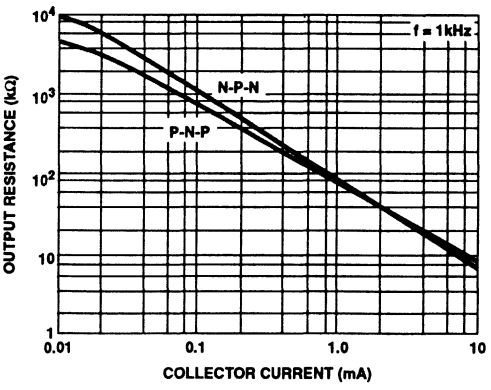


FIGURE 23. OUTPUT RESISTANCE vs COLLECTOR CURRENT

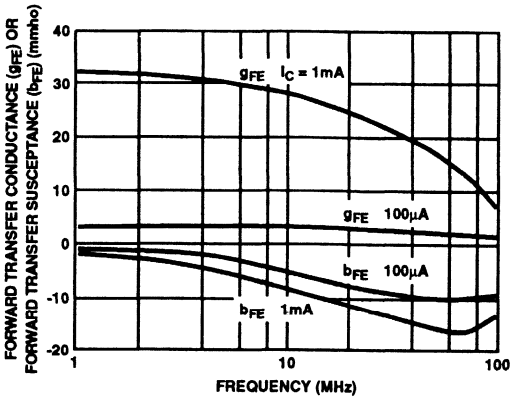


FIGURE 24. FORWARD TRANSCONDUCTANCE vs FREQUENCY

Typical Performance Curves (Continued)

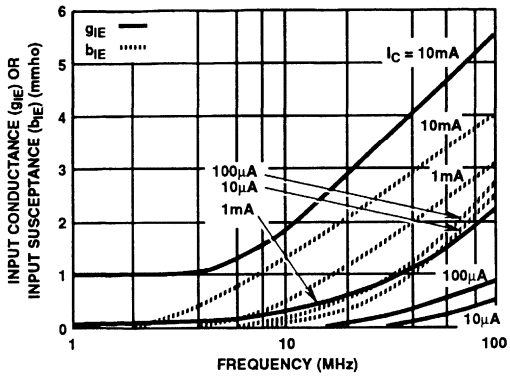


FIGURE 25. INPUT ADMITTANCE vs FREQUENCY

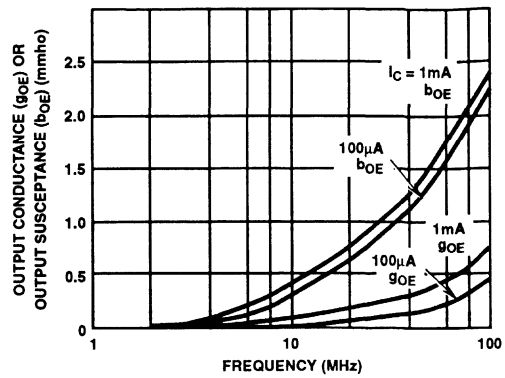


FIGURE 26. OUTPUT ADMITTANCE vs FREQUENCY

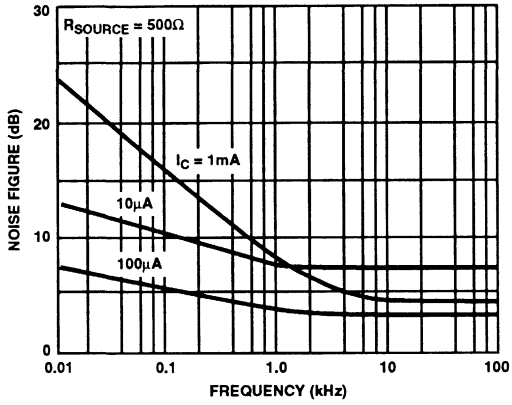


FIGURE 27. NOISE FIGURE vs FREQUENCY (P-N-P)

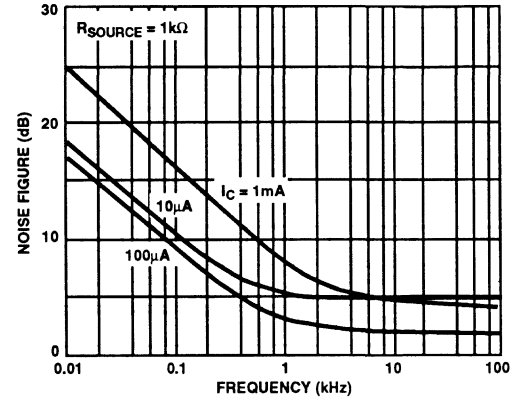


FIGURE 28. NOISE FIGURE vs FREQUENCY (P-N-P)

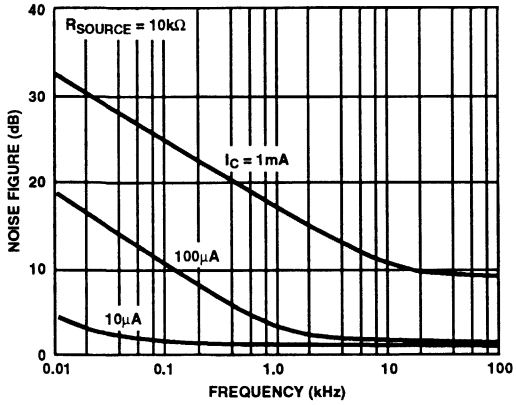


FIGURE 29. NOISE FIGURE vs FREQUENCY (P-N-P)

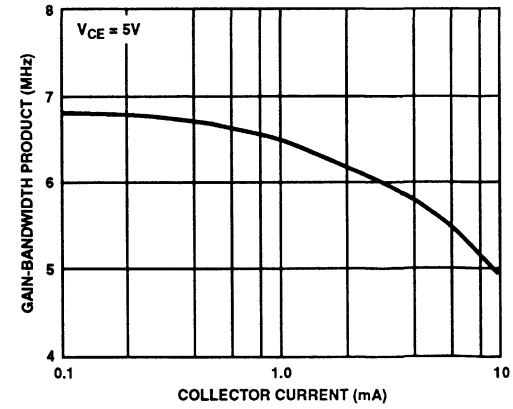


FIGURE 30. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT (P-N-P)

Typical Performance Curves (Continued)

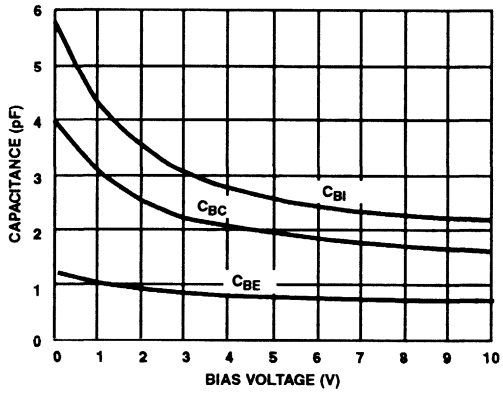


FIGURE 31. CAPACITANCE vs BIAS VOLTAGE (P-N-P)

Typical Applications

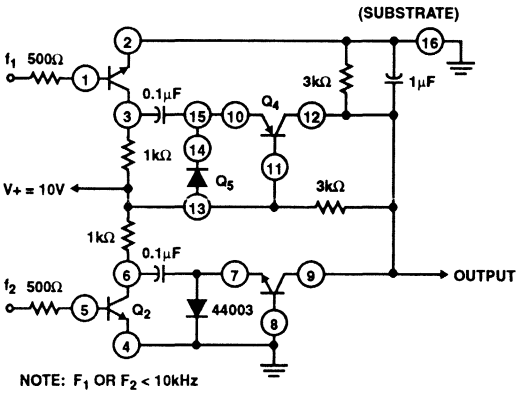


FIGURE 32. FREQUENCY COMPARATOR USING CA3096

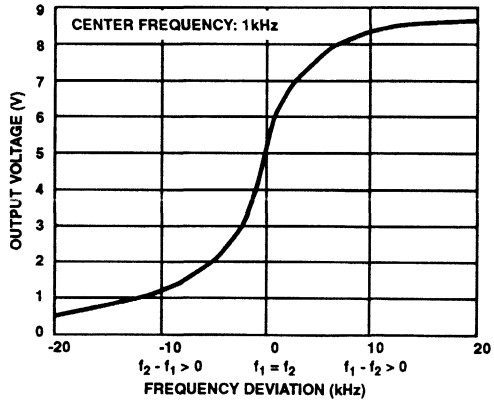


FIGURE 33. FREQUENCY COMPARATOR CHARACTERISTICS

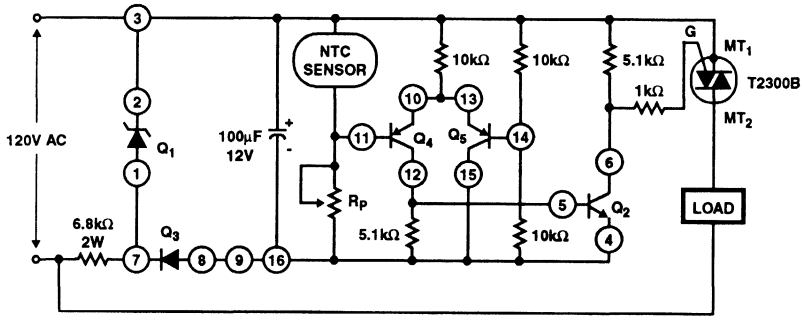


FIGURE 34. LINE-OPERATED LEVEL SWITCH USING CA3096A OR CA3096

Typical Applications (Continued)

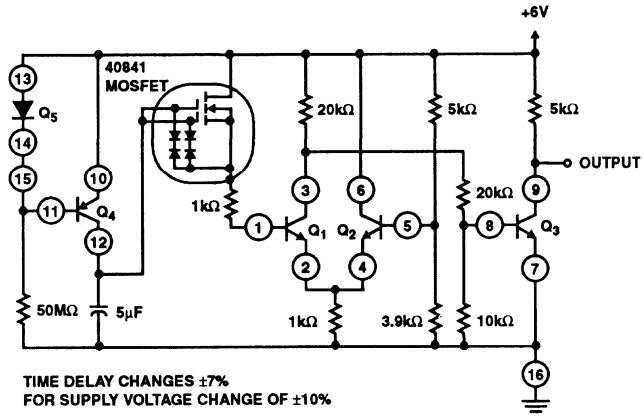
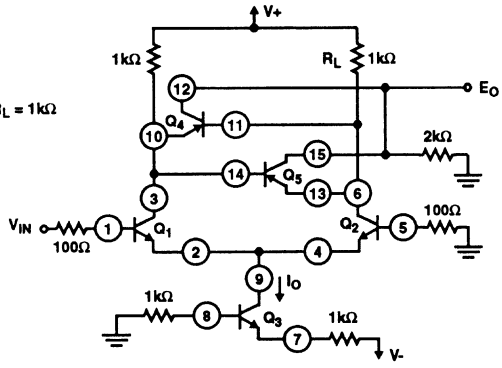


FIGURE 35. ONE-MINUTE TIMER USING CA3096A AND A MOSFET

$$V_T = \pm \frac{36}{I_O R_L}$$

IF I_O = 1mA AND R_L = 1kΩ
V_T = ± 36mV



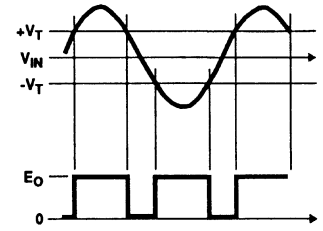


FIGURE 36. CA3096A SMALL-SIGNAL ZERO VOLTAGE DETECTOR HAVING NOISE IMMUNITY

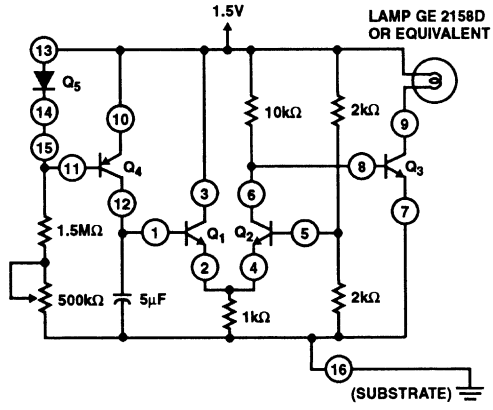
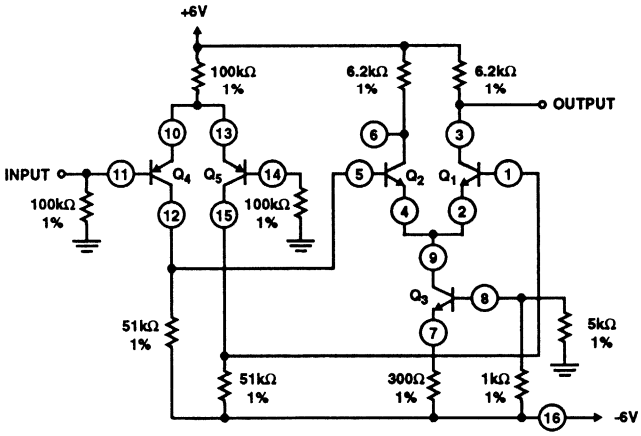


FIGURE 37. TEN-SECOND TIMER OPERATED FROM 1.5V SUPPLY USING CA3096

Typical Applications (Continued)



NOTES:

1. Can be operated with either dual supply or single supply.
2. Wide-input common mode range +5V to -5V.
3. Low bias current: <1μA.

FIGURE 38. CASCADE OF DIFFERENTIAL AMPLIFIERS USING CA3096A

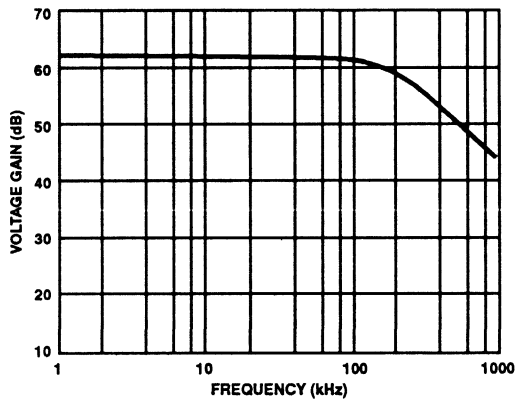


FIGURE 39. GAIN-FREQUENCY CHARACTERISTICS

HARRIS SEMICONDUCTOR

CA3127

March 1993

High Frequency N-P-N Transistor Array

Features

- Gain Bandwidth Product (f_T) . . . . . >1GHz
- Power Gain . . . . . 30dB (Typ) at 100MHz
- Noise Figure . . . . . 3.5dB (Typ) at 100MHz
- Five Independent Transistors on a Common Substrate

Applications

- VHF Amplifiers
- Multifunction Combinations - RF/Mixer/Oscillator
- Sense Amplifiers
- Synchronous Detectors
- VHF Mixers
- IF Converter
- IF Amplifiers
- Synthesizers
- Cascade Amplifiers

Description

The CA3127* consists of five general purpose silicon n-p-n transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1GHz, making the CA3127 useful from DC to 500MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127 provides close electrical and thermal matching of the five transistors.

* Formerly Development Number TA6206.

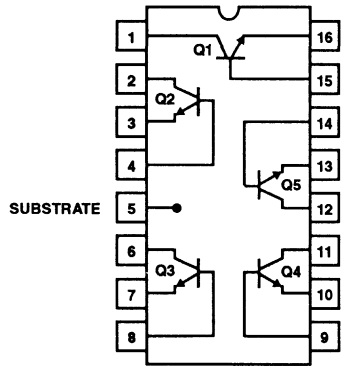
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3127E	-55°C to +125°C	16 Lead Plastic DIP
CA3127F	-55°C to +125°C	16 Lead Ceramic DIP
CA3127M	-55°C to +125°C	16 Lead Narrow Body SOIC
CA3127M96	-55°C to +125°C	16 Lead Narrow Body SOIC*

* Denotes Tape and Reel.

Pinout

CA3127
(PDIP, CDIP, 150MIL SOIC)
TOP VIEW



File Number **662.2**

Absolute Maximum Ratings

Power Dissipation, P_D
- Any One Transistor 85mW
- Total Package
  - For T_A Up to +75°C 425mW
  - For T_A > +75°C ..... Derate Linearly at 6.67mW/°C

The following ratings apply for each transistor in the device
- Collector-to-Emitter Voltage, V_{CEO} 15V
- Collector-to-Base Voltage, V_{CBO} 20V
- Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
- Collector Current, I_C 20mA

Junction Temperature ..... +175°C
Junction Temperature (Plastic Packages) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C

PARAMETERS	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
DC SPECIFICATIONS (For Each Transistor)						
Collector-to-Base Breakdown Voltage	I_C = 10μA, I_E = 0		20	32	-	V
Collector-to-Emitter Breakdown Voltage	I_C = 1mA, I_B = 0		15	24	-	V
Collector-to-Substrate Breakdown-Voltage	I_{C1} = 10μA, I_B = 0, I_E = 0		20	60	-	V
Emitter-to-Base Breakdown Voltage (Note 2)	I_E = 10μA, I_C = 0		4	5.7	-	V
Collector-Cutoff-Current	V_{CE} = 10V I_B = 0		-	-	0.5	μA
Collector-Cutoff-Current	V_{CB} = 10V, I_E = 0		-	-	40	nA
DC Forward-Current Transfer Ratio	V_{CE} = 6V	I_C = 5mA	35	88	-	
		I_C = 1mA	40	90	-	
		I_C = 0.1mA	35	85	-	
Base-to-Emitter Voltage	V_{CE} = 6V	I_C = 5mA	0.71	0.81	0.91	V
		I_C = 1mA	0.66	0.76	0.86	V
		I_C = 0.1mA	0.60	0.70	0.80	V
Collector-to-Emitter Saturation Voltage	I_C = 10mA, I_B = 1mA		-	0.26	0.50	V
Magnitude of Difference in V_{BE}	Q_1 & Q_2 Matched V_{CE} = 6V, I_C = 1mA		-	0.5	5	mV
Magnitude of Difference in I_B			-	0.2	3	μA
SWITCHING SPECIFICATIONS						
Noise Figure	f = 100kHz, R_S = 500Ω, I_C = 1mA		-	2.2	-	dB
Gain-Bandwidth Product	V_{CE} = 6V, I_C = 5mA		-	1.15	-	GHz
Collector-to-Base Capacitance	V_{CB} = 6V, f = 1MHz		-	See Fig. 5	-	pF
Collector-to-Substrate Capacitance	V_{CI} = 6V, f = 1MHz		-		-	pF
Emitter-to-Base Capacitance	V_{BE} = 4V, f = 1MHz		-		-	pF
Voltage Gain	V_{CE} = 6V, f = 10MHz, R_L = 1kΩ, I_C = 1mA		-	28	-	dB
Power Gain	Cascode Configuration f = 100MHz, V+ = 12V, I_C = 1mA		27	30	-	dB
Noise Figure			-	3.5	-	dB
Input Resistance	Common-Emitter Configuration V_{CE} = 6V, I_C = 1mA, f = 200 MHz		-	400	-	Ω
Output Resistance			-	4.6	-	kΩ
Input Capacitance			-	3.7	-	pF
Output Capacitance			-	2	-	pF
Magnitude of Forward Transadmittance			-	24	-	mmho

NOTE:

1. The collector of each transistor of the CA3127 is isolated from the substrate by an integral diode. The substrate (terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. When used as a zener for reference voltage, the device must not be subjected to more than 0.1mJ of energy from any possible capacitance or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10mA.

Typical Performance Curves

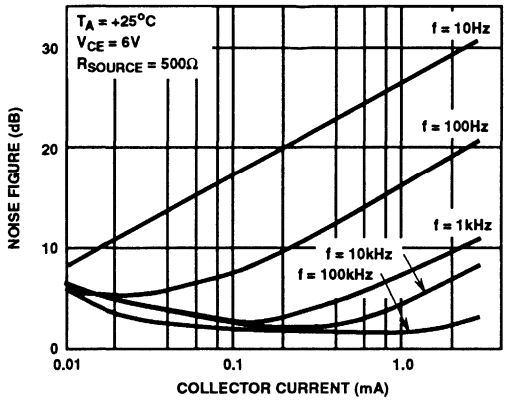


FIGURE 1. NOISE FIGURE vs COLLECTOR CURRENT AT R_{SOURCE} = 500Ω

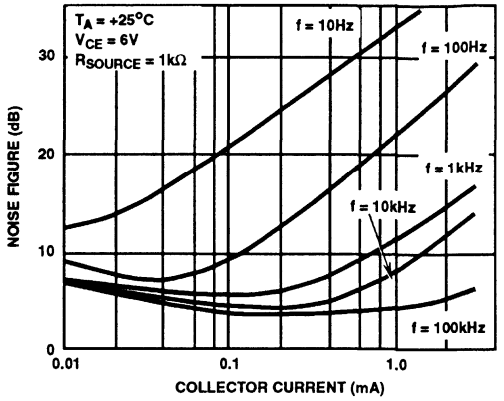


FIGURE 2. NOISE FIGURE vs COLLECTOR CURRENT AT R_{SOURCE} = 1kΩ

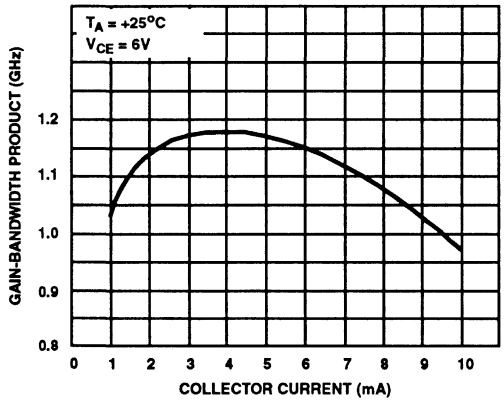


FIGURE 3. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT

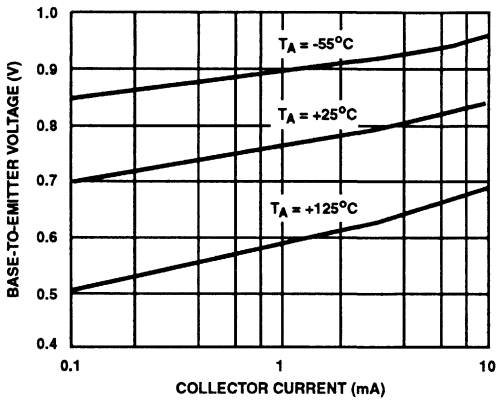


FIGURE 4. BASE-TO-EMITTER VOLTAGE vs COLLECTOR CURRENT

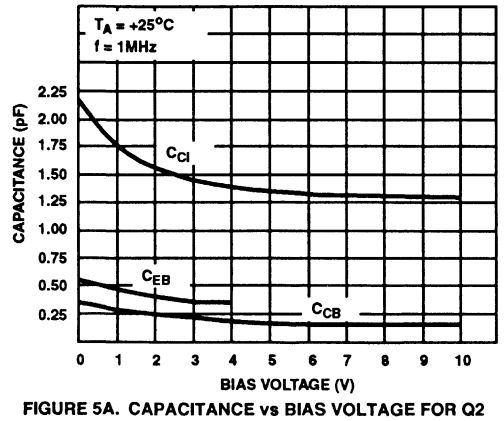


FIGURE 5A. CAPACITANCE vs BIAS VOLTAGE FOR Q2

TRANSISTOR	CAPACITANCE (pF)							
	C_{CB}		C_{CE}		C_{EB}		C_{CI}	
	PKG	TOTAL	PKG	TOTAL	PKG	TOTAL	PKG	TOTAL
BIAS (V)	-	6V	-	6V	-	4V	-	6V
Q1	0.025	0.190	0.090	0.125	0.365	0.610	0.475	1.65
Q2	0.015	0.170	0.225	0.265	0.130	0.360	0.085	1.35
Q3	0.040	0.200	0.215	0.240	0.360	0.625	0.210	1.40
Q4	0.040	0.190	0.225	0.270	0.365	0.610	0.085	1.25
Q5	0.010	0.165	0.095	0.115	0.140	0.365	0.090	1.35

FIGURE 5B. TYPICAL CAPACITANCE VALUES AT f = 1MHz. THREE TERMINAL MEASUREMENT. GUARD ALL TERMINALS EXCEPT THOSE UNDER TEST.

Typical Performance Curves (Continued)

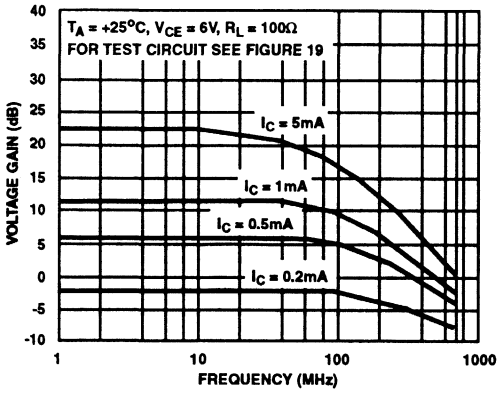


FIGURE 6. VOLTAGE GAIN vs FREQUENCY AT R_L = 100Ω

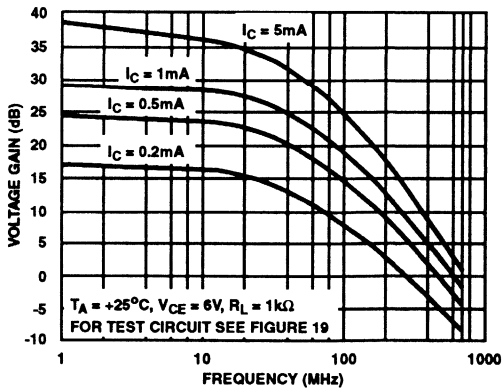


FIGURE 7. VOLTAGE GAIN vs FREQUENCY AT R_L = 1kΩ

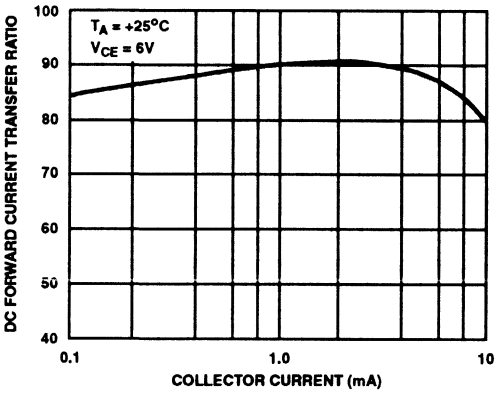


FIGURE 8. DC FORWARD-CURRENT TRANSFER RATIO (h_{FE}) vs COLLECTOR CURRENT

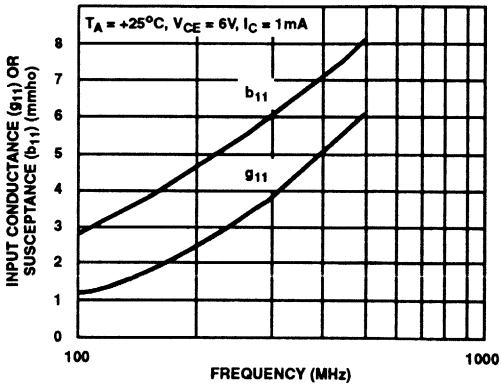


FIGURE 9. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY

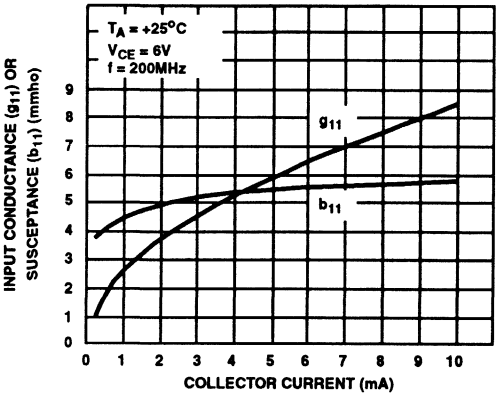


FIGURE 10. INPUT ADMITTANCE (Y_{11}) vs COLLECTOR CURRENT

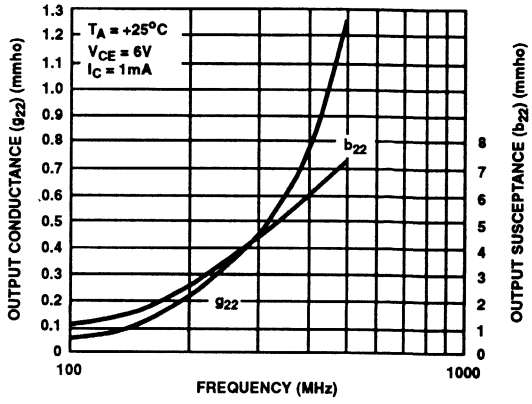


FIGURE 11. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

Typical Performance Curves (Continued)

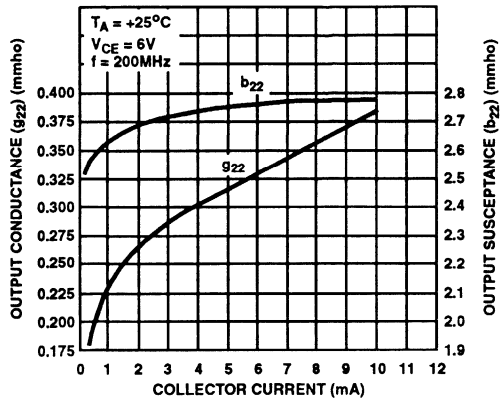


FIGURE 12. OUTPUT ADMITTANCE (Y_{22}) vs COLLECTOR CURRENT

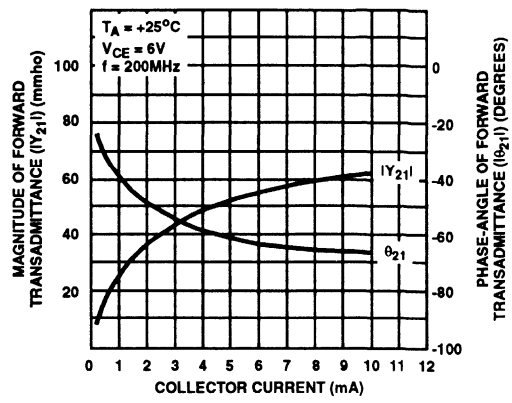


FIGURE 13. FORWARD TRANSADMITTANCE (Y_{21}) vs COLLECTOR CURRENT

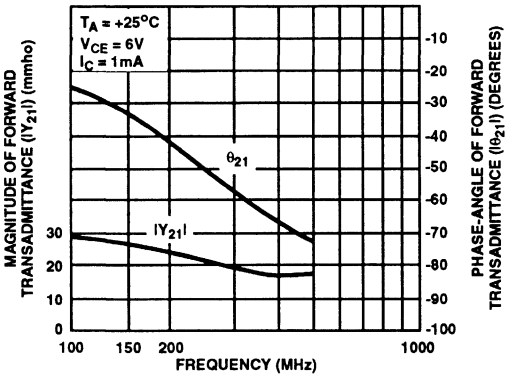


FIGURE 14. FORWARD TRANSADMITTANCE (Y_{21}) vs FREQUENCY

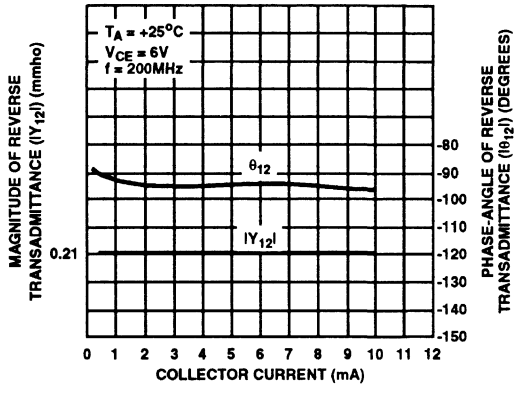


FIGURE 15. REVERSE TRANSADMITTANCE (Y_{12}) vs COLLECTOR CURRENT

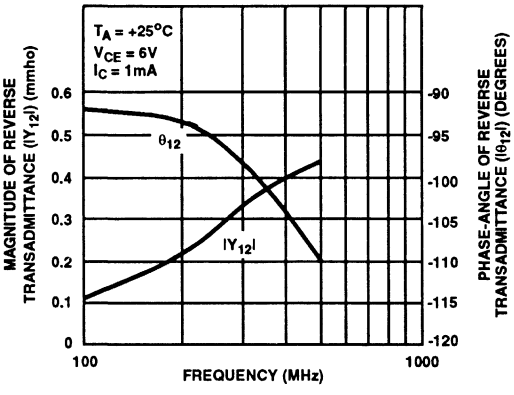


FIGURE 16. REVERSE TRANSADMITTANCE (Y_{12}) vs FREQUENCY

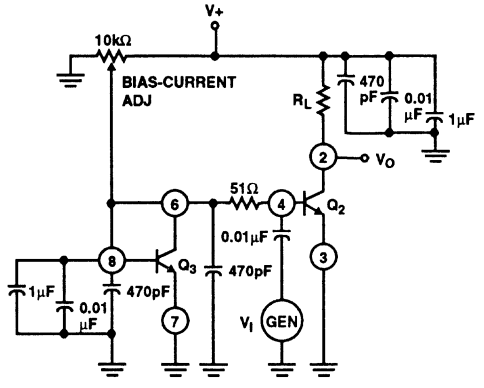
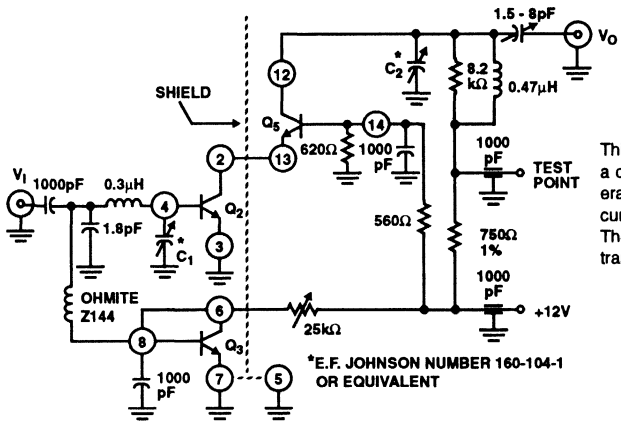


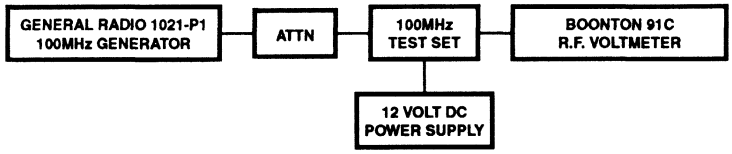
FIGURE 17. VOLTAGE-GAIN TEST CIRCUIT USING CURRENT-MIRROR BIASING FOR Q_2

Typical Performance Curves (Continued)

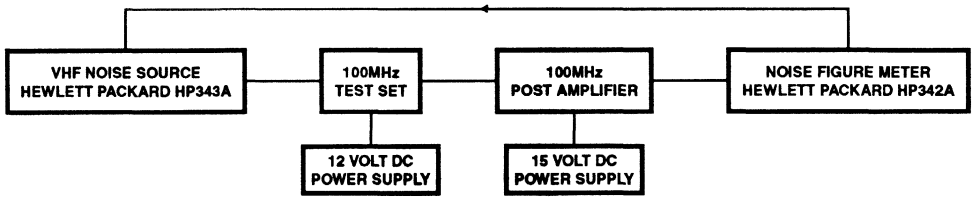


This circuit was chosen because it conveniently represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q3 in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.

FIGURE 18. 100MHz POWER-GAIN AND NOISE-FIGURE TEST CIRCUIT



(a) POWER GAIN SET-UP



(b) NOISE FIGURE SET-UP

FIGURE 19. BLOCK DIAGRAMS OF POWER-GAIN AND NOISE-FIGURE TEST SET-UPS

HARRIS SEMICONDUCTOR

CA3141

High-Voltage Diode Array For Commercial, Industrial & Military Applications

March 1993

Features

- Matched Monolithic Construction - V_F for Each Diode Pair Matched to Within 0.55mV (Typ) at I_F = 1mA
- Low Diode Capacitance - 0.3pF (Typ) at V_R = 2V
- High Diode-to-Substrate Breakdown Voltage - 30V (Min)
- Low Reverse (Leakage) Current - 100nA (Max)

Applications

- Balanced Modulators or Demodulators
- Analog Switches
- High-Voltage Diode Gates
- Current Ratio Detectors

Description

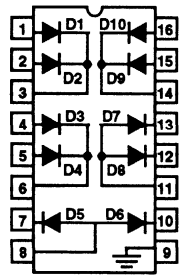
The CA3141E High Voltage Diode Array Consists of ten general purpose high reverse breakdown diodes. Six diodes are internally connected to form three common cathode diode pairs, and the remaining four diodes are internally connected to form two common anode diode pairs. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the CA3141 extremely useful for a wide variety of applications in communications and switching systems.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3141E	-55°C to +125°C	16 Lead Plastic DIP

Pinout

CA3141
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **906.2**

Absolute Maximum Ratings

Inverse Voltage (PIV) 30V
Peak Diode -to-Substrate Voltage 30V
Peak Forward Surge Current [I_F (Surge)] 100mA
DC Forward Current (I_F) 25mA
Dissipation:
  Any One Diode Unit 50mW
  Total Package:
  Up to 55°C 650mW
  For T_A > 55°C ..... Derate Linearly at 6.67mW/°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -55°C ≤ T_A ≤ +125°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
DC Forward Voltage Drop	V_F	I_F (Anode)	100µA	-	0.7	0.9	V
			1mA	-	0.78	1	V
			10mA	-	0.93	1.2	V
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_F = -10µA		30	50	-	V
DC Breakdown Voltage Between Any Diode and Substrate	$V_{(BR)DI}$	I_{DI} = 10µA		30	50	-	V
DC Reverse (Leakage) Current	I_R	V_F = -20V		-	-	100	nA
DC Reverse (Leakage) Current Between Any Diode and Substrate	I_{DI}	V_{DI} = 20V		-	-	100	nA
Magnitude of Diode Offset Voltage Between Diode Pairs		V_{DI} = 20V, I_{FA} = 1mA		-	0.55	-	mV
Temperature Coefficient of Forward Voltage Drop	$\Delta V_F/\Delta T$	I_F = 1mA		-	-1.5	-	mV/°C
Reverse Recovery Time	t_{RR}	I_F = 2mA, I_R = 2mA		-	50	-	ns
Diode Capacitance	C_D			See Figure 4			pF
Diode Anode-to-Substrate Capacitance	C_{DAI}			See Figure 5			pF
Diode Cathode-to-Substrate Capacitance	C_{DCI}			See Figure 6			pF
Magnitude of Cathode-to-Anode Current Ratio	$\lvert I_{FO}/I_{FA} \rvert$	I_{FA} = 1mA, V_{DS} = 10V		0.9	0.96	-	-

Typical Performance Curves

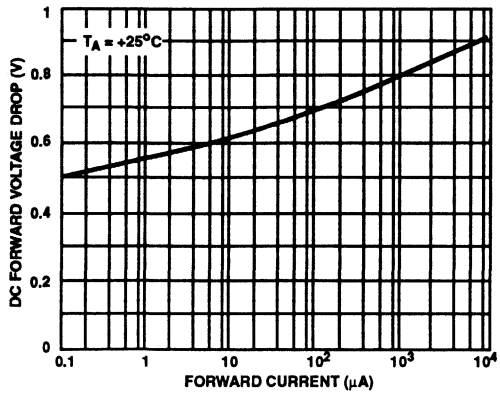


FIGURE 1. DC FORWARD VOLTAGE DROP vs FORWARD CURRENT

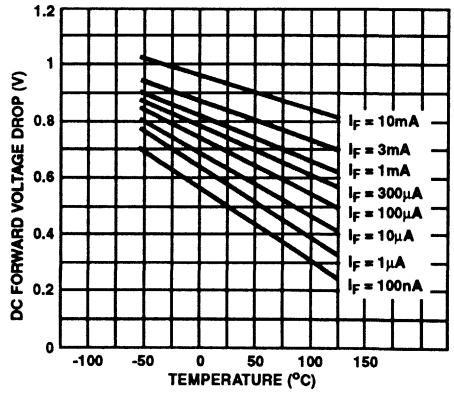


FIGURE 2. DC FORWARD VOLTAGE DROP vs TEMPERATURE

Typical Performance Curves (Continued)

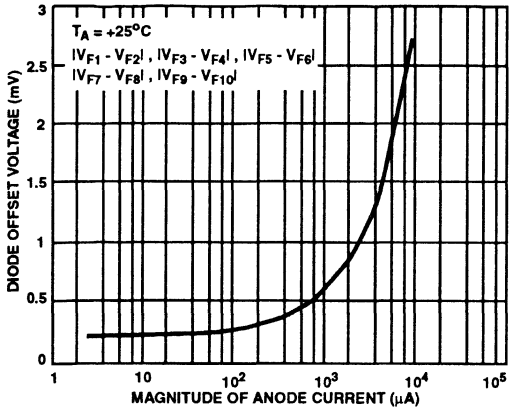


FIGURE 3. DIODE OFFSET VOLTAGE vs MAGNITUDE OF ANODE CURRENT

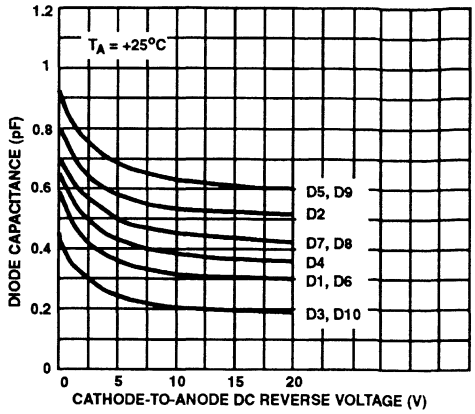


FIGURE 4. DIODE CAPACITANCE vs CATHODE-TO-ANODE REVERSE VOLTAGE

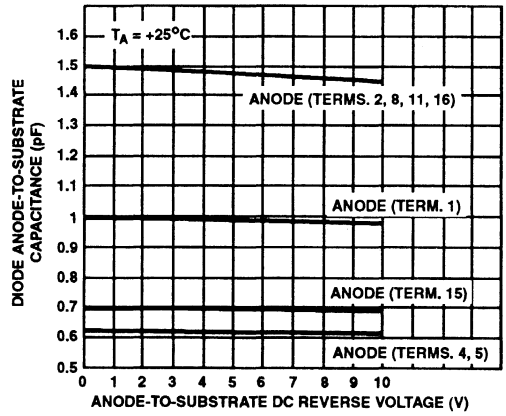


FIGURE 5. DIODE ANODE-TO-SUBSTRATE CAPACITANCE vs REVERSE VOLTAGE

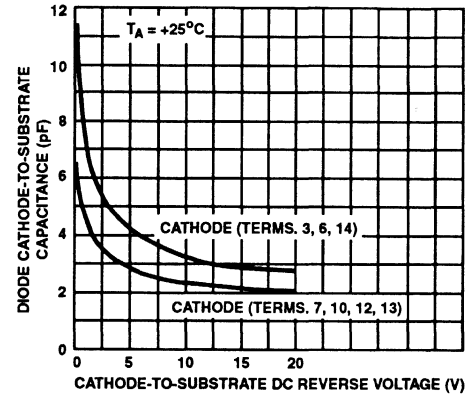


FIGURE 6. DIODE CATHODE-TO-SUBSTRATE CAPACITANCE vs CATHODE-TO-SUBSTRATE DC REVERSE VOLTAGE

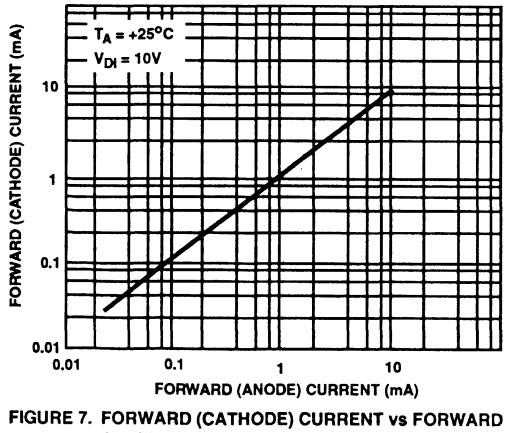


FIGURE 7. FORWARD (CATHODE) CURRENT vs FORWARD (ANODE) CURRENT

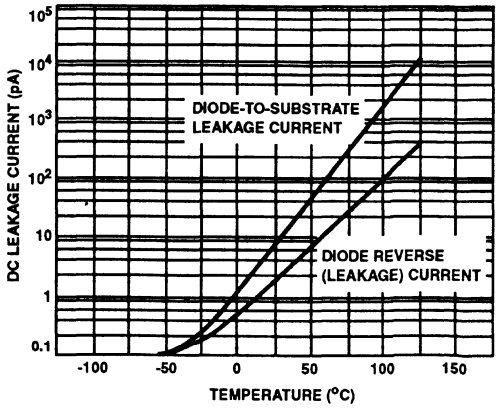


FIGURE 8. DC LEAKAGE CURRENT vs TEMPERATURE

HARRIS SEMICONDUCTOR

CA3146, CA3183

March 1993

High-Voltage Transistor Arrays

Features

- Matched General Purpose Transistors
- V_{BE} Matched ±5mV Max
- Operation from DC to 120MHz (CA3146, A)
- Low Noise Figure: 3.2dB Typ at 1kHz (CA3146, A)
- High I_C: 75mA Max (CA3183, A)

Applications

- General Use In Signal Processing Systems In DC through VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- Lamp and Relay Drivers (CA3183, A)
- Thyristor Firing (CA3183, A)

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3146AE	-40°C to +85°C	14 Lead Plastic DIP
CA3146AM	-40°C to +85°C	14 Lead SOIC
CA3146AM96	-40°C to +85°C	14 Lead SOIC*
CA3146E	-40°C to +85°C	14 Lead Plastic DIP
CA3146M	-40°C to +85°C	14 Lead SOIC
CA3146M96	-40°C to +85°C	14 Lead SOIC*
CA3183AE	-40°C to +85°C	16 Lead Plastic DIP
CA3183AM	-40°C to +85°C	16 Lead Narrow Body SOIC
CA3183AM96	-40°C to +85°C	16 Lead Narrow Body SOIC*
CA3183E	-40°C to +85°C	16 Lead Plastic DIP
CA3183M	-40°C to +85°C	16 Lead Narrow Body SOIC
CA3183M96	-40°C to +85°C	16 Lead Narrow Body SOIC*

*Denotes Tape and Reel

Description

The CA3146A, CA3146, CA3183A, and CA3183* are general purpose high voltage silicon n-p-n transistor arrays on a common monolithic substrate.

Types CA3146A and CA3146 consist of five transistors with two of the transistors connected to form a differentially connected pair. These types are recommended for low power applications in the DC through VHF range. (CA3146A and CA3146 are high voltage versions of the popular predecessor type CA3046.)

Types CA3183A and CA3183 consist of five high current transistors with independent connections for each transistor. In addition two of these transistors (Q1 and Q2) are matched at low current (i.e. 1mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design. (CA3183A and CA3183 are high voltage versions of the popular predecessor type CA3083.)

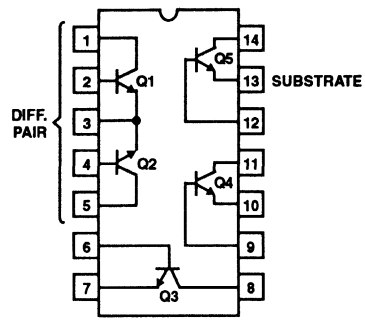
The types with an "A" suffix are premium versions of their non-"A" counterparts and feature tighter control of breakdown voltages making them more suitable for higher voltage applications.

For detailed application information, see companion Application Note AN5296 "Application of the CA3018 Integrated Circuit Transistor Array."

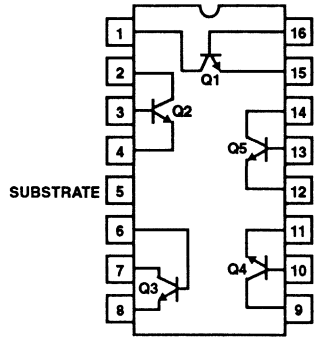
* Formerly Developmental Types Nos.
CA3146A - TA6084
CA3146 - TA6181
CA3183A - TA6094
CA3183 - TA6183

Pinouts

CA3146, A (PDIP, SOIC)
TOP VIEW



CA3183, A (PDIP, 150MIL SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 532.2

Absolute Maximum Ratings

Power Dissipation: (any one transistor)
CA3146A, CA3146 ..... 300mW
CA3183A, CA3183 ..... 500mW
Total Package
Up to +55°C (CA3146A, CA3146, CA3183A, CA3183) 750mW
Above +55°C ..... Derate Linearly 6.67mW/°C
(CA3146, A, CA3183, A)
The following ratings apply for each transistor in the device:
Collector-to-Emitter Voltage (V_{CEO}):
CA3146A, CA3183A 40V
CA3146, CA3183 ..... 30V
Collector-to-Base Voltage (V_{CBO}):
CA3146A, CA3183A 50V
CA3146, CA3183 ..... 40V
Collector-to-Substrate Voltage (V_{CIO}): (Note 1)
CA3146A, CA3183A 50V
CA3146, CA3183 ..... 40V
Emitter-to-Base Voltage (V_{EBO}) all types 5V
Collector Current
CA3146A, CA3146 ..... 50mA
CA3183 ..... 75mA
Base Current (I_B) - CA3183A, CA3183 ..... 20mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
CA3146A, CA3146, CA3183A, CA3183 ..... -40°C to +85°C
Storage Temperature Range (all types) ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Values Apply For Each Transistor

TYPE	(NOTE 2) P_T MAX. (mW)	I_C MAX. (mA)	V_{CEO} (MAX) (V)	V_{CBO} (MAX) (V)	$V_{CE\ SAT}$ AT 10mA TYP (V)	h_{FE} AT 1mA, & V_{CE} = 5V (TYP)	DIFF. PAIR AT 1mA		T_A RANGE (OPERATING)
							V_{IO} MAX (mV)	I_{IO} MAX (μA)	
VALUES APPLY FOR EACH TRANSISTOR									
CA3146A	300	50	40	50	0.33	100	±5	2	-40°C to +85°C
CA3146	300	50	30	40	0.33	100	±5	2	-40°C to +85°C
CA3183A	500	75	40	50	0.16	75	±5	2.5	-40°C to +85°C
CA3183	500	75	30	40	0.16	75	±5	2.5	-40°C to +85°C

Comparison Of Related Predecessor Type with Types in this Data Sheet

TYPE	V_{CEO} MIN (V)	V_{CBO} MIN (V)	$V_{CE\ SAT}$ TYP (V)	V_{BE} TYP (V)	I_C MAX (mA)	C_{CB} TYP (pF)	C_{CI} TYP (pF)	C_{EB} TYP (pF)
			I_C = 10mA	I_C = 1mA				
CA3046	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3146A	40	50	0.33	0.730	50	0.37	2.2	0.7
CA3146	30	40	0.33	0.730	50	0.37	2.2	0.7

Comparison Of Related Predecessor Type with Types in this Data Sheet (Continued)

TYPE	V_{CEO} MIN (V)	V_{CBO} MIN (V)	$V_{CE\ SAT}$ TYP (V)	V_{BE} TYP (V)	I_C MAX (mA)	C_{CB} TYP (pF)	C_{CI} TYP (pF)	C_{EB} TYP (pF)
			I_C = 50mA	I_C = 10mA				
CA3083	15	20	0.4	0.74	100	-	-	-
CA3183A	40	50	1.7	0.75	75	-	-	-
CA3183	30	40	1.7	0.75	75	-	-	-

NOTES:

1. The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transisters, and to provide for normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.
2. Caution on Total Package Power Dissipation: The maximum total package dissipation rating for the CA3146 and CA3183 Series circuits is 750mW at temperatures up to +55°C, then derate linearly at 6.67mW/°C.

Static Electrical Characteristics CA3146 Series

PARAMETERS	SYMBOL	TEST CONDITIONS T_A = +25°C		TYP. CHAR. CURVE FIG. NO.	LIMITS CA3146A MIN	CA3146A TYP	CA3146A MAX	CA3146 MN	CA3146 TYP	CA3146 MAX	UNITS
For Each Transistor											
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10μA, I_E = 0		-	50	72	-	40	72	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		-	40	56	-	30	56	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 10μA, I_B = 0, I_E = 0		-	50	72	-	40	72	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0		-	5	7	-	5	7	-	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0		2	-	See Curve	5	-	See Curve	5	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0		3	-	0.002	100	-	0.002	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 5V	I_C = 10mA	4	-	85	-	-	85	-	-
		V_{CE} = 5V	I_C = 1mA	4	30	100	-	30	100	-	-
		V_{CE} = 5V	I_C = 10μA	4	-	90	-	-	90	-	-
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 1mA		5	0.63	0.73	0.83	0.63	0.73	0.83	V
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	I_C = 10mA, I_B = 1mA		6	-	0.33	-	-	0.33	-	V
For transistors Q3 and Q4 (Darlington Configuration):											
Base-to-Emitter (Q3 to Q4)	V_{BE}	V_{CE} = 5V	I_E = 10mA	8	-	1.46	-	-	1.46	-	V
		V_{CE}=5V	I_E = 1mA	8, 9	-	1.32	-	-	1.32	-	V
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\lvert\frac{\Delta V_{BE}}{\Delta T}\right\rvert$	V_{CE} = 5V, I_E = 1mA		-	-	4.4	-	-	4.4	-	mV/°C

Static Electrical Characteristics CA3146 Series (Continued)

PARAMETERS		SYMBOL	TEST CONDITIONS T_A = +25°C	TYP. CHAR. CURVE FIG. NO.	LIMITS CA3146A MIN	CA3146A TYP	CA3146A MAX	CA3146 MN	CA3146 TYP	CA3146 MAX	UNITS
For transistors Q1 and Q2 (As a Differential Amplifier):											
Magnitude of Input Offset Voltage $\lvert V_{BE1} - V_{BE2}\rvert$		$\lvert V_{IO}\rvert$	V_{CE} = 5V, I_E = 1mA	10, 11	-	0.48	5	-	0.48	5	mV
Magnitude of Base-to-Emitter Temperature Coefficient		$\left\lvert\frac{\Delta V_{BE}}{\Delta T}\right\rvert$	V_{CE} = 5V, I_E = 1mA	-	-	1.9	-	-	1.9	-	mV/°C
Magnitude of V_{IO} (V_{BE1} - V_{BE2}) Temperature Coefficient		$\left\lvert\frac{\Delta V_{IO}}{\Delta T}\right\rvert$	V_{CE} = 5V, I_{C1} = I_{C2} = 1mA	-	-	1.1	-	-	1.1	-	µV/°C
Magnitude of Input Offset Current $\lvert I_{IO1} - I_{IO2}\rvert$	CA3146AE and CA3146E Only	I_{IO}	V_{CE} = 5V, I_{C1} = I_{C2} = 1mA	12	-	0.3	2	-	0.3	2	µA

Dynamic Electrical Characteristics CA3146 Series

PARAMETERS	SYMBOL	TEST CONDITIONS T_A = +25°C	TYP. CHAR. CURVE FIG. NO.	LIMITS CA3146A MIN	CA3146A TYP	CA3146A MAX	CA3146 MIN	CA3146 TYP	CA3146 MAX	UNITS
Low Frequency Noise Figure	NF	f = 1kHz, V_{CE} = 5V, I_C = 100µA, Source resistance = 1kΩ	14	-	3.25	-	-	3.25	-	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Forward-Current Transfer Ratio	h_{FE}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	16	-	100	-	-	100	-	-
Short-Circuit Input Impedance	h_{IE}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	16	-	2.7	-	-	3.5	-	kΩ
Open-Circuit Output Impedance	h_{OE}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	16	-	15.6	-	-	15.6	-	µmho
Open-Circuit Reverse Voltage Transfer Ratio	h_{RE}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	16	-	1.8×10^{-4}	-	-	1.8×10^{-4}	-	-
Admittance Characteristics:										
Forward Transfer Admittance	Y_{FE}	f = 1MHz, V_{CE} = 5V, I_C = 1 mA	17	-	31-j1.5	-	-	31-j1.5	-	mmho
Input Admittance	Y_{IE}	f = 1MHz, V_{CE} = 5V, I_C = 1 mA	18	-	0.35 + j0.04	-	-	0.3 + j0.04	-	mmho
Output Admittance	Y_{OE}	f = 1MHz, V_{CE} = 5V, I_C = 1 mA	19	-	0.001 + j0.03	-	-	0.001 + j0.03	-	mmho
Reverse Transfer Admittance	Y_{RE}	f = 1MHz, V_{CE} = 5V, I_C = 1 mA	20		See Curve			See Curve		mmho

Dynamic Electrical Characteristics CA3146 Series **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS T_A = +25°C	TYP. CHAR. CURVE FIG. NO.	LIMITS CA3146A MIN	CA3146A TYP	CA3146A MAX	CA3146 MIN	CA3146 TYP	CA3146 MAX	UNITS
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 3mA	21	300	500	-	300	500	-	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 5V, I_E = 0	22	-	0.70	-	-	0.70	-	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 5V, I_C = 0	22	-	0.37	-	-	0.37	-	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 5V, I_C = 0	22	-	2.2	-	-	2.2	-	pF

Static Electrical Characteristics CA3183 Series

PARAMETERS	SYMBOL	TEST CONDITIONS T_A = +25°C	TYP. CHAR CURVE FIG. NO.	LIMITS CA3183A MIN	CA3183A TYP	CA3183A MAX	CA3183 MIN	CA3183 TYP	CA3183 MAX	UNITS
For Each Transistor:										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	-	50	-	-	40	-	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	-	40	-	-	30	-	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0	-	50	-	-	40	-	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	-	5	-	-	5	-	-	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	23	-	-	10	-	-	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	24	-	-	1	-	-	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 10mA	25, 26	40	-	-	40	-	-	-
		V_{CE} = 5V, I_C = 50mA	-	40	-	-	40	-	-	-
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	27	0.65	0.75	0.85	0.65	0.75	0.85	V
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$ (Note 1)	I_C = 50mA, I_B = 5mA	28	-	1.7	3.0	-	1.7	3.0	V
For Transistors Q1 and Q2 (As a Differential Amplifier):										
Absolute Input Offset Voltage	$\lvert V_{IO} \rvert$	V_{CE} = 3V, I_C = 1mA	29	-	0.47	5	-	0.47	5	mV
Absolute Input Offset Current	$\lvert I_{IO} \rvert$	V_{CE} = 3V, I_C = 1mA	30	-	0.78	2.5	-	0.78	2.5	μA

NOTE:

1. A maximum dissipation of 5 transistors x 150mW = 750mW is possible for a particular application.

Typical Performance Curves Static Characteristics - CA3146 Series

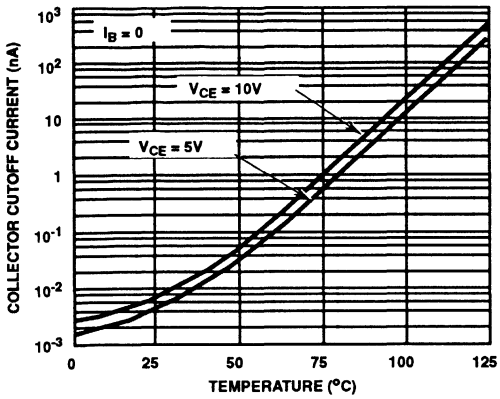


FIGURE 1. I_{CEO} vs TEMPERATURE FOR ANY TRANSISTOR

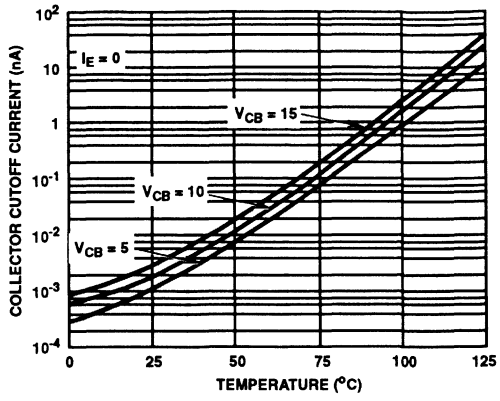


FIGURE 2. I_{CBO} vs TEMPERATURE FOR ANY TRANSISTOR

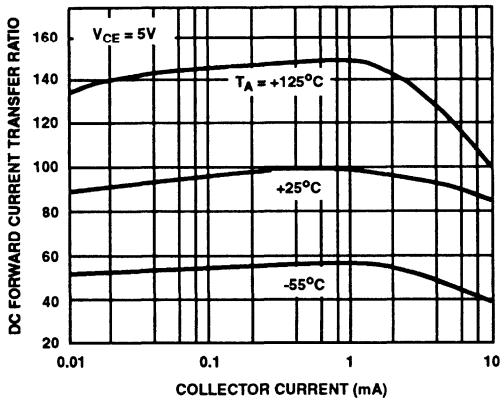


FIGURE 3. h_{FE} vs I_C FOR ANY TRANSISTOR

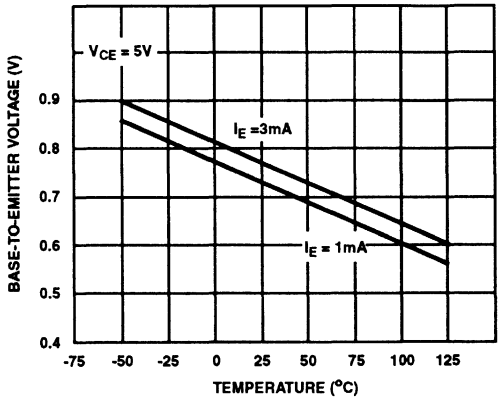


FIGURE 4. V_{BE} vs TEMPERATURE FOR ANY TRANSISTOR

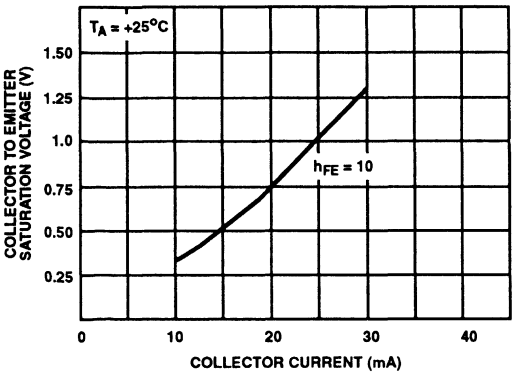


FIGURE 5. $V_{CE\ SAT}$ vs I_C FOR ANY TRANSISTOR

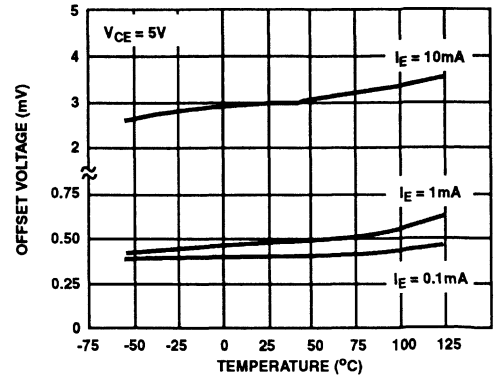


FIGURE 6. V_{IO} vs TEMPERATURE FOR Q1 AND Q2

Typical Performance Curves Static Characteristics - CA3146 Series (Continued)

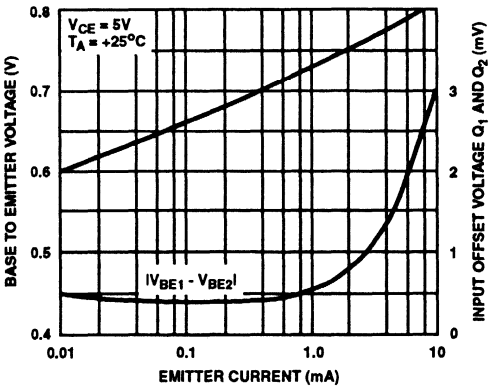


FIGURE 7. V_{BE} AND V_{IO} vs I_E FOR Q1 AND Q2

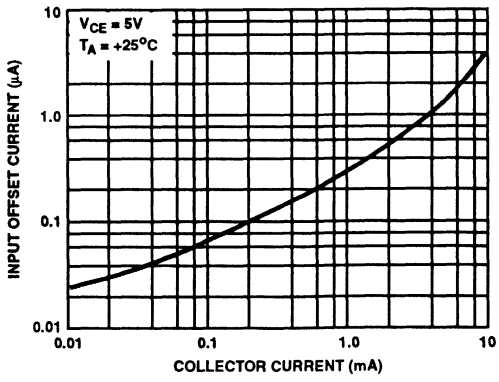


FIGURE 8. I_{IO} vs I_C (Q1 AND Q2) FOR TYPES CA3146A AND CA3146

Typical Performance Curves Dynamic Characteristics (for any transistor) - CA3146 Series

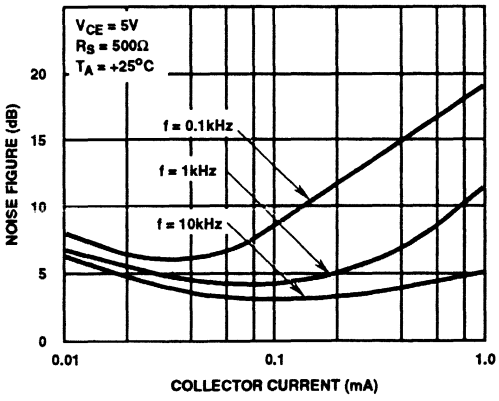


FIGURE 9. NF vs I_C AT R_S = 500Ω

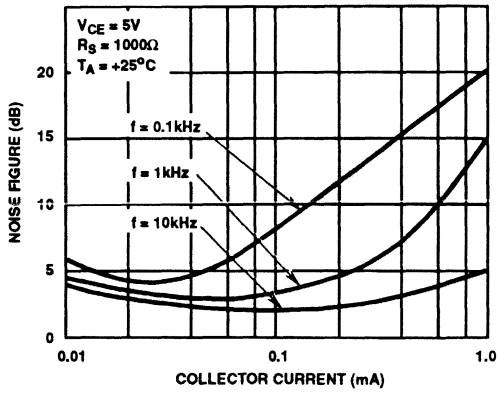


FIGURE 10. NF vs I_C AT R_S = 1kΩ

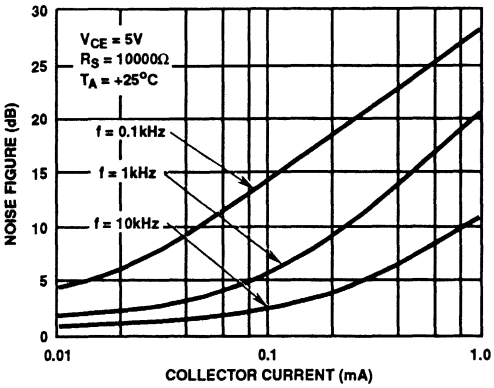


FIGURE 11. NF vs I_C AT R_S = 10kΩ

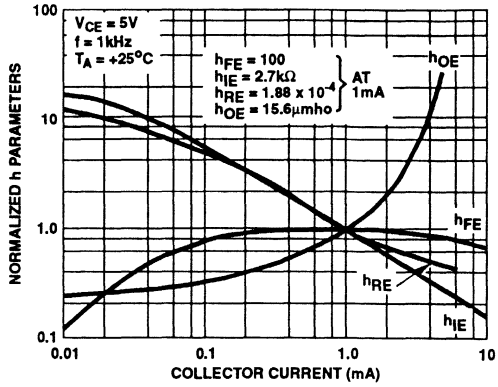


FIGURE 12. h_{FE}, h_{IE}, h_{OE}, h_{RE} vs I_C

Typical Performance Curves Dynamic Characteristics (for any transistor) - CA3146 Series (Continued)

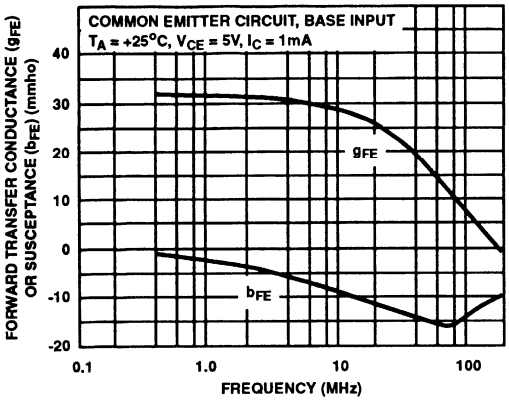


FIGURE 13. y_{FE} vs FREQUENCY

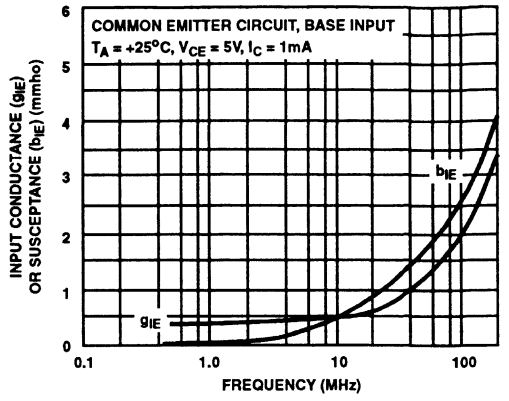


FIGURE 14. y_{IE} vs FREQUENCY

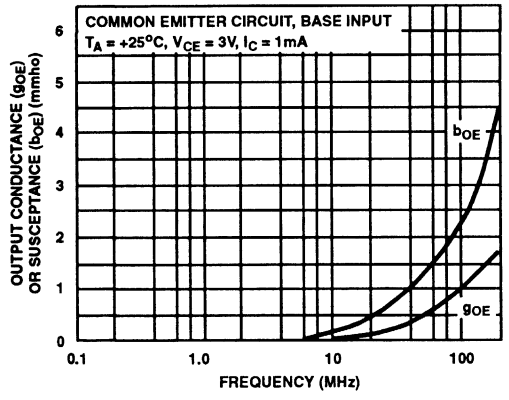


FIGURE 15. y_{OE} vs FREQUENCY

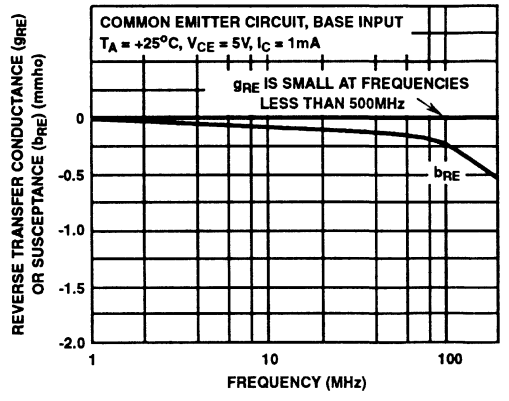


FIGURE 16. y_{RE} vs FREQUENCY

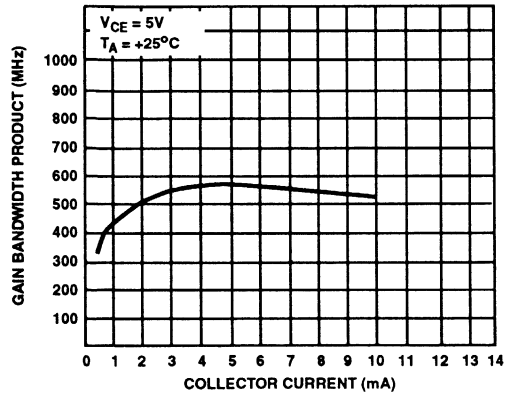


FIGURE 17. f_T vs I_C

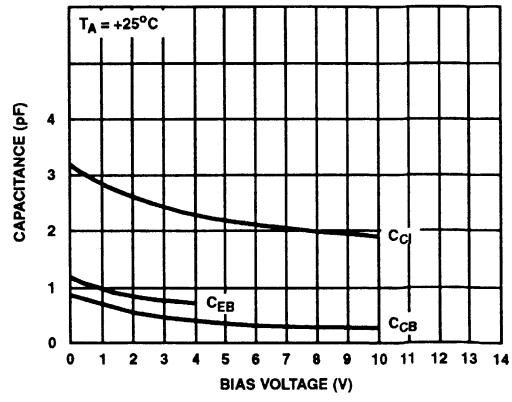


FIGURE 18. C_{EB}, C_{CB}, C_{CI} vs BIAS VOLTAGE

Typical Performance Curves Static Characteristics - CA3183 Series

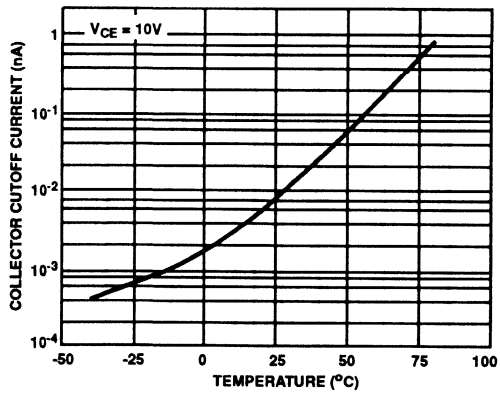


FIGURE 19. I_{CEO} vs TEMPERATURE FOR ANY TRANSISTOR

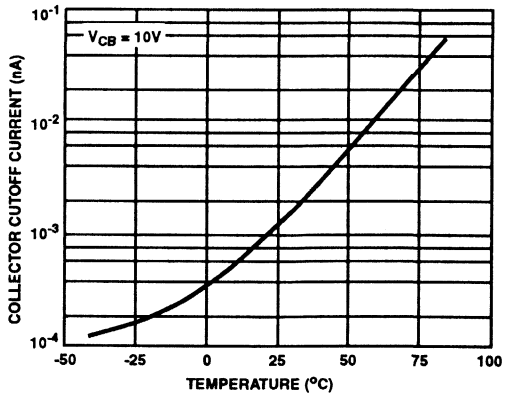


FIGURE 20. I_{CBO} vs TEMPERATURE FOR ANY TRANSISTOR

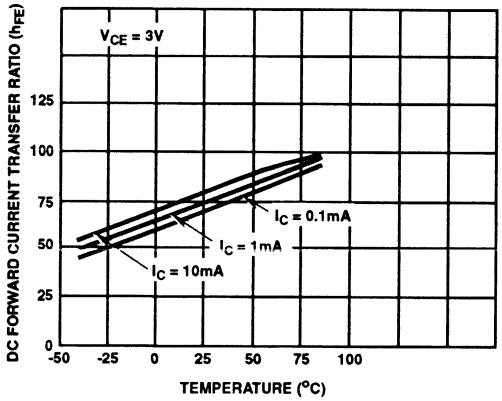


FIGURE 21. h_{FE} vs TEMPERATURE FOR ANY TRANSISTOR

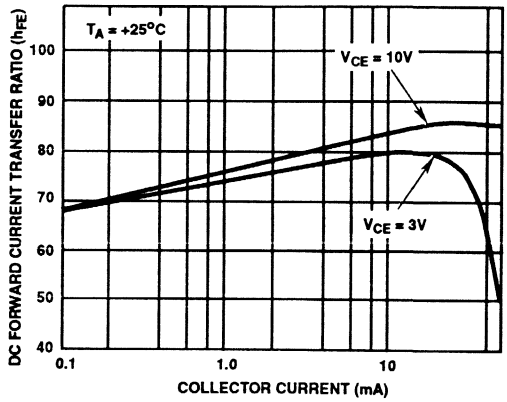


FIGURE 22. h_{FE} vs I_C FOR ANY TRANSISTOR

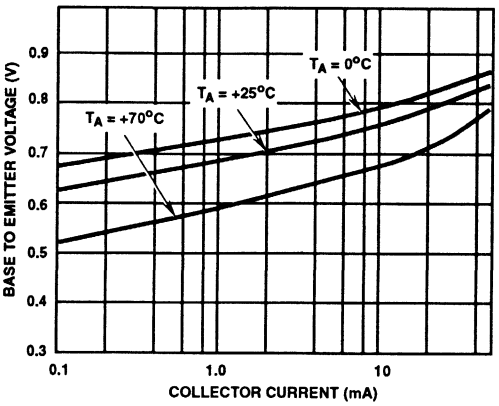


FIGURE 23. V_{BE} vs I_C FOR ANY TRANSISTOR

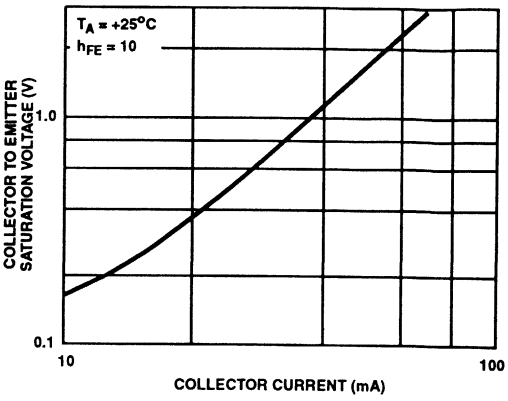


FIGURE 24. $V_{CE\ SAT}$ vs I_C FOR ANY TRANSISTOR

Typical Performance Curves Static Characteristics - CA3183 Series (Continued)

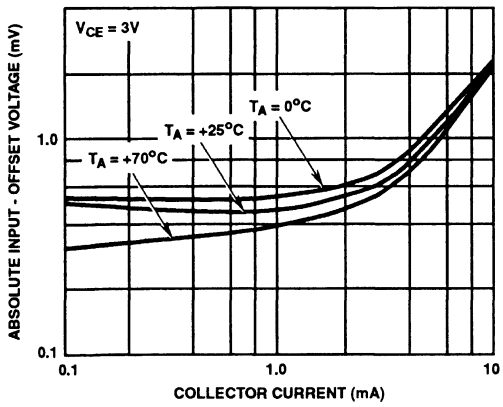


FIGURE 25. $|V_{IO}|$ vs I_C FOR DIFFERENTIAL AMPLIFIER (Q1 AND Q2)

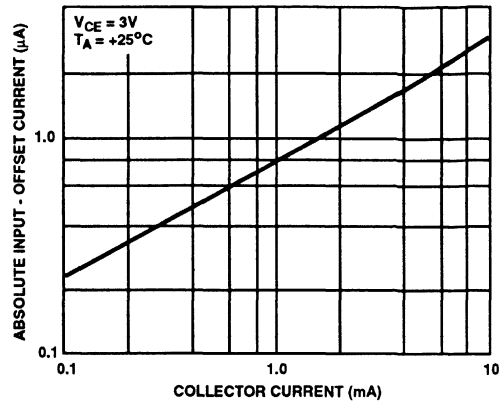


FIGURE 26. $|I_{IO}|$ vs I_C FOR DIFFERENTIAL AMPLIFIER (Q1 AND Q2)

HARRIS SEMICONDUCTOR

CA3227, CA3246

High-Frequency N-P-N Transistor Arrays For Low-Power Applications at Frequencies Up to 1.5GHz

March 1993

Features

- Gain-Bandwidth Product (f_T) > 3GHz
- Five Transistors on a Common Substrate

Applications

- VHF Amplifiers
- VHF Mixers
- Multifunction Combinations-RF/Mixer/Oscillator
- IF Converter
- IF Amplifiers
- Sense Amplifiers
- Synthesizers
- Synchronous Detectors
- Cascade Amplifiers

Description

The CA3227 and CA3246* consist of five general purpose silicon n-p-n transistors on a common monolithic substrate. Each of the transistors exhibits a value of f_T in excess of 3GHz, making them useful from DC to 1.5GHz. The monolithic construction of these devices provides close electrical and thermal matching of the five transistors.

* Formerly RCA Development Nos. TA10854 and TA10855, respectively.

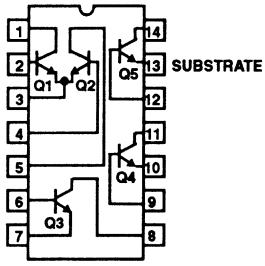
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3227E	-55°C to +125°C	16 Lead Plastic DIP
CA3227M	-55°C to +125°C	16 Lead Narrow Body SOIC
CA3227M96	-55°C to +125°C	16 Lead Narrow Body SOIC *
CA3246E	-55°C to +125°C	14 Lead Plastic DIP
CA3246M	-55°C to +125°C	14 Lead SOIC
CA3246M96	-55°C to +125°C	14 Lead SOIC *

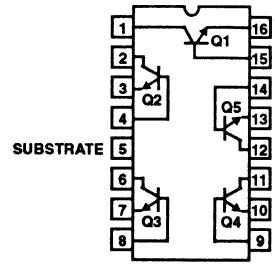
* Denotes Tape and Reel

Pinouts

CA3246
(PDIP, SOIC)
TOP VIEW



CA3227
(PDIP, 150 mil SOIC)
TOP VIEW



6 TRANSISTOR AND DIODE ARRAYS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1345.2

Absolute Maximum Ratings (T_A = +25°C)

Power Dissipation, P_D:
- Any one transistor 85mW
- Total Package:
- For T_A Up To +75°C 425mW
- For T_A > +75°C ..... Derate Linearly at 6.67mW/°C

The following ratings apply for each transistor in the device:
- Collector-to-Emitter Voltage (V_{CEO}) 8V
- Collector-to-Base Voltage (V_{CBO}) 12V
- Collector-to-Substrate Voltage (V_{CIO}) (Note 1) 20V
- Collector Current (I_C) 20mA
- Junction Temperature ..... +175°C
- Junction Temperature (Plastic Package) ..... +150°C
- Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -55°C ≤ T_A ≤ +125°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications T_A = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
FOR EACH TRANSISTOR							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10μA, I_E = 0		12	20	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		8	10	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{C1} = 10μA, I_B = 0, I_E = 0		20	-	-	V
Emitter-Cutoff-Current (Note 2)	I_{EBO}	V_{EB} = 4.5V, I_C = 0		-	-	10	μA
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 5V, I_B = 0		-	-	1	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 8V, I_E = 0		-	-	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 6V	I_C = 10mA	-	110	-	
			I_C = 1mA	40	150	-	
			I_C = 0.1mA	-	150	-	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 6V	I_C = 1mA	0.62	0.71	0.82	V
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	I_C = 10mA, I_B = 1mA		-	0.13	0.50	V
Base-to-Emitter Saturation Voltage	$V_{BE\ SAT}$	I_C = 10mA, I_B = 1mA		0.74	-	0.94	V

NOTES:

1. The collector of each transistor of these devices is isolated from the substrate by an integral diode. The substrate (terminal 5/CA3227 and terminal 13/CA3246) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. On small-geometry, high-frequency transistors, it is very good practice never to take the Emitter Base Junction into reverse breakdown. To do so may permanently degrade the h_{FE}. Hence, the use of I_{EBO} rather than $V_{(BR)EBO}$. These devices are also susceptible to damage by electrostatic discharge and transients in the circuits in which they are used. Moreover, CMOS handling procedures should be employed.

Dynamic Electrical Specifications T_A = +25°C, 200MHz, Common Emitter, Typical Values Intended Only for Design Guidance

PARAMETER	SYMBOL		TEST CONDITION	TYPICAL VALUES	UNITS
FOR EACH TRANSISTOR					
Input Admittance	Y_{11}	b_{11}	I_C = 1mA, V_{CE} = 5V	4	mmho
		g_{11}		0.75	mmho
Output Admittance	Y_{22}	b_{22}	I_C = 1mA, V_{CE} = 5V	2.7	mmho
		g_{22}		0.13	mmho
Forward Transfer Admittance	Y_{21}	Y_{21}	I_C = 1mA, V_{CE} = 5V	29.3	mmho
		θ_{21}		-33	degrees
Reverse Transfer Admittance	Y_{12}	Y_{12}	I_C = 1mA, V_{CE} = 5V	0.38	mmho
		θ_{12}		-97	degrees
Input Admittance	Y_{11}	b_{11}	I_C = 10mA, V_{CE} = 5V	4.8	mmho
		g_{11}		2.85	mmho
Output Admittance	Y_{22}	b_{22}	I_C = 10mA, V_{CE} = 5V	2.75	mmho
		g_{22}		0.9	mmho
Forward Transfer Admittance	Y_{21}	Y_{21}	I_C = 10mA, V_{CE} = 5V	95	mmho
		θ_{21}		-62	degrees
Reverse Transfer Admittance	Y_{12}	Y_{12}	I_C = 10mA, V_{CE} = 5V	0.39	mmho
		θ_{12}		-97	degrees
Small Signal Forward Current Transfer Ratio	h_{21}		I_C = 1mA, V_{CE} = 5V	7.1	
			I_C = 10mA, V_{CE} = 5V	17	
TYPICAL CAPACITIES AT 1MHz, THREE-TERMINAL MEASUREMENT					
Collector-to-Base Capacitance	C_{CB}		V_{CB} = 6V	0.3	pF
Collector-to-Substrate Capacitance	C_{CI}		V_{CI} = 6V	1.6	pF
Collector-to-Emitter Capacitance	C_{CE}		V_{CE} = 6V	0.4	pF
Emitter-to-Base Capacitance	C_{EB}		V_{EB} = 3V	0.75	pF

Spice Model (Spice 2G.6)

.model NPN

+	BF = 2.610E + 02	BR = 4.401E + 00	IS = 6.930E - 16	RB = 130.0E + 00
+	RC = 1.000E + 01	RE = 7.396E - 01	VA = 6.300E + 01	VB = 2.208E + 00
+	IK = 1.000E - 01	ISE = 1.87E - 14	NE = 1.653E + 00	IKR = 1.000E - 02
+	ISC = 9.25E - 14	NC = 1.333E + 00	TF = 1.775E - 11	TR = 1.000E - 09
+	CJS = 1.800E - 12	CJE = 1.010E - 12	PE = 8.350E - 01	ME = 4.460E - 01
+	CJC = 9.100E - 13	PC = 3.850E - 01	MC = 2.740E - 01	KF = 0.000E + 00
+	AF = 1.000E + 00	EF = 1.000E + 00	FC = 5.000E - 01	PJS = 5.410E - 01
+	MJS = 3.530E - 01	RBM = 30.00	RBV = 100	IRB = 0.00

Please Note: No measurements have been made to model the reverse AC operation (tr is an estimation)

Typical Performance Curves

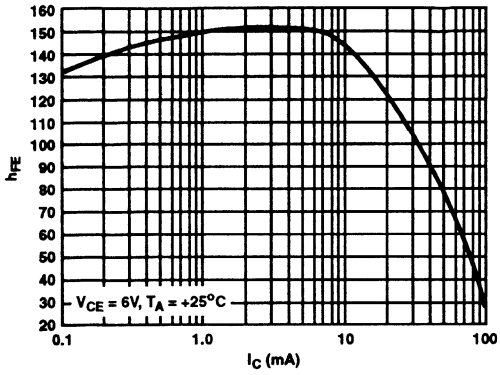


FIGURE 1. h_{FE} vs COLLECTOR CURRENT

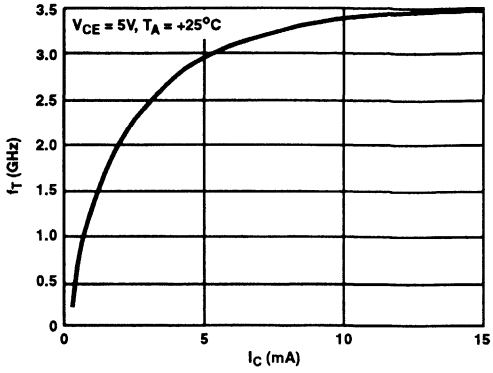


FIGURE 2. f_T vs COLLECTOR CURRENT

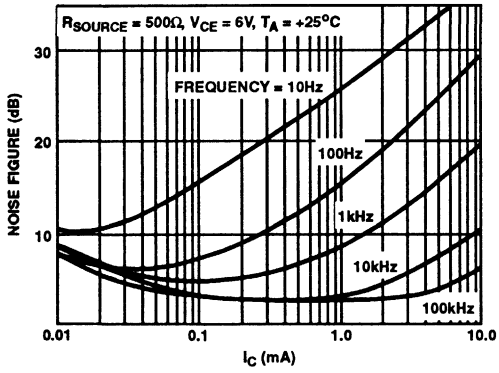


FIGURE 3. NOISE FIGURE vs COLLECTOR CURRENT

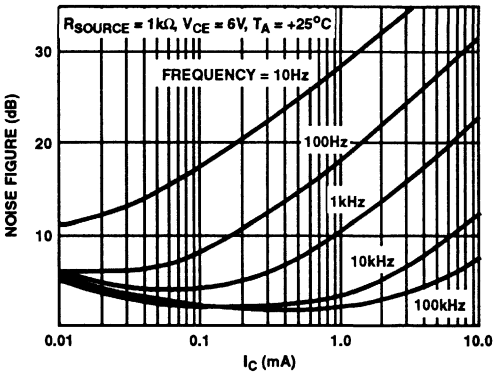


FIGURE 4. NOISE FIGURE vs COLLECTOR CURRENT

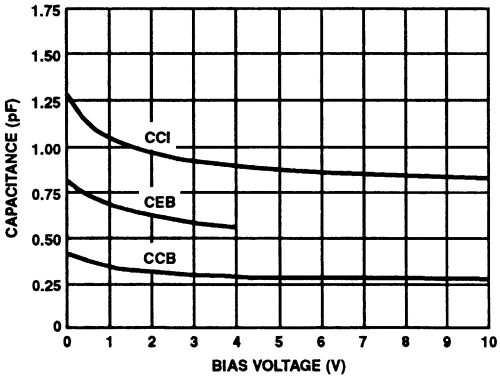


FIGURE 5. CAPACITANCE vs BIAS VOLTAGE

Die Characteristics

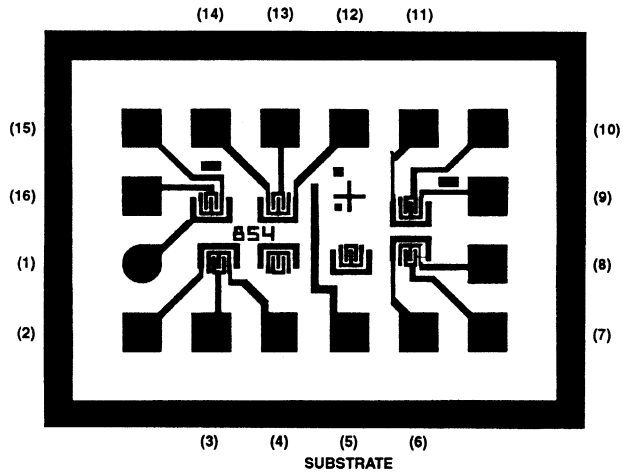
DIE DIMENSIONS:

46 x 32 mils CA3227

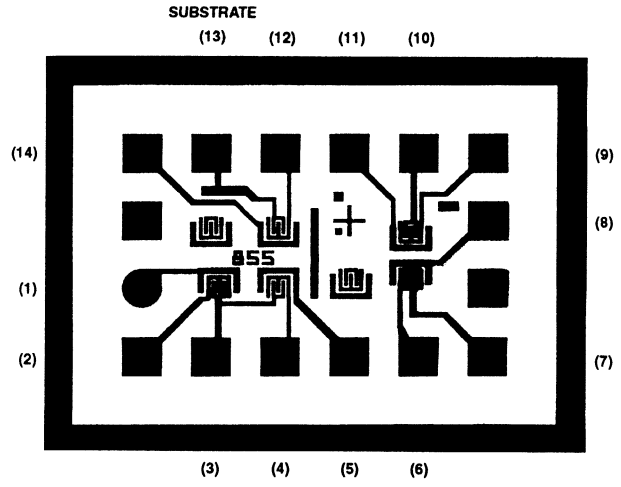
47 x 33 mils CA3246

Metallization Mask Layout

CA3227



CA3246



HARRIS SEMICONDUCTOR

HFA3046, HFA3096 HFA3127, HFA3128

April 1993

Ultra High Frequency Transistor Array

Features

- NPN Transistor (f_T)..... 8GHz
- NPN Current Gain (h_{FE})..... 70
- NPN Early Voltage (V_A)..... 50V
- PNP Transistor (f_T)..... 5.5GHz
- PNP Current Gain (h_{FE})..... 40
- PNP Early Voltage (V_A)..... 25V
- Noise Figure (50Ω) @ 1.0GHz..... 2.5dB
- Collector-to-Collector Leakage..... <1pA
- Complete Isolation Between Transistors
- Pin Compatible with Industry Standard 3XXX Series Arrays

Applications

- VHF/UHF Amplifiers
- VHF/UHF Mixers
- IF Converters
- Synchronous Detectors

Description

The HFA3046, HFA3096, HFA3127 and the HFA3128 are Ultra High Frequency Transistor Arrays that are fabricated from Harris Semiconductor's complementary bipolar UHF-1 process. Each array consists of five dielectrically isolated transistors on a common monolithic substrate. The NPN transistors exhibit a f_T of 8GHz while the PNP transistors provide a f_T of 5.5GHz. Both types exhibit low noise (2.5dB), making them ideal for high frequency amplifier and mixer applications.

The HFA3046 and HFA3127 are all-NPN arrays while the HFA3128 has all PNP transistors. The HFA3096 is a NPN-PNP combination. Access is provided to each of the terminals for the individual transistors for maximum application flexibility. Monolithic construction of these transistor arrays provides close electrical and thermal matching of the five transistors.

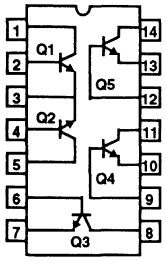
For PSPICE, package models, S-Parameters as well as custom transistor arrays, please contact your local sales office for more information.

Ordering Information

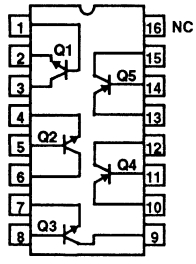
PART NUMBER	PRODUCT DESCRIPTION
HFA3046B	14 Lead SOIC
HFA3096B, HFA3127B, HFA3128B	16 Lead Narrow Body SOIC
HFA3046Y, HFA3096Y	DIE
HFA3127Y, HFA3128Y	DIE

Pinouts

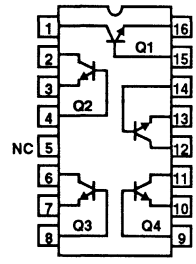
HFA3046



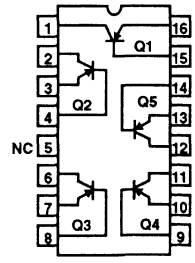
HFA3096



HFA3127



HFA3128



14 and 16 lead SOIC packages are available in narrow body width (150mils). Refer to package outline information.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3076.3**

Absolute Maximum Ratings

Collector to Emitter Voltage (Open Base) 8.0V
Collector to base voltage (Shorted Base) 12.0V
Emitter to Base Voltage (Reverse Bias) 5.5V
Collector Current 40mA
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... -55°C to +125°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic 14 SOIC Package	119°C/W	36°C/W
Plastic 16 SOIC Package	114°C/W	35°C/W

Maximum Package Power Dissipation at +75°C
Plastic SOIC 14 Package ..... 0.63 W
Plastic SOIC 16 Package ..... 0.66 W
Any One Transistor ..... 0.60 W
Derating Factor Above +75°C
Plastic SOIC 14 Package ..... 8.4mW/°C
Plastic SOIC 16 Package ..... 8.8mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static NPN Characteristics at T_A = +25°C

PARAMETERS	TEST CONDITIONS	DIE			SOIC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$	I_C = 100µA, I_E = 0	12	18	-	12	18	-	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CEO}$	I_C = 100µA, I_B = 0	8	12	-	8	12	-	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$	I_C = 100µA, Base Shorted to Emitter	10	20	-	10	20	-	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$	I_E = 10µA, I_C = 0	5.5	6	-	5.5	6	-	V
Collector-Cutoff-Current, I_{CEO}	V_{CE} = 6V, I_B = 0	-	2	100	-	2	100	nA
Collector-Cutoff-Current, I_{CBO}	V_{CB} = 8V, I_E = 0	-	0.1	10	-	0.1	10	nA
Collector-to-Emitter Saturation Voltage, $V_{CE(SAT)}$	I_C = 10mA, I_B = 1mA	-	0.3	0.5	-	0.3	0.5	V
Base-to-Emitter Voltage, V_{BE}	I_C = 10mA	-	0.85	0.95	-	0.85	0.95	V
DC Forward-Current Transfer Ratio, h_{FE}	I_C = 10mA VCE = 2V	40	70	-	40	70	-	
Early Voltage, V_A	I_C = 1mA, V_{CE} = 3.5V	20	50	-	20	50	-	V
Base-to-Emitter Voltage Drift	I_C = 10mA	-	-1.5	-	-	-1.5	-	mV/°C
Collector-to-Collector Leakage		-	1	-	-	1	-	pA

Dynamic NPN Characteristics at T_A = +25°C

PARAMETERS	TEST CONDITIONS	DIE			SOIC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Noise Figure	f = 1.0GHz, V_{CE} = 5V, I_C = 5mA, Z_S = 50Ω	-	2.5	-	-	2.5	-	dB
f_T Current Gain-Bandwidth Product	I_C = 1mA, V_{CE} = 5V	-	5.5	-	-	5.5	-	GHz
	I_C = 10mA, V_{CE} = 5V	-	8	-	-	8	-	GHz
	I_C = 40mA, V_{CE} = 5V	-	5.5	-	-	5.5	-	GHz
Power Gain-Bandwidth Product, f_{MAX}	I_C = 10mA, V_{CE} = 5V	-	6	-	-	2.5	-	GHz
Base-to-Emitter Capacitance	V_{BE} = -3V	-	200	-	-	500	-	fF
Collector-to-Base Capacitance	V_{CB} = 3V	-	200	-	-	500	-	fF

Static PNP Characteristics at $T_A = +25°C$

PARAMETERS	TEST CONDITIONS	DIE			SOIC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$	$I_C = -100\mu A$, $I_E = 0$	10	15	-	10	15	-	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CEO}$	$I_C = -100\mu A$, $I_B = 0$	8	15	-	8	15	-	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$	$I_C = -100\mu A$, Base Shorted to Emitter	10	15	-	10	15	-	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$	$I_E = -10\mu A$, $I_C = 0$	4.5	5	-	4.5	5	-	V
Collector-Cutoff-Current, I_{CEO}	$V_{CE} = -6V$, $I_B = 0$	-	2	100	-	2	100	nA
Collector-Cutoff-Current, I_{CBO}	$V_{CB} = -8V$, $I_E = 0$	-	0.1	10	-	0.1	10	nA
Collector-to-Emitter Saturation Voltage, $V_{CE(SAT)}$	$I_C = -10mA$, $I_B = -1mA$	-	0.3	0.5	-	0.3	0.5	V
Base-to-Emitter Voltage, V_{BE}	$I_C = -10mA$	-	0.85	0.95	-	0.85	0.95	V
DC Forward-Current Transfer Ratio, h_{FE}	$I_C = -10mA$, $V_{CE} = -2V$	25	40	-	25	40	-	
Early Voltage, V_A	$I_C = -1mA$, $V_{CE} = -3.5V$	10	25	-	10	25	-	V
Base-to-Emitter Voltage Drift	$I_C = -10mA$	-	-1.5	-	-	-1.5	-	mV/°C
Collector-to-Collector Leakage		-	1	-	-	1	-	pA

Dynamic PNP Characteristics at $T_A = +25°C$

PARAMETERS	TEST CONDITIONS	DIE			SOIC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Noise Figure	$f = 1.0GHz$, $V_{CE} = -5V$, $I_C = -5mA$, $Z_S = 50\Omega$	-	2.5	-	-	2.5	-	dB
f_T Current Gain-Bandwidth Product	$I_C = -1mA$, $V_{CE} = -5V$	-	2	-	-	2	-	GHz
	$I_C = -10mA$, $V_{CE} = -5V$	-	5.5	-	-	5.5	-	GHz
	$I_C = -40mA$, $V_{CE} = -5V$	-	2	-	-	2	-	GHz
Power Gain-Bandwidth Product	$I_C = -10mA$, $V_{CE} = -5V$	-	3	-	-	2	-	GHz
Base-to-Emitter Capacitance	$V_{BE} = 3V$	-	200	-	-	500	-	fF
Collector-to-Base Capacitance	$V_{CB} = -3V$	-	300	-	-	600	-	fF

Differential Pair Matching Characteristics for the HFA3046

PARAMETERS	TEST CONDITIONS	DIE			SOIC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$I_C = 10mA$, $V_{CE} = 5V$	-	1.5	5.0	-	1.5	5.0	mV
Input Offset Current	$I_C = 10mA$, $V_{CE} = 5V$	-	5	25	-	5	25	µA
Input Offset Voltage TC	$I_C = 10mA$, $V_{CE} = 5V$	-	0.5	-	-	0.5	-	µV/°C

S-Parameter and PSPICE model data is available from Harris Sales Offices.

Die Characteristics

PROCESS:
UHF-1

DIE DIMENSIONS:
53 x 52 x 19 ± 1mils
1340µm x 1320µm ± 25.4µm

METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

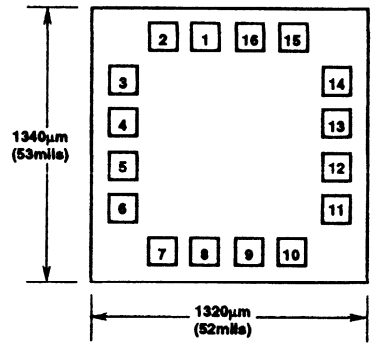
DIE ATTACH:
Material: Epoxy

WORST CASE CURRENT DENSITY:
1.39×10^5 A/cm^2

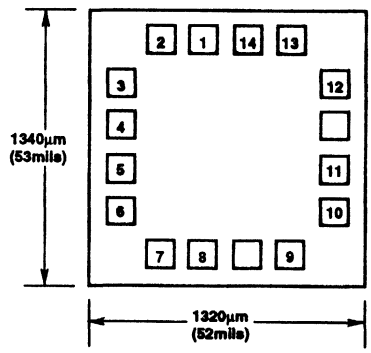
Metallization Mask Layout

Pad numbers correspond to package part pin out.

HFA3096, HFA3127, HFA3128



HFA3046



Typical Performance Curves

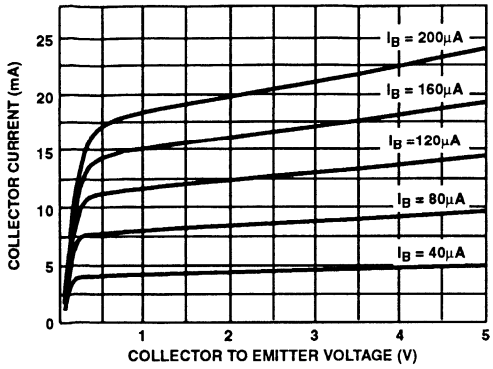


FIGURE 1. NPN COLLECTOR CURRENT vs COLLECTOR TO EMITTER VOLTAGE

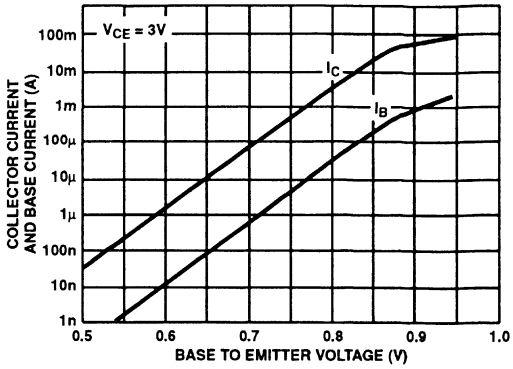


FIGURE 2. NPN COLLECTOR CURRENT AND BASE CURRENT TO EMITTER VOLTAGE

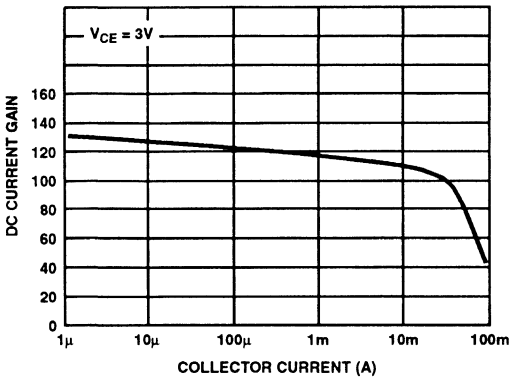


FIGURE 3. NPN DC CURRENT GAIN vs COLLECTOR CURRENT

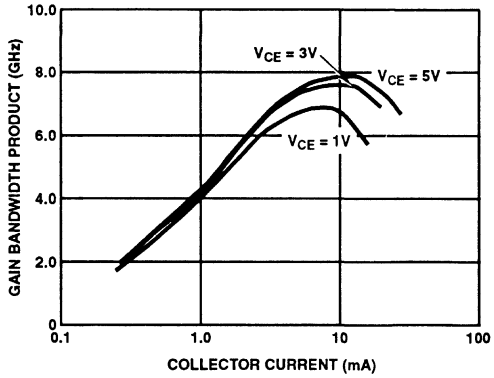


FIGURE 4. NPN GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT (UHF 3 x 50 WITH BOND PADS)

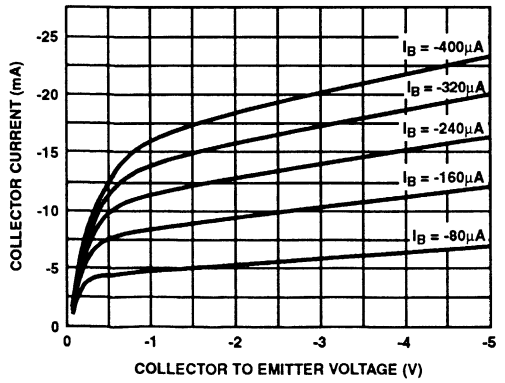


FIGURE 5. PNP COLLECTOR CURRENT vs COLLECTOR TO EMITTER VOLTAGE

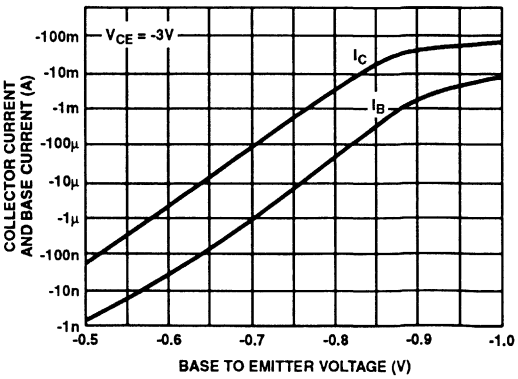


FIGURE 6. PNP COLLECTOR CURRENT AND BASE CURRENT TO EMITTER VOLTAGE

Typical Performance Curves (Continued)

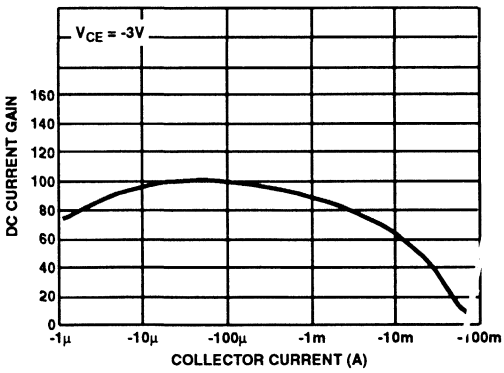


FIGURE 7. PNP DC CURRENT GAIN vs COLLECTOR CURRENT

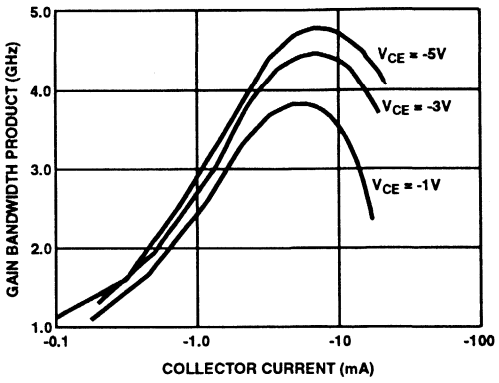


FIGURE 8. PNP GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT (UHF 3 x 50 WITH BOND PADS)

LINEAR 7

SPECIAL ANALOG CIRCUITS

NOTE: Bold Type Designates a New Product from Harris.

HARRIS SEMICONDUCTOR

CA555, LM555

Timers for Timing Delays and Oscillator Applications in Commercial, Industrial and Military Equipment

March 1993

Features

- Accurate Timing from Microseconds through Hours
- Astable and Monostable Operation
- Adjustable Duty Cycle
- Output Capable of Sourcing or Sinking up to 200mA
- Output Capable of Driving TTL Devices
- Normally ON and OFF Outputs
- High Temperature Stability . . . . . 0.005%/°C
- Directly Interchangeable with SE555, NE555, MC1555, and MC1455

Applications

- Precision Timing
- Sequential Timing
- Time Delay Generation
- Pulse Generation
- Pulse Detector
- Pulse Width and Position Modulation

Ordering Information

PART NO.	TEMP. RANGE	PACKAGE
CA0555E	-55°C to +125°C	8 Lead Plastic DIP
CA0555M	-55°C to +125°C	8 Lead SOIC
CA0555M96	-55°C to +125°C	8 Lead SOIC*
CA0555T	-55°C to +125°C	8 Pin TO-5 Metal Can
CA0555CE	0°C to +70°C	8 Lead Plastic DIP
CA0555CM	0°C to +70°C	8 Lead SOIC
CA0555CM96	0°C to +70°C	8 Lead SOIC*
CA0555CT	0°C to +70°C	8 Pin TO-5 Metal Can
LM555N	0°C to +70°C	8 Lead Plastic DIP
LM555CN	0°C to +70°C	8 Lead Plastic DIP

* Denotes Tape and Reel

Description

The CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours. These devices are also useful for astable oscillator operation and can maintain an accurately controlled free running frequency and duty cycle with only two external resistors and one capacitor.

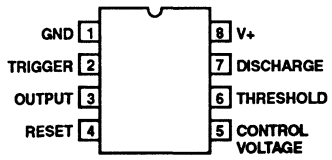
The circuits of the CA555 and CA555C may be triggered by the falling edge of the waveform signal, and the output of these circuits can source or sink up to a 200mA current or drive TTL circuits.

These types are direct replacements for industry types in packages with similar terminal arrangements e.g. SE555 and NE555, MC1555 and MC1455, respectively. The CA555 type circuits are intended for applications requiring premium electrical performance. The CA555C type circuits are intended for applications requiring less stringent electrical characteristics.

Technical data on LM branded types is identical to the corresponding CA branded types.

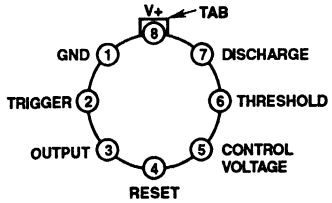
Pinouts

CA555, CA555C, LM555C (PDIP, SOIC)
TOP VIEW

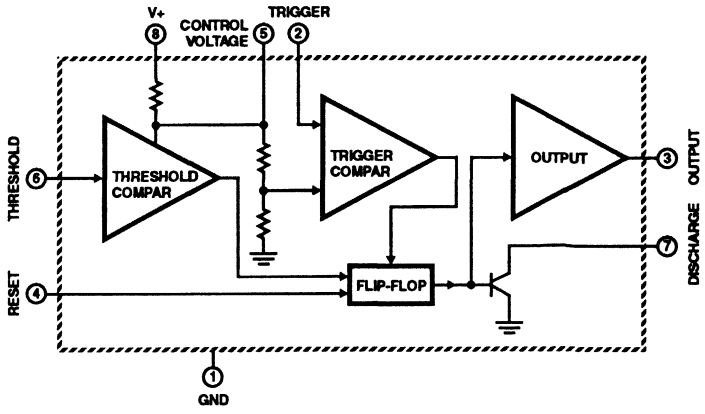


TO-5 Style Package with Formed Leads

CA555, CA555C, LM555C (METAL CAN)
TOP VIEW



Functional Diagram



7 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 834.2

Absolute Maximum Ratings

DC Supply Voltage 18V
Power Dissipation
  Up to T_A = +55°C 600mW
  Above T_A = +55°C ..... Derate Linearly 5mW/°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Packages) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
  CA555 ..... -55°C to +125°C
  CA555C ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, V+ = 5V to 15V Unless Otherwise Specified

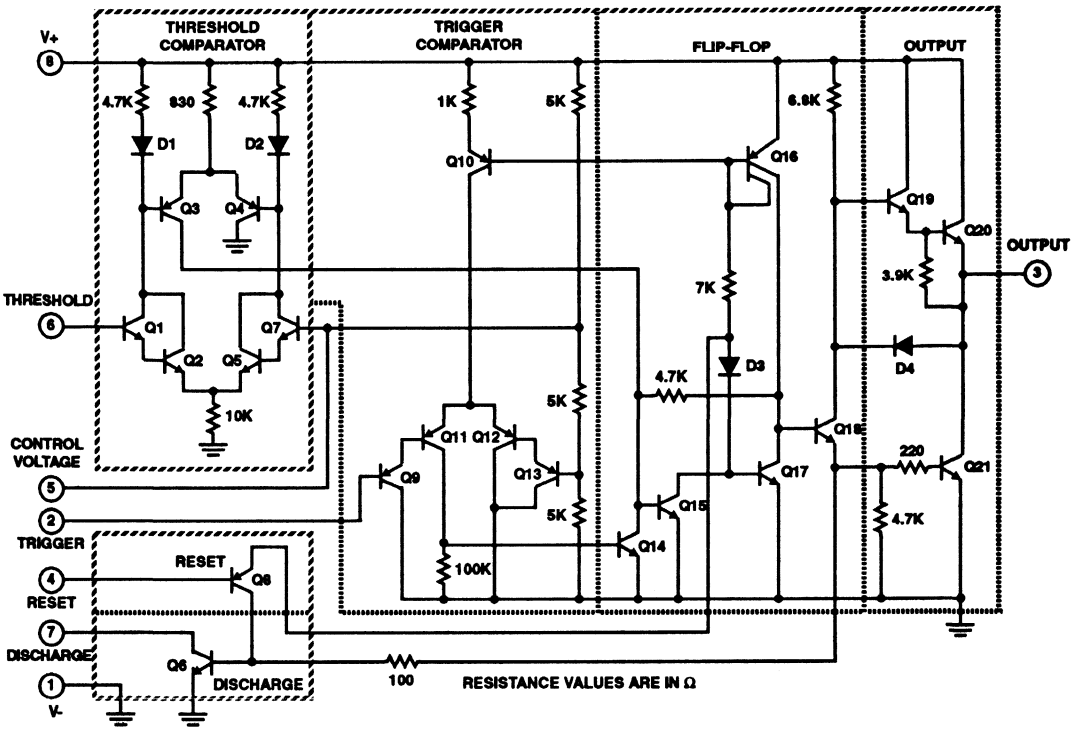
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA555			CA555C			
			MIN	TYP	MAX	MIN	TYP	MAX	
DC Supply Voltage	V+		4.5	-	18	4.5	-	16	V
DC Supply Current (Low State), Note 1	I+	V+ = 5V, $R_L = \infty$	-	3	5	-	3	6	mA
		V+ = 15V, $R_L = \infty$	-	10	12	-	10	15	mA
Threshold Voltage	V_{TH}		-	(2/3)V+	-	-	(2/3)V+	-	V
Trigger Voltage		V+ = 5V	1.45	1.67	1.9	-	1.67	-	V
		V+ = 15V	4.8	5	5.2	-	5	-	V
Trigger Current			-	0.5	-	-	0.5	-	µA
Threshold Current, Note 2	I_{TH}		-	0.1	0.25	-	0.1	0.25	µA
Reset Voltage			0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			-	0.1	-	-	0.1	-	mA
Control Voltage Level		V+ = 5V	2.9	3.33	3.8	2.6	3.33	4	V
		V+ = 15V	9.6	10	10.4	9	10	11	V
Output Voltage Low State	V_{OL}	V+ = 5V, I_{SINK} = 5mA	-	-	-	-	0.25	0.35	V
		I_{SINK} = 8mA	-	0.1	0.25	-	-	-	V
		V+ = 15V, I_{SINK} = 10mA	-	0.1	0.15	-	0.1	0.25	V
		I_{SINK} = 50mA	-	0.4	0.5	-	0.4	0.75	V
		I_{SINK} = 100mA	-	2.0	2.2	-	2.0	0.5	V
		I_{SINK} = 200mA	-	2.5	-	-	2.5	-	V
Output Voltage High State	V_{OH}	V+ = 5V, I_{SOURCE} = 100mA	3.0	3.3	-	2.75	3.3	-	V
		V+ = 15V, I_{SOURCE} = 100mA	13.0	13.3	-	12.75	13.3	-	V
		I_{SOURCE} = 200mA	-	12.5	-	-	12.5	-	V
Timing Error (Monostable)		R_1, R_2 = 1kΩ to 100kΩ, C = 0.1µF Tested at V+ = 5V, V+ = 15V	-	0.5	2	-	1	-	%
Frequency Drift with Temperature			-	30	100	-	50	-	ppm/°C
Drift with Supply Voltage			-	0.05	0.2	-	0.1	-	%/V
Output Rise Time	t_R		-	100	-	-	100	-	ns
Output Fall Time	t_F		-	100	-	-	100	-	ns

NOTES:

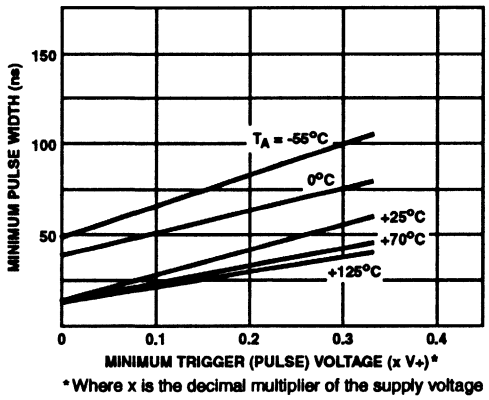
1. When the output is in a high state, the DC supply current is typically 1mA less than the low state value.
2. The threshold current will determine the sum of the values of R_1 and R_2 to be used in Figure 14 (astable operation); the maximum total $R_1 + R_2$ = 20MΩ.

Schematic Diagram

CA555 AND CA555C



Typical Performance Curves



*Where x is the decimal multiplier of the supply voltage

FIGURE 1. MINIMUM PULSE WIDTH vs MINIMUM TRIGGER VOLTAGE

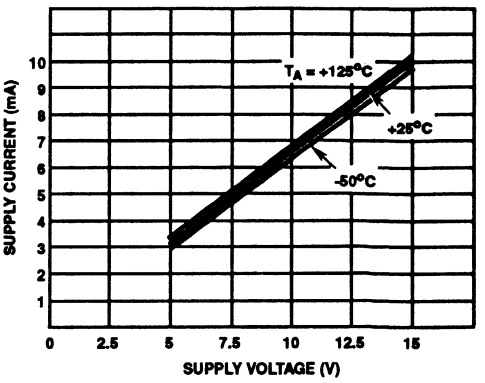


FIGURE 2. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves

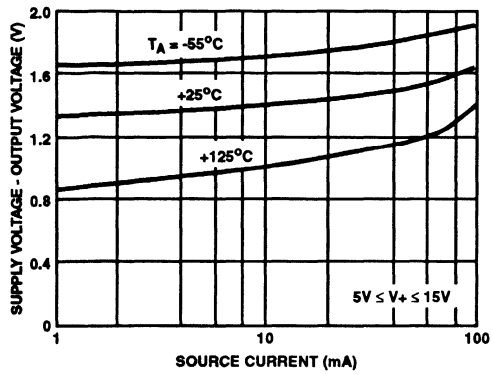


FIGURE 3. OUTPUT VOLTAGE DROP (HIGH STATE) vs SOURCE CURRENT

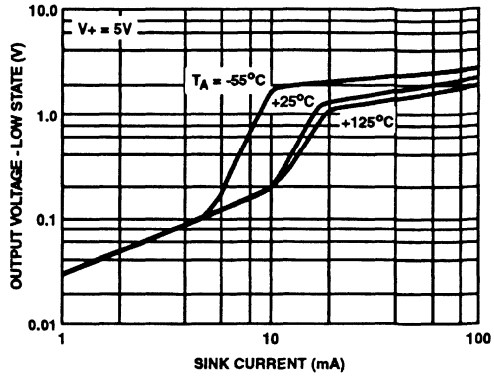


FIGURE 4. OUTPUT VOLTAGE LOW STATE vs SINK CURRENT AT V+ = 5V

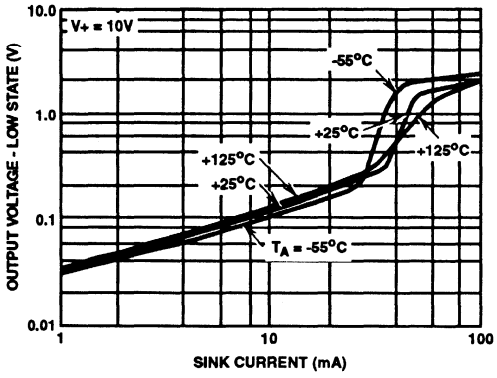


FIGURE 5. OUTPUT VOLTAGE LOW STATE vs SINK CURRENT AT V+ = 10V

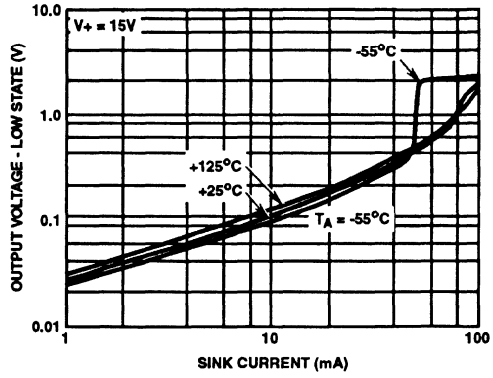


FIGURE 6. OUTPUT VOLTAGE LOW STATE vs SINK CURRENT AT V+ = 15V

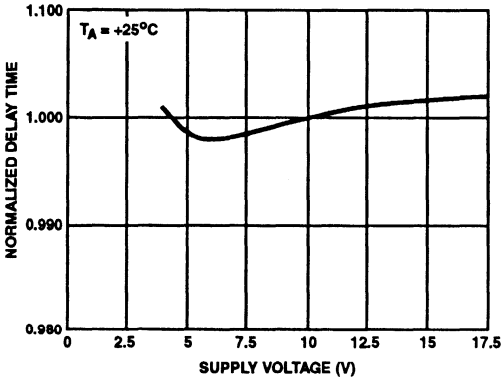


FIGURE 7. DELAY TIME vs SUPPLY VOLTAGE

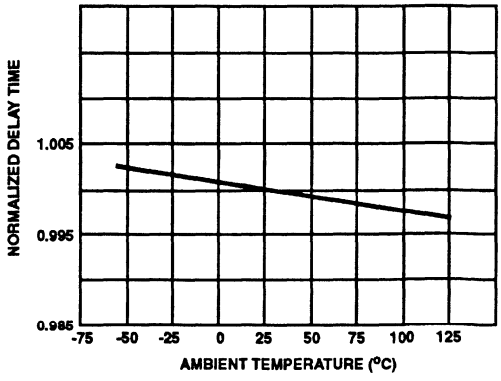


FIGURE 8. DELAY TIME vs TEMPERATURE

Typical Performance Curves

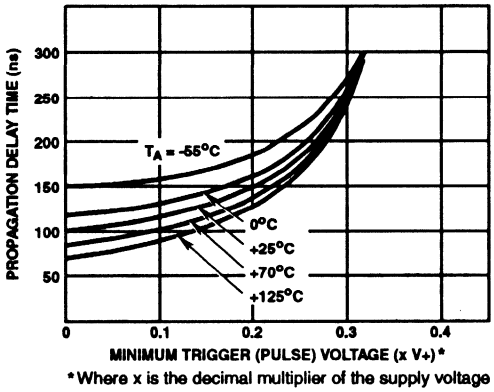


FIGURE 9. PROPAGATION DELAY TIME vs TRIGGER VOLTAGE

Typical Applications

Reset Timer (Monostable Operation)

Figure 10 shows the CA555 connected as a reset timer. In this mode of operation capacitor C_T is initially held discharged by a transistor on the integrated circuit. Upon closing the "start" switch, or applying a negative trigger pulse to terminal 2, the integral timer flip-flop is "set" and releases the short circuit across C_T which drives the output voltage "high" (relay energized). The action allows the voltage across the capacitor to increase exponentially with the constant $t = R_1C_T$. When the voltage across the capacitor equals 2/3 V+, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state.

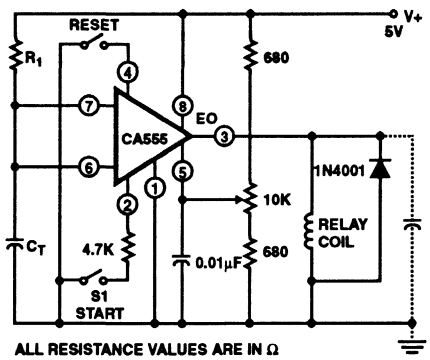


FIGURE 10. RESET TIMER (MONOSTABLE OPERATION)

Since the charge rate and threshold level of the comparator are both directly proportional to V+, the timing interval is relatively independent of supply voltage variations. Typically, the timing varies only 0.05% for a 1V change in V+.

Applying a negative pulse simultaneously to the reset terminal (4) and the trigger terminal (2) during the timing cycle discharges C_T and causes the timing cycle to restart. Momentarily closing only the reset switch during the timing interval discharges C_T, but the timing cycle does not restart.

Figure 11 shows the typical waveforms generated during this mode of operation, and Figure 12 gives the family of time delay curves with variations in R_1 and C_T.

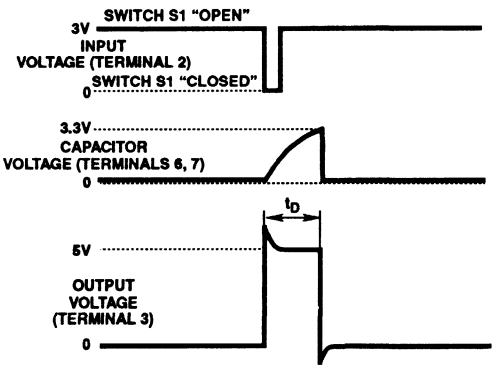


FIGURE 11. TYPICAL WAVEFORMS FOR RESET TIMER

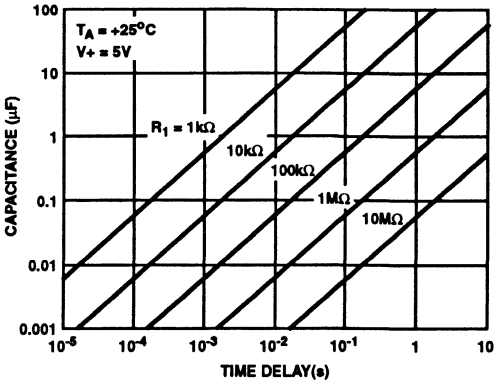


FIGURE 12. TIME DELAY vs RESISTANCE AND CAPACITANCE

Repeat Cycle Timer (Astable Operation)

Figure 13 shows the CA555 connected as a repeat cycle timer. In this mode of operation, the total period is a function of both R_1 and R_2.

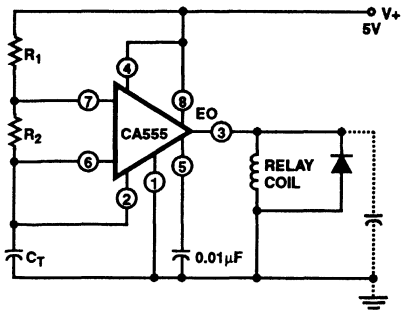


FIGURE 13. REPEAT CYCLE TIMER (ASTABLE OPERATION)

$$T = 0.693\ (R_1 + 2R_2)\ C_T = t_1 + t_2$$

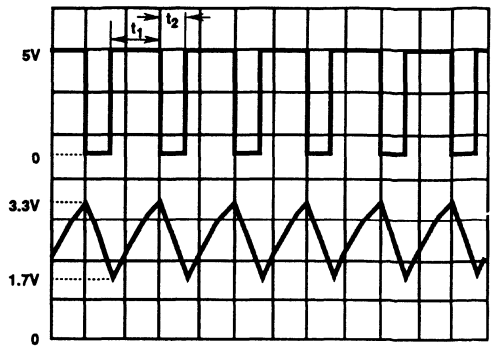
where $t_1 = 0.693\ (R_1 + R_2)\ C_T$

and $t_2 = 0.693\ (R_2)\ C_T$

the duty cycle is:

$$\frac{t_1}{t_1 + t_2} = \frac{R_1 + R_2}{R_1 + 2R_2}$$

Typical waveforms generated during this mode of operation are shown in Figure 14. Figure 15 gives the family of curves of free running frequency with variations in the value of (R_1 + $2R_2$) and C_T.



Top Trace: Output voltage (2V/div. and 0.5ms/div.)
Bottom Trace: Capacitor voltage (1V/div. and 0.5ms/div.)

FIGURE 14. TYPICAL WAVEFORMS FOR REPEAT CYCLE TIMER

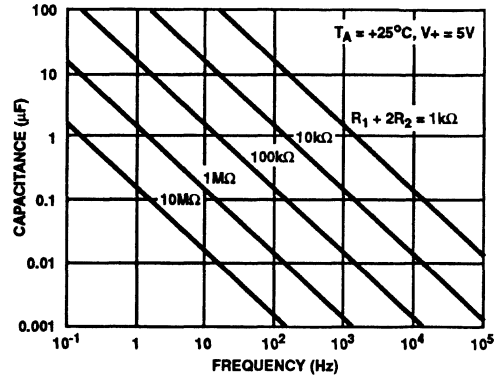


FIGURE 15. FREE RUNNING FREQUENCY OF REPEAT CYCLE TIMER WITH VARIATION IN CAPACITANCE AND RESISTANCE

CA1391, CA1394

March 1993

TV Horizontal Processors

Features

- **CA1391E - Positive Horizontal Sawtooth Input**
- **CA1394E - Negative Horizontal Sawtooth Input**
- **Internal Shunt Regulator**
- **Linear Balanced Phase Detector**
- **Preset Hold Control Capability**
- **Pull-In ..... ±300Hz (Typ.)**
- **Low Thermal Frequency Drift**
- **Small Static Phase Error**
- **Variable Output Duty Cycle**
- **Adjustable DC Loop Gain**

Description

The Harris CA1391E and CA1394E are monolithic integrated circuits designed for use in the low-level horizontal section of monochrome or color television receivers. Functions include a phase detector, an oscillator, a regulator, and a pre-driver.

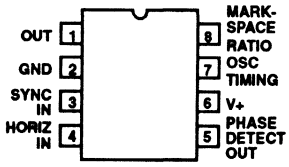
The CA1391E and CA1394E are electrically equivalent and pin compatible with industry types 1391 and 1394 in similar packages.

Ordering Information

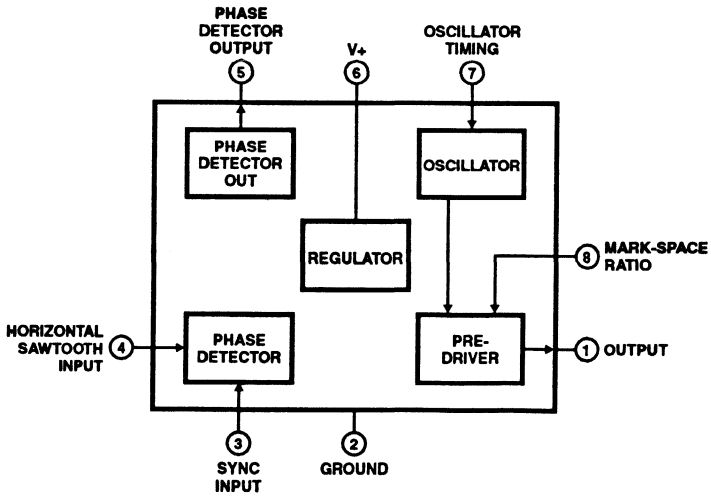
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA1391E	0°C to +85°C	8 Lead Plastic DIP
CA1394E	0°C to +85°C	8 Lead Plastic DIP

Pinout

CA1391, CA1394
(PDIP)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings T_A = +25°C, Unless Otherwise Specified

DC Supply Current 40mA
DC Output Voltage 40V
DC Output Current 30mA
Sync Input Voltage ..... $5V_{P-P}$
Sawtooth Input Voltage ..... $5V_{P-P}$
Power Dissipation
  Up to T_A = +25°C 625mW
  Above T_A = +25°C ..... Derate Linearly 5mW/°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... 0°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

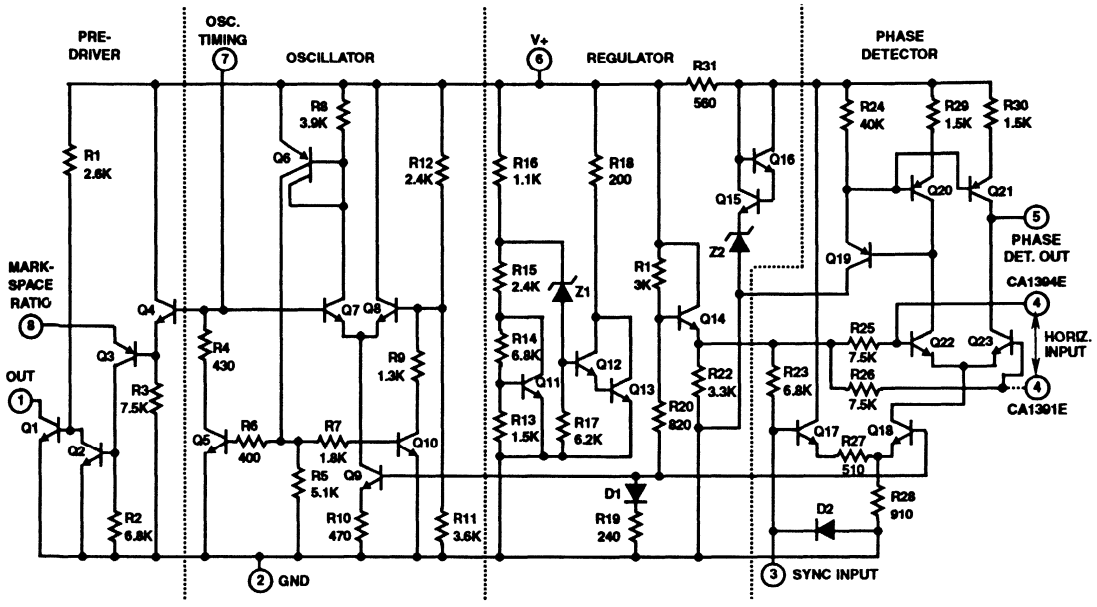
Electrical Specifications T_A = +25°C (See Figure 2)

PARAMETERS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Supply Voltage	S1, S5, S6 = 2 S2, S3, S4, S7, S8 = 1 Measure Terminal 6 to GND	8	-	9	V
Free Running Frequency	S1, S5, S6 = 2 S2, S3, S4, S7, S8 = 1 Counter to Terminal 1	14734	-	16734	Hz
Output Leakage	S2, S3, S6, S8 = 1 S1, S4, S5, S7 = 2 Measure Terminal 1 to 25V	-	10	-	mV
Output Saturation	S2, S3, S5, S6, S8 = 1 S1, S4, S7 = 2 Measure Terminal 1 to GND	-	60	-	mV
Phase Detector Bias	S2, S5, S6, S8 = 1 S1, S3, S4, S7 = 2 Measure Terminal 3 to GND	-	1.9	-	V
Phase Detector Leak	S5, S8 = 1 S1, S2, S3, S4, S6, S7 = 2 Measure Terminal 5 to +4V	-2	-	2	mV
Phase Detector Low	S1, S5, S8 = 1 S2, S3, S4, S6, S7 = 2 Measure Terminal 5 to +4V	-0.55 (Note 1)	-	-	V
Phase Detector High	S1, S5, S6, S8 = 1 S2, S3, S4, S7 = 2 Measure Terminal 5 to +4V	+0.55 (Note 1)	-	-	V
Phase Detector Balance	$V_{DET2} + V_{DET3}$	-100	-	100	mV
Sync Diode	S1, S2, S3, S4, S6, S7 = 1 S5, S8 = 2	0.3	-	1.2	V
Static Phase Error	See Figure 3	-	0.5	-	µs
Oscillator Pull In Range		-	±300	-	Hz
Oscillator Hold In Range		-	±900	-	Hz

NOTE:

1. Polarity reversed in the CA1391.

Schematic Diagram



NOTE: All resistances are in Ω

Circuit Operation (See Schematic Diagram)

The CA1391 and CA1394 contain the oscillator, phase detector, and predriver sections necessary for the television horizontal oscillator and AFC loop.

The oscillator is an RC type with terminal 7 used to control the timing. If it is assumed that Q7 is initially off, then an external capacitor connected from terminal 7 to ground charges through an external resistance connected between terminals 6 and 7. As soon as the voltage at terminal 7 exceeds the potential set at the base of Q8 by resistors R11 and R12, Q7 turns on, and Q6 supplies base current to Q5 and Q10. Transistor Q5 discharges the capacitor through R4 until the base bias of Q7 falls below that of Q8 at which time, Q7 turns off, and the cycle repeats.

The sawtooth generated at the base of Q4 appears across R3 and turns off Q3 whenever the sawtooth voltage rises to a value that exceeds the bias set at terminal 8. By adjusting the potential at terminal 8, the duty cycle at the pre-drive output (terminal 1) may be changed. The phase detector is isolated from the remainder of the circuit by R31, Z2, Q15 and Q16. The phase detector consists of the comparator Q22 and Q23, and the gated current source Q18. Negative going sync pulses at terminal 3 turn off Q17, and the current division between Q22 and Q23 is then determined by the phase relationship of the sync and the sawtooth waveform at terminal 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents flow in the collectors of Q22 and Q23 during each half of the sync pulse period. The current in Q22 is turned around by current mirror Q20 and Q21 so that there is no net output current at terminal 5 for balanced conditions. When a phase offset occurs, current flows either in or out of terminal 5. In circuit applications, this terminal is connected to terminal 7 through an external low pass filter, thereby controlling the oscillator.

Shunt regulation for the circuit is obtained by using a V_{BE} and zener multiplier. Resistors R13 and R14 multiply the V_{BE} of Q11, and the ratio of R15 and R16 multiplies the voltage of the zener diode Z1.

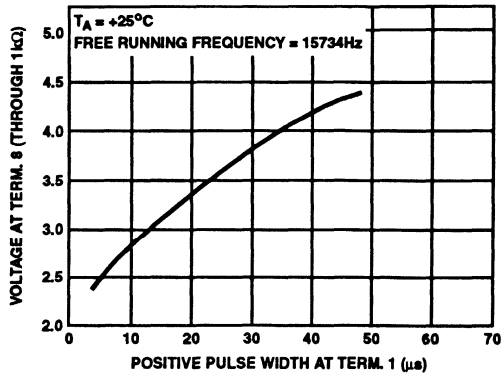


FIGURE 1. DUTY CYCLE AT THE PRE-DRIVE OUTPUT (TERM. 1) AS IT IS AFFECTED BY THE INPUT AT TERM. 8

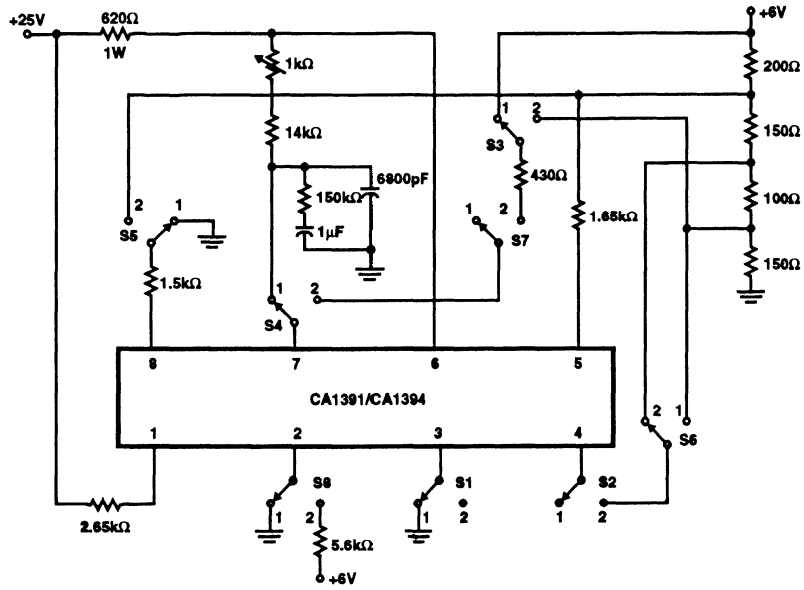


FIGURE 2. DC TEST CIRCUIT

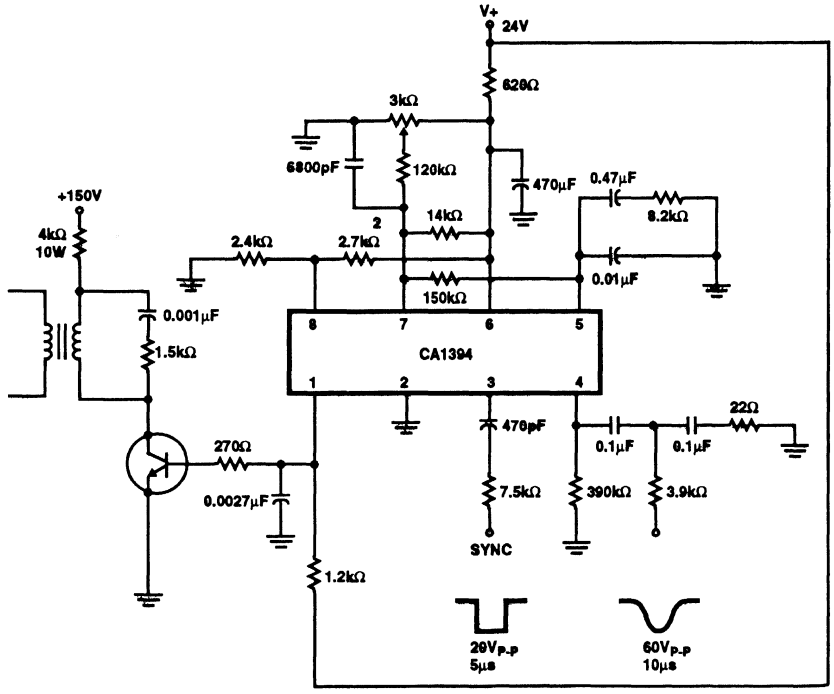


FIGURE 3. TYPICAL CIRCUIT APPLICATION

HARRIS SEMICONDUCTOR

CA3089

March 1993

FM IF System

Features

- For FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers
- Includes: IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Muting (Squelch), and Tuning Meter
- Exceptional Limiting Sensitivity..... 12μV (Typ.) at -3dB Point
- Low Distortion: .....(with Double-Tuned Coil) - 0.1% (Typ.)
- Single-Coil Tuning Capability
- High Recovered Audio.....400mV (Typ.)
- Provides Specific Signal for Control of Interchannel Muting (Squelch)
- Provides Specific Signal for Direct Drive of a Tuning Meter
- Provides Delayed AGC Voltage for RF Amplifier
- Provides a Specific Circuit for Flexible AFC
- Internal Supply-Voltage Regulators

Description

Harris CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. The block diagram shows the CA3089 features, which include a three-stage FM-IF amplifier/ limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as delayed AGC for the RF tuner, and AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5V to +16 V.

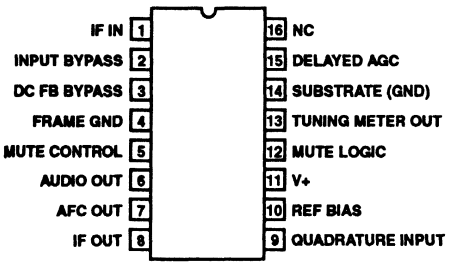
The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

Ordering Information

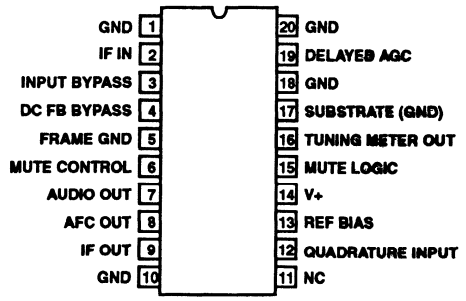
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3089E	-40°C to +85°C	16 Lead Plastic DIP
CA3089F	-40°C to +85°C	16 Lead Ceramic DIP
CA3089M1	-40°C to +85°C	20 Lead SOIC

Pinouts

CA3089
(PDIP, CDIP)
TOP VIEW



CA3089
(SOIC)
TOP VIEW



SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 561.2

Absolute Maximum Ratings

Supply Voltage
- Between V+ and Frame GND 16V
- Between V+ and Substrate GND 16V

DC Current (Out of Delayed AGC) 2mA

Power Dissipation
- Up to T_A = +60°C 600mW
- Above T_A = +60°C ..... Derate Linearly 6.7mW/°C

Junction Temperature ..... +175°C

Junction Temperature (Plastic Package) ..... +150°C

Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -40°C ≤ T_A ≤ +85°C

Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

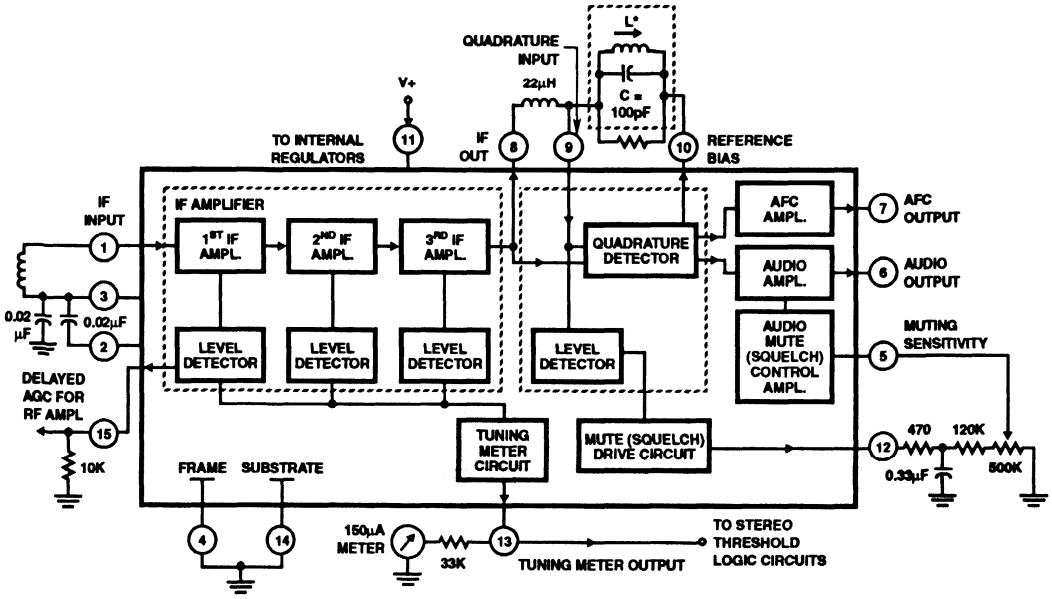
T_A = +25°C, V+ = 12V (See Figures 3 and 4)

PARAMETERS (Note 2)	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
STATIC (DC) CHARACTERISTICS						
Quiescent Circuit Current	No signal input, Non muted		16	23	30	mA
DC Voltages:						
Terminal 1 (IF Input)			1.2	1.9	2.4	V
Terminal 2 (AC Return to Input)			1.2	1.9	2.4	V
Terminal 3 (DC Bias to Input)			1.2	1.9	2.4	V
Terminal 6 (Audio Output)			5.0	5.6	6.0	V
Terminal 10 (DC Reference)			5.0	5.6	6.0	V
DYNAMIC CHARACTERISTICS						
Input Limiting Voltage (-3dB point), V_1 (lim)	-	f_O = 10.7MHz, f_{MOD} = 400Hz, Deviation = ±75kHz	-	12	25	µV
AM Rejection (Term. 6), AMR	V_{IN} = 0.1V, AM Mod. = 30%		45	55	-	dB
Recovered AF Voltage (Term. 6) V_O (AF)	V_{IN} = 0.1V		300	400	500	mV
Total Harmonic Distortion, THD: (Note 1)						
Single Tuned (Term. 6)			-	0.5	1.0	%
Double Tuned (Term. 6)			-	0.1	-	%
Signal plus Noise to Noise Ratio (Term. 6)			60	67	-	dB

NOTES:

1. THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.
2. Terminal numbers refer to 16 pin DIP.

Block Diagram



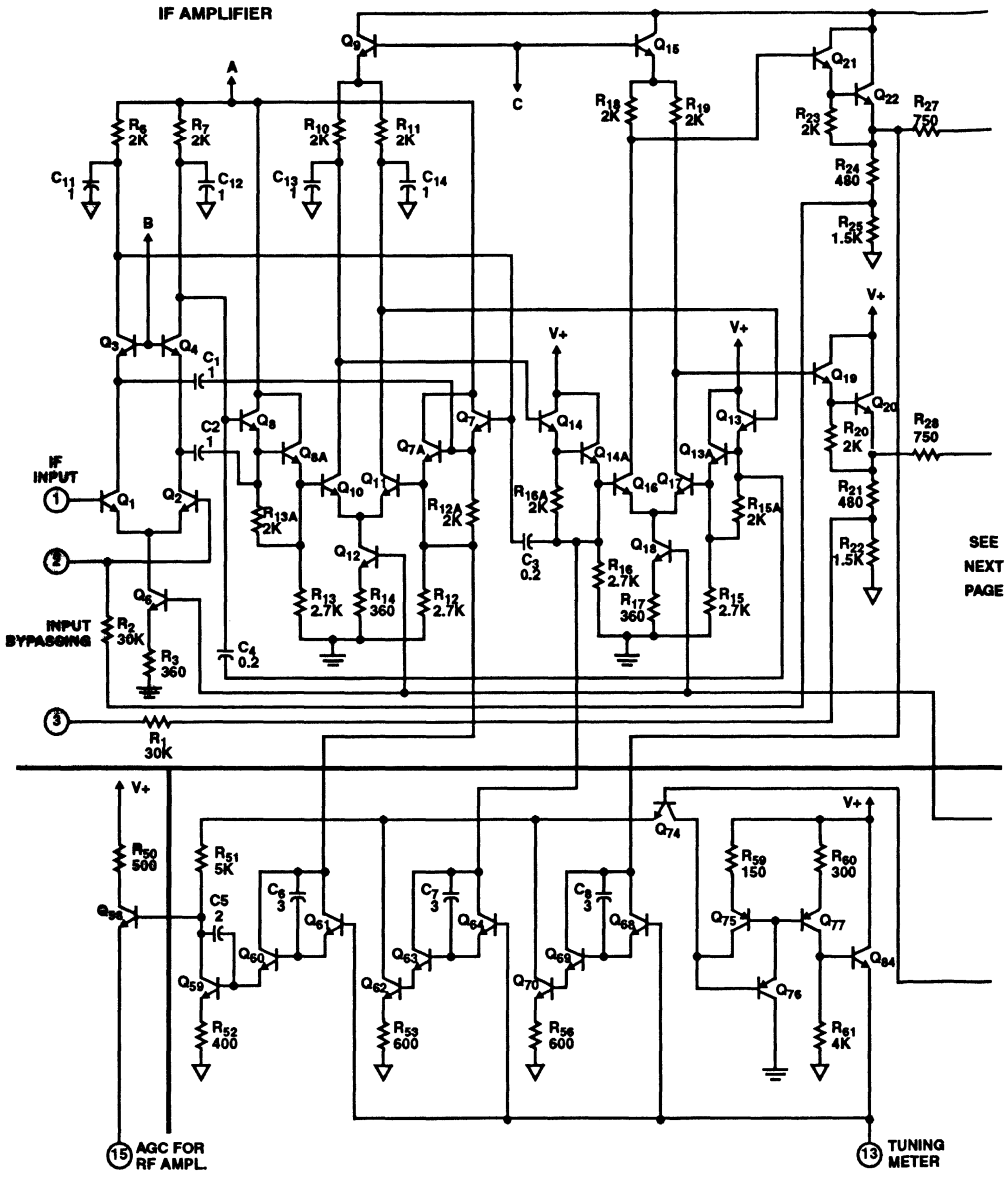
All resistance values are in Ω

*L Tunes with 100pF (C) at 10.7MHz

$Q_O \equiv 75$ (G.I. EX22741 or equivalent)

Pin numbers refer to 16 pin DIP

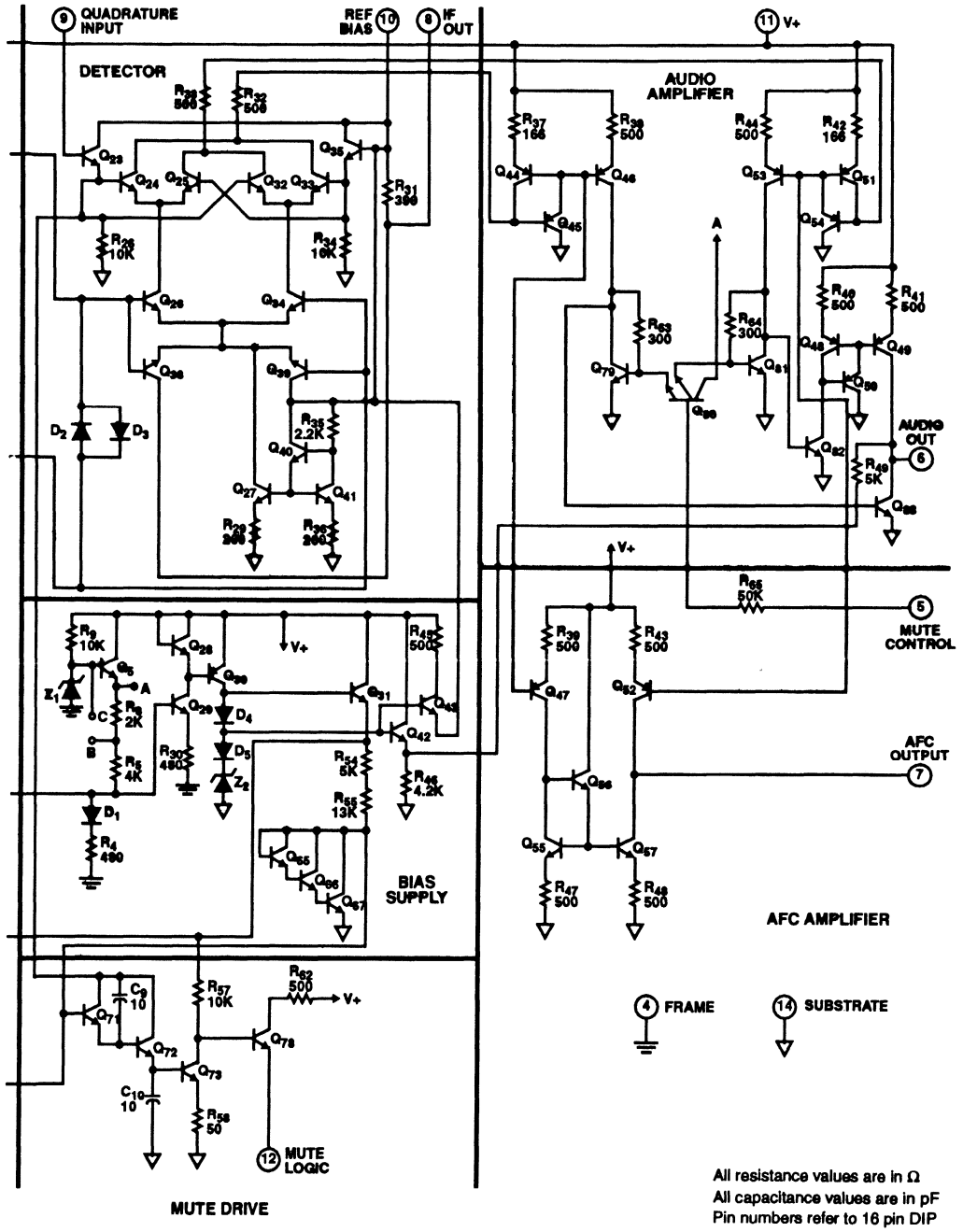
Schematic Diagram



Pin numbers refer to 16 pin DIP

LEVEL DETECTOR & METER CIRCUIT

Schematic Diagram (Continued)



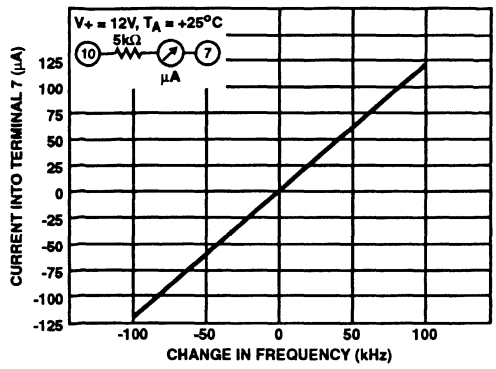


FIGURE 1. AFC CHARACTERISTICS (CURRENT AT TERM. 7) AS A FUNCTION OF CHANGE IN FREQUENCY. (SEE TEST CIRCUIT FIGURE 3.)

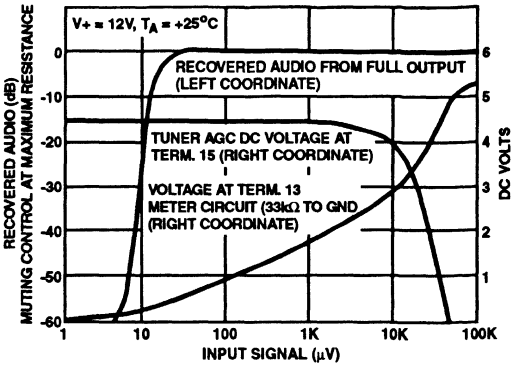
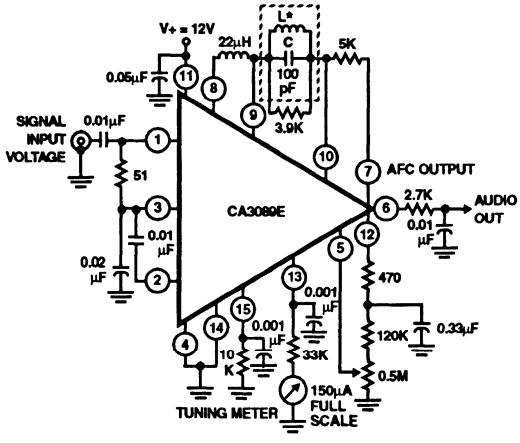
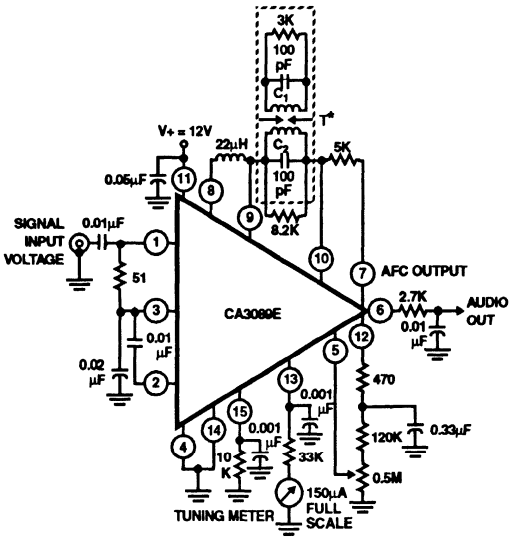


FIGURE 2. MUTING ACTION, TUNER AGC, AND TUNING METER OUTPUT AS A FUNCTION OF INPUT SIGNAL VOLTAGE. (SEE TEST CIRCUIT FIGURE 3.)



All resistance values are in Ω
* L tunes with 100pF (C) at 10.7MHz
Q_0 (unloaded) ≅ 75 (G.I. Automatic Mfg. Div. EX22741 or equivalent)

FIGURE 3. TEST CIRCUIT FOR CA3089E USING A SINGLE-TUNED DETECTOR COIL.



All resistance values are in Ω

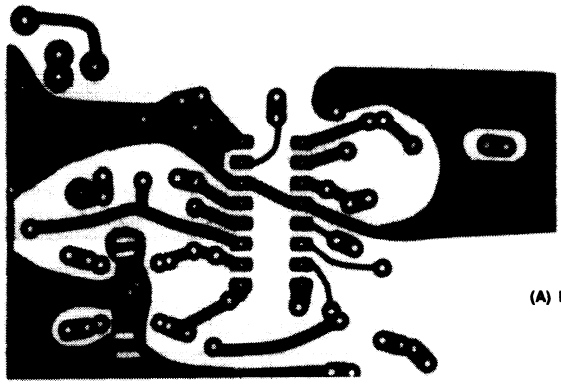
* T PRI. - Q_0 (unloaded) ≅ 75 (tunes with 100pF (C_1) 20↑ of 34e on $^7/_{32}$" dia. form)

SEC. - Q_0 (unloaded) ≅ 75 (tunes with 100pF (C_2) 20↑ of 34e on $^7/_{32}$" dia. form)

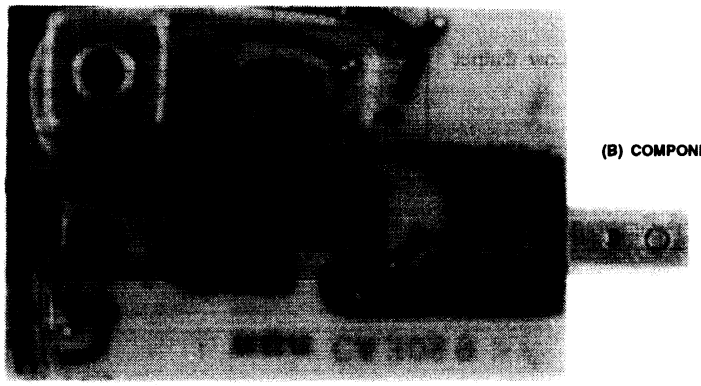
kQ (percent of critical coupling) ≅ 70%
(Adjusted for coil voltage V_C) = 150mV

Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4mm.

FIGURE 4. TEST CIRCUIT FOR CA3089E USING A DOUBLE-TUNED DETECTOR COIL.

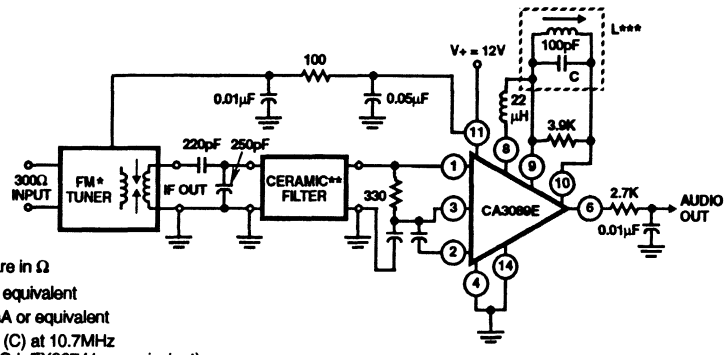


(A) BOTTOM VIEW OF PRINTED CIRCUIT BOARD



(B) COMPONENT SIDE - TOP VIEW

FIGURE 5. ACTUAL SIZE PHOTOGRAPHS OF THE CA3089E & OUTBOARD COMPONENTS MOUNTED ON A PRINTED-CIRCUIT BOARD.



All resistance values are in Ω

* Waller 4SN3FIC or equivalent

** Murata SFG 10.7mA or equivalent

*** L tunes with 100pF (C) at 10.7MHz
Q_0 unloaded ≡ 75 (G.I. EX22741 or equivalent)

Performance data at f_O = 98MHz, f_{MOD} = 400Hz, Deviation = ±75kHz:

-3dB Limiting Sensitivity . . . . . 2μV (Antenna Level)
20dB Quieting Sensitivity . . . . . 1μV (Antenna Level)
30dB Quieting Sensitivity . . . . . 1.5μV (Antenna Level)

FIGURE 6. TYPICAL FM TUNER USING THE CA3089E WITH A SINGLE TUNED DETECTOR COIL

HARRIS SEMICONDUCTOR

CA3126

March 1993

TV Chroma Processor

Features

- Phase Locked Subcarrier Regeneration Utilizes Sample-and-Hold Techniques
- Automatic Chrominance Control (ACC)/Killer Detector Employs Sample-and-Hold Techniques
- Supplementary ACC with an Overload Detector to Prevent Oversaturation of this Picture Tube
- Sinusoidal Subcarrier Output
- Keyed Chroma Output
- Emitter Follower Buffered Outputs for Low Output Impedance
- Linear DC Saturation Control

Applications

- TV/CATV Receiver Circuits
- NTSC Color Decoder/Processor
- Computer Graphics Subcarrier Regenerator
- Timing Reference for Frame Grabbers
- DSP Clock Timing Reference Source

Description

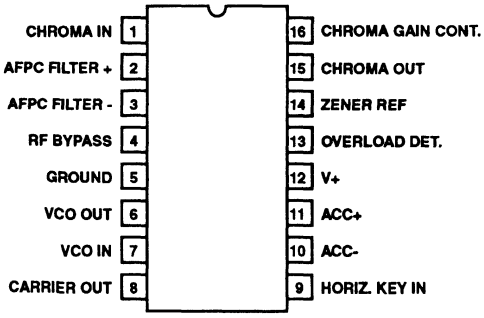
The Harris CA3126 is a monolithic silicon integrated circuit designed for TV chroma processing and is ideally suited for NTSC color graphic applications that require subcarrier regeneration of the color burst signal.

Ordering Information

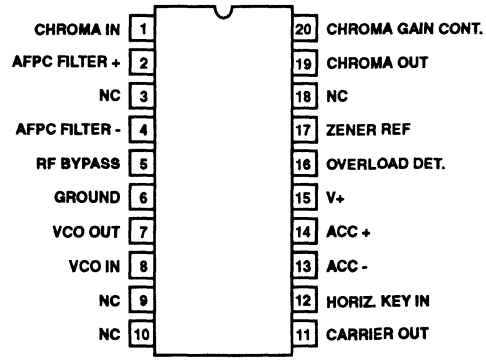
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3126E	-40°C to +85°C	16 Lead Plastic DIP
CA3126Q	-40°C to +85°C	16 Lead Quad-In-Line Plastic DIP
CA3126M1	-40°C to +85°C	20 Lead SOIC

Pinouts

CA3126
(PDIP, QUAD FLATPACK)
TOP VIEW



CA3126
(SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **860.2**

Absolute Maximum Ratings (T_A = +25°C)

Power Dissipation
- Up to T_A = +55°C 750mW
- Above T_A = -55°C ..... Derate Linearly 7.9mW/°C

DC Supply Voltage (V+ to GND)* 13.2V

DC Current:
- Into V+ Pin 38mA
- Into Zener Reference Pin 20mA

DC Voltage (Horizontal Key In)
- Negative Rating ..... -5V
- Positive Rating 3V

Junction Temperature (Plastic Packages) ..... +150°C

Lead Temperature (Soldering 10 Sec.) ..... +300°C

* This rating does not apply when using the internal zener reference in conjunction with an external pass transistor.

Operating Conditions

Operating Temperature Range ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, chroma control at maximum position for all characteristics tests except for chroma output test. For this test, control should be set at minimum position. Electrical characteristics referenced to test circuit, Figure 1.

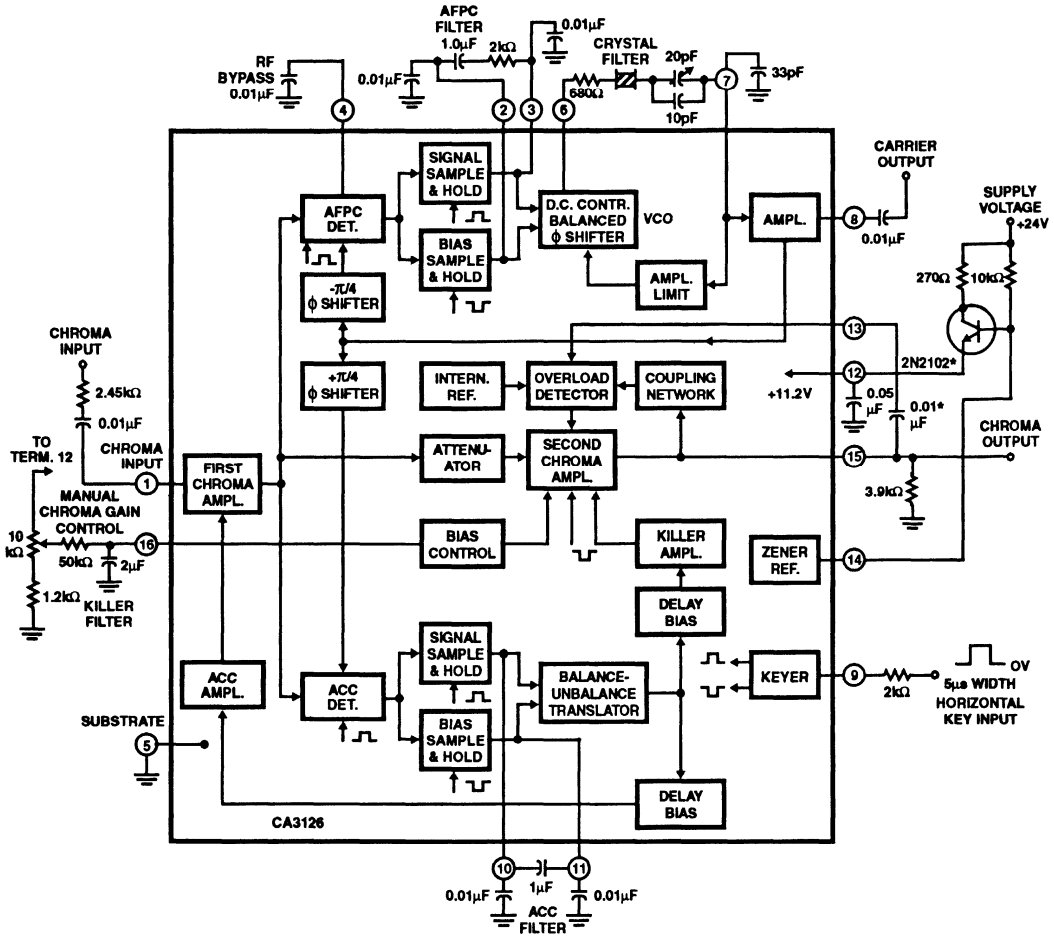
PARAMETERS	TERMINAL, MEASUREMENT AND SYMBOL	SWITCH POS.		V_{CHROMA} INPUT TP1	LIMITS			UNITS
		S1	S2		MIN	TYP	MAX	
DC ELECTRICAL SPECIFICATIONS								
Voltage Regulator	V_{12}	2	2	0	10.1	11.2	12.1	V
Supply Current	I_{12}	2	2	0	16	25	38	mA
SWITCHING ELECTRICAL SPECIFICATIONS (Note 1)								
Pull-In Range (Note 2)	V_8	(Note 2)	2	$0.5V_{P-P}$	±250	-	-	Hz
Oscillator Output	V_8	2	2	0	0.6	1.0	-	V_{P-P}
100% Chroma Output	V_{15}	1	2	$0.5V_{P-P}$	1.4	2.7	-	V_{P-P}
Overload Detector	V_{15}	1	1	$0.5V_{P-P}$	0.4	-	0.7	V_{P-P}
Minimum Chroma Output	V_{15}	1	2	$0.5V_{P-P}$	-	-	20	mV_{P-P}
200% Chroma Output	V_{15}	1	2	$1V_{P-P}$	70	100	140	% of 100% reading
20% Chroma Output	V_{15}	1	2	$0.1V_{P-P}$	40	-	105	
Kill Level	V_{TP1}	1	2	Vary	5	-	60	mV_{P-P}

NOTES:

1. Except for pull-in range testing, tune oscillator trimmer capacitor for free running frequency of 3.579545MHz ±10Hz.
2. Set Switch 1 to Position 2, detune oscillator ±250Hz, set Switch 1 to Position 1, and check for oscillator pull-in.

Block Diagram

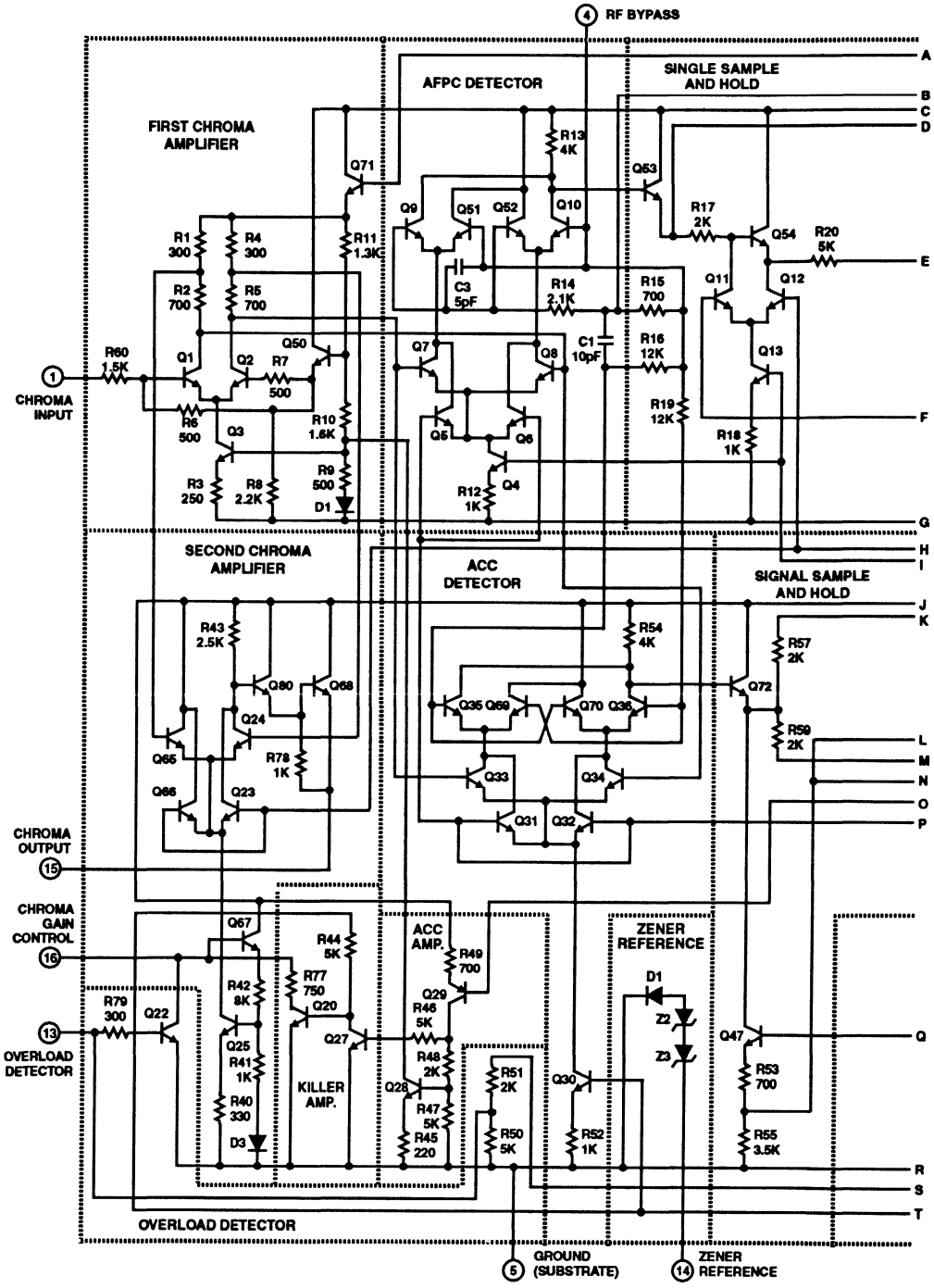
TV CHROMA PROCESSOR



* Optional design features

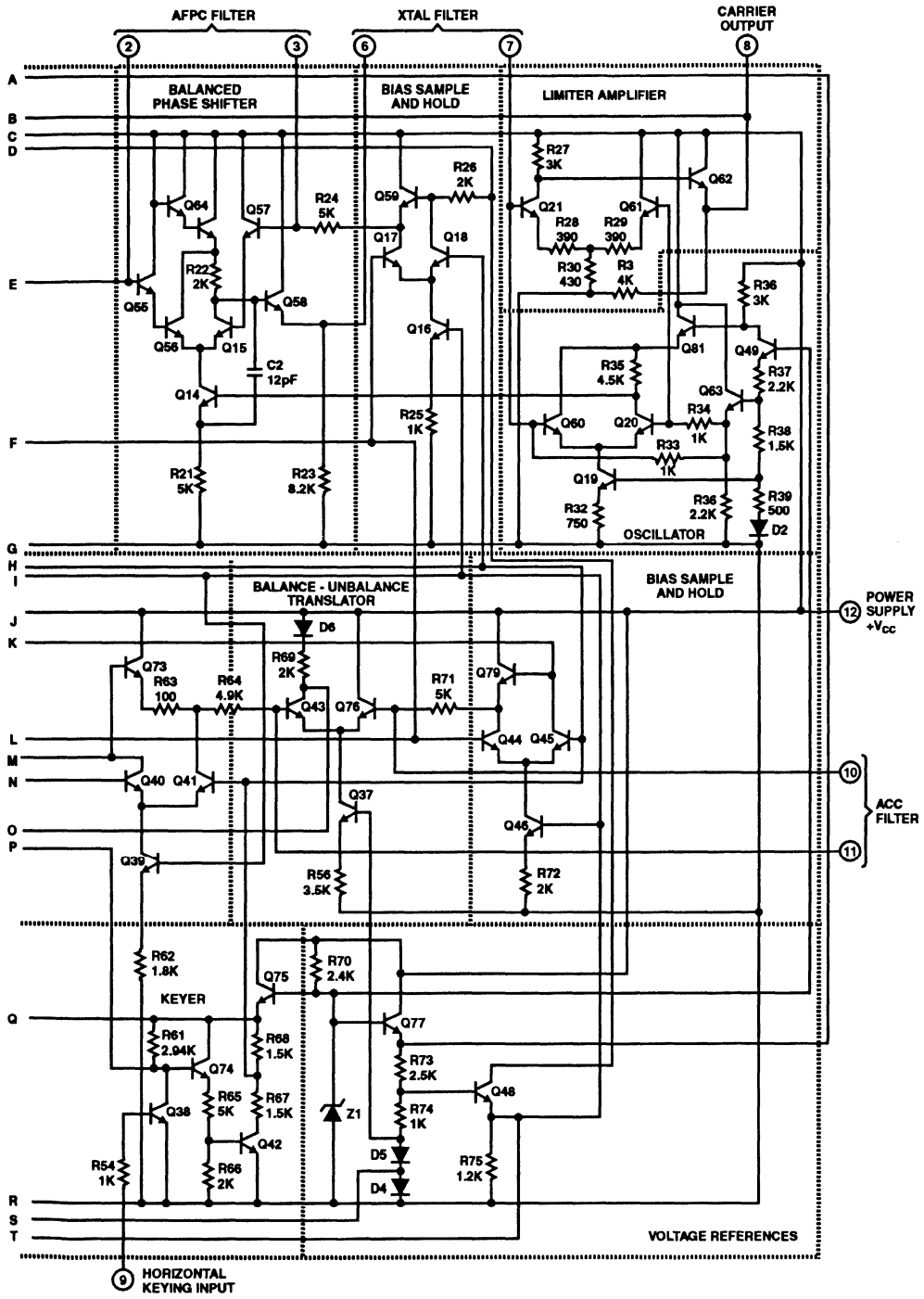
Pinout numbers refer to CA3126E & CA3126Q

Schematic Diagram

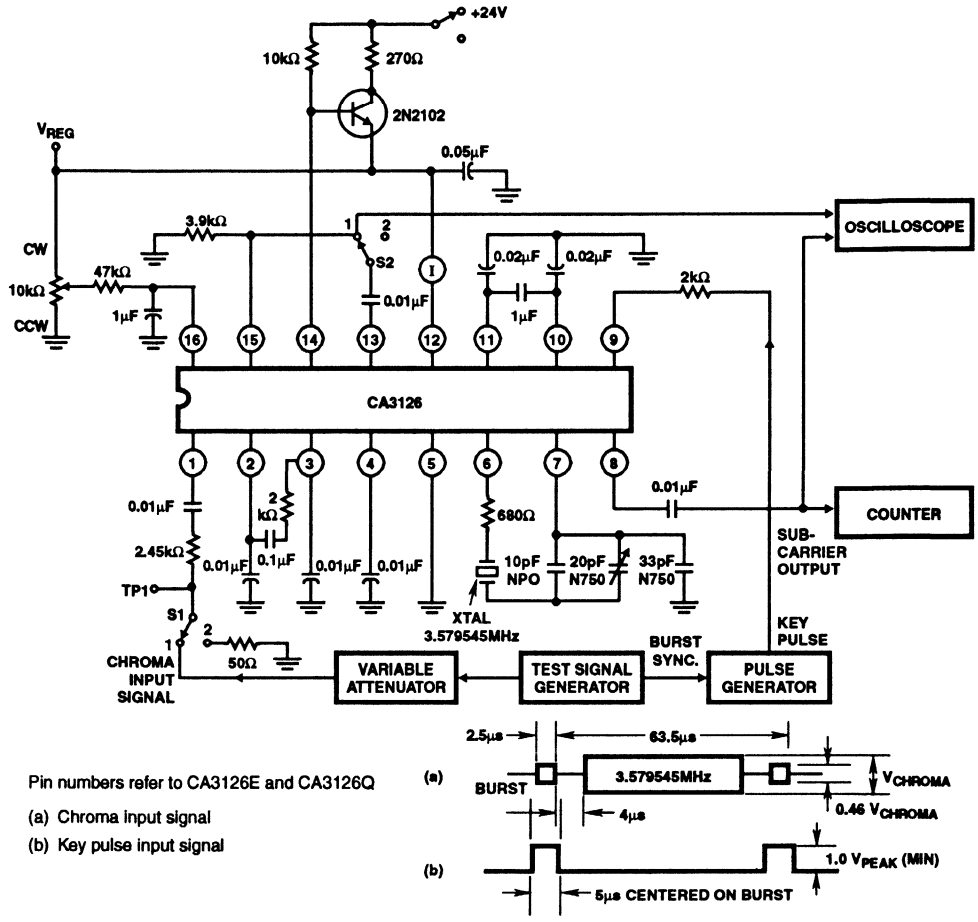


Pin numbers refer to CA3126E and CA3126Q. Resistance values are in Ω.

Schematic Diagram (Continued)



Test Circuit



Pin numbers refer to CA3126E and CA3126Q

(a) Chroma input signal

(b) Key pulse input signal

FIGURE 1.

Circuit Description (Pin numbers refer to E and Q packages)

The following paragraphs briefly describe the circuit operation of the CA3126 (shown in the Block Diagram and Schematic Diagram). A detailed description of the operation of various portions of the CA3126 is given in ICAN-6247, "Application of the CA3126 Chroma-Processing IC Using Sample-and-Hold Techniques".

The chroma input is applied to Terminal 1 through the desired band-shaping network. A 2,450Ω resistor should be placed in series with Terminal 1 to minimize oscillator pickup in the first chroma amplifier. This amplifier supplies signals to the second chroma amplifier and to the ACC and AFPC detectors. The first chroma amplifier is gain-controlled by the ACC amplifier.

A horizontal keying pulse is applied to Terminal 9. This pulse must be present to ensure proper operation of the oscillator circuit. The subcarrier burst is sampled during the keying interval in the AFPC detector. The error voltage, produced at Terminal 2 and proportional to the burst phase, is compared to the quiescent bias voltage at Terminal 3 by the sample-and-hold circuitry. This "compared" voltage controls the phase- shifting network in the phase-locked loop. The operation of the AFPC loop is independent of any external adjustments or voltages except for an initial capacitor adjustment to set the free-running frequency.

The regenerated oscillator signal at Terminal 8 is applied internally to the AFPC and ACC detectors through +45 and

-45-degree phase-shifter networks to establish the proper phase relationship for these detectors. The ACC detector, which also samples the burst during the keying interval, produces a correction voltage proportional to the burst amplitude. The correction voltage is compared to the quiescent bias level using sample-and-hold circuitry similar to that used in the AFPC portion of the circuit. The "compared" voltage is applied internally to the ACC amplifier and killer amplifier. Because the amplifier gains and killer threshold are determined by the ratios of the internal resistors, these functions are independent of external voltages or controls.

The attenuated chroma signal is fed to the second chroma amplifier, where the burst is removed by keyer action. The killer amplifier, the chroma gain control, and the overload detector control the action of the second chroma amplifier, whose gain is proportional to the dc voltage at Terminal 16. The overload detector (Terminal 13) receives a sample of the chroma output (Terminal 15) and detects the peak of the signal. The detected voltage is stored in an external capacitor connected to Terminal 16. This stored voltage on Terminal 16 affects the gain of the second chroma in the same manner as the chroma gain control.

Applications Information

General Considerations

The block diagram shown is typical of the type of circuit used in the practical application of the CA3126. Several items are critical for proper operation of the circuit.

1. A series resistor of approximately 2,450Ω (or high source impedance) must be used at the chroma input, Terminal 1. This high impedance minimizes pickup of unbalanced currents, particularly of the subcarrier oscillator signal.
2. When the overload detector is used, a large resistor (nominally 47,000Ω) must be placed in series with Terminal 16 to set the required RC time constant. The same RC network series serves to set the killer time constant.
3. The setting of the free-running oscillator frequency requires the presence of the keying pulse. The free-running frequency will be erroneous if Terminal 1 is dc shorted during the setting operation because of the dc offset voltage introduced to the AFPC detector.
4. Care must be taken in PC board designs to provide reasonable isolation between the oscillator portion of the circuit (Terminals 6, 7, and 8) and the chroma input (Terminal 1).

Overload Detector

The overload detector accomplishes two purposes:

1. It prevents oversaturation due to low burst-to-chroma ratios.
2. It prevents overload conditions due to noise.

Both of these conditions are discussed in more detail in ICAN-6247. The extent to which the overload detector is used depends upon the individual receiver design goals. If greater than 0.5V peak-to-peak output is desired, the chroma output at Terminal 15 can be tapped to yield any desired degree of overload detector action.

Chroma Gain Control

The chroma gain control operates by varying the base bias on current source transistor Q25. To ensure proper temperature tracking of the chroma gain control, it is essential that the control be operated from a supply source derived from the reference voltage at Terminal 12. Because the control operates from a current source, chroma gain is much more predictable and far less temperature sensitive than controls that steer current by means of a differential amplifier. The typical chroma gain characteristic for the CA3126 is shown in Figure 2.

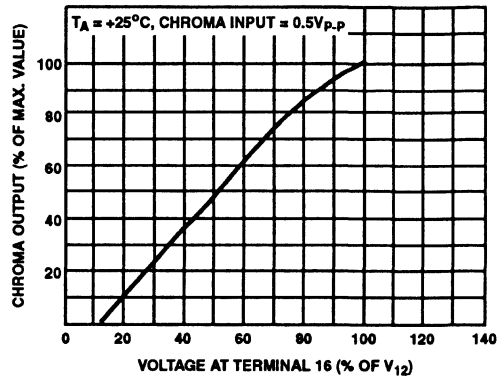


FIGURE 2. CHROMA GAIN CONTROL

Subcarrier Regenerator Oscillator

The oscillator filter consists of a 3.579545MHz crystal, a 680Ω resistor, and a 10pF capacitor connected in series across Terminals 6 and 7. A 33pF capacitor, shunt connected from Terminal 7 to ground, rolls off higher order harmonics, thereby preventing oscillation at the crystal third-harmonic frequency. A curve of the typical static phase error as a function of the free-running oscillator frequency is shown in Figure 3. It should be noted that the slope of the curve determines the dc gain of the phase-locked loop, i.e., 40Hz per degree.

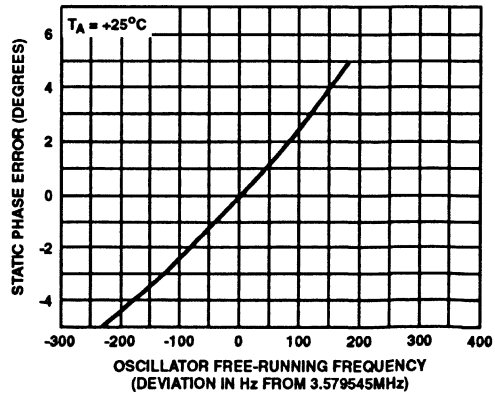


FIGURE 3. STATIC PHASE ERROR

Thermal Considerations

The circuit of the CA3126 is thermally compensated to achieve the optimal operating characteristics over the normal operating temperature range of TV receivers. Figures 4 and 5 show the oscillator and chroma-output amplitudes and phases as a function of temperature (Terminals 8 and 15), respectively.

Both the oscillator and chroma-output amplitudes and phases are measured relative to the chroma-input phase. The performance of the oscillator free-running frequency as a function of temperature is shown in Figure 6. All the temperature plots are characteristic of the test circuit with the indicated component types and values given in Figure 1.

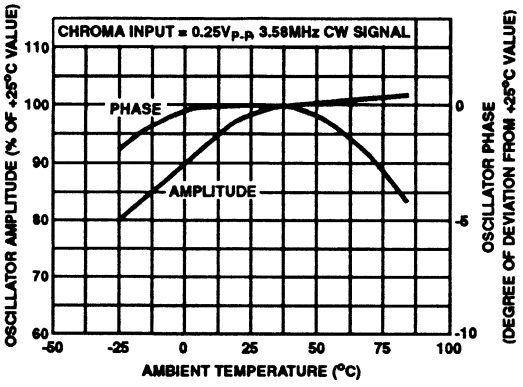


FIGURE 4. AMPLITUDE AND PHASE VARIATIONS OF OSCILLATOR OUTPUT vs TEMPERATURE

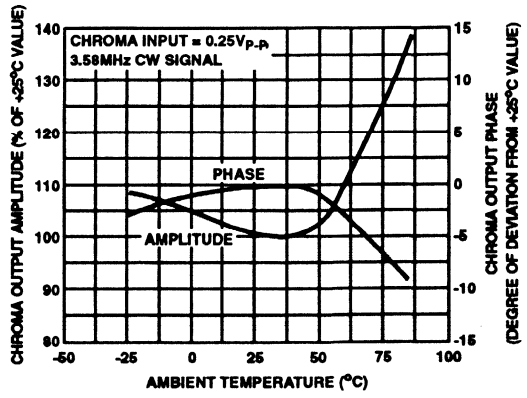


FIGURE 5. AMPLITUDE AND PHASE VARIATIONS OF CHROMA OUTPUT vs TEMPERATURE

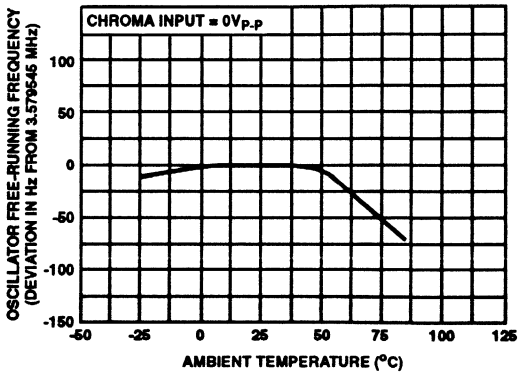
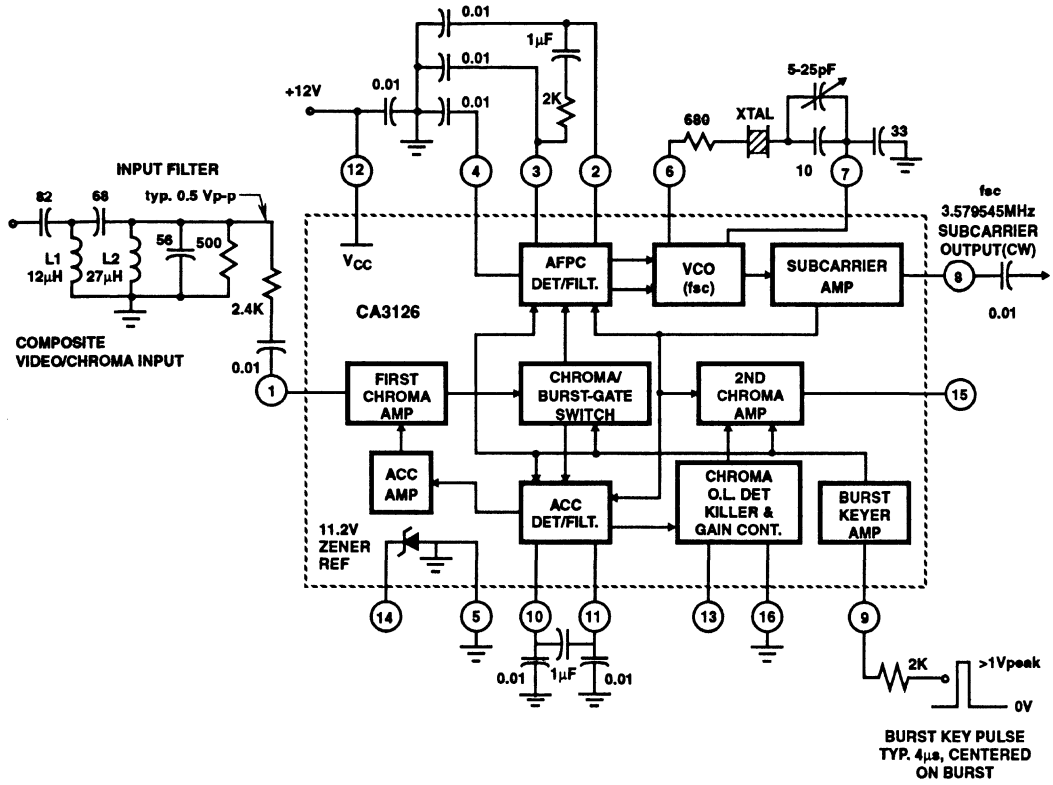


FIGURE 6. VARIATION OF OSCILLATOR FREE RUNNING FREQUENCY vs TEMPERATURE



NOTE: For Subcarrier Regenerator, the second chroma amp is not used; Pins 13,14 & 15 are not connected and pin 16 is grounded.

FIGURE 7. TYPICAL APPLICATION OF THE CA3126 AS A SUBCARRIER REGENERATOR

HARRIS SEMICONDUCTOR

CA3189

March 1993

FM IF System

Features

- Includes IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Tuning Meter, Deviation-Noise Muting, and ON Channel Detector
- FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers
- Exceptional Limiting Sensitivity -12μV (Typ.) at -3dB Point
- Low Distortion -0.1% (Typ.) (with Double-Tuned Coil)
- Single-Coil Tuning Capability
- Improved S + N/N Ratio
- Externally Programmable Recovered Audio Level
- Provides Specific Signal for Control of Interchannel Muting (Squelch)
- Provides Specific Signal for Direct Drive of a Tuning Meter
- On Channel Step for Search Control
- Provides Programmable AGC Voltage for RF Amplifier
- Provides a Specific Circuit for Flexible Audio Output
- Internal Supply Voltage Regulators
- Externally Programmable "On" Channel Step Width, and Deviation at Which Muting Occurs

Description

The Harris CA3189E* is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. The block diagram of the CA3189E includes a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as programmable delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power-supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5V to +16V.

The CA3189E is ideal for high-fidelity operation. Distortion in a CA3189E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil. The CA3189E has all the features of the CA3089E plus additions. See CA3189E features compared to the CA3089E in Table 1.

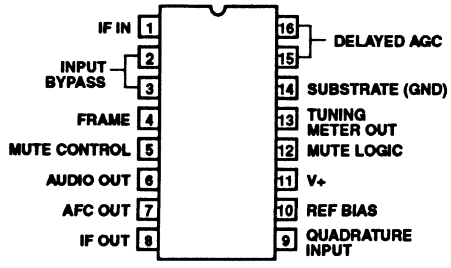
*Formerly Developmental Type No. TA10038.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3189E	-40°C to +85°C	16 Lead Plastic DIP

Pinout

CA3189
(PDIP)
TOP VIEW



7 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1046.2

Absolute Maximum Ratings T_A = +25°C

DC Supply Voltage
(Between Terminals 11 and 4) 16V
(Between Terminals 11 and 14) 16V
DC Current (Out of Terminal 15) 2mA
Power Dissipation:
Up to T_A = +85°C 640mW
Above T_A = +85°C..... Derate Linearly at 9.9mW/°C
Lead Temperature (Soldering 10 Sec.)..... +300°C

Operating Conditions

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C, V+ = 12V

PARAMETERS	SYMBOL	TEST CONDITIONS		CIRCUIT OR FIG. NO.	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
STATIC (DC) SPECIFICATIONS								
Quiescent Circuit Current	I_{11}	No Signal Input, Non Muted		1, 2	20	31	40	mA
DC Voltages		No Signal Input, Non Muted						
Terminal 1 (IF Input)	V_1			1, 2	1.2	1.9	2.4	V
Terminal 2 (AC Return to Input)	V_2			1, 2	1.2	1.9	2.4	V
Terminal 3 (DC Bias to Input)	V_3			1, 2	1.2	1.9	2.4	V
Terminal 15 (RF AGC)	V_{15}			1, 2	7.5	9.5	11	V
Terminal 10 (DC Reference)	V_{10}			1, 2	5	5.6	6	V
DYNAMIC SPECIFICATIONS								
Input Limiting Voltage (-3dB Point)	V_I(lim)		f_O = 10.7MHz, $f_{MOD.}$ = 400Hz, Deviation ±75kHz	1, 2	-	12	25	µV
AM Rejection (Terminal 6)	AMR	V_{IN} = 0.1V, AM Mod. = 30%		1, 2	45	55	-	dB
Recovered AF Voltage (Terminal 6)	V_O(AF)			1, 2	325	500	650	mV
Total Harmonic Distortion (Note 1)								
Single Tuned (Terminal 6)	THD	V_{IN} = 0.1V		1	-	0.5	1	%
Double Tuned (Terminal 6)	THD			2	-	0.1	-	%
Single Plus Noise to Noise Ratio (Terminal 6)	S + N/N	V_{IN} = 0.1V		1, 2	65	72	-	dB
Deviation Mute Frequency	$f_{DEV.}$		$f_{MOD.}$ = 0	1, 4, 5	-	±40	-	kHz
RF AGC Threshold	V_{16}			1, 2	-	1.25	-	V
On Channel Step	V_{12}	V_{IN} = 0.1V	$f_{DEV.}$ < ±40kHz	1	-	0	-	V
			$f_{DEV.}$ > ±40kHz	1	-	5.6	-	V

NOTE:

1. THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.

TABLE 1. CA3189E FEATURES COMPARED TO CA3089E

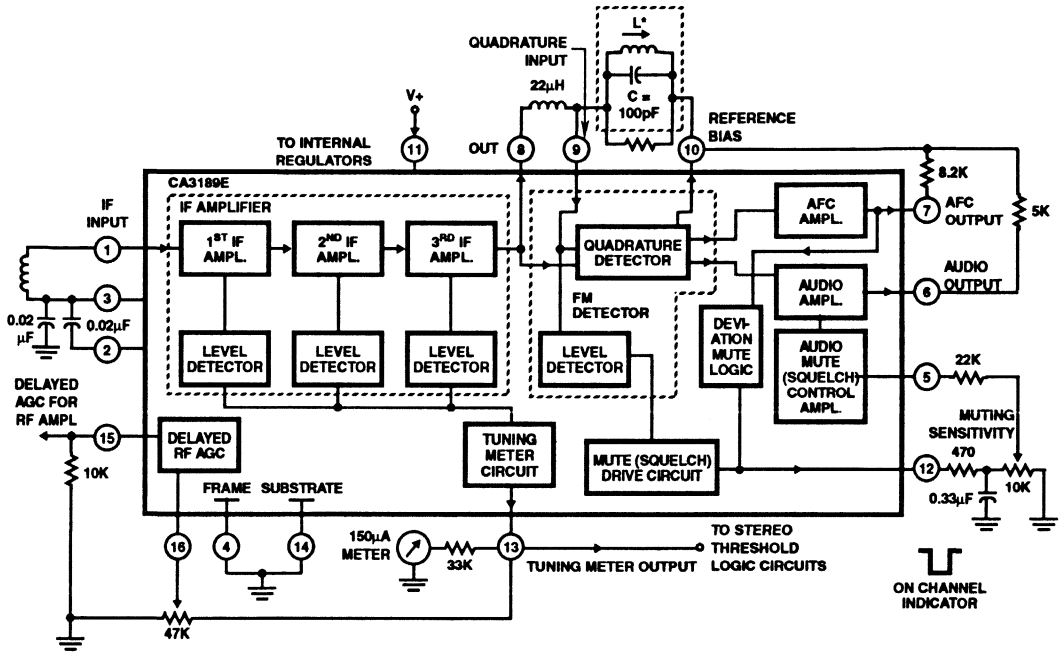
FEATURES	CA3189E	CA3089E
Low Limiting Sensitivity (12µV Typ.)	Yes	Yes
Low Distortion	Yes	Yes
Single-Coil Tuning Capability	Yes	Yes
Programmable Audio Level	Yes	No
S/N Mute	Yes	Yes
Deviation Mute	Yes	No

TABLE 1. CA3189E FEATURES COMPARED TO CA3089E (Continued)

FEATURES	CA3189E	CA3089E
Flexible AFC	Yes	Yes
Programmable AGC Threshold and Voltage	Yes	No
Typical S + N/N > 70 dB	Yes	No
Meter Drive Voltage Depressed at Very Low Signal Levels	Yes	No
On-Channel Step Control Voltage	Yes	No

Block Diagram

CA3189E



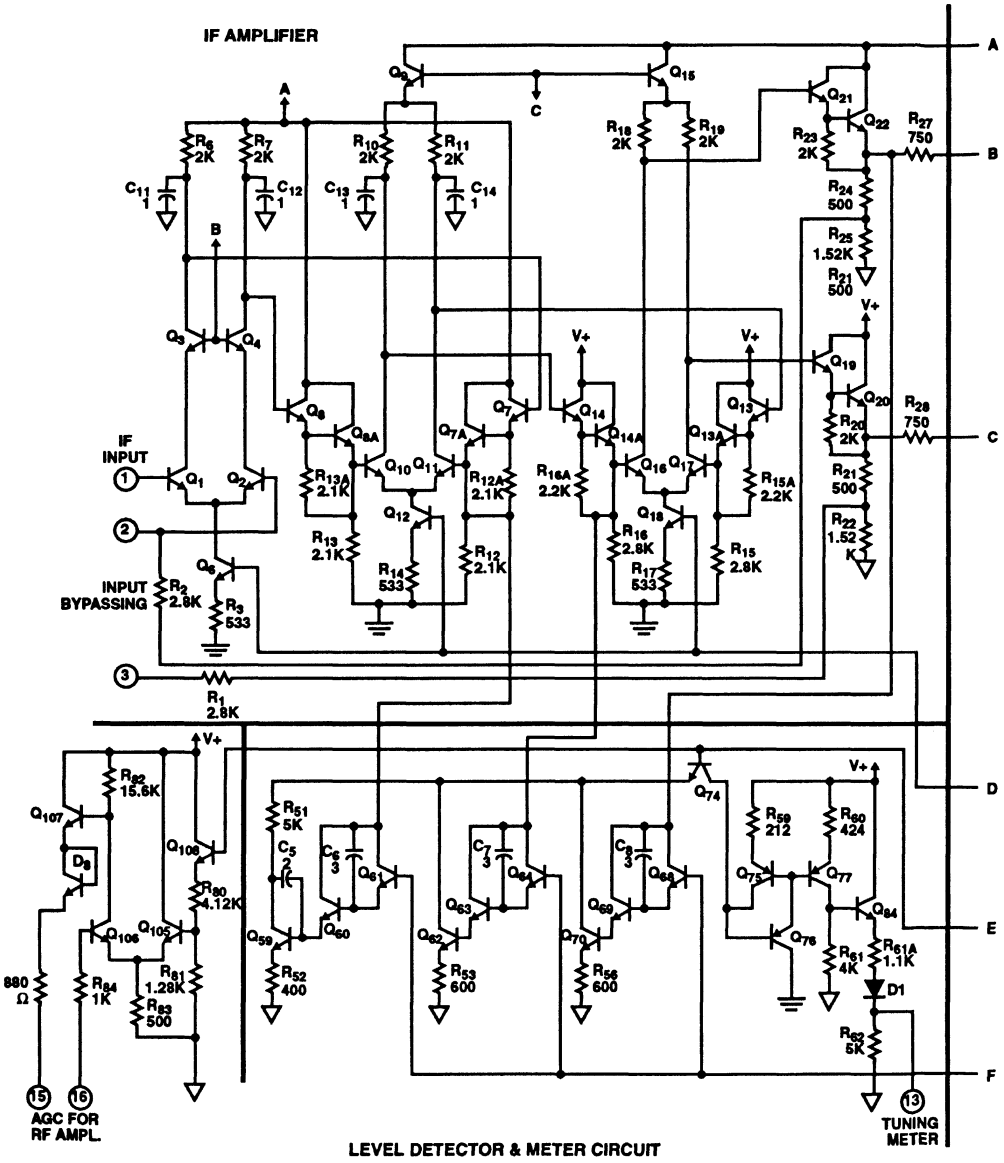
All resistance values are in Ω

*L Tunes with 100pF (C) at 10.7MHz

$Q_O \cong 75$ (TOKO No. KACS K586HM or equivalent)

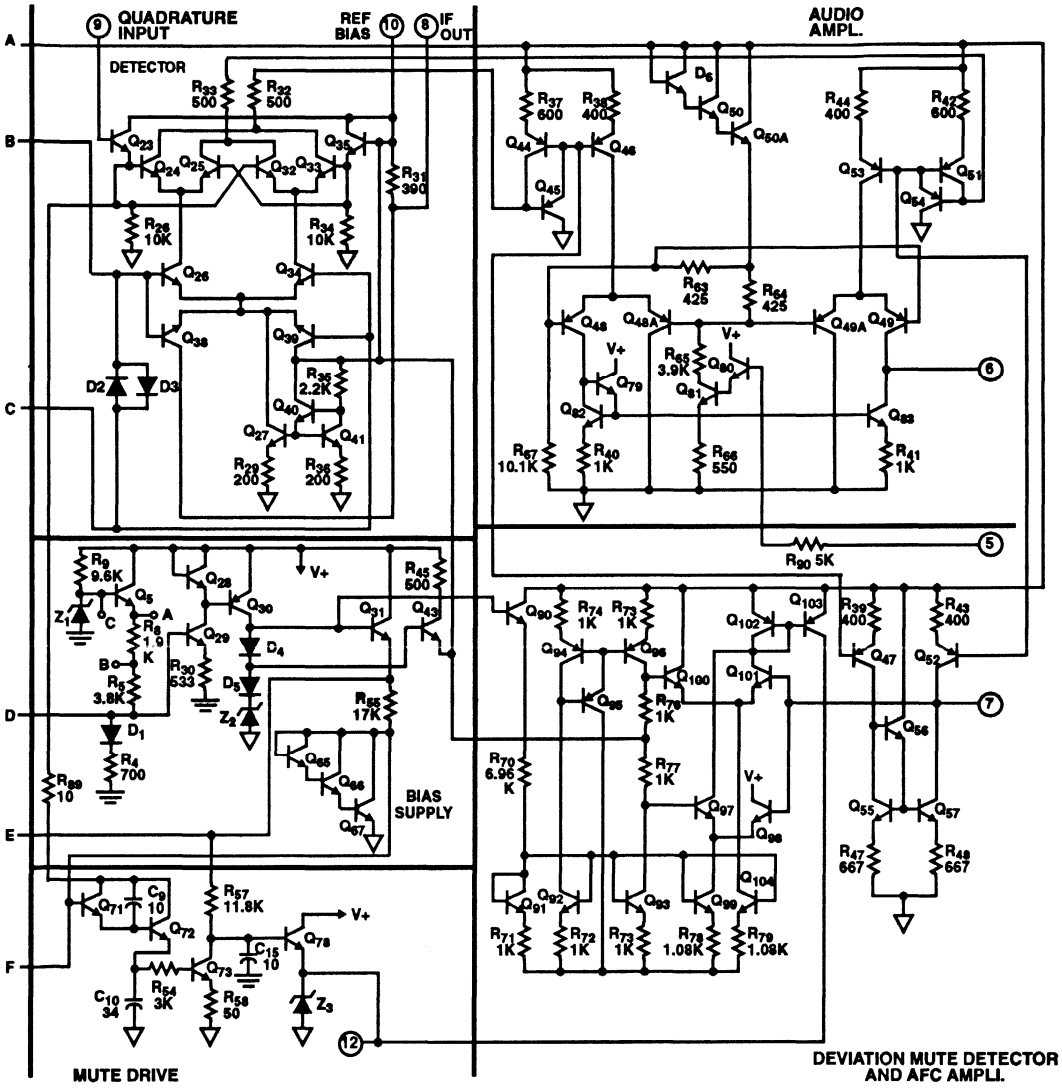
Schematic Diagram

CA3189E

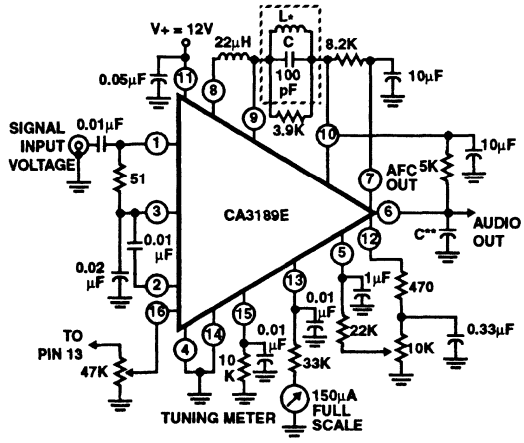


Schematic Diagram (Continued)

CA3189E

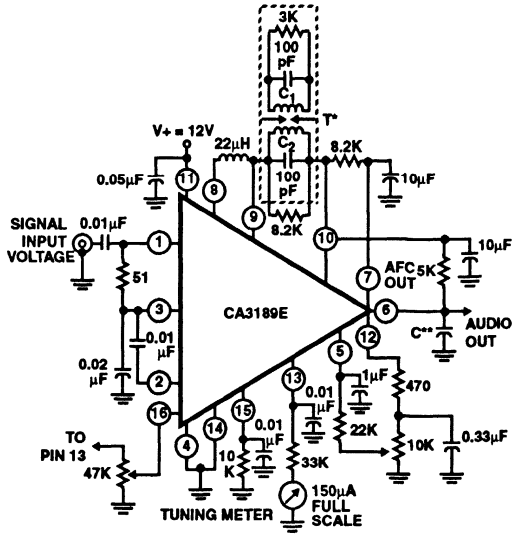


Test Circuits



All resistance values are in Ω
* L tunes with 100pF (C) at 10.7MHz
Q_0 (unloaded) ≅ 75 (TOKO No. KACS K586HM or equivalent)
** C = 0.01µF for 50µs deemphasis (Europe)
= 0.015µF for 75µs deemphasis (USA)

FIGURE 1. TEST CIRCUIT FOR CA3189E USING A SINGLE-TUNED DETECTOR COIL



All resistance values are in Ω
* T: PRI. - Q_0 (unloaded) ≅ 75 (tunes with 100pF (C_1) 20↑ of 34e on $^7/_{32}$" dia. form
SEC. - Q_0 (unloaded) ≅ 75 (tunes with 100pF (C_2) 20↑ of 34e on $^7/_{32}$" dia. form
kQ (percent of critical coupling) ≅ 70%
(Adjusted for coil voltage V_C) = 150mV
Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4mm.
** C = 0.01µF for 50µs deemphasis (Europe)
= 0.015µF for 75µs deemphasis (USA)

FIGURE 2. TEST CIRCUIT FOR CA3189E USING A DOUBLE-TUNED DETECTOR COIL

Typical Performance Curves

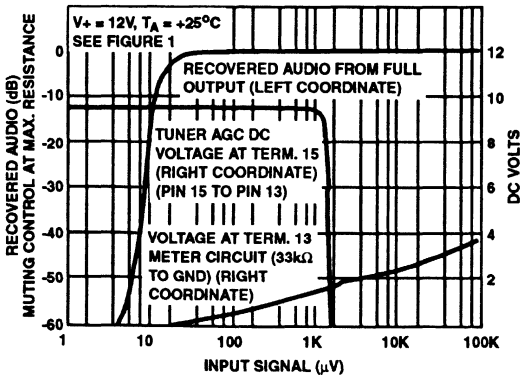


FIGURE 3. MUTING ACTION, TUNER AGC, AND TUNING METER OUTPUT AS A FUNCTION OF INPUT SIGNAL VOLTAGE

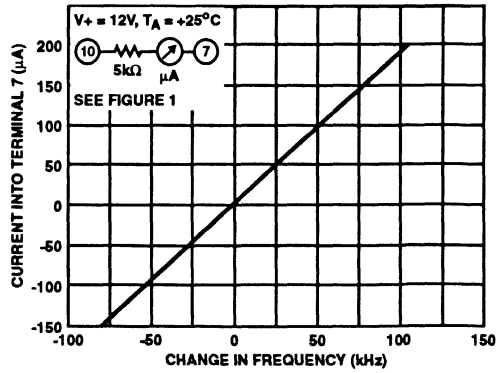


FIGURE 4. AFC CHARACTERISTICS (CURRENT AT TERMINAL 7 AS A FUNCTION OF CHANGE IN FREQUENCY)

Typical Performance Curves

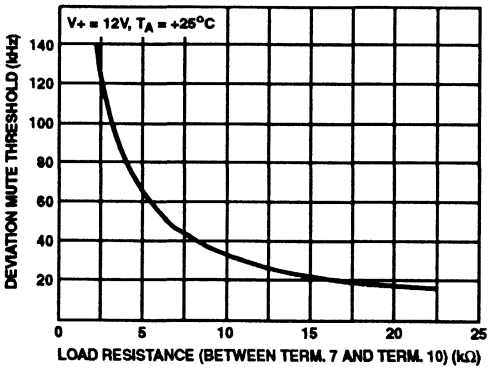


FIGURE 5. DEVIATION MUTE THRESHOLD AS A FUNCTION OF LOAD RESISTANCE (BETWEEN TERMINAL 7 AND TERMINAL 10)

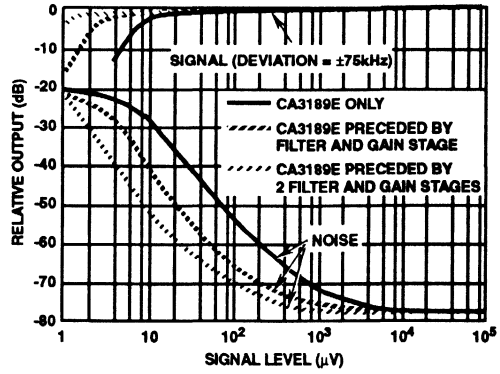


FIGURE 6. TYPICAL LIMITING AND NOISE CHARACTERISTICS

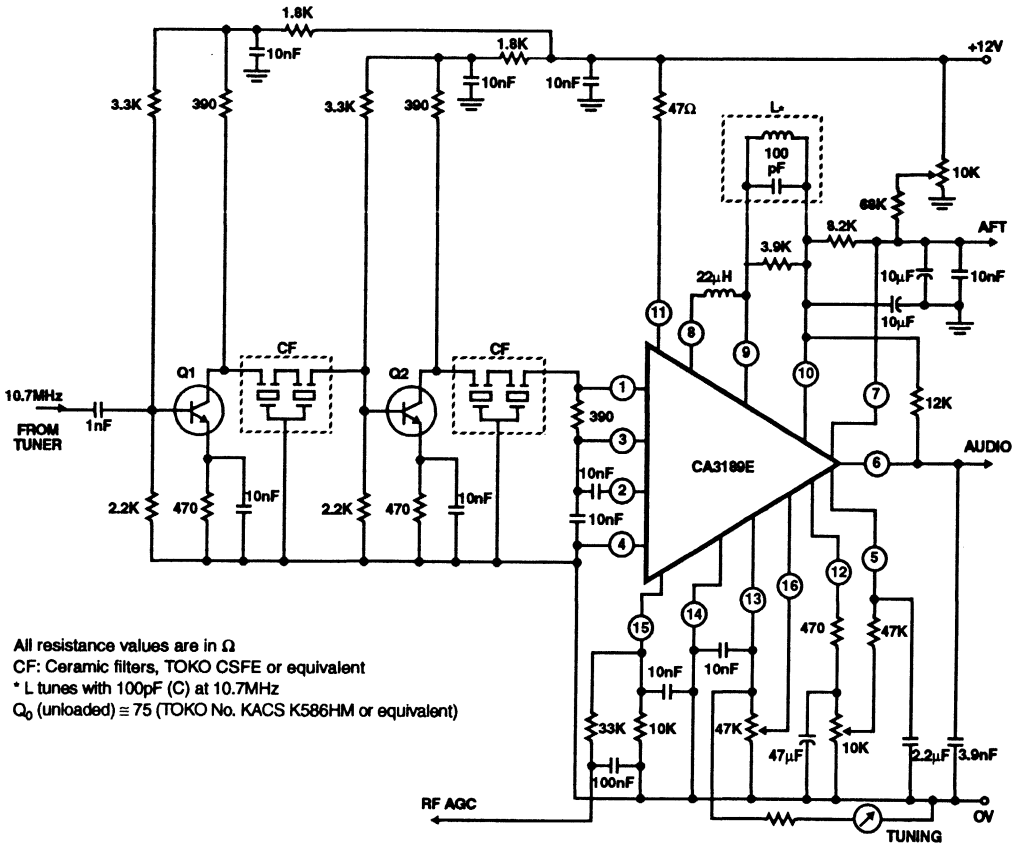


FIGURE 7. COMPLETE FM IF SYSTEM FOR HIGH QUALITY RECEIVERS

HARRIS SEMICONDUCTOR

CA3194

Single Chip PAL Luminance/Chroma Processor

March 1993

Features

- **All PAL Luminance and Chrominance Processing Circuitry on a Single Chip in a 24-Lead Plastic Package**
- **Phase-Locked Subcarrier Regeneration Utilizing Sample-and-Hold**
- **DC Controls for Brightness, Contrast, and Color Saturation Functions**
- **Input for Average Beam-Current Limiting**
- **Contrast Control Having Excellent Tracking of Luma and Chroma Channels**
- **Low-Impedance RGB Outputs with Excellent Tracking for Direct Coupling to Video Driver Circuitry**

Description

The Harris CA3194E* is a silicon monolithic integrated circuit designed to perform all of the signal processing functions for both the chroma and luminance signals of PAL color television receivers.

This circuit performs all the functions needed between the video detector and the video RGB output stages. DC contrast, brightness, and saturation controls and average beam limiting functions are included. The RGB buffer stages are capable of delivering 5mA of current into the video output stages.

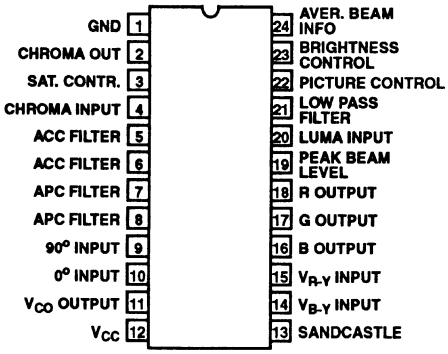
* Formerly Dev. No. TA10313.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3194E	-40°C to +85°C	24 Lead Plastic DIP

Pinout

CA3194
(PDIP)
TOP VIEW



TERMINAL VOLTAGE AND CURRENT RATINGS

TERMINAL	VOLTAGE* -V		CURRENT - mA	
	MIN	MAX	I_{IN}	I_{OUT}
1	-	-	-	-
2	0	13	0	30
3	0	8	10	-
4	0	5	-	-
5	0	Note	-	-
6	-	-	0.1	0.5
7	0	Note	-	-
8	0	Note	-	-
9	0	8	-	-
10	0	8	-	0.7
11	0	13	-	10
12	0	13	-	-
13	0	12	-	-
14	0	5	-	1.5
15	0	5	-	1.5
16	0	13	-	10
17	0	13	-	10
18	0	13	-	10
19	0	Note	-	-
20	0	5	-	-
21	0	Note	-	-
22	0	8	-	-
23	0	5	-	-
24	0	12	-	-

NOTE: The maximum should not exceed the V_{CC} voltage. Voltage with respect to Terminal 1 for V_{CC} (Terminal 12) of 12V ±10%.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1270.2**

Absolute Maximum Ratings

Supply Voltage and Current
- Pin 12 Voltage Range ..... 11V (Min) to 13V (Max)
- Pin 12 Current Range ..... 44mA (Typ) to 60mA (Max)

Power Dissipation
- Up to T_A = +25°C 825mW
- Above T_A = +25°C ..... Derate Linearly 8.7mW/°C

Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

Thermal Package Characteristics (°C/W)	θ_{JA}
Plastic DIP Package	115

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, V_{CC} = 12V, V_S = 2.85V, V_C = 2.85V, V_{AB} = V_{PB} = V_{CC}, V_B adjusted for V18 = 6.3V, C_X adjusted for F_{OSC} = 4.43361875MHz, Sandcastle: V_{BG} = 8.0V, V_{BLANK} = 3.5V - Burst Gate centered on Burst. These conditions exist except as otherwise noted. See Figure 19 for test circuit.

PARAMETERS	TEST CONDITIONS	TYPICAL VALUE	UNITS
LUMINANCE SECTION			
Input Impedance (Terminal 20)		6	kΩ
		5	pF
Luminance Channel Input Voltage	Luma Input Signal = 30% Sync.	0.5	V_{P-P}
Bandwidth of Luminance Channel	Luma Input Signal: 0.5V_{P-P} (30% Sync) modulated CW Adj. modulation frequency for -3dB at color outputs.	8	MHz
Brightness Control Range (Terminal 23)	For Control Characteristics, See Figures 1 and 2.	0 - 3.5	V_{DC}
Output Black Level Range	Luma Input Signal: 0.5V_{P-P} (30% Sync) V_B 0V - 5V,Measured at Pin 18 black level. See Figures 1 and 2.	5.9-9.7	V_{DC}
Offset		0.6 Max.	V_{DC}
Contrast Control Range (Terminal 22)	Luminance Input: 0.5V_{P-P} (30% Sync), for Control Characteristics. See Figure 3	0 - 5	V_{DC}
Luminance Gain Control Range	Luminance Input: 0.5V_{P-P} (30% Sync), V_C = 0.5V - 5V measure Pin 18 black level to maximum white level. See Figure 4.	32	dB
RGB Output Swing	Luminance Input: 0.5V_{P-P} (30% Sync), V_C = 5V, read black level to peak white. See Figures 5 and 6.	4	V_{P-P}
CHROMINANCE SECTION			
Input Impedance (Terminal 4)	See Figures 7 and 8.	4.5	kΩ
		5	pF
Chroma Channel Input Voltage	Chroma	220	mV_{P-P}
	Burst	100	mV_{P-P}
ACC Range		+6 - (-20)	dB
Input Burst Level for Kill (Note 1)	Adjust chroma input Pin 4 until Pin 2 ≤ 25mV_{P-P}. Measure Burst level at Pin 4	10	mV_{P-P}
Contrast Control Chroma/Luma Tracking	Chroma Input: Burst = 100mV_{P-P}, Chroma = 220mV_{P-P}. Luminance Input: 0.35V_{P-P}, V_S adjusted for Chroma at Pin 18 = 2V_{P-P}. V_C is adjusted for luminance at Pin 18 = 2V_{P-P}, V_C is again adjusted for luminance of +6 and -9dB. Then read chroma percentage difference. See Figure 9	±5	%
Saturation Control Range (Terminal 3)	For control characteristic, see Figure 10.	0 - 5	V_{DC}

Electrical Specifications T_A = +25°C, V_{CC} = 12V, V_S = 2.85V, V_C = 2.85V, V_{AB} = V_{PB} = V_{CC}, V_B adjusted for V18 = 6.3V, C_X adjusted for F_{OSC} = 4.43361875MHz, Sandcastle: V_{BG} = 8.0V, V_{BLANK} = 3.5V - Burst Gate centered on Burst. These conditions exist except as otherwise noted. See Figure 19 for test circuit. **(Continued)**

PARAMETERS	TEST CONDITIONS	TYPICAL VALUE	UNITS
Saturation Control Range (Terminal 3)	For control characteristic, see Figure 10.	0 - 5	V_{DC}
Maximum Chroma Output Voltage (Terminal 2)	Chroma Input: Burst = 100mV_{P-P}, Chroma = 220mV_{P-P}. Adjust V_C and V_S for maximum Pin 2 output.	2.5	V_{P-P}
OSCILLATOR SECTION			
Pull-In Range	Chroma Input: Burst = 100mV_{P-P}, Chroma = 220mV_{P-P}. Adjust C_X for HI/LO f_{OSC} without Chroma signal. Apply signal to lock.	±500	Hz
Static Phase Error		2	Deg./ 100Hz
DEMODULATOR SECTION			
R-Y Demodulator Conversion Gain	Chroma Input: Burst =100mV, Chroma = 220mV_{P-P},VØ. Adjust V_C for V18 = 1V. Read V15. Calculate V18/V15.	10	Ratio
B-Y Demodulator Conversion Gain	Chroma Input: Burst = 100mV_{P-P}, UØ. Read V16 and V14. Calculate V16/V14. V_C remains as for R-Y gain.	18	Ratio
G-Y/B-Y Matrix Ratio	Chroma Input: Burst =100mV_{P-P}, Chroma = 220mV_{P-P}, UØ read V17 and V16, Calculate V17/V16. V_C remains as above.	0.2	Ratio
G-Y/R-Y Matrix Ratio	Chroma Input: Burst =100mV_{P-P}, Chroma = 220mV_{P-P}, VØ. Read V17 and V18. Calculate V17/V18. V_C remains as above.	0.5	Ratio
Sub-Carrier and Harmonic Content at Outputs	No Chroma or Luma Input. Read residual carrier at outputs.	30	mV_{P-P}
SANDCASTLE PULSE			
Horizontal and Vertical Blanking Pedestal		2 - 5	V
Burst Gate Pulse		6.5 - V_{CC}	V

NOTES:

1. If a different value is desired, see the Threshold Adjustment Circuit of Figure 17.
2. Use of the circuit of Figure 18 is suggested to prevent increased color saturation at low level RF signals.
3. The reference voltage can be adjusted by changing the values of the voltage divider.

Circuit Description (See Block Diagram and Figure 20)

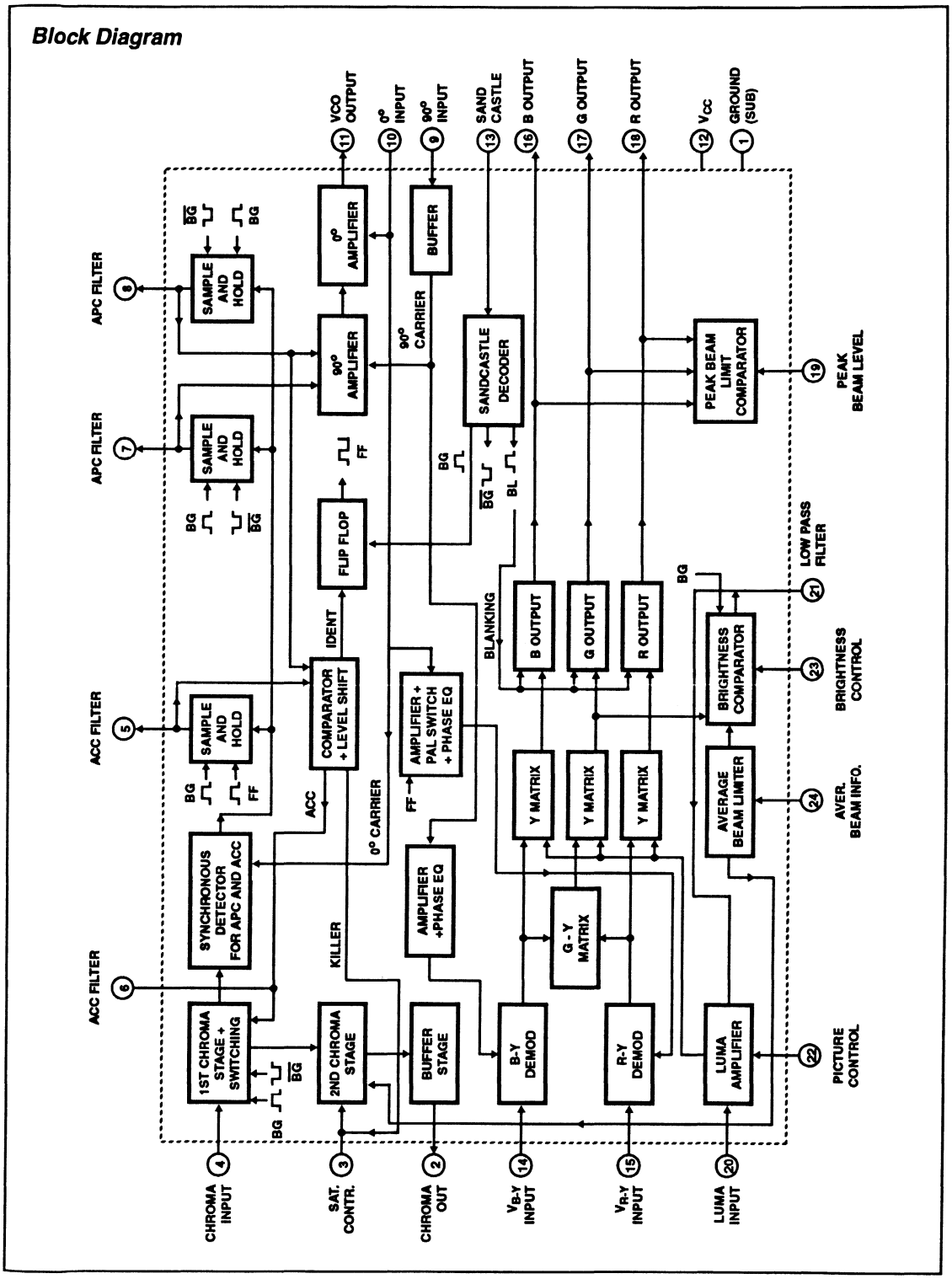
The chroma signal is externally separated from the video signal by means of a bandpass or high-pass filter and applied to pin 4. The burst is separated in the first chroma stage and applied to the synchronous detector which provides information to sample-and-hold circuits for APC (phase-locked loop), ACC (automatic chroma gain control) and identification and killing. The 4.43-MHz crystal oscillator is phase-locked to the burst and provides 0° and 90° (via an external phase shifter) carriers to the chroma demodulators. The burst and chroma amplitude at the output of the first chroma amplifier is kept constant by the automatic gain control.

The second chroma stage provides saturation control (pin 3) which tracks the contrast control in the luminance channel. This stage is also used for color killing.

A buffer stage drives the external PAL delay line. The separated U and V signals are applied to pins 14 and 15, respectively, and demodulated. A standard G-Y matrix is included on the chip.

The luminance signal passes through the subcarrier trap and through the luminance delay line and enters the chip at pin 20. Contrast and brightness control is provided before the luminance signal is combined with the color difference signals in the Y matrix. Average and peak beam limiting circuits are controlled from pins 24 and 19.

Block Diagram



Typical Performance Curves

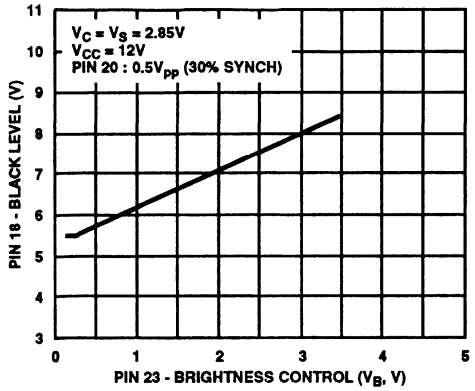


FIGURE 1. BRIGHTNESS CONTROL (V_B) MEASURED AT PIN 18 OUTPUT TERMINAL

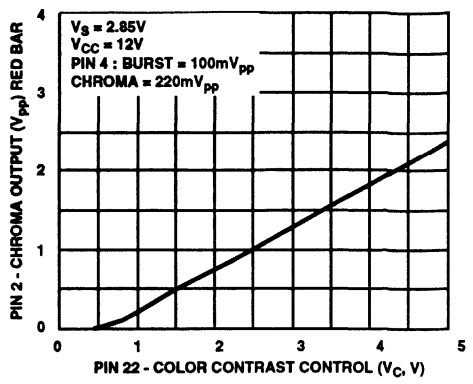


FIGURE 2. CONTRAST CONTROL (V_C) MEASURED AT 2ND CHROMA AMPLIFIER OUTPUT TERMINAL

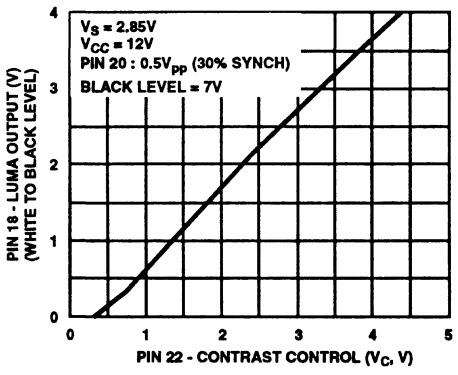


FIGURE 3. CONTRAST CONTROL (V_C) MEASURED AT PIN 18 OUTPUT TERMINAL

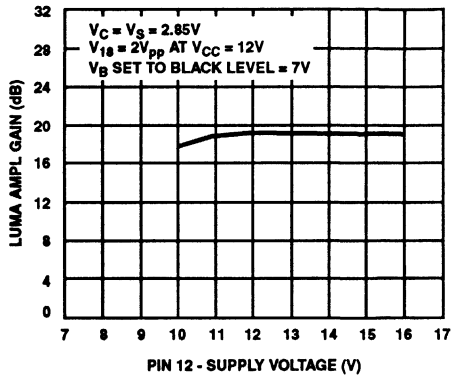


FIGURE 4. LUMA GAIN vs SUPPLY VOLTAGE (V_{CC}) MEASURED AT LUMA AMPLIFIER OUTPUT TERMINAL

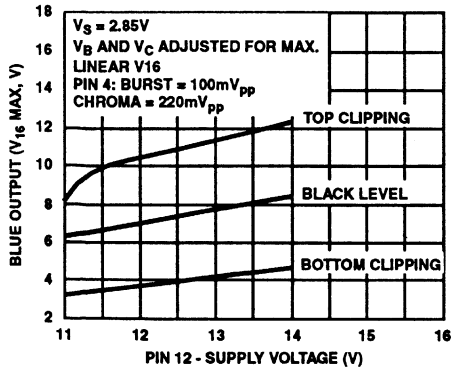


FIGURE 5. LINEAR OPERATING RANGE AS A FUNCTION OF V_{CC} MEASURED AT PIN 16 OUTPUT TERMINAL (BEST OPERATING RANGE IS 11-13V V_{CC})

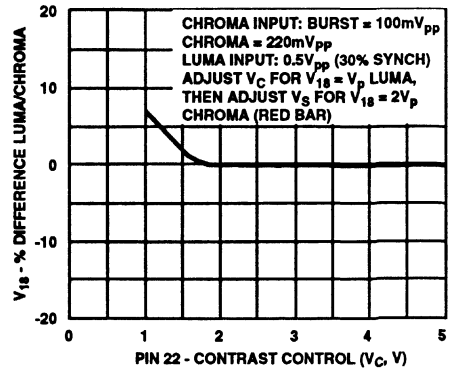


FIGURE 6. LUMA/CHROMA TRACKING AS A FUNCTION OF V_C MEASURED AT PIN 18 OUTPUT TERMINAL

Typical Performance Curves (Continued)

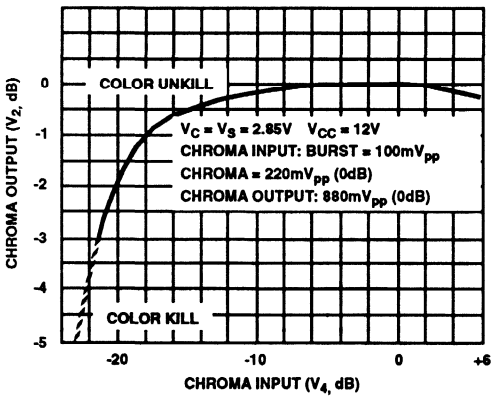


FIGURE 7. ACC CHARACTERISTICS MEASURED AT PIN 2 OUTPUT TERMINAL

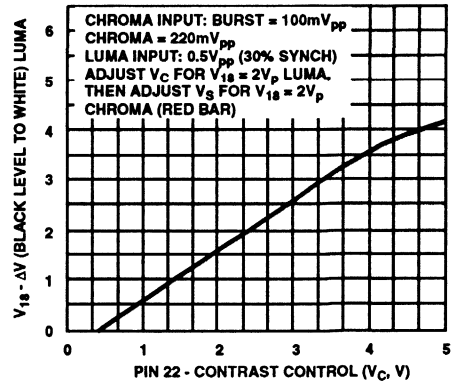


FIGURE 8. LUMA/CHROMA TRACKING vs CONTRAST CONTROL MEASURED AT PIN 18 OUTPUT TERMINAL

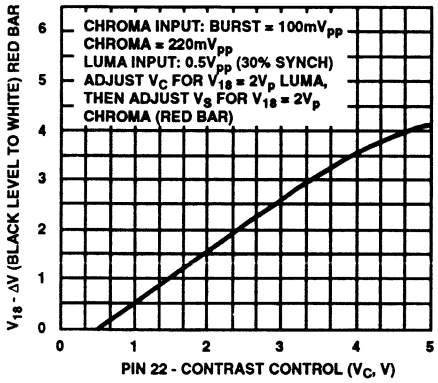


FIGURE 9. LUMA/CHROMA TRACKING WITH CONTRAST CONTROL MEASURED AT PIN 18 OUTPUT TERMINAL

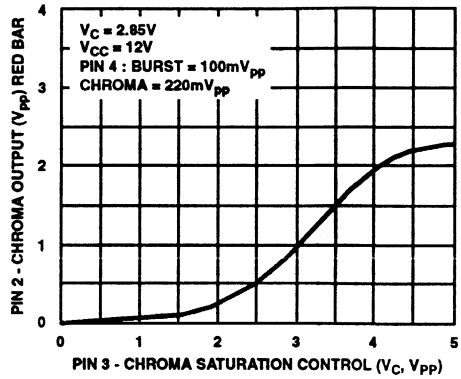


FIGURE 10. SATURATION CONTROL (V_S) MEASURED AT CHROMA AMPLIFIER OUTPUT TERMINAL PIN 2

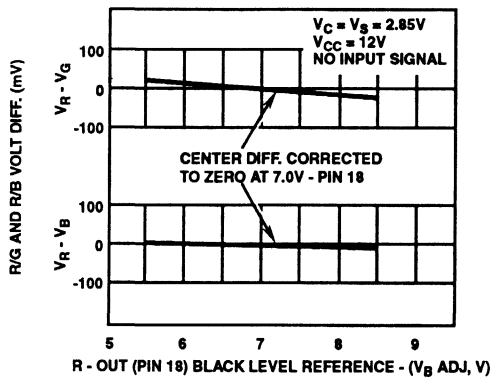


FIGURE 11. DIFFERENTIAL BLACK-LEVEL TRACKING MEASURED AT RGB OUTPUT TERMINALS

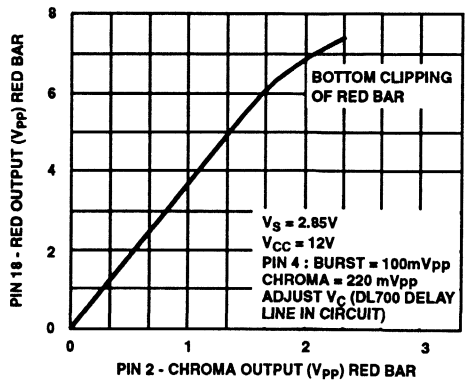


FIGURE 12. PIN 18 OUTPUT vs PIN 2 VOLTAGE MEASURED AT CHROMA OUTPUT TERMINALS AND R OUTPUT

Typical Performance Curves (Continued)

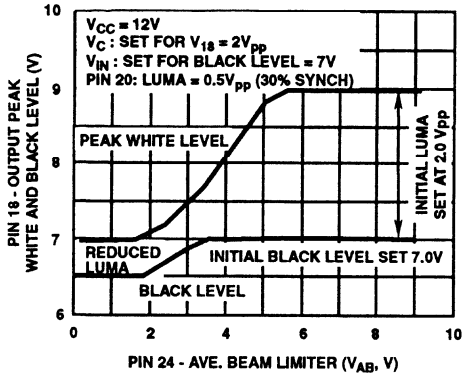


FIGURE 13. AVERAGE BEAM LIMITER (V_{AB}) MEASURED AT PIN 18 OUTPUT

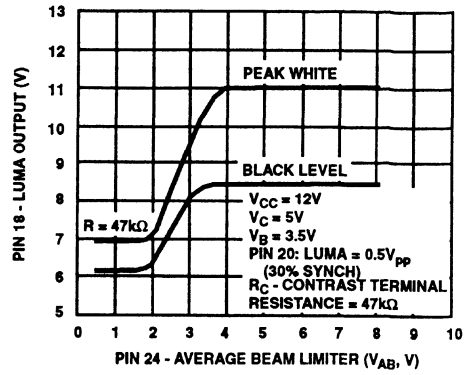


FIGURE 14. AVERAGE BEAM LIMITER (V_{AB}) MEASURED AT PIN 18 OUTPUT

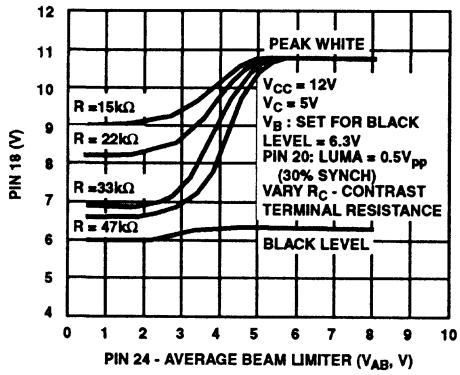


FIGURE 15. AVERAGE BEAM LIMITER (V_{AB}) MEASURED AT PIN 18 OUTPUT

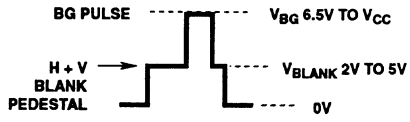


FIGURE 16. SANDCASTLE INPUT WAVEFORM

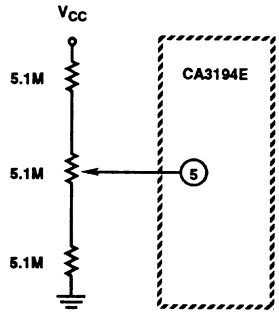


FIGURE 17. KILLER-THRESHOLD LEVEL CONTROL

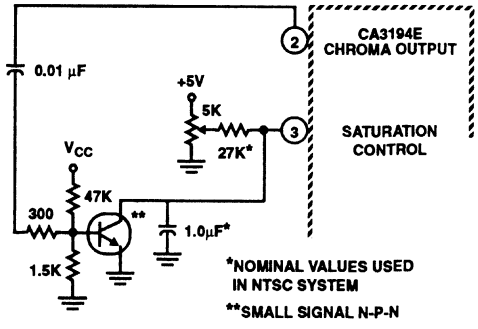
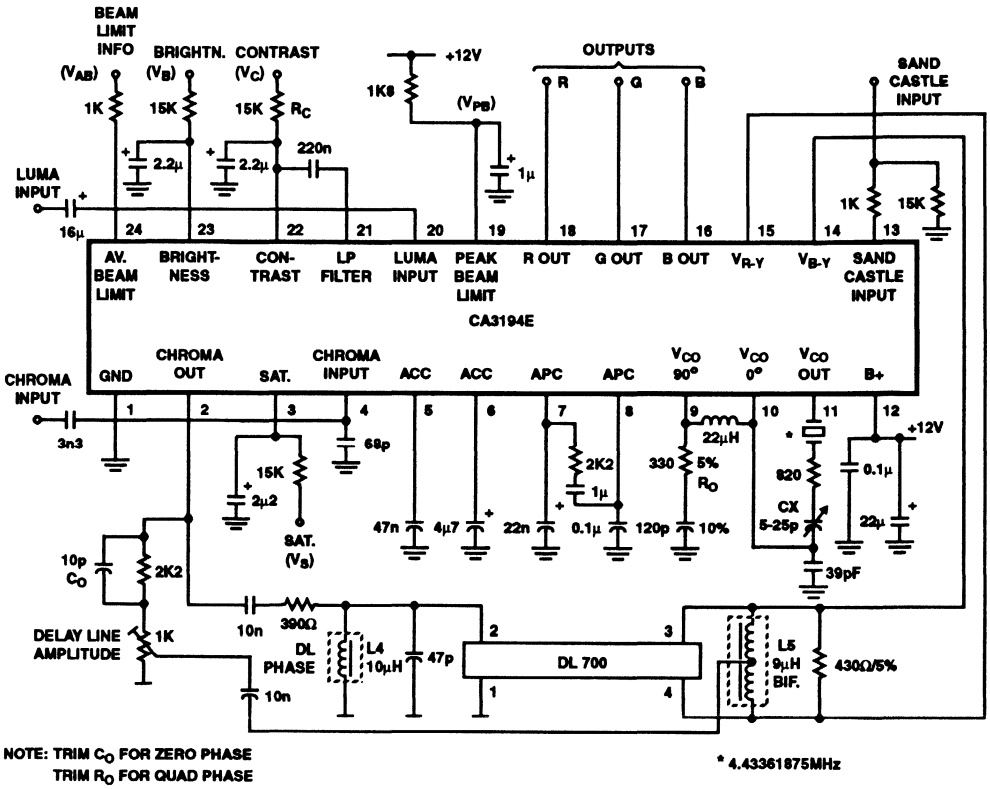


FIGURE 18. EXTERNAL OVERLOAD DETECTOR

Test Circuit



NOTE: TRIM C_O FOR ZERO PHASE
TRIM R_O FOR QUAD PHASE

* 4.43361875MHz

FIGURE 19. TEST CIRCUIT

Test Circuit (Continued)

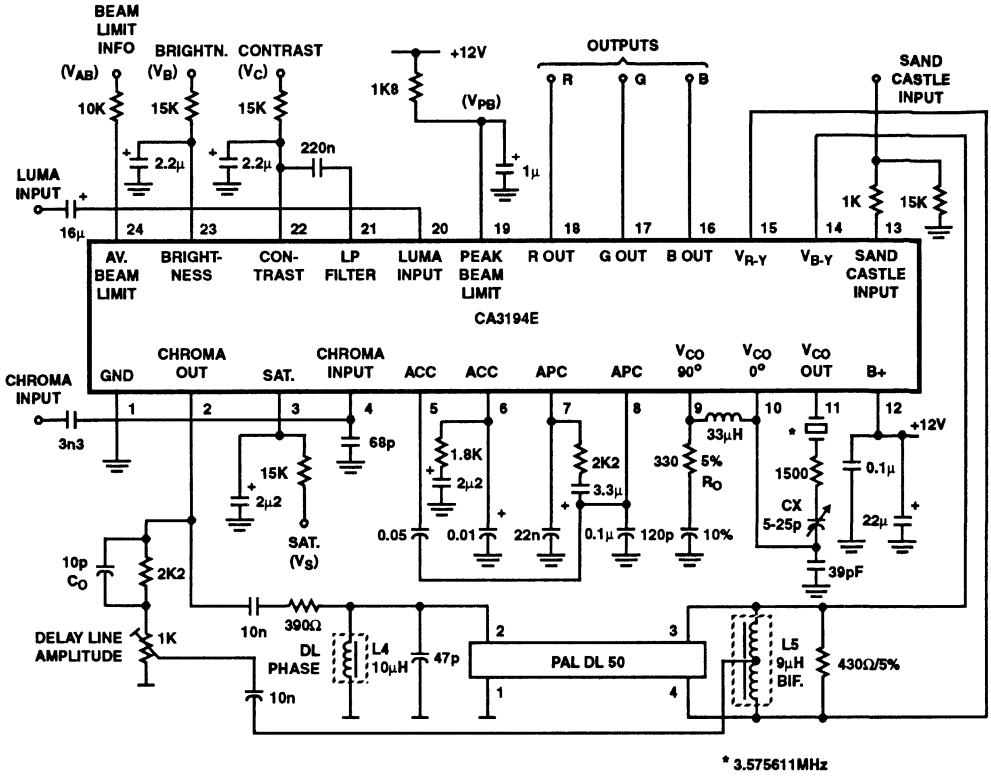


FIGURE 20. APPLICATION CIRCUIT FOR PAL M

HARRIS SEMICONDUCTOR

CA3217

Single Chip TV Chroma/Luminance Processor

March 1993

Features

- All Chroma Processing and Demodulating Circuitry on a Single Chip in a 28 Lead Plastic Package
- Phase Locked Subcarrier Regeneration Utilizing Sample and Hold Techniques
- Supplementary ACC with Overload Detector to Prevent Over Saturation of the Picture Tube
- Linear DC Controls for Chroma Gain and Tint
- Dynamic "Flesh Correction" - Corrects Purple and Green Flesh Colors without Affecting Primary Colors
- Balanced Chroma Demodulators with Low Output Impedance for Direct Coupling
- Internal RF Filtering
- Requires Few External Components
- Automatic Beam Limiter
- Chroma Luminance Tracking Picture Control

Description

The Harris CA3217E* is a monolithic silicon integrated circuit. It contains all the required circuit functions between the video detector and the picture tube RGB driver stages of a color television receiver. The CA3217E decodes the chrominance signals and then produces three different color signals that are internally combined with the luminance to develop the RGB signals. The picture saturation, hue and brightness DC controls are externally adjustable by the viewers. The AFPC, ACC, Dynamic flesh control, Beam limiting and Gate black level (Brightness) control are servo loops used to stabilize the RGB output and reduce frequent manual adjustment. The automatic beam limiter circuit reduces picture contrast and brightness to prevent excessive drive output at the picture tube.

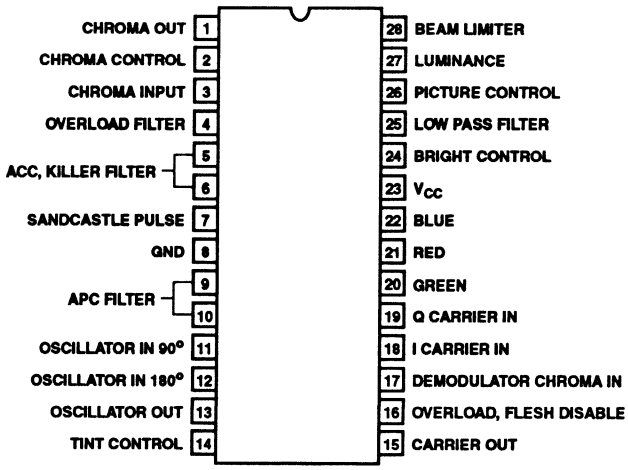
* Formerly dev. type no. TA10806.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3217E	-40°C to +85°C	28 Lead Plastic DIP

Pinout

CA3217
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1332.2

Absolute Maximum Ratings

DC Voltage (Between Terms 23 & 8) 14.0V
Power Dissipation
Up to T_A = +55°C 1.27W
Above T_A = +55°C..... Derate Linearly at 13.3mW/°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.)..... +300°C

Operating Conditions

Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C

PARAMETERS	TEST CONDITIONS										LIMITS			UNITS
	TEST	S2	S3	S4	S5	S6	mV_{P-P} CHROMA	mV_{P-P} BURST IN	mV_{P-P} LUMA	RELAYS ENERGIZED	MIN	TYP	MAX	
DC ELECTRICAL SPECIFICATIONS (Test 1-5)														
Dissipation	Pin 23	6.3V	11.2V	4.0V	6.3V	11.2V					30	48	66	mA
Pin 1 Bal	XPT1	1.2V	11.2V	4.0V	6.3V	11.2V						10.5		V DC
Pin 3 Bal	XPT1	1.2V	11.2V	4.0V	6.3V	11.2V						2.2		V DC
Pin 17 Bal	XPT9	1.2V	11.2V	4.0V	6.3V	11.2V						3.0		V DC
Pin 13 Bal	XPT 13	1.2V	11.2V	4.0V	6.3V	11.2V						7.5		V DC
SWITCHING ELECTRICAL SPECIFICATIONS (Tests 6-26)														
Oscillator Pull-In (Note 1)	"D"	6.3V	11.2V	4.0V	6.3V	11.2V	25	25		K4, K7	-350		+350	Hz
Oscillator Level	"D"	6.3V	11.2V	4.0V	6.3V	11.2V	0	0		K7		0.7		V_{P-P}
100% ACC (Note 2)	P21	Vary	11.2V	4.0V	6.3V	11.2V	125	125		K4, K7		1.5		V_{P-P}
200% ACC (Note 3)	P21	T8	11.2V	4.0V	6.3V	11.2V	250	250		K4, K7		100		%
20% ACC (Note 3)	P21	T8	11.2V	4.0V	6.3V	11.2V	25	25		K4, K7		90		%
Tint Center (Note 4)	S5	Vary	11.2V	4.0V	Vary	11.2V	250	125		K4, K7		6.5		V DC
R-Y Maximum	P21	11.2V	11.2V	6.0V	T11	11.2V	250	125		K1, K4, K7		6.0		V_{P-P}
Unkill	P21	11.2V	11.2V	4.0V	T11	11.2V	25	12.5		K4, K7		4.5		V_{P-P}
Kill	P21	11.2V	11.2V	4.0V	T11	11.2V	25	2.5		K4, K7			150	mV_{P-P}
Chroma Reserver	P21	11.2V	11.2V	4.0V	T11	11.2V	12.5	125		K2, K4, K7		2.0		V_{P-P}
Maximum Luma (Note 5)	P21	11.2V	11.2V	4.0V	T11	11.2V			125	K1, K3, K7		2.2		V_{P-P}
Luma Ratio (Note 6)	P21	11.2V	6.3V	4.0V	T11	11.2V			125	K1, K3, K7		50		%
Linearity (Note 7)	P21	11.2V	Vary	3.0	T11	11.2V			425	K3, K7		4		V_{P-P}
T19 = T19/T18	P21	11.2V	T18	3.0	T11	11.2V			212.5	K3, K7		50		%
4.78MHz Response (Note 8)	P21	11.2V	11.2V	4.0V	T11	11.2V			125	K3, K6, K7	-3		3	dB
Contrast Limit 1 (Note 9)	P24	11.2V	11.2V	4.0V	T11	11.2V			250	K3, K5, K7		3.9		V DC
Contrast Limit 2 (Note 9)	P26	11.2V	11.2V	4.0V	T11	11.2V			250	K3, K5, K7		8.2		V DC
Bright Limit 1 (Note 10)	P24	11.2V	11.2V	4.0V	T11	11.2V			250	K3, K5, K7		3.1		V DC
Bright Limit 2 (Note 10)	P26	11.2V	11.2V	4.0V	T11	11.2V			250	K3, K5, K7		5.6		V DC
G-Y Ratio (Note 11)	P20	Vary T25	11.2V	4.0V	T11	11.2V	250	125				0.33		R
B-Y Ratio (Note 11)	P22		11.2V	4.0V	T11	11.2V	250	125				1.20		R

NOTES:

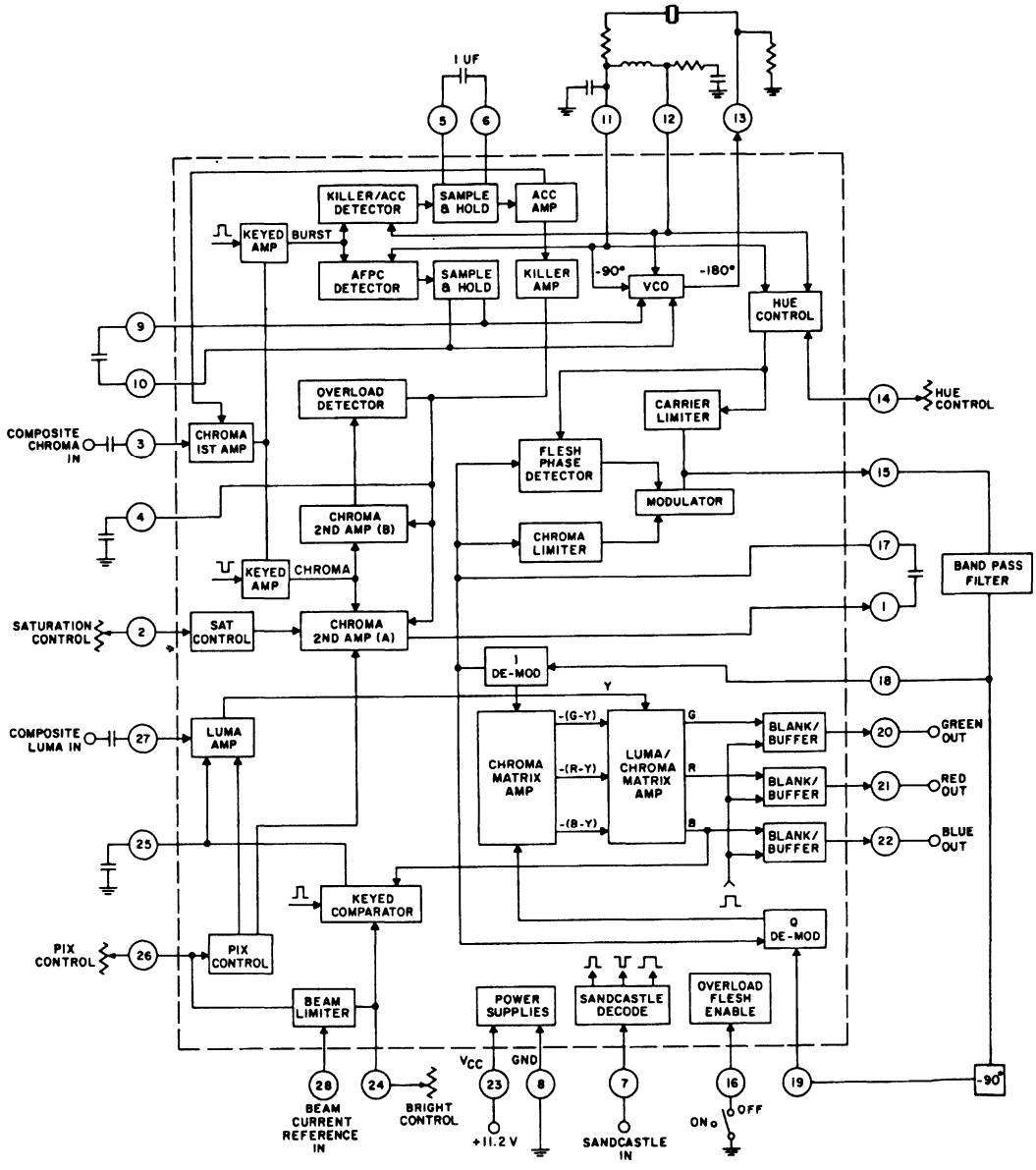
1. With K7 energized and frequency counter at D vary C1 for 3.579175MHz. Then with K4 energized, check for pull-in. Repeat for frequency tuned to 3.579875MHz. For all other tests tune to 3.579545MHz ±10Hz.
2. Vary S2 for $1.5V_{P-P}$ at Pin 21.
3. % of 100% ACC.
4. Adjust C1 for 3.579545MHz ±10Hz. Adjust S2 for $1.6V_{P-P}$ at Pin 22 and 0 reference, then adjust S5 for minimum at P21. Read and record S5 voltage.
5. Black to White.
6. T17 = T17/T16.
7. Adjust S3 for $4.0V_{P-P}$.
8. AC amplitude = $50mV_{P-P}$ reference 15kHz.
9. Adjust beam limiter to 10.7V.
10. Adjust beam limiter to 9.8V.
11. Adjust S2 for $1.5V_{P-P}$ at Pin 21, then calculate P20/P21 and P22/P21.

Typical Performance of the CA3217E

FUNCTION	TYPICAL DATA	
Nominal Supply	11.2V	
Nominal Dissipation	500mW	
Oscillator Stability		
Supply Variation 10^{-14}V	5Hz	
Variation With Temperature (ΔT = +50°C)	25Hz	
AFPC Characteristics		
DC Loop Gain	33Hz/Degree	
Pull In Range	±500Hz	
ACC Characteristics		
100% Chroma Input Level	250mV_{p-p} on Red Bar	
3dB Point	At 20% Nominal Input Level	
Hue Control Range	100°	
Saturation Control Range	40dB Min.	
DEMODULATOR PARAMETERS	**RELATIVE AMPLITUDE**	**ANGLE**
R - Y	1.0	93°
B - Y	1.2	2°
G - Y	0.3	258°
Bandwidth (Chroma)	900kHz	
Flesh Control	Primary Control in the +1 Half Plane	
Chroma Overload Control	Two Levels	
Picture Control	40dB	
Brightness Control	Black Level Clamped on 3V to 5V Level	
Beam Limiting	On Picture and Brightness Controls	
Luma Bandwidth	5MHz Min.	
Sandcastle Input		
1.2 - 2.3V	Blanking	
>3.3V	Burst Gate	
Maximum Linear Output		
R	5V	
G	3V	
B	3.7V	

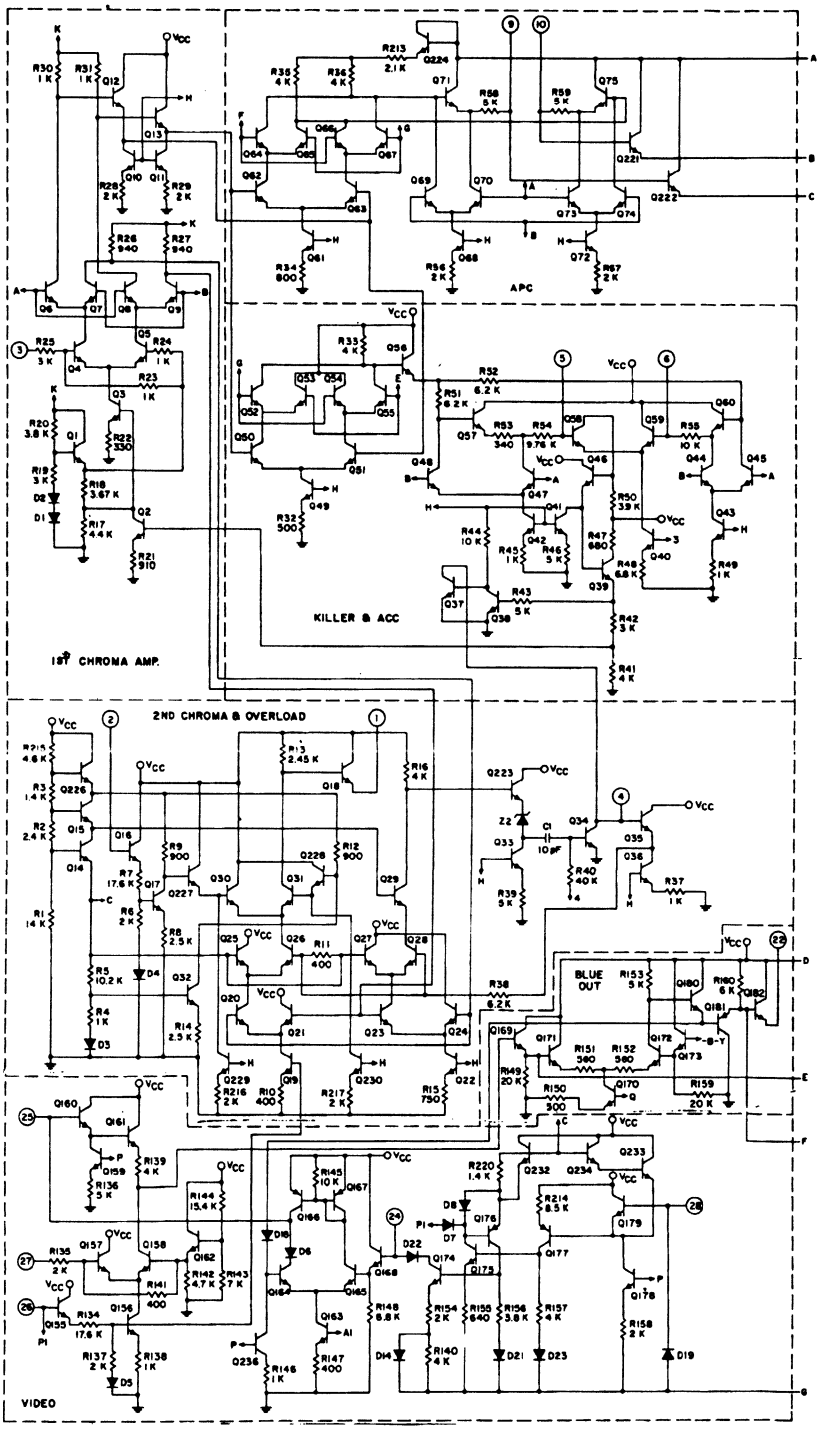
Functional Block Diagram

CA3217E



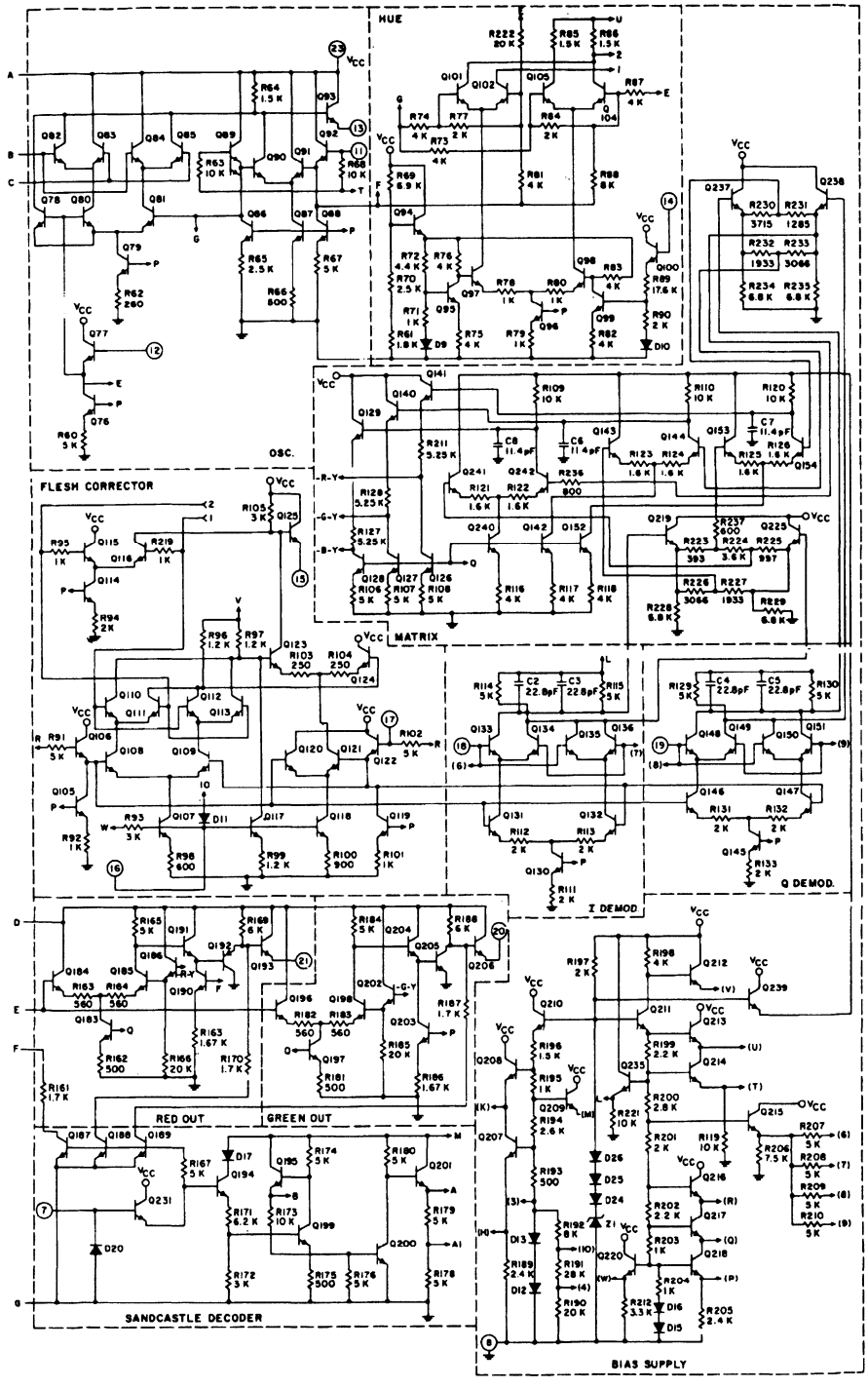
Schematic Diagram

CA3217E



Schematic Diagram (Continued)

CA3217E



Test Circuit

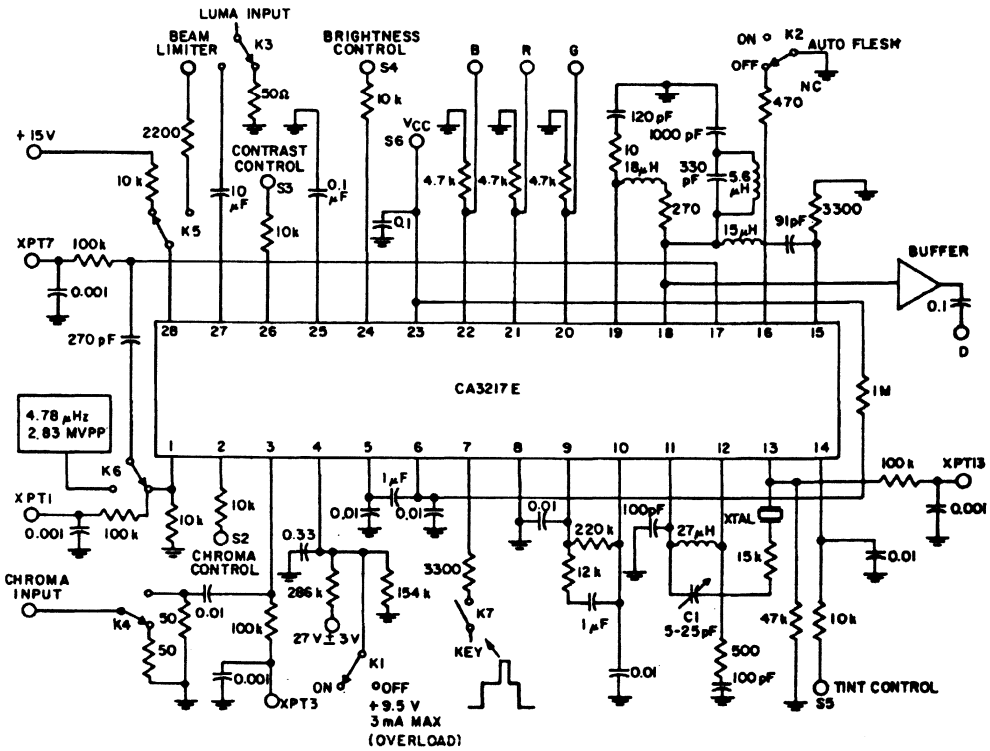


FIGURE 1. TEST CIRCUIT FOR CA3217E

Typical Performance Curves

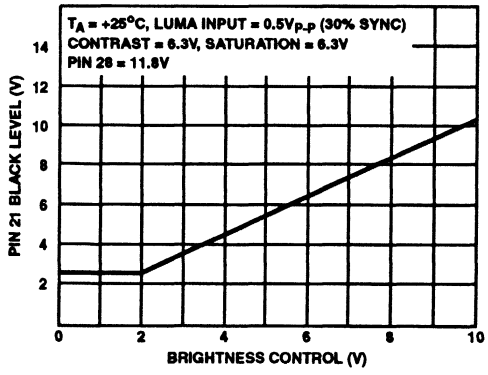


FIGURE 2. TYPICAL P21 BLACK LEVEL VERSUS BRIGHTNESS CONTROL

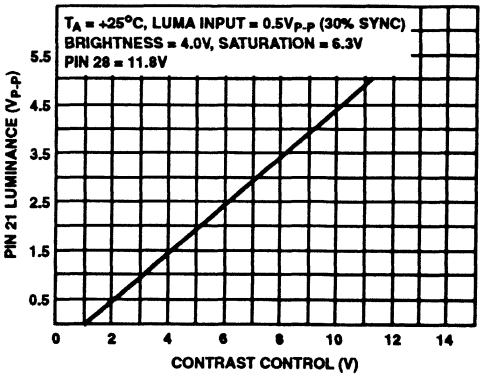


FIGURE 3. TYPICAL P21 LUMINANCE OUTPUT vs CONTRAST CONTROL

Typical Performance Curves (Continued)

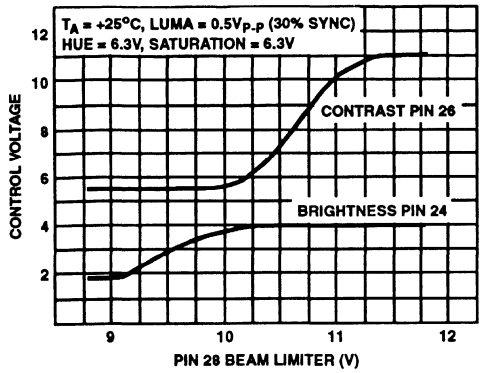


FIGURE 4. TYPICAL BEAM LIMITER vs CONTRAST AND BRIGHTNESS

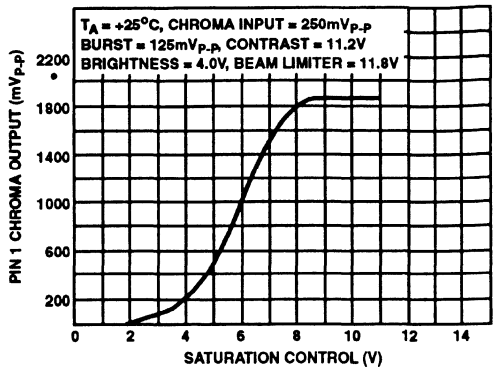


FIGURE 5. TYPICAL P1 CHROMA OUTPUT vs SATURATION CONTROL

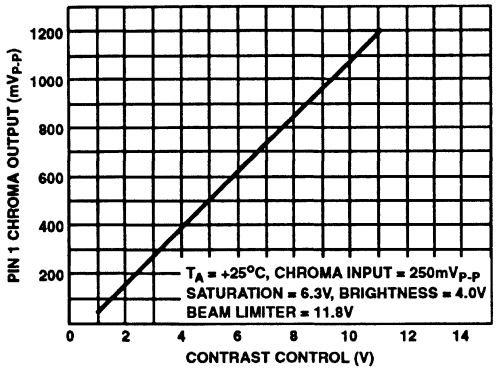


FIGURE 6. TYPICAL P1 CHROMA OUTPUT vs CONTRAST CONTROL

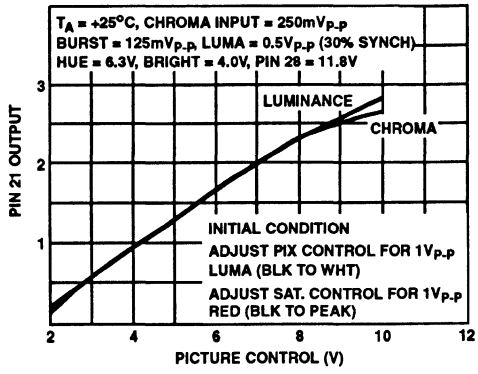


FIGURE 7. TYPICAL LUMA/CHROMA TRACK

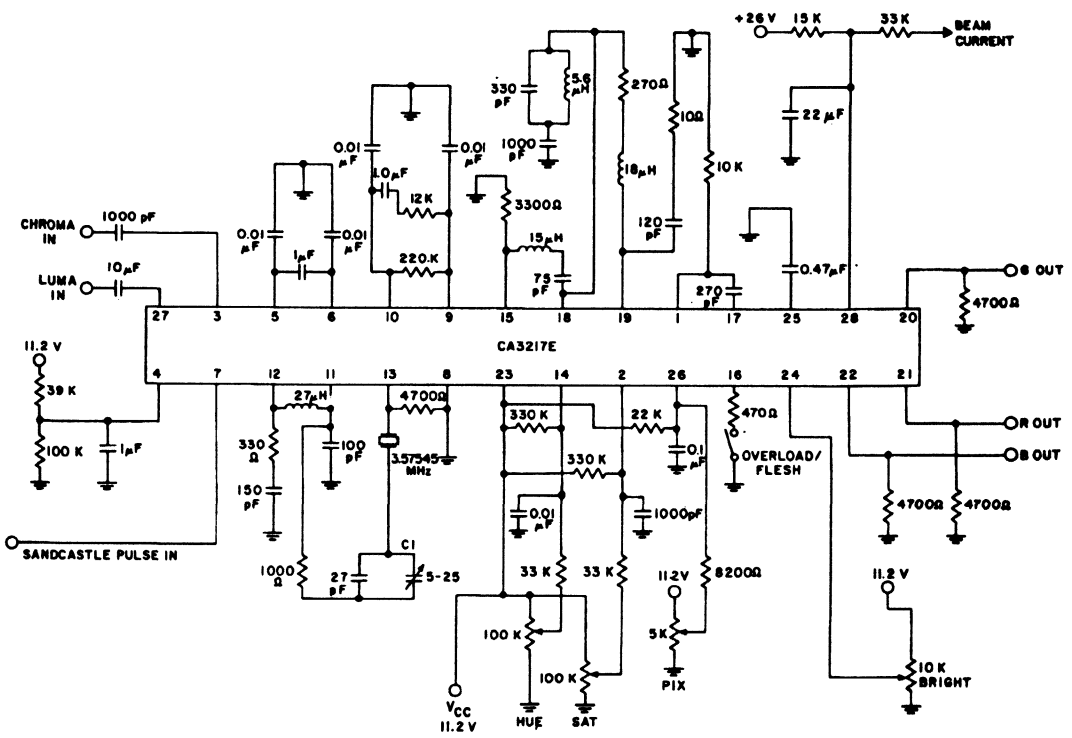


FIGURE 8. TYPICAL APPLICATION CIRCUIT

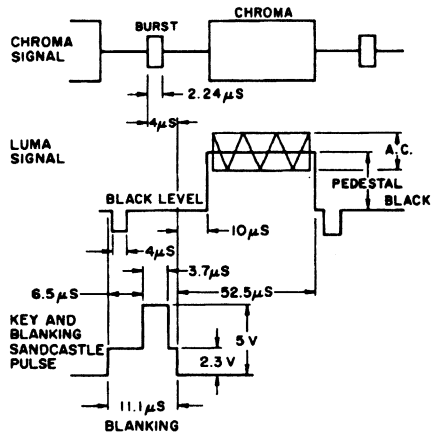


FIGURE 9. TEST SIGNALS FOR THE CA3217E

HARRIS SEMICONDUCTOR

CA3256

BiMOS Analog Video Switch and Amplifier

March 1993

Features

- 5 Multiplex Video Channels
  - 1 Independent Channel
  - 4 Channels with Enable
- 4 LED Channel Indicator Outputs
- Wideband Video Amplifier .....25MHz Unity Gain
- Adjustable Video Amplifier Gain
- High Signal-Drive Capability

Applications

- Video Multiplex Switch
- 75Ω Video Amplifier/Line Driver
- Video Signal-Level Control
- Monitor Switching Control
- TV/CATV Audio/Video Switch
- Video Signal Adder/Fader Control

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3256E	-40°C to +85°C	18 Lead Plastic DIP
CA3256M	-40°C to +85°C	20 Lead SOIC

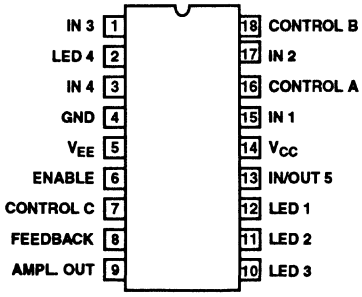
Description

The CA3256 BiMOS analog video switch has five channels of CMOS multiplex switching for general-purpose video-signal control. One of four CMOS channels may be selected in parallel with channel 5. The CMOS switches are inputs to the video amplifier but may be used in bilateral switching between channels 1 to 4 and channel 5. The analog switches of channels 1 to 4 are digitally controlled with logic level conversion and binary decoding to select 1 of 4 channels. The enable function controls channels 1 to 4 but does not affect channel 5. LED output drivers are selected with the channel 1-to-4 switch selection to indicate the ON-channel. Channel 5 may be used as a monitor output for data or signal information on channels 1 to 4. The transmission gate switches shown in the block diagram of the CA3256 are configured in a "T" design to minimize feedthrough. When the switch is off, the shunt or center of the "T" is grounded.

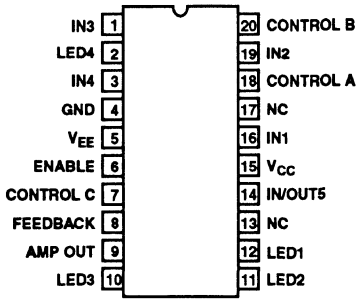
The amplifier has high input impedance to minimize the R_{ON} transmission gate insertion loss. The amplifier output impedance is typically 5Ω in a complementary symmetry output. The amplifier can directly drive a nominal 75Ω coaxial cable to provide line-to-line video switching. The gain of the amplifier is programmable by different feedback resistor values between pins 8 and 9. Compensation may also be used between these pins for an optimally flat frequency response. An internal regulated 5V DC bias reference with temperature compensation permits stable direct-coupled output drive and minimizes DC offset during signal switching.

Pinouts

CA3256
(PDIP)
TOP VIEW



CA3256
(SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1769.3

Block Diagram

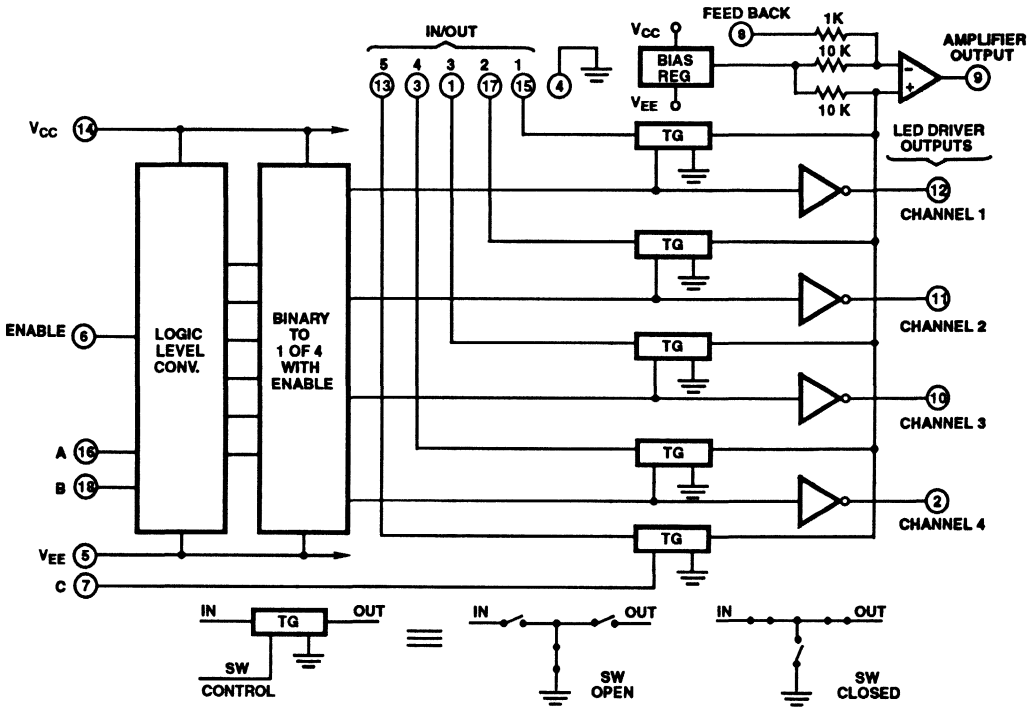


FIGURE 1

(DIP PIN OUT)

Switch Control Logic

CHANNEL NUMBER	C	A	B	ENABLE
1	O	O	O	I
2	O	O	I	I
3	O	I	O	I
4	O	I	I	I
5 + (1-4)*	I	Channel 1-4		I
5	I	Channel 5 Only		O
None	O	X	X	O

* For Maximum Video Bandwidth, Use Single Channel Selections

Absolute Maximum Ratings

DC Supply Voltage Range, V_{CC} (Referenced to V_{EE}) ..... +18V
Control Input Voltage Range, All Inputs ..... V_{EE} to V_{CC}
Signal Input Voltage Range, Channel 1-5 ..... 3Vp-p
Amplifier Output Current 30mA
DC LED Sink Current 30mA
Junction Temperature (Plastic Packages) ..... +150°C
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, Nominal Data for V_{CC} = 12V; V_{EE} = GND

CHARACTERISTICS	SYMBOL	TYPICAL VALUES		UNITS
Power Supply Voltage V_{CC}-V_{EE}		10 to 17		VDC
Power Supply Current V_{CC}-V_{EE} = 12V		20		mA
		SWITCH	AMPLIFIER	
Open Loop Gain	A_{OL}	-	35	dB
Programmable Gain, FB Adjustment Range		-	-0.8 A_{OL}	dB
Power Bandwidth		-	10	MHz
Unity Gain Bandwidth, 1kΩ, 7pF Compensation		-	25	MHz
Insertion Loss		-0.8	-	dB
Signal Feedthrough, 5MHz		-66	-	dB
Input Impedance	Z_{IN}	-	10	kΩ
Output Impedance	Z_{OUT}	-	5	Ω
Maximum Input Voltage	$V_{I(max)}$	3	2.5	Vp-p
Maximum Output Voltage, Clipped	$V_{O(max)}$	-	7	Vp-p
Reference Bias Output Voltage (V8 - V_{EE})		-	5	VDC
Differential Gain		-	1	%
Differential Phase		-	1	Degree
Off Isolation, Channel to Channel, Z_{IN} = 75Ω		-66	-	dB
LLC Switch Turn On/Off Time Delay		-	0.5	µs
Maximum LED Sink Current		-	30	mA
Typical Output Source Current		-	16	mA
Channel Control Switch A, B, C and E_N Threshold (Note 1, 2)	V_{TH}	Approximately. (V_{CC}-V_{EE})/2		V

CAUTION: Connect the V_{EE} power supply voltage before or during the V_{CC} turn-on.

NOTES:

1. Threshold value is referenced to GND.
2. V_{TH} is restricted by the equation. $V_{TH} < V_{CC}$ -1.

Electrical Specifications T_A = +25°C, V_{CC} = +12, V_{LED} = +12, V_{EE} = GND, Pin 4 = GND, Feedback Switch Closed, V_{HIGH} = 9V, V_{LOW} = 3V (See Figure 3), Unless Otherwise Specified.

	INPUTS					CHANNEL SWITCH CONTROL								
	CH 1	CH 2	CH 3	CH 4	CH 5	A	B	C	ENABLE	NOTE 3 TEST PIN#	MIN	TYP	MAX	UNITS
PARAMETERS	PIN 15	PIN 17	PIN 1	PIN 3	PIN 13	PIN 16	PIN 18	PIN 7	PIN 6					
Supply Current, I_{CC} V_{LED} = 0V	0V	0V	0V	0V	0V	3V	3V	3V	3V	14	10	16	22	mA
Dual Supply Current V_{CC} = +7, V_{EE} = -5	0V	0V	0V	0V	0V	0V	0V	0V	7V	14/5	10	20	26	mA
Amplifier Output, Open Loop V_{LED} = 0V	0V	0V	0V	0V	0V	3V	3V	3V	3V	9	6	8.5	10	V
Amplifier Output, Closed Loop, V_{LED} = 0V	0V	0V	0V	0V	0V	3V	3V	3V	3V	9	4.8	5.1	5.4	V
I_{OUT} MAX. (Source) Open Loop	0V	0V	0V	0V	0V	3V	3V	3V	3V	9 Note 1	-	-70	-25	mA
I_{OUT} MAX. (Sink) Open Loop	0V	0V	0V	0V	0V	3V	3V	3V	3V	9 Note 2	10	16	-	mA
Input Leakage Channel 1-5	3V	3V	3V	3V	3V	3V	3V	3V	3V	1, 3, 15, 17	-15	5	15	nA
Channel Control Input A, B, C, Enable Leakage	0V	0V	0V	0V	0V	Measure at 3V, 9V each; Enable and Channel Switching Control Inputs				6, 7, 16, 18	-20	10	20	nA
LED Off, V_{OFF}	0V	0V	0V	0V	0V	Select Channel 0-5				2, 10, 11, 12	11.97	11.99	-	V
LED On, V_{ON}	0V	0V	0V	0V	0V	Select Channel 0-5				2, 10, 11, 12	-	0.1	0.3	V
Switch Resistance, R_{DS}	±100µA Input Each Switch, Channel 1-4 + 5					Select Channel 1-4		9V	9V		0.8	1.1	1.4	kΩ
R_{DS} Match	Calculation: (Max R_{DS} - Min R_{DS})/Min R_{DS}									-	-	3.6	5	%
Amplifier Output Offset V_O Feedback Switch Closed V_{CC} = +7, V_{EE} = -5	0V	0V	0V	0V	0V	0V	0V	0V	7V	9	-100	45	100	mV
Closed Loop Unity Gain	3V	0V	0V	0V	0V	3V	3V	3V	9V	9	-0.5	-0.1	0.5	dB

NOTES:

1. V_{OUT} = +3V.
2. V_{OUT} = +7V.
3. DIP Pinout

Typical Applications

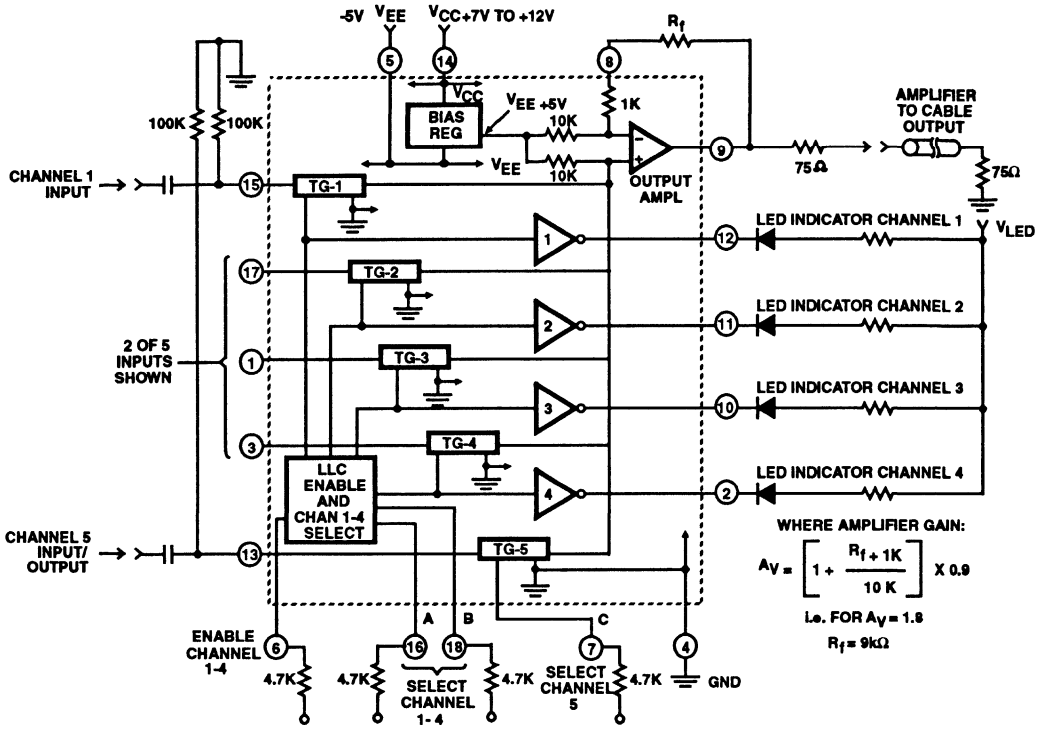


FIGURE 2(a). TYPICAL APPLICATION BIAS CIRCUIT DIRECT-COUPLED OUTPUT WITH V_{EE} = -5V (DIP PINOUT)

Typical Applications (Continued)

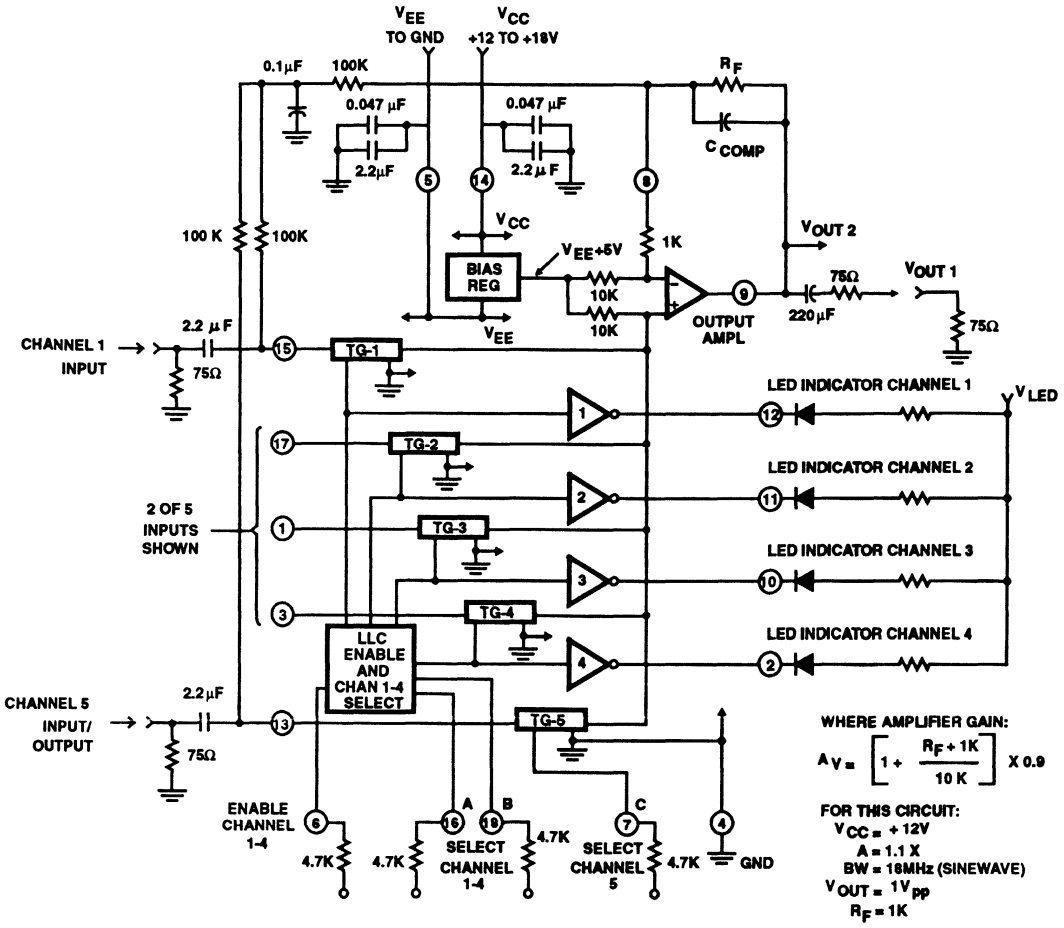
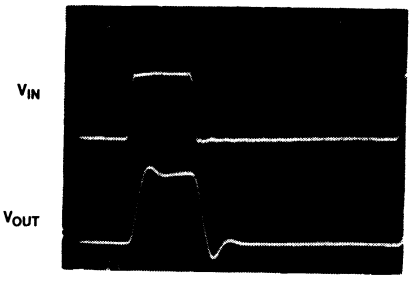


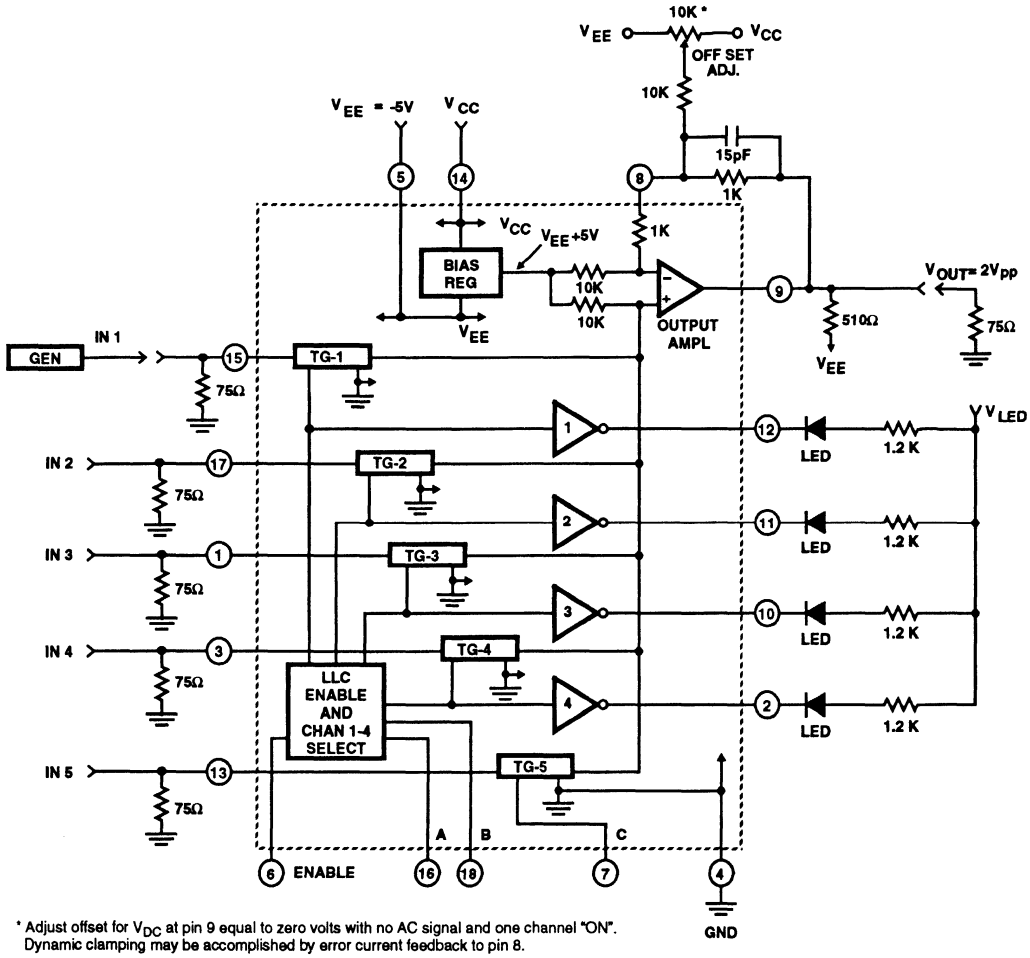
FIGURE 2(b). TYPICAL APPLICATION BIAS CIRCUIT AC-COUPLED INPUT WITH V_{EE} = GND (DIP PINOUT)



Waveform Display (Figure 2b) Pulse Performance = 20ns t_R for 0 to 2V Pulse.

V_{CC} = +12V, R_F = 1kΩ, C_{COMP} = 6pF, Pin 9 at $V_{EE(GND)}$.

Typical Applications (Continued)



* Adjust offset for V_{DC} at pin 9 equal to zero volts with no AC signal and one channel "ON". Dynamic clamping may be accomplished by error current feedback to pin 8.

FIGURE 2(c). TYPICAL APPLICATION BIAS CIRCUIT DC-COUPLED INPUT AND OUTPUT. THE V_{P-P} OUTPUT CAPABILITY IS FIXED BY THE V_{CC} AND V_{EE} RANGE. (DIP PINOUT)

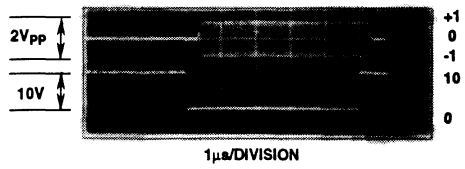


PHOTO 1. WAVEFORM DISPLAY (FIGURE 2c) GATED OUTPUT FOR V_{CC} = +12V ENABLE = HIGH, CONTROL B = C = LOW, CONTROL A = 10V PULSE. THE BURST OUTPUT IS DELAYED ~ 400ns AT t_{ON}, t_{OFF}.

Typical Applications (Continued)

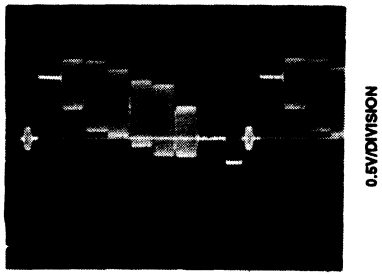


PHOTO 2. STANDARD NTS COLOR BAR

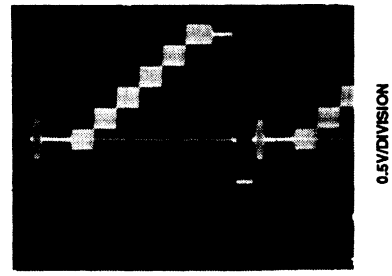


PHOTO 3. UNIFORM STEP SIGNAL WITH 3.58MHz MODULATION

Test Circuits

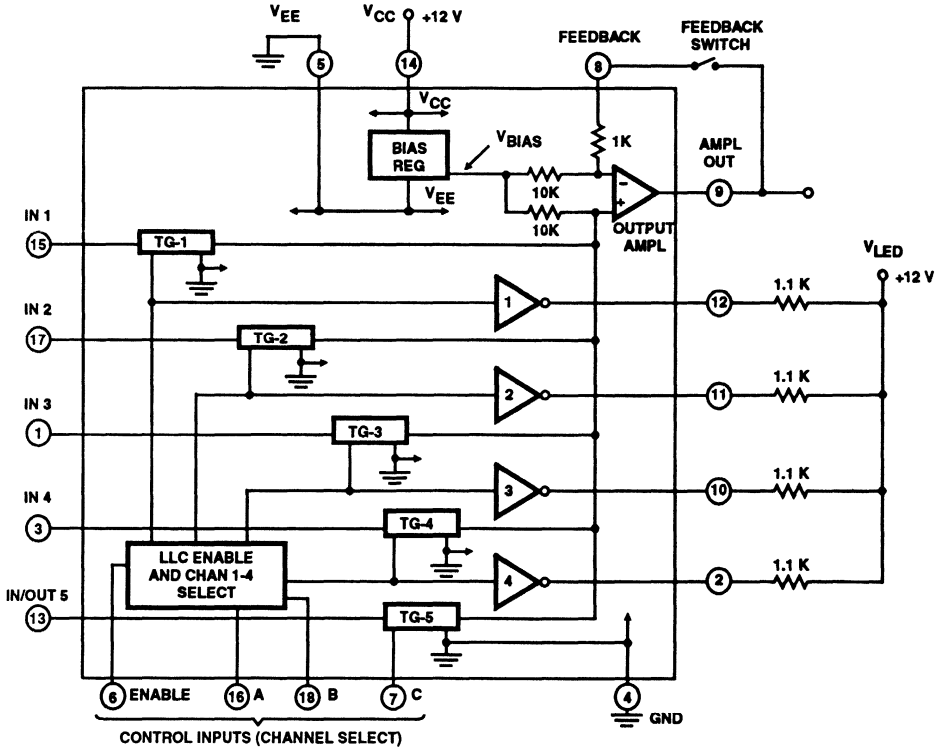


FIGURE 3. CA3256 TEST CIRCUIT (DIP PINOUT)

Test Circuits (Continued)

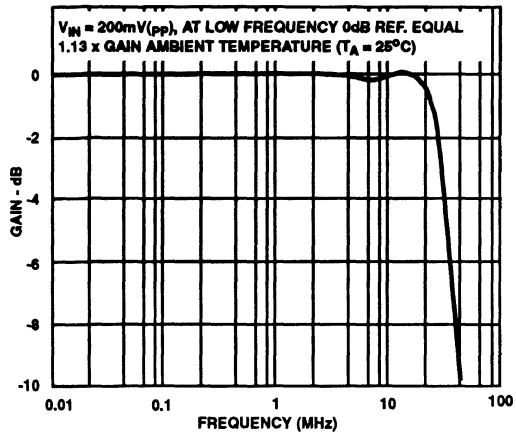


FIGURE 4(a). GAIN-BANDWIDTH CHARACTERISTICS OF FIGURE 2(b) WITH COMPENSATION CAPACITOR, C_{COMP}, AND R_f, SEE FIGURE 4(b) AND FIGURE 6(1).

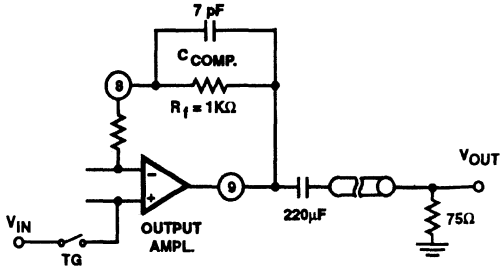


FIGURE 4(b). TEST CIRCUIT

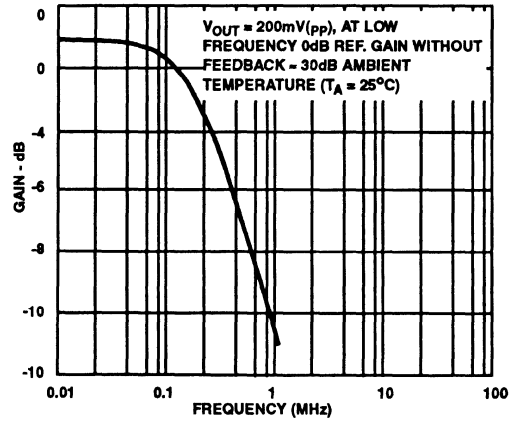


FIGURE 5(a). OPEN LOOP GAIN-BANDWIDTH CHARACTERISTIC OF FIGURE 2(b) WITH NO FEEDBACK, SEE FIGURE 5(b) AND FIGURE 6(5)

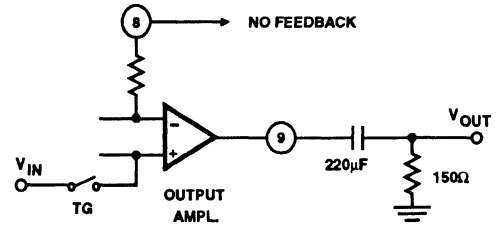
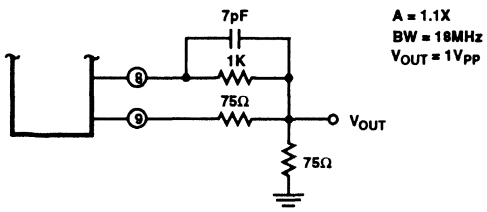
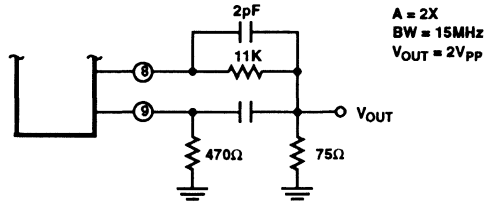


FIGURE 5(b). TEST CIRCUIT

Test Circuits (Continued)

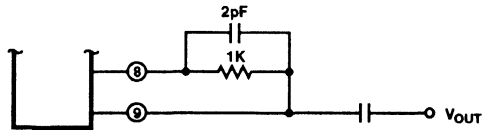


(1)



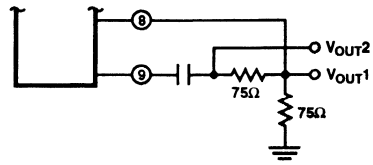
NOTE: 470Ω added to increase source drive current.

(2)



A = 1.1X
BW = 40MHz (1.2 X GAIN PEAK AT 25MHz)
VOUT = 200m VPP

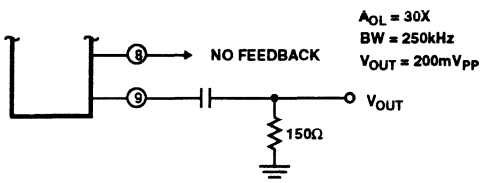
(3)



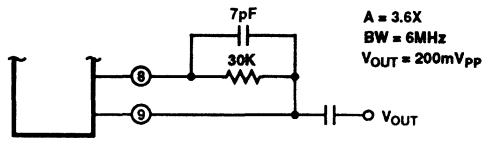
VOUT1
A = 1.1X
BW = 15MHz
VOUT = 200mVPP

VOUT2
2X
26MHz (UNITY GAIN)
400mVPP

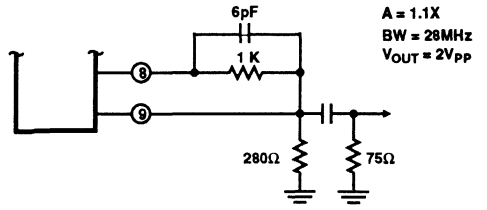
(4)



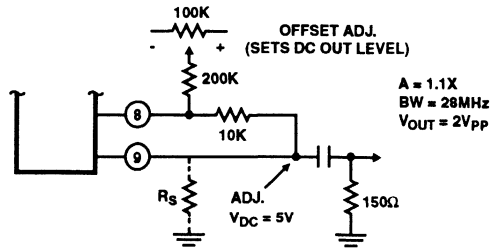
(5)



(6)



(7)



NOTE: Add R_S to reduce high-frequency slewing.

(8)

FIGURE 6. OTHER TABULATED RESULTS FOR VARIATIONS OF LOAD AND FEEDBACK FOR CIRCUIT, FIGURE 2(b); V_{CC} = +12V

Application of High Speed CMOS Analog Switches

CMOS analog switches are available in a wide variety of forms, and have been known and used for some time. There are a number of advantages to using the CMOS transmission gate as a switch:

- Ideal Suitability to Series Cascade Arrangements.
- Simple Multiple Parallel Input Switching Arrangements.
- No Bipolar Junctions and, Hence, No Offset.
- Very Low Power Consumption.
- Wide Signal-Swing Capability.
- Fast Multiplexing and Video Switching in High-speed CMOS.
- Wide Bandwidth in High-Speed CMOS.
- Low RON Channel Resistance In High-Speed CMOS.
- Bidirectional Signal Handling.

An Integrated Video-Switch Amplifier

Commonly, integrated video-switch amplifiers have been fabricated in the bipolar technology using differential amplifiers in a current-switching mode. In this form, two differential pairs are needed for two input-signal sources. The handling of multiple sources is very much more complex. The advantages of the CMOS video-switch amplifier have already been noted. While the bipolar video switch has high output drive and switching speed as advantages, the price is high in voltage offset and current drain. The integrated device solution that is offered here is in the use of the BiMOS technology, where both the CMOS and bipolar processes complement each other to provide CMOS switching with bipolar amplifiers. The BiMOS process allows several CMOS switches to be coupled to a bipolar drive-amplifier in the same process to exploit the best of two technologies.

Other advantages are gained when the BiMOS process is used for an IC video-switch amplifier design. The BiMOS process calls for a p-substrate and, therefore, isolated n-epitaxial boats can be built for both n and p channel parts. The boats provide for better isolation of the n and p channels. The n and p wells in a transmission-gate cell can be switched between source and rail; therefore, they have a smaller body effect on both n and p devices, which results in better gain linearity. Where desired, oxide capacitors are available for bipolar amplifier compensation.

CA3256 Video-Switch Amplifier

The block diagram of Figure 1 shows the functional diagram of the CA3256, which consists of five MOS channels, each comprising a three-element T-switch. The output of the five switches is made common and fed into the input of a bipolar buffer amplifier. The T-switch, together with the input impedance of the buffer, is typically 10kΩ, and has an insertion loss of approximately 0.8dB. The T-switch was designed to handle up to $3V_{PP}$ input signal with low distortion. The T-switches of the CA3256 conform to a break-before-make format; hence, shorting to ground is eliminated.

The amplifier is programmable for gain and, typically, can provide a gain of 1 into a 75Ω load or a gain of 5 into a 1kΩ load. The maximum output signal swing with linearity is greater than $5V_{PP}$ for (V_{CC} - V_{EE}) greater than or equal to 12 volts, while the maximum output current is approximately 20mA. The amplifier has base-current compensation to reduce offset and a temperature compensated 5-volt zener referenced bias. Other features include LED-selector indicators for channels 1 through 4. The fifth channel is independently selectable for use as a separate input or output in parallel with any on channel, and may be used as a monitor, or for pass-through, signal summing, or parallel distribution.

In the application, the user has the option to specify -5 volts V_{EE} for the switch and a ground reference for the amplifier input and output. Alternatively, the CA3256 may be used with a single +12 volt supply. The logic select for channels 1 through 4 is controlled by the A, B and Inhibit lines with ground to V_{CC} logic switching. The logic threshold is approximately ~ (V_{CC} - V_{EE})/2 referenced to ground. DC coupling may also be used at the output (when VEE is returned to a -5 volt supply). For the circuit of Figure 2(b). AC coupling is used at the output and input. The switching bias arrangement shown provides for stable bias across each switch when in the off position to minimize transients when the input is switched.

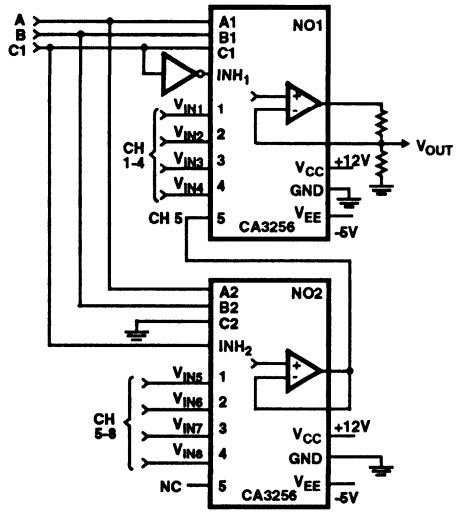
Any combination of switch input circuits can be configured with multiple, parallel, line-drive outputs. The video-switch amplifier circuit of Figure 7 illustrates how the CA3256 may be configured in pairs to provide an 8-to-1 video-switch amplifier using a 3-bit address to select the input. It is also possible to use the fifth channel input to tie signals to a common bus line for distribution from the selected amplifier; however, distributed capacitance loading will result in reduced bandwidth. The 4 plus 1 combination of input-signal switching provides for a wide assortment of video-switch circuit configurations.

While the BiMOS process does provide some compromises for both the switch and the amplifier, the combined system is capable of the performance needed in most high-quality, switching applications. As an integrated system, many of the problems in pc-board layout are simplified, and there is a reduction in component count. In its simplest form, with +12 and -5 volt supplies, the CA3256 may be DC connected at the input and output; the LED indicators need not be connected. Under these conditions, the circuit may be as simple as the one in Figure 7.

Summary

While each video-switch amplifier is designed for a specific application and, to that end, is tailored as far as performance to a given set of specifications, the circuit-designer's goal is generally the same in every case: to make the best possible switch for the lowest cost. In this respect, the CA3256 IC switch and amplifier discussed provide an excellent choice for a cost-effective high-performance video-switch amplifier, by taking advantage of the complementary features of both high-speed CMOS and bipolar integrated circuits.

Typical Applications (Continued)



TRUTH TABLE

CH	C1	A	B
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

FIGURE 7. AN 8-TO-1 VIDEO-SWITCH AMPLIFIER USING TWO CA3256 DEVICES.

HARRIS SEMICONDUCTOR

CD22402

Sync Generator for TV Applications and Video Processing Systems

March 1993

Features

- Interlaced Composite Sync Output
- Automatic Genlock Capability
- Crystal Oscillator Operation
- 525 or 625 Line Operation
- Vertical Reset Option
- Wide Power Supply Operating Voltage 4-15V

Applications

- Cameras
- Monitors and Displays
- CATV
- Teletext
- Video Games
- Sync Restorer
- Video Service Instruments

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CD22402D	-40°C to +85°C	24 Lead Ceramic Sidebraze DIP
CD22402E	-40°C to +85°C	24 Lead Plastic DIP

Description

The Harris CD22402* is a CMOS LSI sync generator that produces all the timing signals required to drive a fully 2-to-1 interlaced 525-line 30-frame/second, or 625-line 25-frame/second TV camera or video processing system. A complete sync waveform is produced which begins each field with six serrated vertical sync pulses, preceded and followed by six half-width double frequency equalizing pulses. The sync output is gated by the master clock to preserve horizontal phase continuity during the vertical interval.

The CD22402 can be operated either in "genlock" mode, in which it is synchronized with a reference sync pulse train from another TV camera, or in "stand-alone" mode, in which it is synchronized with a local on-chip crystal oscillator (the crystal and two passive components are off chip). Also, the circuit can sense the presence or absence of a reference sync pulse train and automatically select the "genlock" or "stand-alone" mode.

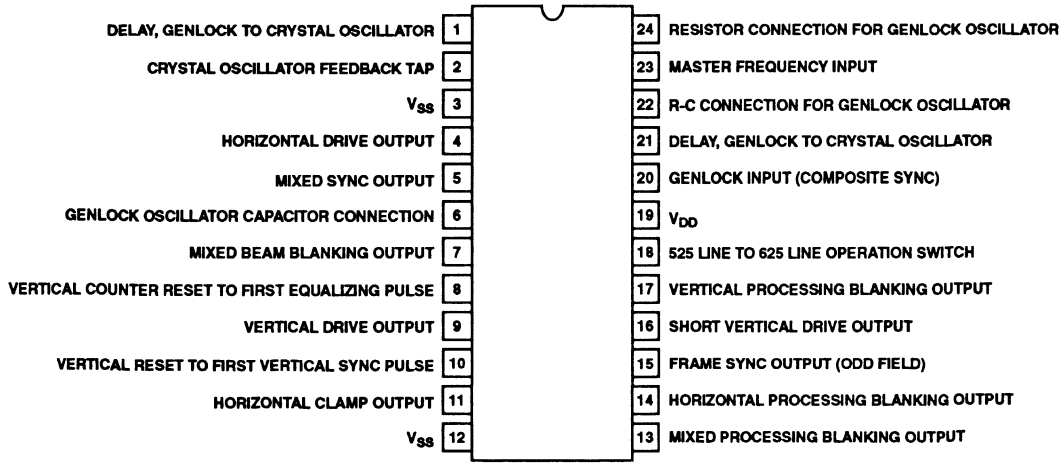
A frame sync pulse is produced at the beginning of every odd field. The vertical counter can be reset to either the first equalizing pulse or the first vertical sync pulse of the vertical interval. The interlaced sync provided by the CD22402 differs from RS-170 by having slightly narrower sync and equalizing pulses. The clock frequency of 32 times horizontal rate allows for approximately 4μs horizontal pulse widths and 2μs equalizing pulses. Otherwise operation can be phase locked to a color sub-carrier for a full interlaced operating system.

The CD22402 is operable with a single supply over a voltage range of 4V to 15V.

* Formerly Developmental Type No. TA6993.

Pinout

CD22402 (PDIP, CDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1686.2**

Absolute Maximum Ratings

DC Supply Voltage
Voltage Referenced to V_{SS} Terminal 15V
Input Voltage Range, All Inputs (Notes 2, 3) ..... $V_{SS} \le V_I \le V_{DD}$
DC Input Current, Any One Input (Note 2) ..... ±10mA
Power Dissipation Per Package
T_A = -40°C to +60°C (Package Type E) 500mW
T_A = +60°C to +85°C
(Package Type E) .... Derate Linearly at 12mW/°C to 200mW
T_A = -55°C to +100°C (Package Type D) 500mW
T_A = +100°C to +125°C
(Package Type D) .... Derate Linearly at 12mW/°C to 200mW
Power Dissipation Per Output Transistor
T_A = Full Package Temp. Range (All Package Types) 100mW
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
Package Type D ..... -55°C to +125°C
Package Type E ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

Values at -55°C, +25°C, +125°C Apply to D, H Packages.
Values at -40°C, +25°C, +85°C Apply to E Package

PARAMETERS	SYMBOL	TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES -55°C	-40°C	+85°C	+125°C	+25°C MIN	+25°C TYP	+25°C MAX	UNITS
DC ELECTRICAL SPECIFICATIONS											
Quiescent Device Current	I_{DD} Max.	-	5	-	-	-	-	0.5	0.75	1	mA
		-	10	-	-	-	-	1.5	2	2.5	mA
		-	15	-	-	-	-	3	4	5	mA
Output Low (Sink) Current	I_{OL} Min.	0.5	5	100	96	66	56	80	160	-	µA
		5	5	1200	1155	787	672	960	1920	-	µA
		0.5	10	248	239	164	140	200	400	-	µA
		10	10	3000	2868	1968	1680	2400	4800	-	µA
Output High (Source) Current	I_{OH} Min.	4.5	5	-100	-96	-66	-56	-80	-160	-	µA
		0	5	-1200	-1155	-787	-672	-960	-1920	-	µA
		9.5	10	-248	-239	-164	-140	-200	-400	-	µA
		0	10	-3000	-2868	-1968	-1680	-2400	-4800	-	µA
Output Voltage Low Level	V_{OL} Max.	-	5	0.15	0.15	0.15	0.15	-	-	0.15	V
		-	10	0.15	0.15	0.15	0.15	-	-	0.15	V
Output Voltage High Level	V_{OH} Min.	-	5	4.85	4.85	4.85	4.85	4.85	-	-	V
		-	10	9.85	9.85	9.85	9.85	9.85	-	-	V
Input Low Voltage	V_{IL} Max.	0.5, 4.5	5	1.5	1.5	1.4	1.4	-	2.25	1.5	V
		1, 9	10	3	3	2.9	2.9	-	4.5	3	V
Input High Voltage	V_{IH} Min.	0.5, 4.5	5	3.6	3.6	3.5	3.5	3.5	2.25	-	V
		1, 9	10	7.1	7.1	7	7	7	4.5	-	V
Input Current	I_{IN} Max.	-	-	-	-	-	-	-	10	-	pA

Refer to the CD4000B Series data book 250.5 for general operating and application considerations.

Switching Electrical Specifications T_A = +25°C and C_L = 15pF. Typical Temperature Coefficient for All Values of V_{DD} = 0.3%/°C

PARAMETERS (NOTE 1)	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
		V_{DD} (V)	MIN	TYP	MAX	
Output State Propagation Delay Time (50% to 50%)						
Low-to-High Level	t_{PLH}	5	-	40	80	ns
High-to-Low Level	t_{PHL}	10	-	20	40	ns
Output State Transition Time (10% to 90%)						
Low-to-High	t_{TLH}	5	-	45	90	ns
High-to-Low	t_{THL}	10	-	30	60	ns
Input Capacity (Per Input)	C_I	-	-	5	-	pF

NOTE:

1. The characteristics given are defined for unbuffered gate in the CMOS process of the CD22402.
2. To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10mA even when the power is off.
3. A connection must be provided at every input terminal. All unused inputs must be connected to V_{DD} or V_{SS}, whichever is appropriate.

Pin Descriptions

PIN NO.	SYMBOL	DESCRIPTION
1	XRC	**Delay, Genlock to Crystal Oscillator.** Resistor, diode and capacitor connection for delay that automatically turns on the crystal oscillator when the genlock input is removed. When the signal on terminal 1 is high the crystal oscillator is inhibited. Typical values for R and C are 1MΩ and 0.001μF. For operation as a crystal controlled stand alone sync generator without genlock, terminal 1 should be hardwired to V_{SS}.
2	XTP	**Crystal Oscillator Feedback Tap.** Feedback connection (tap) for crystal oscillator. When a crystal (shunted by a 1MΩ resistor) is connected between this terminal and terminal 23, and a 100pF capacitor is connected from this terminal to V_{SS}, the sync generator creates its own master frequency. For a 525-line, 30-frame/second raster, the crystal frequency is 504.000kHz*; and for a 625-line, 25-frame/second raster, the crystal frequency is 500.000kHz*.
3	V_{SS}	**Negative Power Supply Voltage.** This terminal must be hardwired to terminal 12 (V_{SS}).
4	HD	**Horizontal Drive Output.**
5	MS	**Mixed Sync Output.**
6	C	**Capacitor Connection for R-C Genlock Oscillator.**
7	MBB	**Mixed Beam Blanking Output.**
8	VRE	**Vertical Counter Reset to First Equalizing Pulse.** A low level signal on this terminal resets the vertical counter to the first equalizing pulse of a field. When not in use this terminal should be connected to V_{DD}.
9	VD	**Vertical Drive Output.**
10	VRV	**Vertical Counter Reset to First Vertical Sync Pulse.** A low level signal on this terminal resets the sync generator to the first vertical sync pulse of a field. For genlock operation, terminal 10 is used as a resistor and capacitor connection for an integrator network that detects vertical sync pulses in a master sync waveform to which the sync generator is to be genlocked. R is 22kΩ, and C is 0.001pF. When not in use this terminal should be connected to V_{DD}.
11	HC	**Horizontal Clamp Output.**
12	V_{SS}	**Negative Power Supply Voltage.**
13	MPB	**Mixed Processing Blanking Output.**
14	HPB	**Horizontal Processing Blanking Output.**
15	FS2	**Frame Sync Output (Odd Field).** A pulse coinciding with the first equalizing pulse is produced at the beginning of every odd field.
16	SVD	**Short Vertical Drive Output.**
17	VPB	**Vertical Processing Blanking Output.**

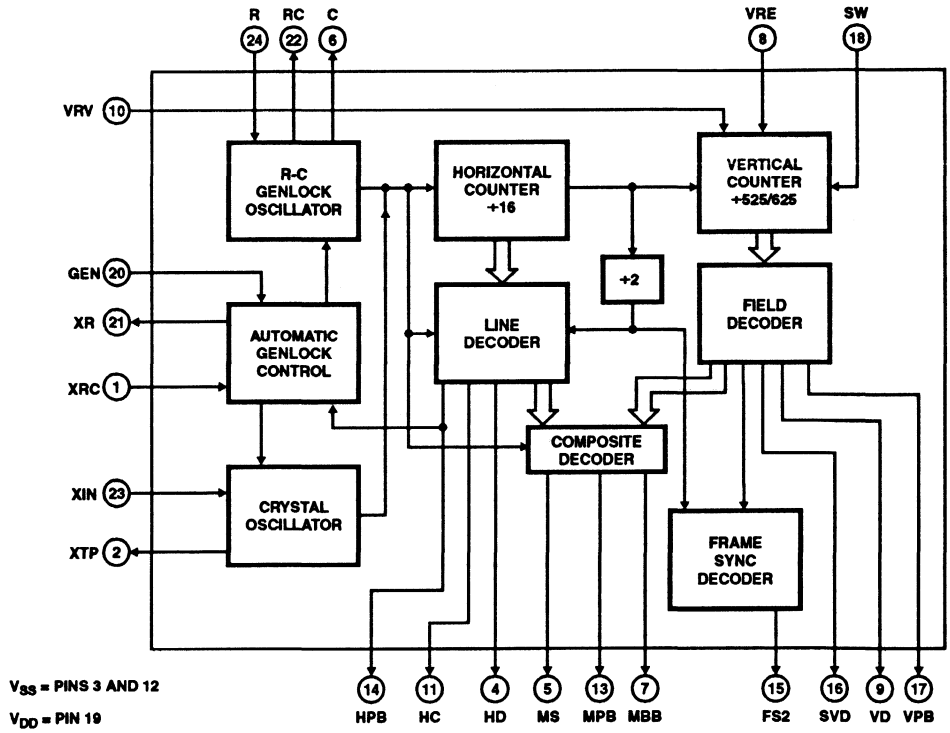
Pin Descriptions (Continued)

PIN NO.	SYMBOL	DESCRIPTION
18	SW	**Operation Switch for 525-Line or 625-Line Raster.** A high level signal on terminal 18 causes the sync generator to generate a 625-line raster. An internal pulldown resistor is connected to terminal 18, so in the absence of an applied input to this terminal, a 525-line raster is produced.
19	V_{DD}	**Positive Power Supply Voltage.** V_{DD} can be any voltage between +4 and +15 relative to V_{SS}.
20	GEN	**Genlock Input Composite Sync.** A negative going reference mixed sync waveform applied to terminal 20 disables the crystal oscillator and locks the R-C genlock oscillator to the horizontal pulses of the reference sync waveform. Vertical sync detection is achieved by an R-C integrator connected from terminal 20 to terminal 10 (vertical reset to first vertical sync pulse). An internal pull-up resistor is connected to terminal 20 so that in the absence of an applied input the crystal oscillator is enabled and the R-C genlock oscillator is disabled.
21	XR	**Delay, Genlock to Crystal Oscillator, Resistor and Diode Connection for Delay, Genlock to Crystal Oscillator.** Automatically turns on the crystal oscillator when the input to terminal 20 is removed.
22	RC	**Resistor and Capacitor Connection for Genlock Oscillator.** If the genlock oscillator is not used this terminal should be connected to V_{SS}. C should be 100pF, and R should be a 10kΩ potentiometer.
23	XIN	**Master Frequency Input.**
24	R	**Resistor Connection for Genlock Oscillator.**

* 32 times horizontal frequency

Block Diagram

CD22402 MONOCHROME TV SYNC GENERATOR WITH AUTOMATIC GENLOCK



Logic Diagram

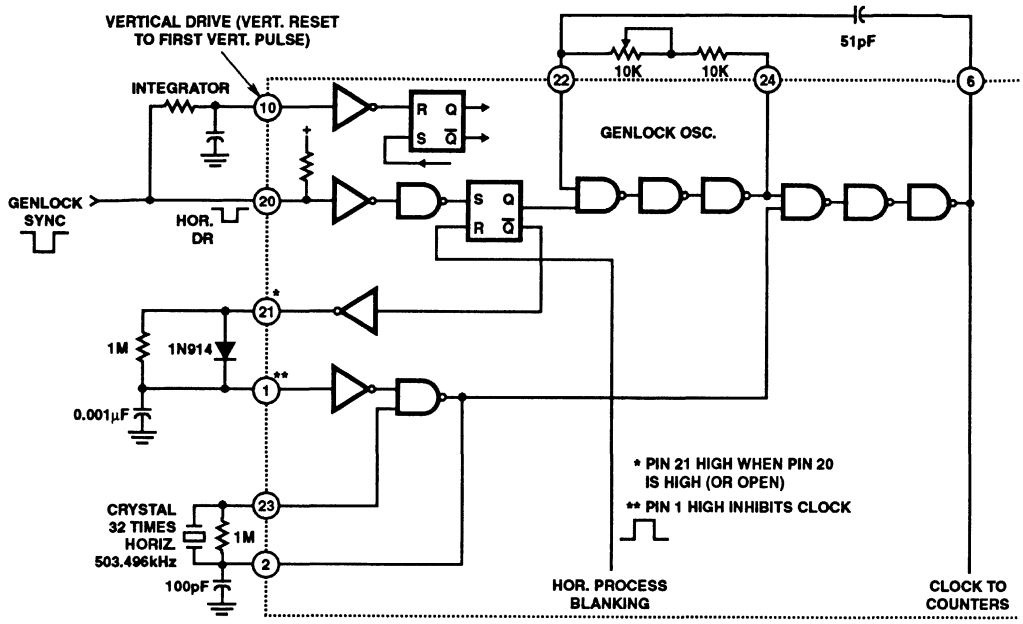


FIGURE 1. DETAIL OF THE OSCILLATOR/GENLOCK PORTION OF THE CD22402

Timing Waveforms

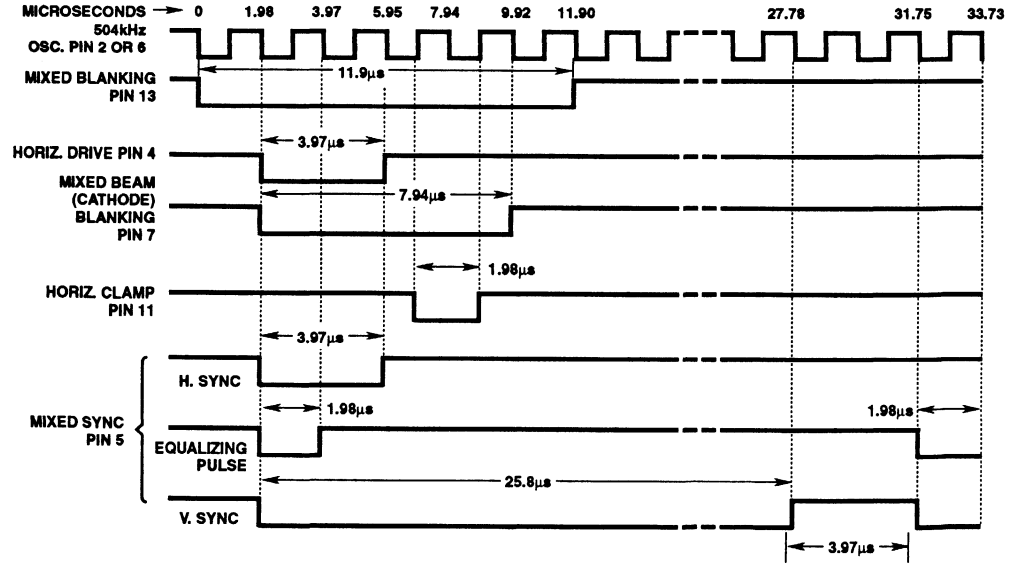


FIGURE 2. SYNC GENERATOR TIMING - 525/60Hz, HORIZONTAL TIMING WAVEFORMS

Timing Waveforms (Continued)

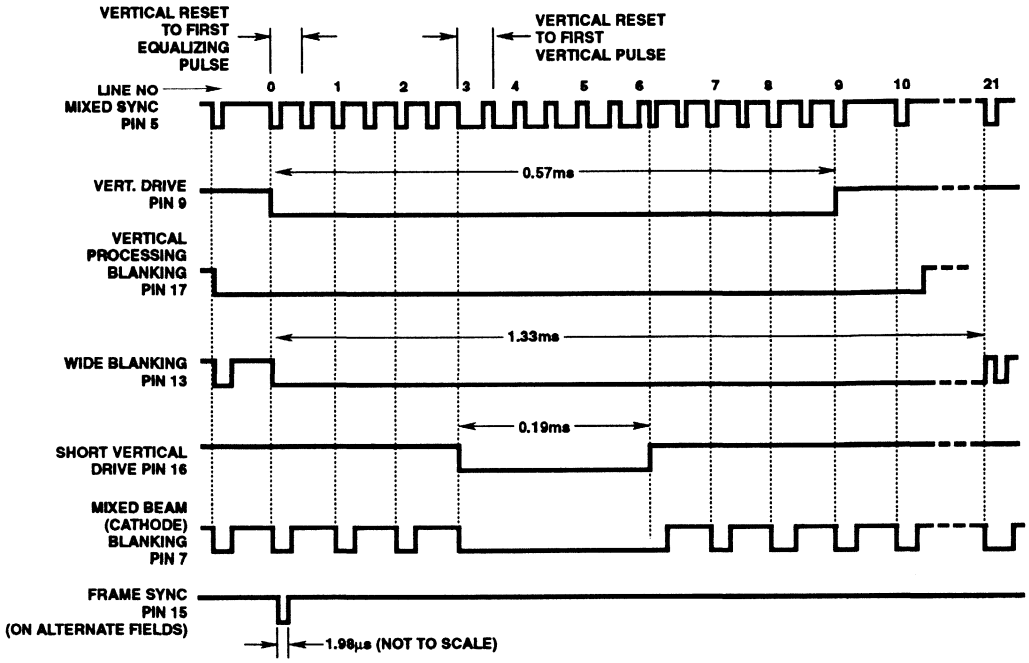


FIGURE 3. SYNC GENERATOR TIMING - 525/60Hz, VERTICAL TIMING WAVEFORMS

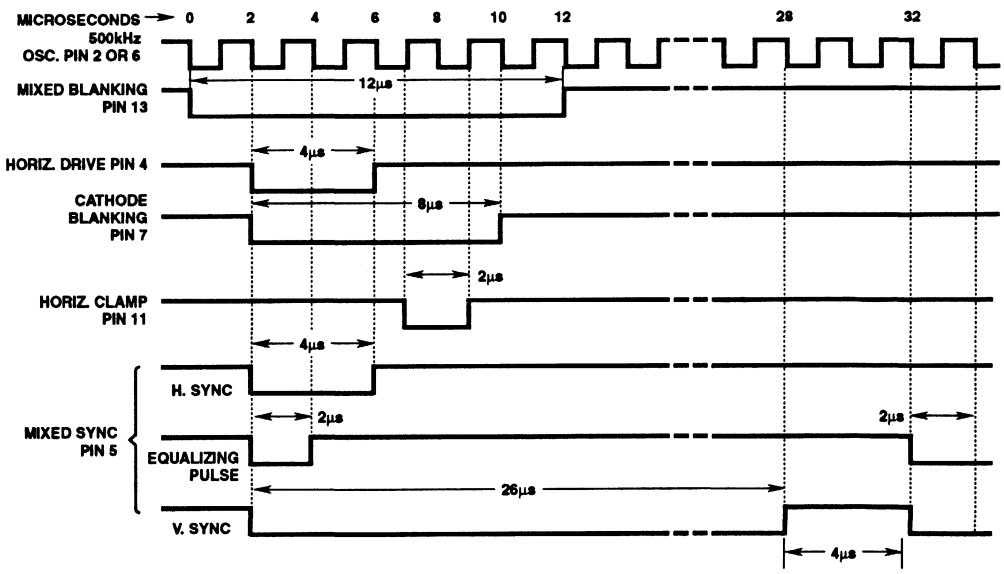


FIGURE 4. SYNC GENERATOR TIMING - 625/50Hz, HORIZONTAL TIMING WAVEFORMS

Timing Waveforms (Continued)

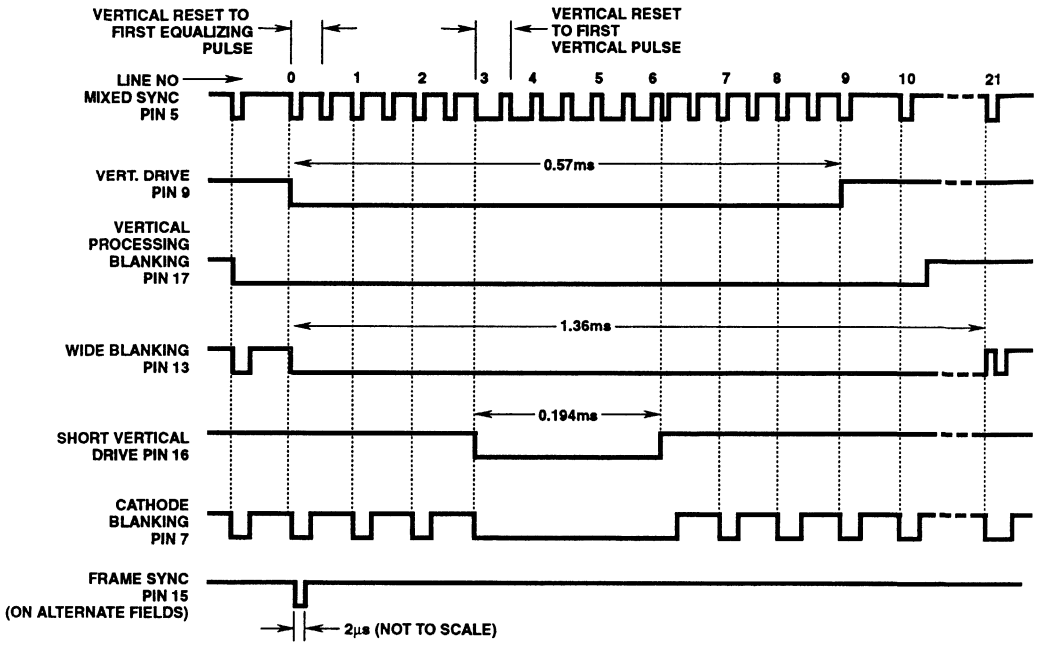


FIGURE 5. SYNC GENERATOR TIMING - 625/50Hz, VERTICAL TIMING WAVEFORMS

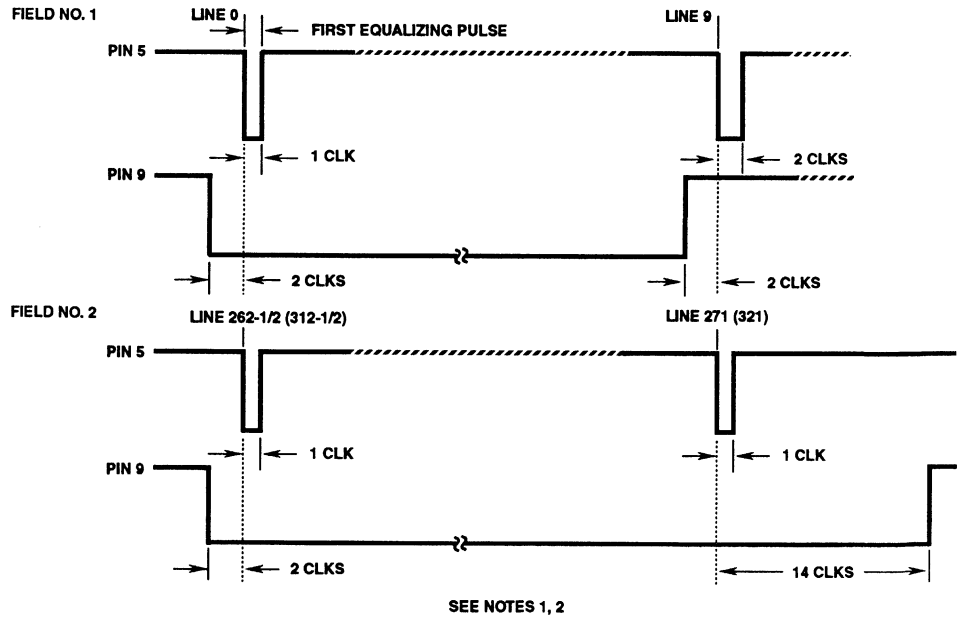


FIGURE 6. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (VERTICAL DRIVE - PIN 9)

Timing Waveforms (Continued)

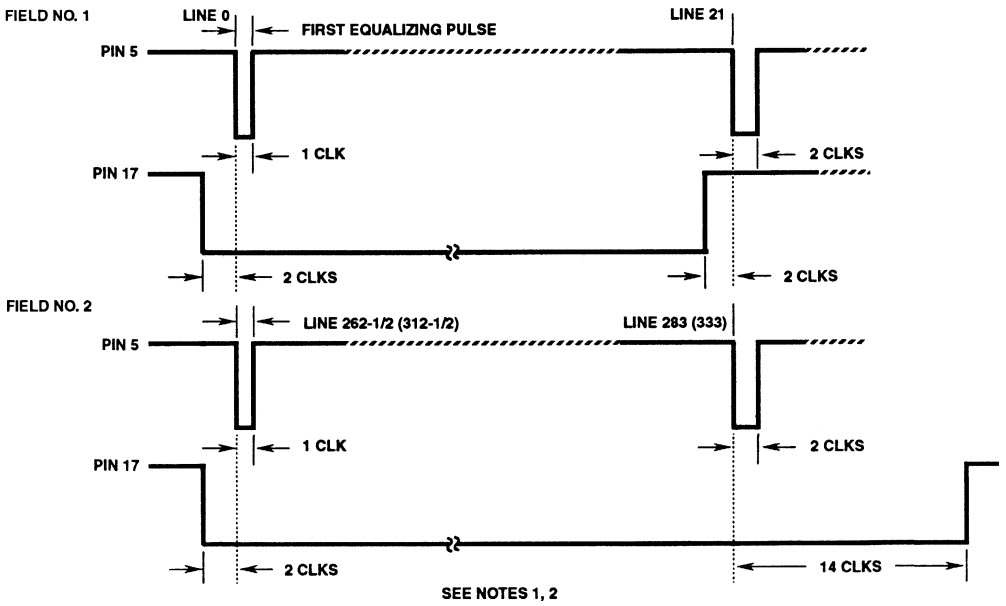


FIGURE 7. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (VERTICAL PROCESSING BLANKING - PIN 17)

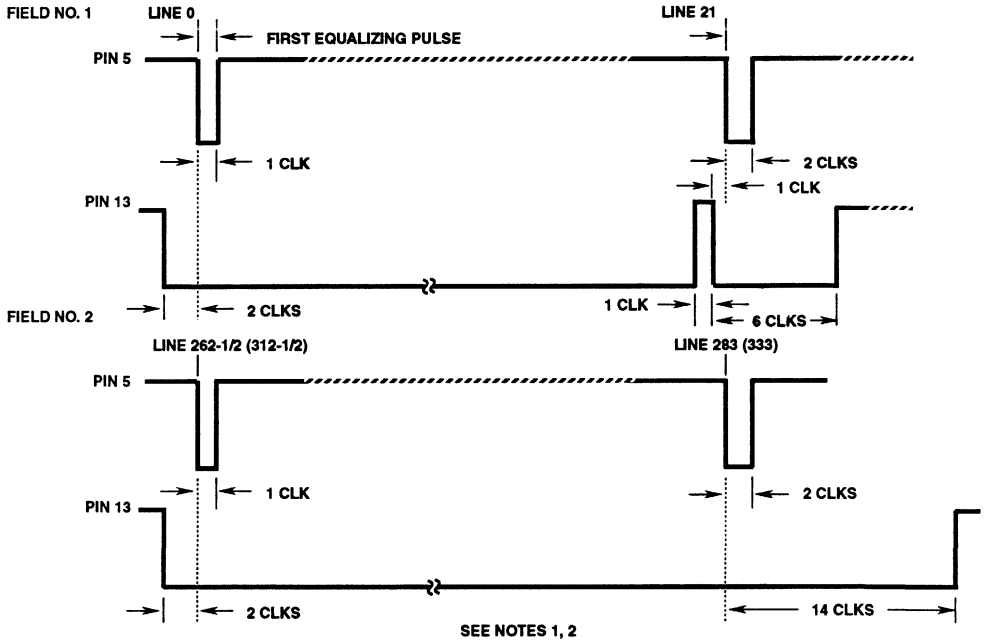


FIGURE 8. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (MIXED PROCESSING BLANKING - PIN 13)

Timing Waveforms (Continued)

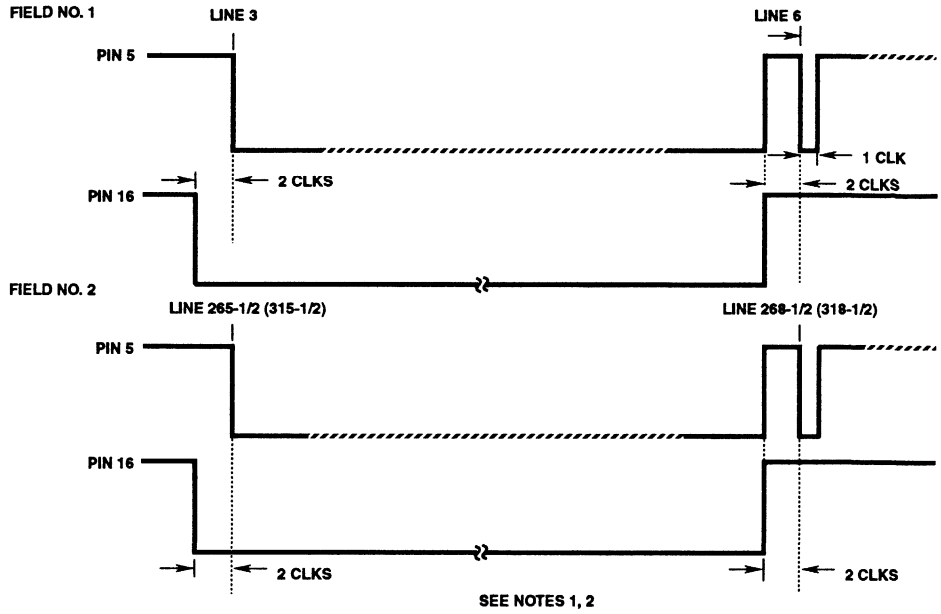


FIGURE 9. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (SHORT VERTICAL DRIVE - PIN 16)

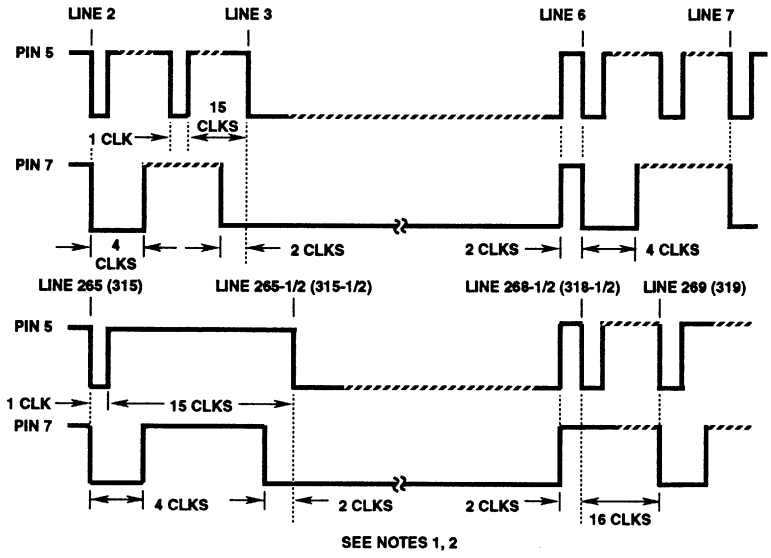


FIGURE 10. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (MIXED BEAM BLANKING - PIN 7)

NOTES:

1. Waveforms shown are for 525 line/60Hz, line number in parenthesis are for (625 line/50Hz).
2. Timing widths by clock count; for 525 line, 1 CLK = 1.98µs; for 625 line, 1 CLK = 2µs; 1 horizontal period = 32 CLKS.

Typical Applications (Refer to Application Note, AN-8742, for more information)

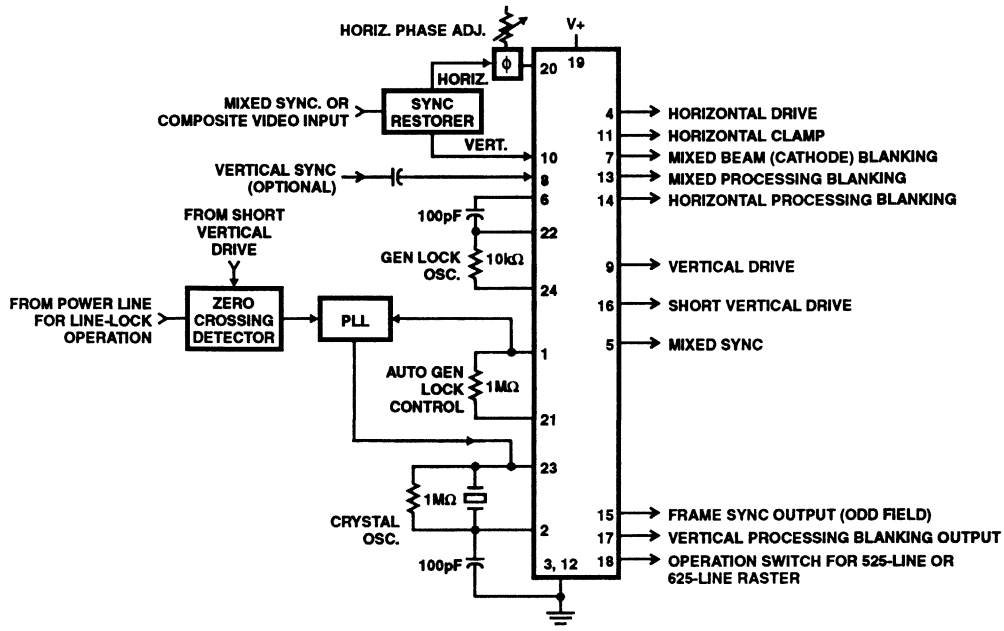
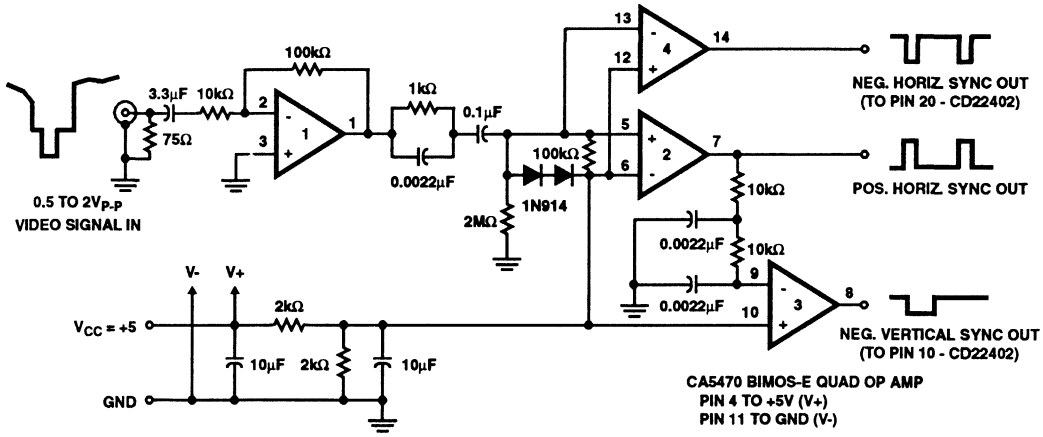


FIGURE 11. TYPICAL APPLICATION IN A TV CAMERA



THE GENLOCK INPUT TO PINS 10 AND 20 OF THE CD22402 ARE DIRECT COUPLED TO THE OUTPUT FROM PINS 8 AND 14 OF THE CA5470. REFER TO APPLICATION NOTE AN-8742 FOR ADDITIONAL INFORMATION.

FIGURE 12. SUGGESTED SYNC-SEPARATOR CIRCUIT USING THE CA5470 BIMOS-E QUAD OP AMP IN THE V_{CC} RANGE OF 4V TO 12V

HARRIS SEMICONDUCTOR

HA-2546

Wideband Two Quadrant Analog Multiplier

March 1993

Features

- High Speed Voltage Output 300V/μs
- Low Multiplication error 1.6%
- Input Bias Currents 1.2μA
- Signal Input Feedthrough . . . . . -52dB
- Wide Signal Bandwidth 30MHz
- Wide Control Bandwidth 17MHz
- Gain Flatness to 5MHz. 0.10dB

Applications

- Military Avionics
- Missile Guidance Systems
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generator

Description

The HA-2546 is a monolithic, high speed, two quadrant, analog multiplier constructed in the Harris Dielectrically Isolated High Frequency Process. The HA-2546 has a voltage output with a 30MHz signal bandwidth, 300V/μs slew rate and a 17MHz control bandwidth. High bandwidth and slew rate make this part an ideal component for use in video systems. The suitability for precision video applications is demonstrated further by the 0.1dB gain flatness to 5MHz, 1.6% multiplication error, -52dB feedthrough and differential inputs with 1.2μA bias currents. The HA-2546 also has low differential gain (0.1%) and phase (0.1°) errors.

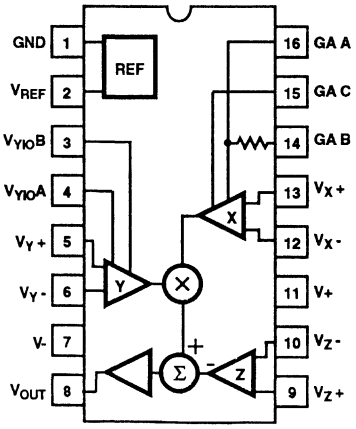
The HA-2546 is well suited for AGC circuits as well as mixer applications for sonar, radar, and medical imaging equipment. The voltage output simplifies many designs by eliminating the current to voltage conversion stage required for current output multipliers. For MIL-STD-883 compliant product, consult the HA-2546/883 datasheet.

Ordering Information

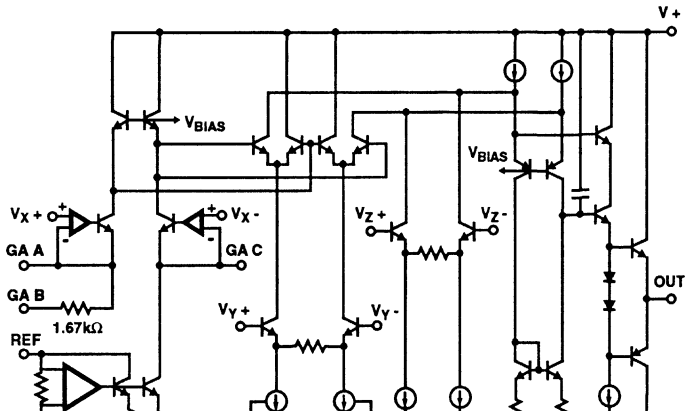
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-2546-5	0°C to +75°C	16 Lead Ceramic DIP
HA1-2546-9	-40°C to +85°C	16 Lead Ceramic DIP
HA3-2546-5	0°C to +75°C	16 Lead Plastic DIP
HA9P2546-5	0°C to +65°C	16 Lead Wide Body SOIC

Pinout

HA-2546 (PDIP, CDIP, 300mil SOIC)
TOP VIEW



Simplified Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2861.1**

Absolute Maximum Ratings

Voltage Between V+ and V- 35V
Differential Input Voltage 6V
Output Current ..... ±60mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Packages) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA1-2546-9 ..... $-40°C \le T_A \le +85°C$
HA3-2546-5 ..... $0°C \le T_A \le +75°C$
HA9P2546-5 ..... $0°C \le T_A \le +65°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	71°C/W	13°C/W
Plastic DIP Package	86°C/W	25°C/W
Wide Body SOIC Package	96°C/W	26°C/W

Maximum Package Power Dissipation
Ceramic DIP Package at 85°C ..... 1.27 W
Plastic DIP Package at 75°C ..... 0.87 W
Wide Body SOIC Package at 65°C ..... 0.88 W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = 15V, V- = -15V, R_L = 1kΩ, C_L = 50pF, Unless Otherwise Specified

PARAMETER	TEMP	ALL GRADES MIN	ALL GRADES TYP	ALL GRADES MAX	UNITS
MULTIPLIER PERFORMANCE					
Multiplication Error (Note 2)	+25°C	-	1.6	3	%
	Full	-	3.0	7	%
Multiplication Error Drift	Full	-	0.003	-	%/°C
Differential Gain (Note 3, 11)	+25°C	-	0.1	0.2	%
Differential Phase (Note 3, 11)	+25°C	-	0.1	0.3	Deg.
Gain Flatness (Note 6, 11)					
DC to 5 MHz	+25°C	-	0.1	0.2	dB
5 MHz to 8 MHz	+25°C	-	0.18	0.3	dB
Scale Factor Error	Full	-	0.7	5.0	%
1% Amplitude Bandwidth Error	+25°C	-	6	-	MHz
1% Vector Bandwidth Error	+25°C	-	260	-	kHz
THD + N (Note 4)	+25°C	-	0.03	-	%
Voltage Noise (Note 16)					
f_O = 10Hz	+25°C	-	400	-	$nV/\sqrt{Hz}$
f_O = 100Hz	+25°C	-	150	-	$nV/\sqrt{Hz}$
f_O = 1kHz	+25°C	-	75	-	$nV/\sqrt{Hz}$
Common Mode Range	+25°C	-	±9	-	V
SIGNAL INPUT, V_Y					
Input Offset Voltage	+25°C	-	3	10	mV
	Full	-	8	20	mV
Average Offset Voltage Drift	Full	-	45	-	µV/°C

Electrical Specifications V+ = 15V, V- = -15V, R_L = 1kΩ, C_L = 50pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	ALL GRADES			UNITS
		MIN	TYP	MAX	
Input Bias Current	+25°C	-	7	15	µA
	Full	-	10	15	µA
Input Offset Current	+25°C	-	0.7	2	µA
	Full	-	1.0	3	µA
Input Capacitance	+25°C	-	2.5	-	pF
Differential Input Resistance	+25°C	-	720	-	kΩ
Small Signal Bandwidth (-3dB) (Note 6)	+25°C	-	30	-	MHz
Full Power Bandwidth (Note 5)	+25°C	-	9.5	-	MHz
Feedthrough (Note 14)	+25°C	-	-52	-	dB
CMRR (Note 7)	Full	60	78	-	dB
V_Y TRANSIENT RESPONSE (Note 12)					
Slew Rate (Note 8)	+25°C	-	300	-	V/µs
Rise Time (Note 9)	+25°C	-	11	-	ns
Overshoot (Note 9)	+25°C	-	17	-	%
Propagation Delay	+25°C	-	25	-	ns
Settling Time (Note 8) 0.1%	+25°C	-	200	-	ns
CONTROL INPUT, V_X					
Input Offset Voltage	+25°C	-	0.3	2	mV
	Full	-	3	20	mV
Average Offset Voltage Drift	Full	-	10	-	µV/°C
Input Bias Current	+25°C	-	1.2	2	µA
	Full	-	1.8	5	µA
Input Offset Current	+25°C	-	0.3	2	µA
	Full	-	0.4	3	µA
Input Capacitance	+25°C	-	2.5	-	pF
Differential Input Resistance	+25°C	-	360	-	kΩ
Small Signal Bandwidth (-3dB) (Note 13)	+25°C	-	17	-	MHz
Feedthrough (Note 15)	+25°C	-	-40	-	dB
Common Mode Rejection Ratio (Note 18)	+25°C	-	80	-	dB
V_X TRANSIENT RESPONSE (Note 12)					
Slew Rate (Note 18)	+25°C	-	95	-	V/µs
Rise Time (Note 19)	+25°C	-	20	-	ns
Overshoot (Note 19)	+25°C	-	17	-	%

Electrical Specifications V+ = 15V, V- = -15V, R_L = 1kΩ, C_L = 50pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	ALL GRADES			UNITS
		MIN	TYP	MAX	
Propagation Delay	+25°C	-	50	-	ns
Settling Time (Note 18) 0.1%	+25°C	-	200	-	ns
V_Z CHARACTERISTICS					
Input Offset Voltage (Note 16)	+25°C	-	4	15	mV
	Full	-	8	20	mV
Open Loop Gain	+25°C	-	70	-	dB
Differential Input Resistance	+25°C	-	900	-	kΩ
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 17)	Full	-	±6.25	-	V
Output Current	Full	±20	±45	-	mA
Output Resistance	+25°C	-	1	-	Ω
POWER SUPPLY					
PSRR (Note 10)	Full	58	63	-	dB
Supply Current	Full	-	23	29	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Error is percent of full scale, 1% = 50mV.
3. f_O = 3.58MHz/4.43MHz, V_Y = 300mV_{P-P}, 0 to 1Vdc offset, V_X = 2V.
4. f_O = 10kHz, V_Y = 1V_{RMS}, V_X = 2V.
5. V_X = 2V, Full Power Bandwidth calculated by equation: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$, V_{PEAK} = 5V
6. V_X = 2V.
7. V_Y = 0 to ±5V, V_X = 2V.
8. V_{OUT} = ±5V, V_X = 2V.
9. V_{OUT} = 0 to ±100mV, V_X = 2V.
10. V_S = ±12V to ±15V, V_Y = 5V, V_X = 2V.
11. Guaranteed by characterization and not 100% tested.
12. See Test Circuit.
13. V_Y = 5V, V_{X^-} = -1V.
14. f_O = 5MHz, V_X = 0, V_Y = 200mV_{RMS}.
15. f_O = 100kHz, V_Y = 0, V_{X^+} = 200mV_{RMS}, V_{X^-} = -0.5V.
16. V_X = V_Y = 0.
17. V_X = 2.5V, V_Y = ±5V.
18. V_X = 0 to 2V, V_Y = 5V.
19. V_X = 0 to 200mV, V_Y = 5V.

Die Characteristics

DIE DIMENSIONS:
154.3 x 173.2 x 19 ± 1mils

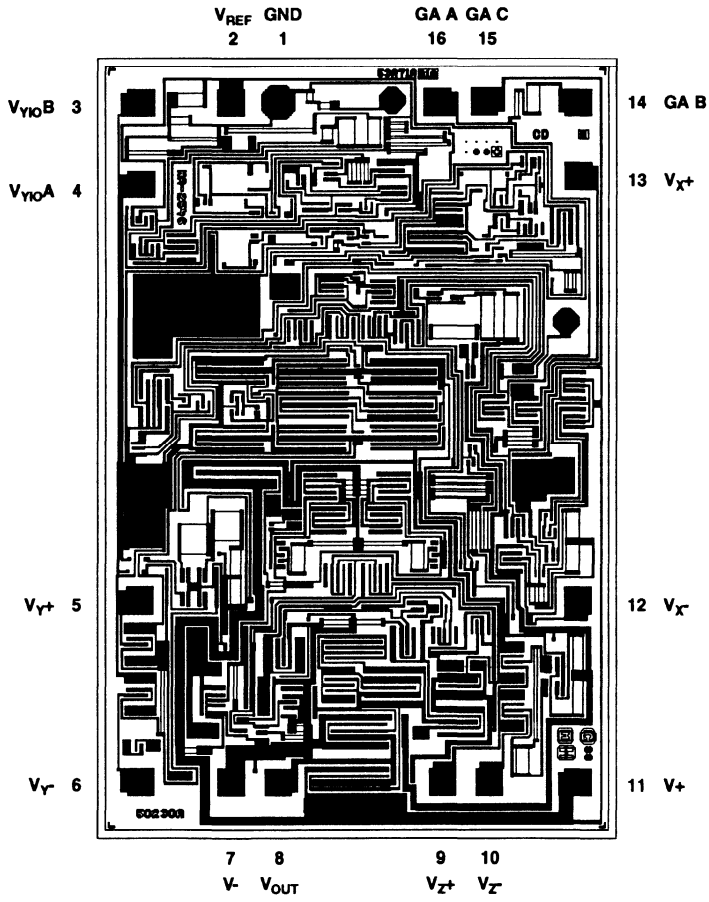
METALLIZATION:
Type: Al, 1% Cul
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos)
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 2kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP - 460°C (Max)

Metallization Mask Layout

HA-2546



Test Circuits

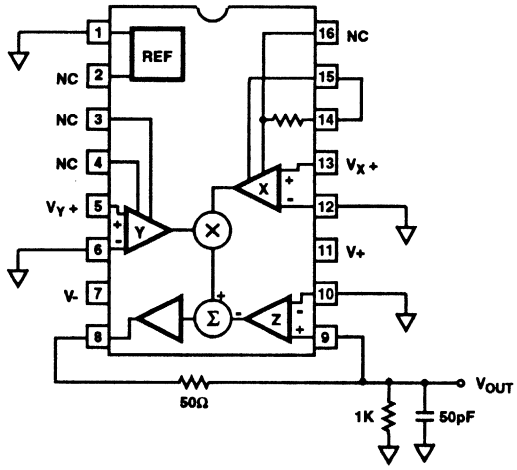
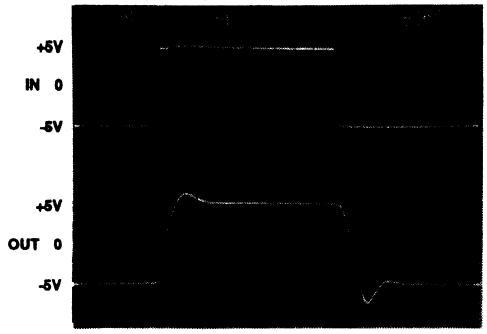
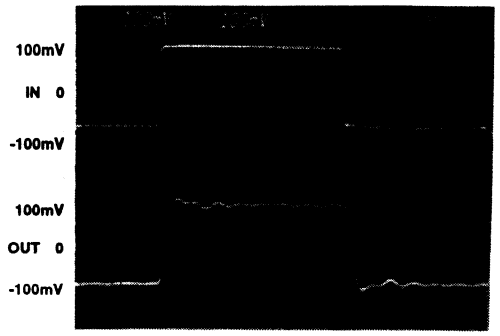


FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

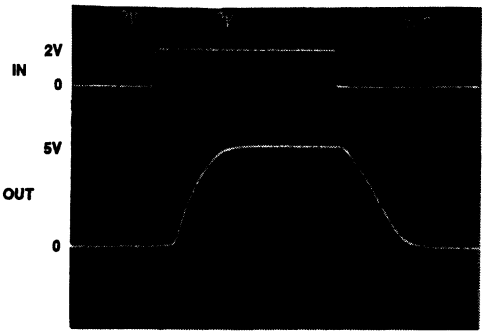
V_Y LARGE SIGNAL RESPONSE
Vertical Scale: 5V/Div. Horizontal Scale: 50ns/Div.



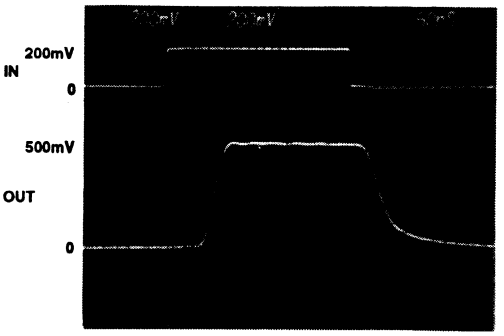
V_Y SMALL SIGNAL RESPONSE
Vertical Scale: 100mV/Div. Horizontal Scale: 50ns/Div.



V_X LARGE SIGNAL RESPONSE
Vertical Scale: 2V/Div. Horizontal Scale: 50ns/Div.



V_X SMALL SIGNAL RESPONSE
Vertical Scale: 200mV/Div. Horizontal Scale: 50ns/Div.



Typical Performance Curves

$V_S = \pm 15V$, $T_A = +25°C$, See Test Circuit For Multiplier Configuration

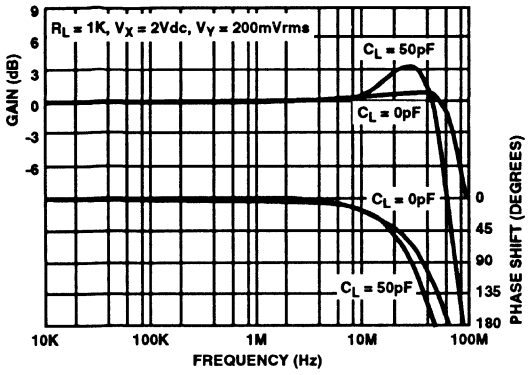


FIGURE 2. V_Y GAIN AND PHASE vs FREQUENCY

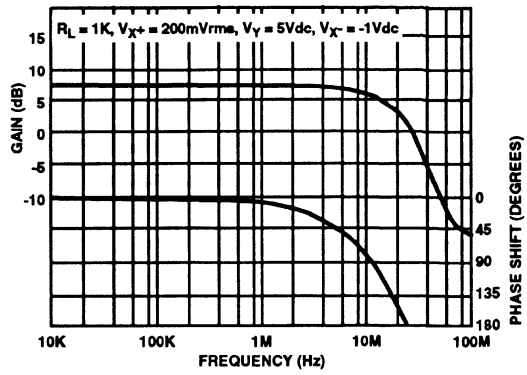


FIGURE 3. V_X GAIN AND PHASE vs FREQUENCY

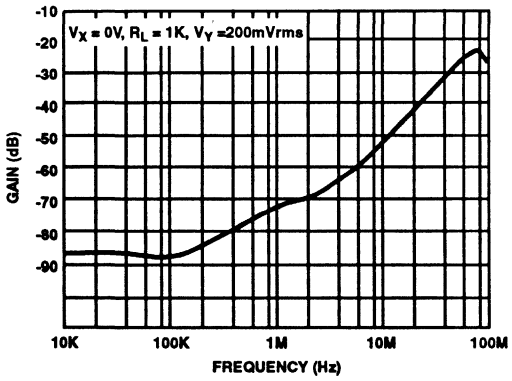


FIGURE 4. V_Y FEEDTHROUGH vs FREQUENCY

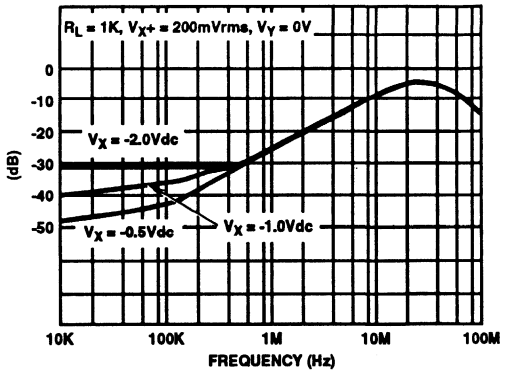


FIGURE 5. V_Y FEEDTHROUGH vs FREQUENCY

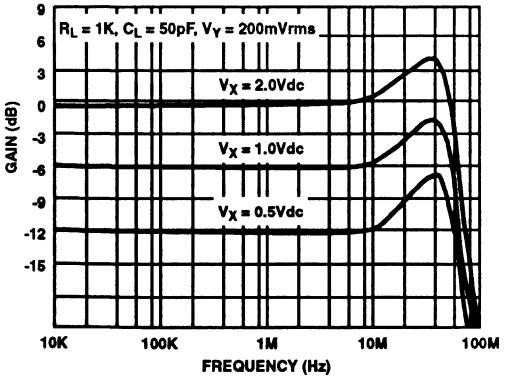


FIGURE 6. VARIOUS V_Y FREQUENCY RESPONSES

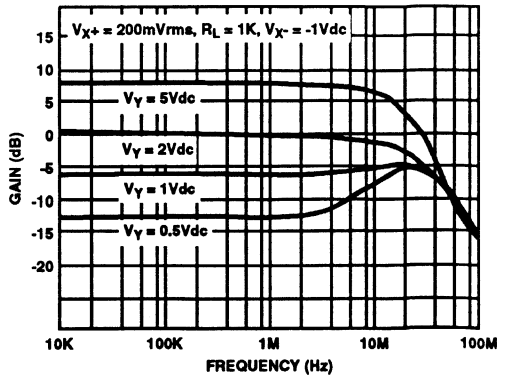


FIGURE 7. VARIOUS V_X FREQUENCY RESPONSES

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$, See Test Circuit For Multiplier Configuration (Continued)

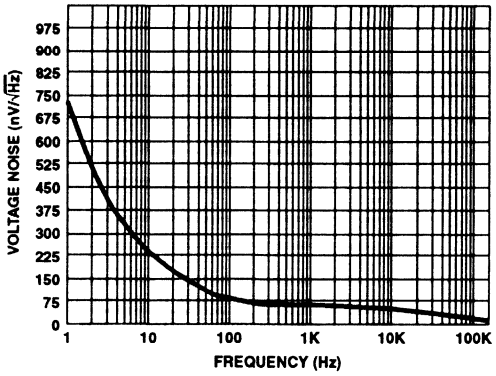


FIGURE 8. VOLTAGE NOISE DENSITY

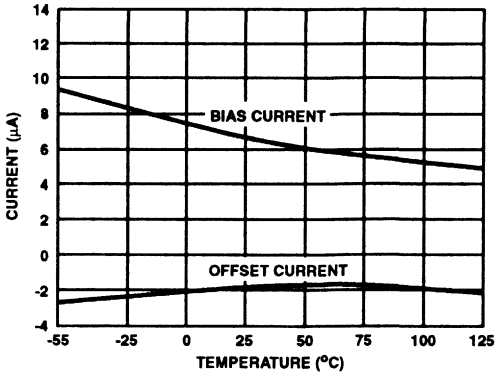


FIGURE 9. V_Y OFFSET AND BIAS CURRENT vs TEMPERATURE

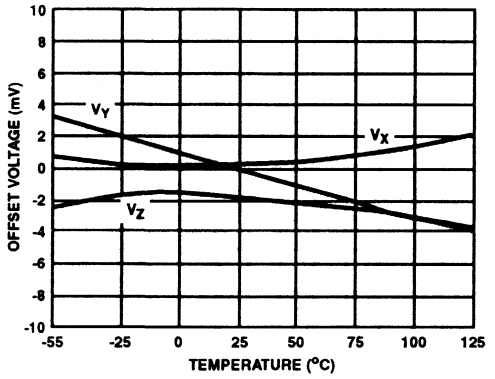


FIGURE 10. OFFSET VOLTAGE vs TEMPERATURE

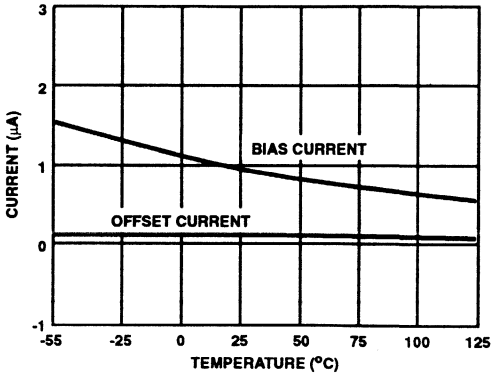


FIGURE 11. V_X OFFSET AND BIAS CURRENT vs TEMPERATURE

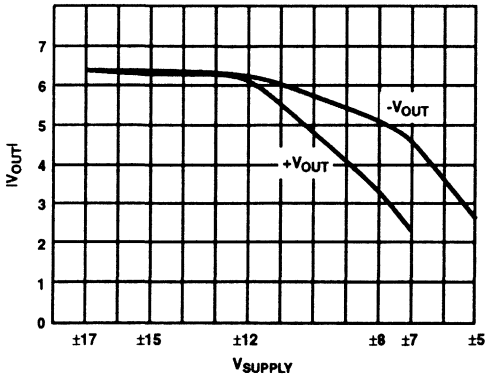


FIGURE 12. V_{OUT} vs V_{SUPPLY}

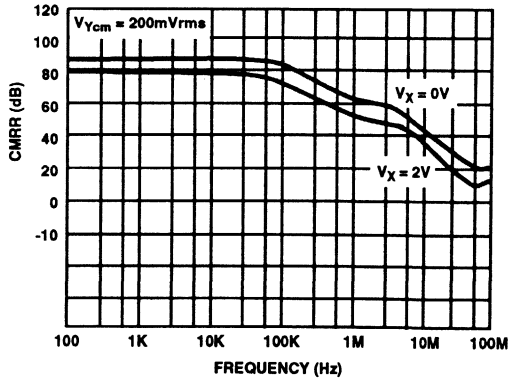


FIGURE 13. V_Y CMRR vs FREQUENCY

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$, See Test Circuit For Multiplier Configuration (Continued)

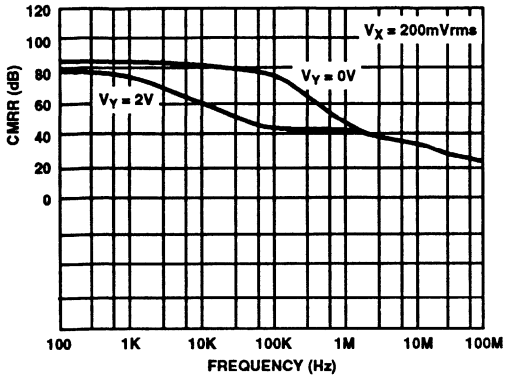


FIGURE 14. V_X COMMON MODE REJECTION RATIO vs FREQUENCY

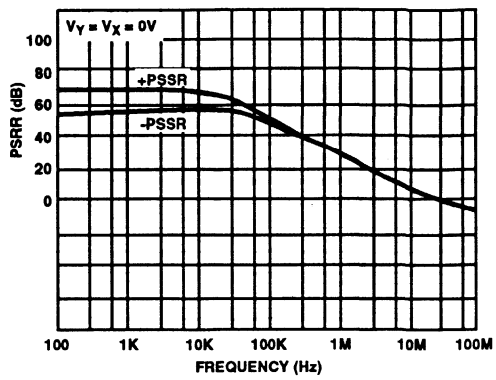


FIGURE 15. PSRR vs FREQUENCY

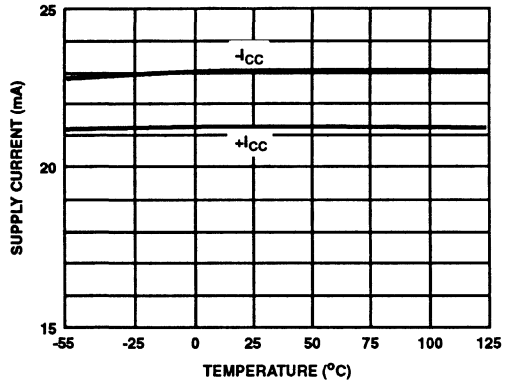


FIGURE 16. SUPPLY CURRENT vs TEMPERATURE

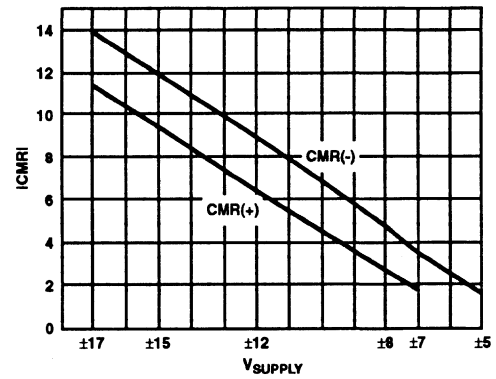


FIGURE 17. CMR vs V_{SUPPLY}

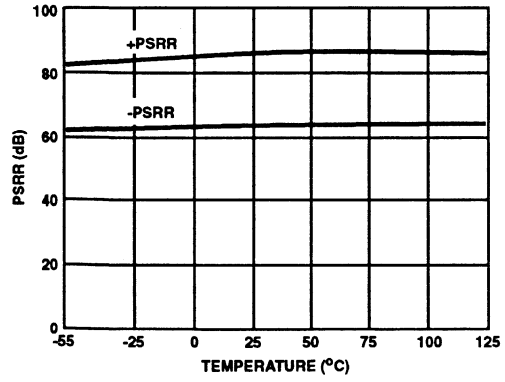


FIGURE 18. PSRR vs TEMPERATURE

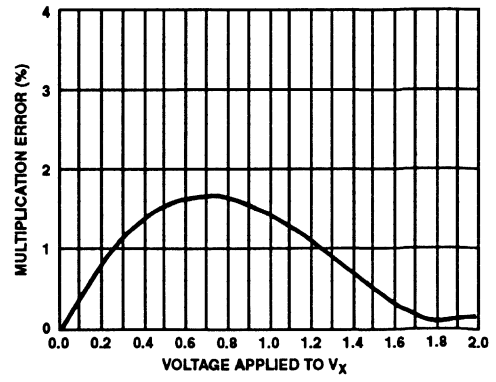


FIGURE 19. MULTIPLICATION ERROR vs V_X

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$, See Test Circuit For Multiplier Configuration (Continued)

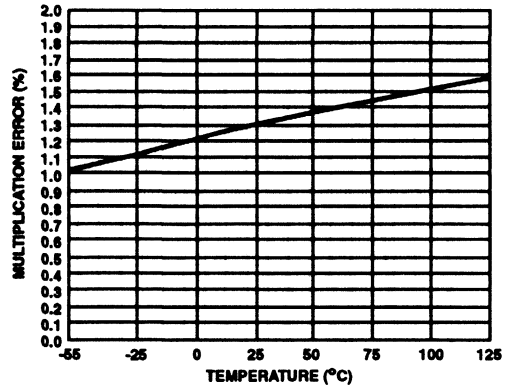


FIGURE 20. WORST CASE MULTIPLICATION ERROR vs TEMPERATURE

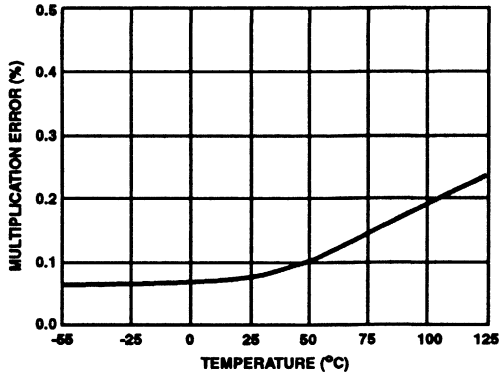


FIGURE 21. MULTIPLICATION ERROR vs TEMPERATURE

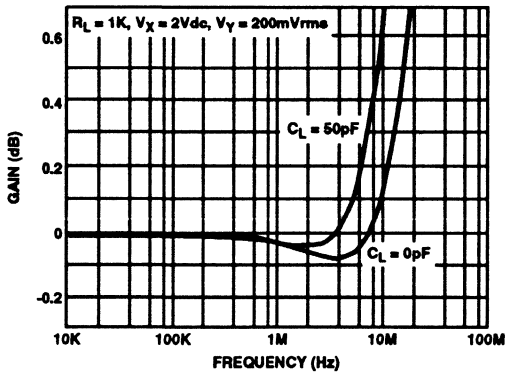


FIGURE 22. GAIN VARIATION vs FREQUENCY

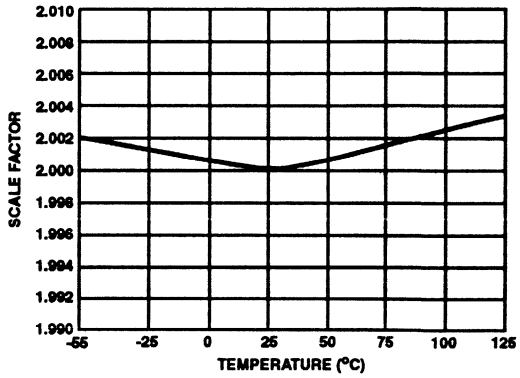


FIGURE 23. SCALE FACTOR vs TEMPERATURE

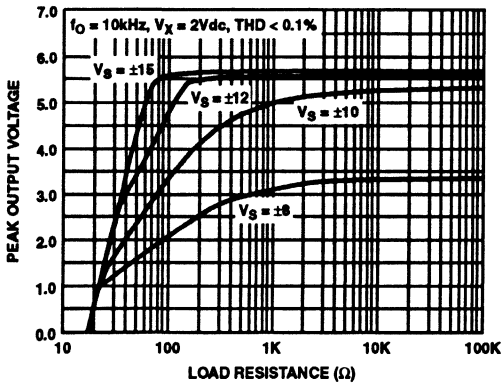


FIGURE 24. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

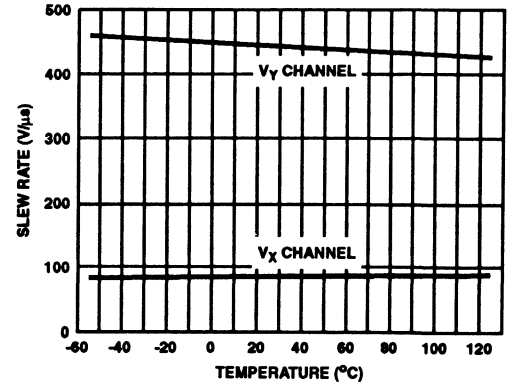


FIGURE 25. SLEW RATE vs TEMPERATURE

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$, See Test Circuit For Multiplier Configuration (Continued)

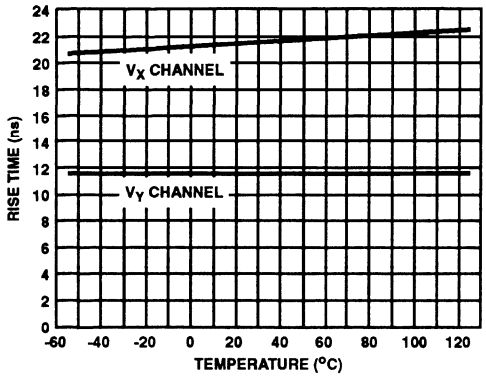


FIGURE 26. RISE TIME vs TEMPERATURE

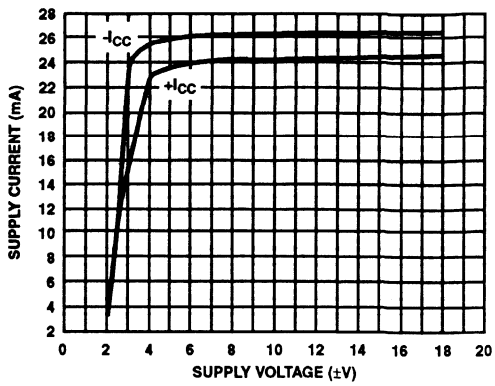


FIGURE 27. SUPPLY CURRENT vs SUPPLY VOLTAGE

Applications

Theory of Operation

The HA-2546 is a two quadrant multiplier with the following three differential inputs; the signal channel, V_{Y+} and V_{Y-}, the control channel, V_{X+} and V_{X-}, and the summed channel, V_{Z+} and V_{Z-}, to complete the feedback of the output amplifier. The differential voltages of channel X and Y are converted to differential currents. These currents are then multiplied in a circuit similar to a Gilbert Cell multiplier, producing a differential current product. The differential voltage of the Z channel is converted into a differential current which then sums with the products currents. The differential "product/sum" currents are converted to a single-ended current and then converted to a voltage output by a transimpedance amplifier.

The open loop transfer equation for the HA-2546 is:

$$V_{OUT} = A\left[\frac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-})}{SF} - (V_{Z+} - V_{Z-})\right]$$

where;

A = Output Amplifier Open Loop Gain

SF = Scale Factor

V_X, V_Y, V_Z = Differential Inputs

The scale factor is used to maintain the output of the multiplier within the normal operating range of ±5V. The scale factor can be defined by the user by way of an optional external resistor, R_{EXT}, and the Gain Adjust pins, Gain Adjust A (GA A), Gain Adjust B (GA B), and Gain Adjust C (GA C). The scale factor is determined as follows:

SF = 2, when GA B is shorted to GA C

SF ≅ 1.2 R_{EXT}, when R_{EXT} is connected between GA A and GA C (R_{EXT} is in kΩ)

SF ≅ 1.2 (R_{EXT} + 1.667kΩ), when R_{EXT} is connected to GA B and GA C (R_{EXT} is in kΩ)

The scale factor can be adjusted from 2 to 5. It should be noted that any adjustments to the scale factor will affect the AC performance of the control channel, V_X. The normal input operating range of V_X is equal to the scale factor voltage.

The typical multiplier configuration is shown in Figure 28. The ideal transfer function for this configuration is:

$$V_{OUT} = \begin{cases} \dfrac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-})}{2} + V_{Z-}, & \text{when } V_X \geq 0V \\ 0, & \text{when } V_X < 0V \end{cases}$$

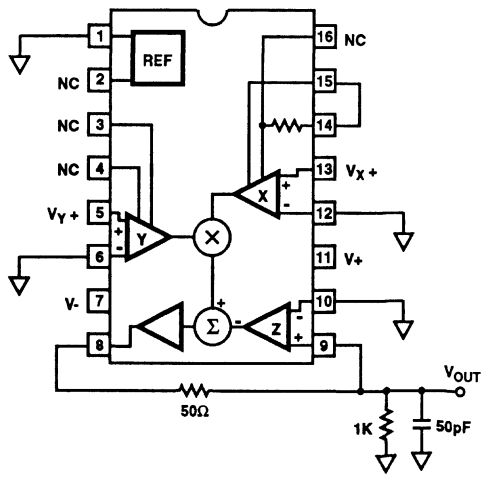


FIGURE 28

The V_{X-} pin is usually connected to ground so that when V_{X+} is negative there is no signal at the output, i.e. two quadrant operation. If the V_X input is a negative going signal the V_{X+} pin maybe grounded and the V_{X-} pin used as the control input.

The V_{Y-} terminal is usually grounded allowing the V_{Y+} to swing ±5V. The V_{Z+} terminal is usually connected directly to V_{OUT} to complete the feedback loop of the output amplifier while V_{Z-} is grounded. The scale factor is normally set to 2 by connecting GA B to GA C. Therefore the transfer equation simplifies to $V_{OUT} = (V_X V_Y) / 2$.

Offset Adjustment

The signal channel offset voltage may be nulled by using a 20kΩ potentiometer between V_{YIO} Adjust pins A and B and connecting the wiper to V-. Reducing the signal channel offset will reduce V_X AC feedthrough. Output offset voltage can also be nulled by connecting V_{Z-} to the wiper of a 20kΩ potentiometer which is tied between V+ and V-.

Capacitive Drive Capability

When driving capacitive loads > 20pF, a 50Ω resistor is recommended between V_{OUT} and V_{Z+}, using V_{Z+} as the output (See Figure 28). This will prevent the multiplier from going unstable.

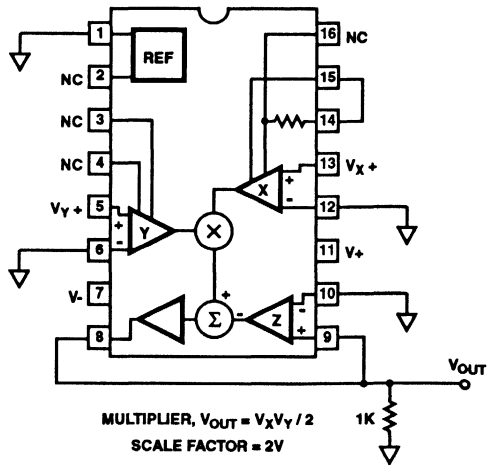
Power Supply Decoupling

Power supply decoupling is essential for high frequency circuits. A 0.01µF high quality ceramic capacitor at each supply pin in parallel with a 1µF tantalum capacitor will provide excellent decoupling. Chip capacitors produce the best results due to the close spacing with which they may be placed to the supply pins minimizing lead inductance.

Adjusting Scale Factor

The HA-2546 two quadrant multiplier may be configured for many uses. Following are examples of a few typical applications.

Adjusting the scale factor will tailor the control signal, V_X, input voltage range to match your needs. Referring to the simplified schematic on the front page and looking for the V_X input stage, you will notice the unusual design. The internal reference sets up a 1.2mA current sink for the V_X differential pair. The control signal applied to this input will be forced across the scale factor setting resistor and set the current flowing in the V_{X+} side of the differential pair. When the current through this resistor reaches 1.2mA, all the current available is flowing in the one side and full scale has been reached. Normally the 1.67kΩ internal resistor sets the scale factor to 2 volts when the Gain Adjust pins B and C are connected together, but you may set this resistor to any convenient value using pins 16 (GA A) and 15 (GA C).



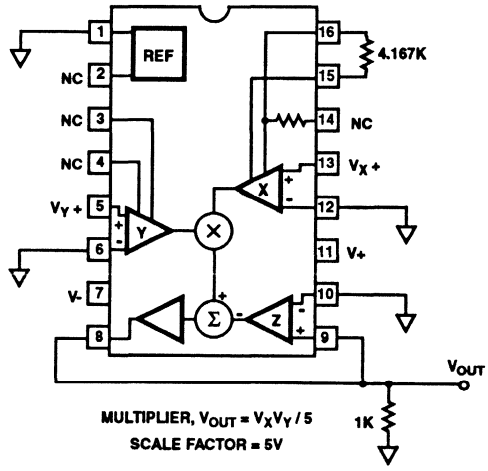


FIGURE 29

Example Application Circuits

In Figure 30 the HA-2546 is configured in a true Automatic Gain Control or AGC application. The HA-5127, low noise op amp, provides the gain control level to the X input. This level will set the peak output voltage of the multiplier to match the reference level. The feedback network around the HA-5127 provides stability and a response time adjustment for the gain control circuit.

This multiplier has the advantage over other AGC circuits, in that the signal bandwidth is not affected by the control signal gain adjustment.

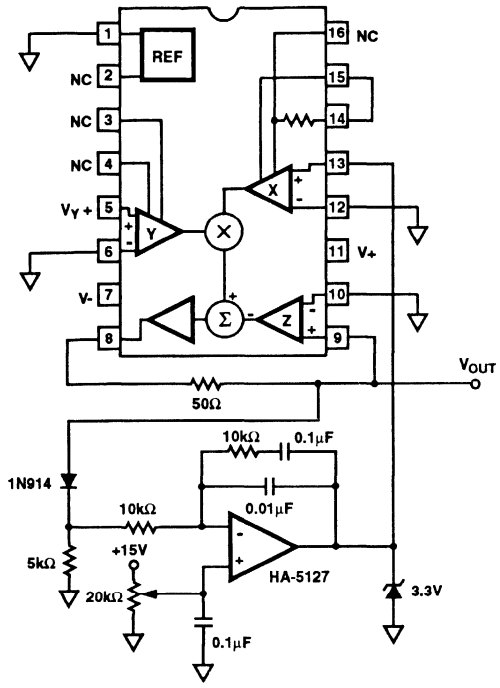
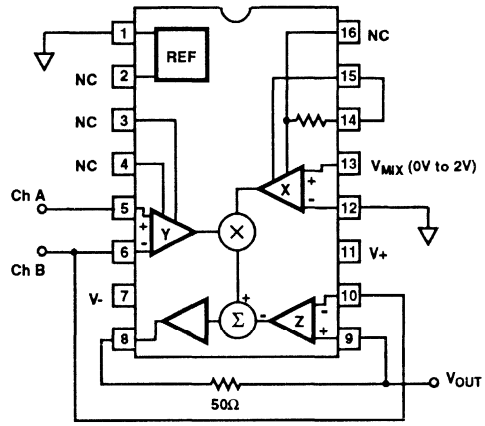


FIGURE 30. AUTOMATIC GAIN CONTROL

A wide range of gain adjustment is available with the Voltage Controlled Amplifier configuration shown in Figure 31. Here the gain of the HFA0002 is swept from 20V/V at a control voltage of 0.902V to a gain of almost 1000V/V with a control voltage of 0.03V.

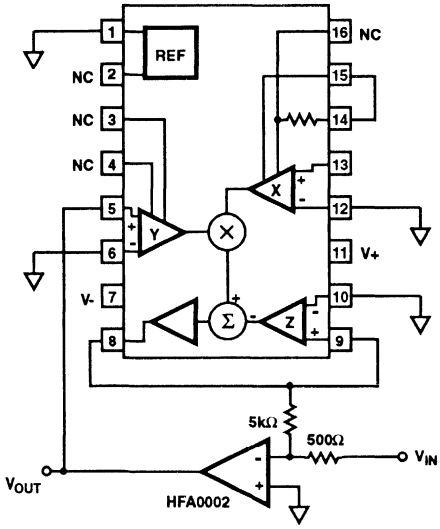
The Video Fader circuit provides a unique function. Here Ch B is applied to the minus Z input in addition to the minus Y input. In this way, the function in Figure 32 is generated. V_{MIX} will control the percentage of Ch A and Ch B that are mixed together to produce a resulting video image or other signal.

Many other applications are possible including division, squaring, square-root, percentage calculations, etc. Please refer to the HA-2556 four quadrant multiplier for additional applications.



V_{OUT} = Ch B + (Ch A - Ch B) V_{MIX} / Scale Factor
Scale Factor = 2
V_{OUT} = All Ch B; if V_{MIX} = 0V
V_{OUT} = All Ch A; if V_{MIX} = 2V (Full Scale)
V_{OUT} = Mix of Ch A and Ch B; if 0V < V_{MIX} < 2V

FIGURE 32. VIDEO FADER



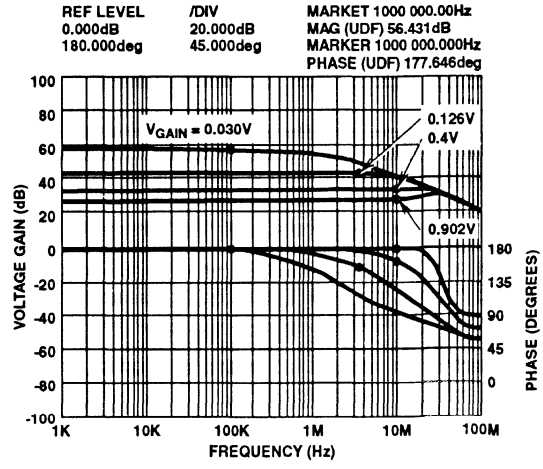


FIGURE 31. VOLTAGE CONTROLLED AMPLIFIER

HARRIS SEMICONDUCTOR

HA-2547

March 1993

Wideband Two Quadrant Analog Multiplier

Features

- Low Multiplication Error 1.6%
- Input Bias Currents 1.2μA
- Signal Input Feedthrough at 5MHz ..... -50dB
- Wide Signal Bandwidth 100MHz
- Wide Control Bandwidth 22MHz

Applications

- Military Avionics
- Missile Guidance Systems
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generator

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-2547-5	0°C to +75°C	16 Lead Ceramic DIP
HA1-2547-9	-40°C to +85°C	16 Lead Ceramic DIP

Description

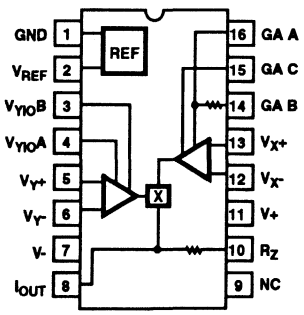
The HA-2547 is a monolithic, high speed, two quadrant, analog multiplier constructed in Harris' Dielectrically Isolated High Frequency Process. The high frequency performance of the HA-2547 rivals the best analog multipliers currently available including hybrids.

The single-ended current output of the HA-2547 has a 100MHz signal bandwidth (R_L = 50Ω) and a 22MHz control input bandwidth. High bandwidth and low distortion make this part an ideal component in video systems. The suitability for precision video applications is demonstrated further by low multiplication error (1.6%), low feedthrough (-50dB), and differential inputs with low bias currents (1.2μA). The HA-2547 is also well suited for mixer circuits as well as AGC applications for sonar, radar, and medical imaging equipment.

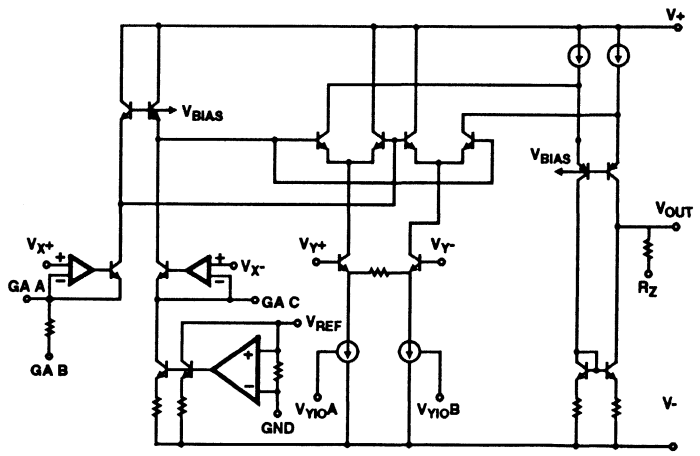
The current output of the HA-2547 allows it to achieve higher bandwidths than voltage output multipliers. An internal feedback resistor is provided to give an accurate current-to-voltage conversion and is trimmed to give a full scale output voltage of ±5V. The HA-2547 is not limited to multiplication applications only; frequency doubling and power detection are also possible.

Pinout

HA-2547 (CDIP)
TOP VIEW



Schematic



File Number 2862.1

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Output Current 3mA
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-2547-9 ..... $-40°C \le T_A \le +85°C$
HA-2547-5 ..... $0°C \le T_A \le +75°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V+ = +15V$, $V- = -15V$, R_Z (Pin 10) Grounded, Unless Otherwise Specified. Pin 14 connected to pin 15 for scale factor = 2.

PARAMETER	TEMP	ALL GRADES			UNITS
		MIN	TYP	MAX	
MULTIPLIER PERFORMANCE					
Multiplication Error (Note 2)	+25°C	-	1.6	3	%FS
	Full	-	3.0	7	%FS
Multiplication Error Drift	Full	-	0.003	-	%/°C
Scale Factor Error	Full	-	0.7	5	%
THD+N (Note 3)	+25°C	-	0.03	-	%
Output Offset Voltage (Note 4)	+25°C	-	6	15	mV
	Full	-	14	20	mV
Average Offset Voltage Drift	Full	-	-	-	µV/°C
SIGNAL INPUT, V_Y					
Input Offset Voltage	+25°C	-	4	10	mV
	Full	-	8	20	mV
Average Offset Voltage Drift	Full	-	35	-	µV/°C
Input Bias Current	+25°C	-	7	15	µA
	Full	-	10	15	µA
Input Offset Current	+25°C	-	0.7	2	µA
	Full	-	1.0	3	µA
Input Differential Resistance	+25°C	-	720	-	kΩ
Input Capacitance	+25°C	-	2.5	-	pF
Small Signal Bandwidth (-3dB) (Notes 5, 10)	+25°C	-	100	-	MHz
Feedthrough (Note 13)	+25°C	-	-50	-	dB
Differential Input Range	+25°C	±5	-	-	V
Common Mode Range	+25°C	-	±9	-	V
CMRR (Note 6)	Full	60	78	-	dB
V_Y TRANSIENT RESPONSE					
Rise Time (Note 15)	+25°C	-	5	-	ns
Propagation Delay	+25°C	-	3	-	ns
CONTROL INPUT, V_X					
Input Offset Voltage	+25°C	-	1	2	mV
	Full	-	2	20	mV
Average Offset Voltage Drift	Full	-	12	-	µV/°C
Input Bias Current	+25°C	-	1.2	2	µA
	Full	-	1.8	5	µA
Input Offset Current	+25°C	-	0.3	2	µA
	Full	-	0.4	3	µA
Input Capacitance	+25°C	-	2.5	-	pF

Electrical Specifications V+ = +15V, V- = -15V, R_Z (Pin 10) Grounded, Unless Otherwise Specified. Pin 14 connected to pin 15 for scale factor = 2. **(Continued)**

PARAMETER	TEMP	ALL GRADES MIN	ALL GRADES TYP	ALL GRADES MAX	UNITS
Input Differential Resistance	+25°C	-	360	-	kΩ
Small Signal Bandwidth (-3dB) (Notes 5, 10)	+25°C	-	22	-	MHz
Feedthrough (Note 14)	+25°C	-	-40	-	dB
Input Range (Note 12)	Full	+2	-	-	V
Common Mode Range	+25°C	-	±9	-	V
CMRR (Note 7)	+25°C	-	75	-	dB
V_X TRANSIENT RESPONSE					
Rise Time (Note 16)	+25°C	-	15	-	ns
Propagation Delay	+25°C	-	25	-	ns
OUTPUT CHARACTERISTICS					
Full Scale Output Voltage (Note 8)	Full	-	±6.25	-	V
Full Scale Output Current (Note 11)	+25°C	-	2	-	mA
Output Capacitance	+25°C	-	6.5	-	pF
Output Resistance	+25°C	-	4	-	MΩ
POWER SUPPLY					
PSRR (Note 9)	Full	58	63	-	dB
I_{CC}	Full	-	20	29	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Error is percent of full scale, 1% = 50mV.
3. f = 10kHz, $V_Y = 1V_{RMS}$, $V_X = 2V$.
4. $V_X = 0V$, $V_Y = 0V$.
5. $R_L = 50\Omega$.
6. $V_Y = 0$ to $\pm 5V$, $V_X = 2V$.
7. $V_X = 0$ to 2V, $V_Y = 5V$.
8. $V_Y = \pm 5$, $V_X = 2.5V$.
9. $V_S = \pm 12V$ to $\pm 15V$, $V_Y = 5V$, $V_X = 2V$.
10. Guaranteed by sample test and not 100% tested.
11. Output current tolerance is ±20%.
12. Scale Factor = 2. See Applications Information.
13. f = 5MHz, $V_X = 0$, $V_Y = 200mV_{RMS}$. Relative to full scale output.
14. f = 5MHz, $V_Y = 0$, $V_{X+} = 200mV_{RMS}$, $V_{X-} = -0.5V$. Relative to full scale output.
15. $V_Y = \pm 5V$, $V_X = 2V$, $R_L = 50\Omega$.
16. $V_X = 0$ to 2V, $V_Y = 5V$, $R_L = 50\Omega$.

Die Characteristics

Transistor Count 75
Die Dimensions ..... 79.9 x 119.7 x 19 mils (2030 x 3040 x 480µm)
Substrate Potential* ..... V-
Process ..... High Frequency, Bipolar, DI
Passivation ..... Nitride

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
HA1-2547	71	13

* The substrate maybe left floating (Insulating Die Mount) or it may be on a conductor at V- potential.

Test Circuits

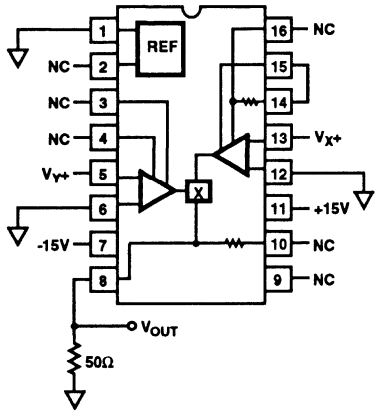
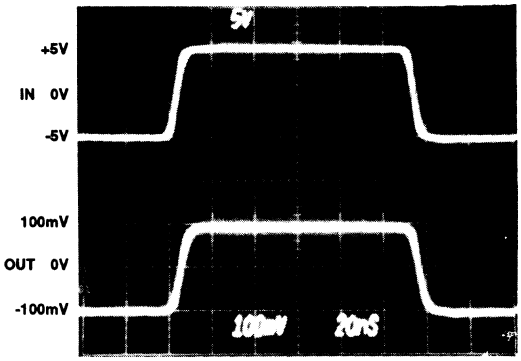
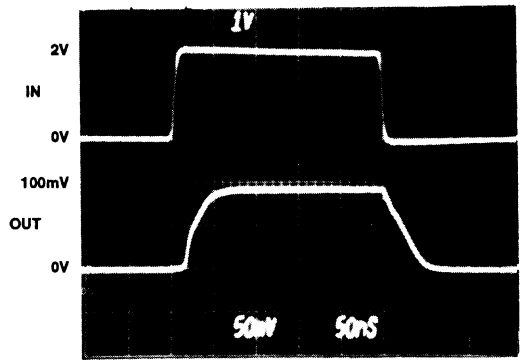


FIGURE 1. AC AND TRANSIENT RESPONSE TEST CIRCUIT

V_Y TRANSIENT RESPONSE
Vertical Scale: Top: 5V/Div Bottom: 100mV/Div
Horizontal Scale: 20ns/Div



V_X TRANSIENT RESPONSE
Vertical Scale: Top: 1V/Div Bottom: 50mV/Div
Horizontal Scale: 50ns/Div



Typical Performance Curves $V_S = \pm 15V, T_A = +25°C$

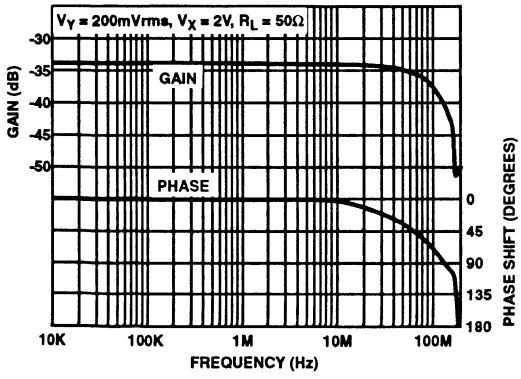


FIGURE 2. V_Y vs FREQUENCY

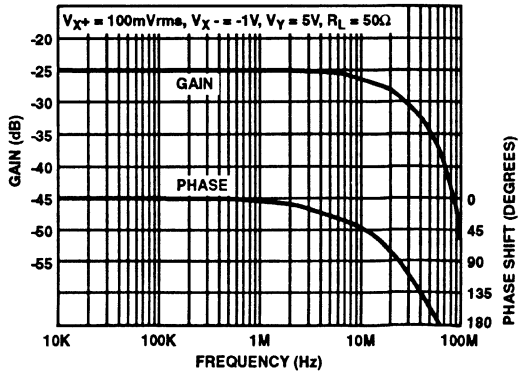


FIGURE 3. V_X vs FREQUENCY

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$ (Continued)

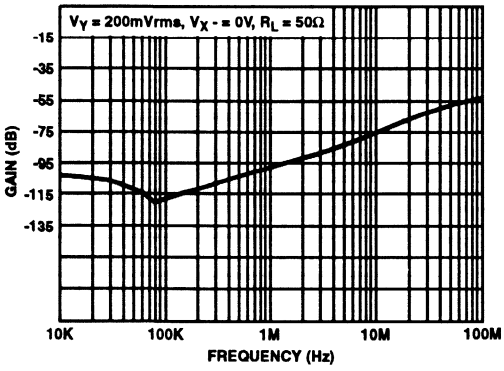


FIGURE 4. V_Y FEEDTHROUGH vs FREQUENCY

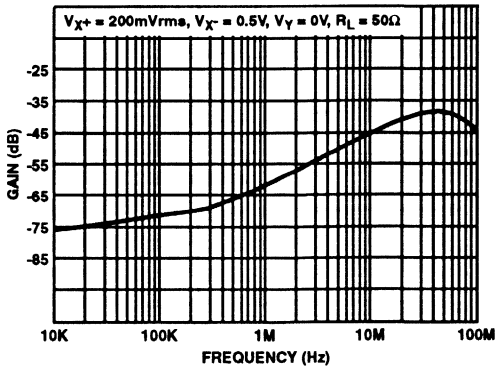


FIGURE 5. V_X FEEDTHROUGH vs FREQUENCY

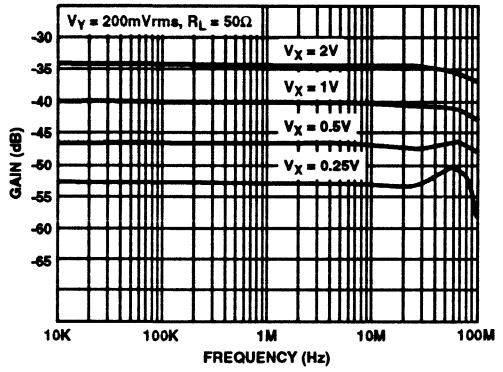


FIGURE 6. VARIOUS V_Y FREQUENCY RESPONSES

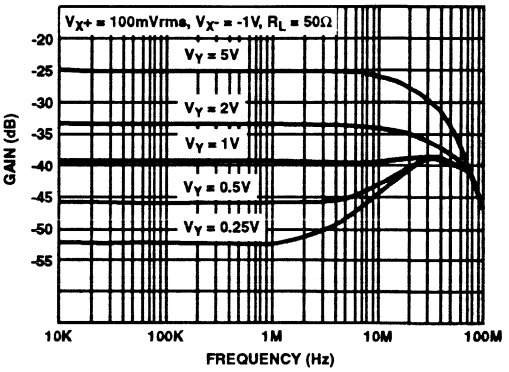


FIGURE 7. VARIOUS V_X FREQUENCY RESPONSES

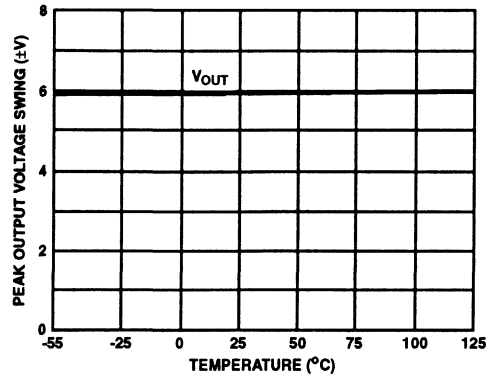


FIGURE 8. OUTPUT VOLTAGE SWING vs TEMPERATURE

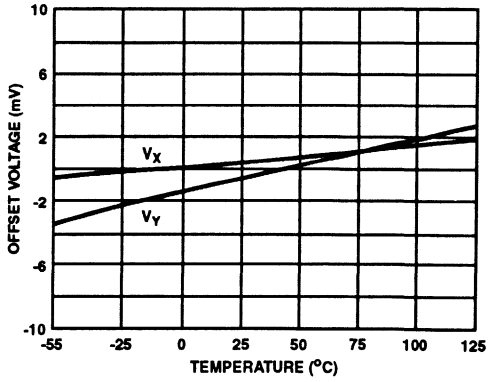


FIGURE 9. OFFSET VOLTAGE vs TEMPERATURE

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$ (Continued)

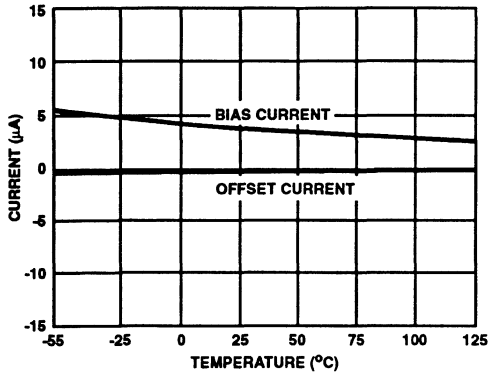


FIGURE 10. V_Y OFFSET/BIAS CURRENT vs TEMPERATURE

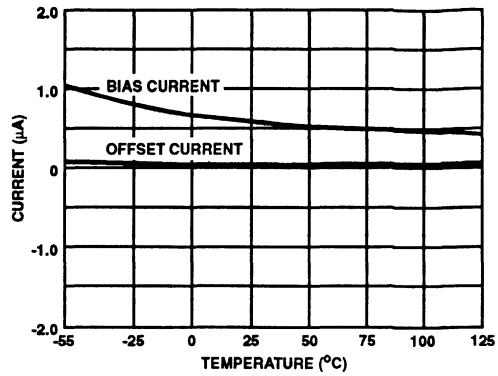


FIGURE 11. V_X OFFSET/BIAS CURRENT vs TEMPERATURE

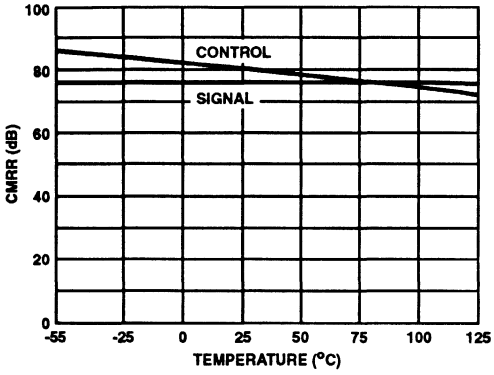


FIGURE 12. SIGNAL/CONTROL CMRR vs TEMPERATURE

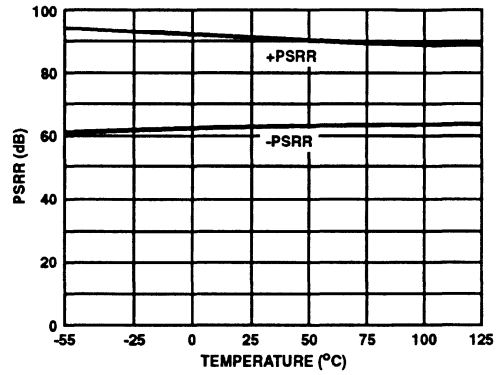


FIGURE 13. PSRR vs TEMPERATURE

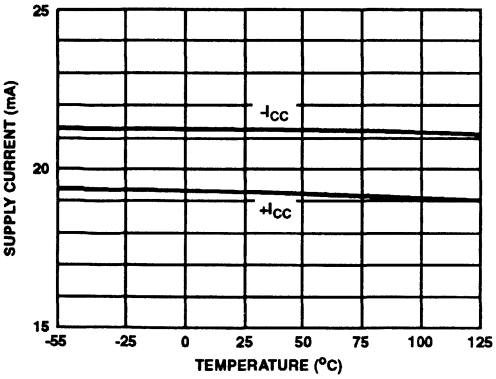


FIGURE 14. I_{CC} vs TEMPERATURE

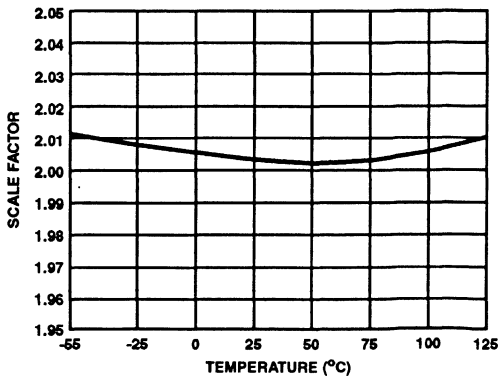


FIGURE 15. SCALE FACTOR vs TEMPERATURE

Typical Performance Curves $V_S = \pm15V$, $T_A = +25°C$ (Continued)

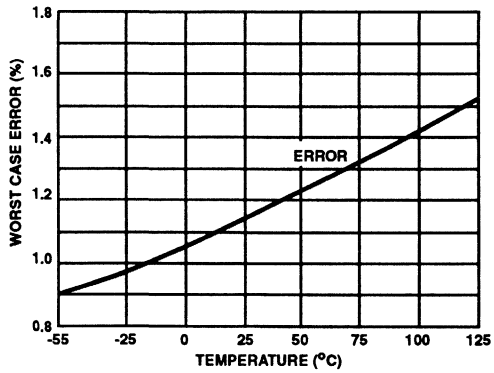


FIGURE 16. WORST CASE MULTIPLICATION ERROR vs TEMPERATURE

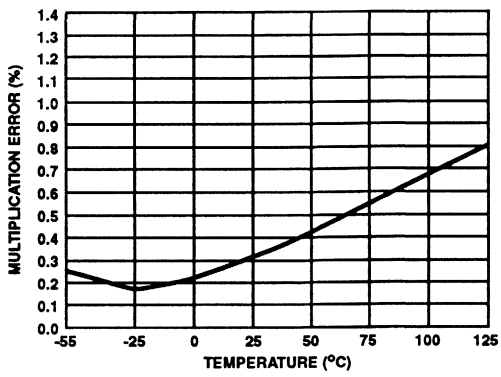


FIGURE 17. MULTIPLICATION ERROR vs TEMPERATURE

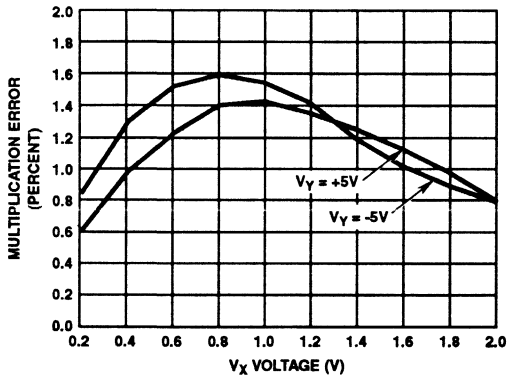


FIGURE 18. MULTIPLICATION ERROR vs V_X

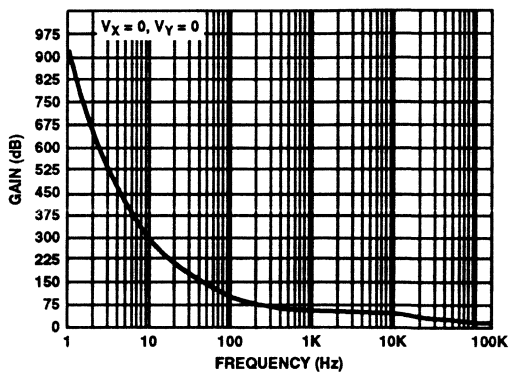


FIGURE 19. VOLTAGE NOISE DENSITY

Applications Information

Theory of Operation

The HA-2547 is a current output, two quadrant multiplier with one differential signal channel, V_Y+ and V_Y-, and one differential control channel, V_X+ and V_X-. Figure 20 shows a detailed functional block diagram of the HA-2547. The differential voltages of channels V_X and V_Y are converted to differential currents. These differential currents are then multiplied in a circuit similar to a Gilbert Cell multiplier, producing a differential current product. The differential product currents are then converted to a single-ended output current which is typically 2mA, ±20% at full scale (V_X = 2V, V_Y = ±5V). A trimmed internal scaling resistor, R_Z, is designed to convert the output current to an accurate voltage by grounding R_Z (pin 10). R_Z is trimmed such that at full scale output current the voltage drop across R_Z will be ±5.0V.

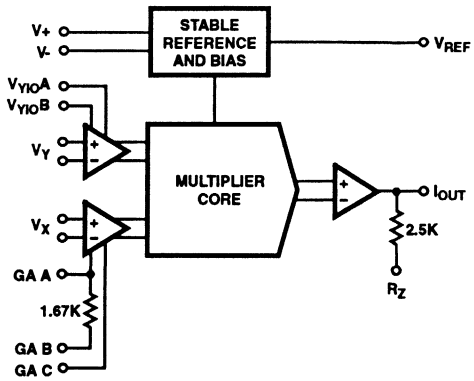


FIGURE 20.

The transfer equation for the HA-2547 is:

$$I_{OUT} = \frac{V_{OUT}}{R_Z} = \frac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-})}{SF \bullet R_Z}, \text{ where}$$

SF = Scale Factor

R_Z = 2.5kV (Internal)

V_X, V_Y = Differential Inputs

The scale factor is used to maintain the output of the multiplier within the normal operating range of ±5V. The scale factor can be defined by the user by way of an optional external resistor, R_{EXT}, and the Gain Adjust pins: Gain Adjust A (GA A), Gain Adjust B (GA B), and Gain Adjust C (GA C). The scale factor is determined as follows:

SF = 2, when GA B is shorted to GA C

SF ≈ (1.2)(R_{EXT}), when R_{EXT} is connected between GA A and GA C (R_{EXT} is in kΩ)

SF ≈ (1.2)(R_{EXT} + 1.667kΩ), when R_{EXT} is connected to GA B and GA C (R_{EXT} is in kΩ).

The scale factor can be adjusted from 2 to 5. It should be noted that any adjustments to the scale factor will affect the AC performance of the control channel, V_X. The normal input operating range of V_X is equal to the scale factor value.

A typical multiplier configuration is shown in Figure 21. The ideal transfer function for this configuration is shown below, illustrating two quadrant operation:

$$V_{OUT} = \frac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-})}{2},$$

when $(V_{X+} - V_{X-}) \geq 0$

V_{OUT} = 0, when $(V_{X+} - V_{X-}) < 0$

The V_{X-} pin is usually connected to ground so that when V_{X+} is negative there is no signal at the output, i.e. two quadrant operation. If the V_X input is a negative going signal the V_{X+} pin maybe grounded and the V_{X-} pin used as the input. The V_{Y-} terminal is usually grounded allowing V_{Y+} to swing ±5V.

R_Z is normally used as a feedback resistor for an external op amp to provide an accurate current-to-voltage conversion. The scale factor is normally set to 2 by connecting GA B to GA C. Therefore, the transfer function becomes:

$$V_{OUT} = \frac{(V_{X+})(V_{Y+})}{2}$$

The multiplication error is trimmed to be minimum at full scale, V_X = 2V and V_Y = ±5V. When V_Y = ±5V, the worst case multiplication error occurs when V_X ≈ 0.8V (Refer to typical performance curves).

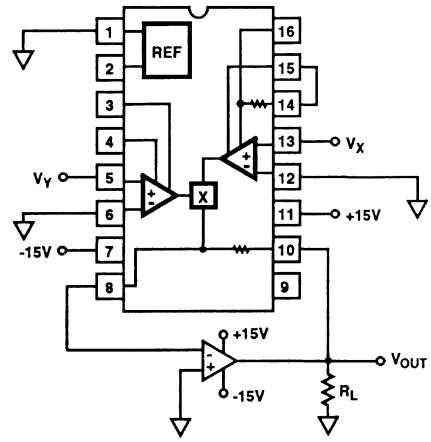


FIGURE 21.

Operation At Various Supply Voltages

The HA-2547 will operate over a range of supply voltages, ±8V to ±15V. Use of supply voltages below ±12V will cause degradation of electrical parameters.

Offset Adjustment

The signal channel offset voltage may be nulled by using a 20K potentiometer between V_{YIO} Adjust pins A and B and connecting the wiper to V-. Reducing the signal channel offset voltage will reduce V_X AC feedthrough and improve the multiplication error.

HARRIS SEMICONDUCTOR

HA-2556

PRELIMINARY

March 1993

Wideband Four Quadrant Voltage Output Analog Multiplier

Features

- High Speed Voltage Output 420V/μs
- Low Multiplication Error 1.5%
- Input Bias Currents 8μA
- 5MHz Feedthrough ..... -50dB
- Wide X and Y Channel Bandwidth 65MHz
- V_Y 0.2dB Gain Flatness 8.5MHz

Applications

- Military Avionics
- Missile Guidance Systems
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generator

Description

The HA-2556 is a monolithic, high speed, four quadrant, analog multiplier constructed in the Harris Dielectrically Isolated High Frequency Process. The high frequency performance of the HA-2556 rivals the best analog multipliers currently available including hybrids.

The HA-2556 has a voltage output X and Y channel bandwidth of 65MHz, and a 420V/μs slew rate. High bandwidth and slew rate make this part an ideal component for use in video systems. The suitability for precision video applications is demonstrated further by the 0.2dB gain flatness to 8.5MHz, 1.5% multiplication error, -50dB feedthrough and differential inputs with 8μA bias currents. The HA-2556 also has low differential gain (0.1%) and phase (0.1°) errors.

The HA-2556 is well suited for AGC circuits as well as mixer applications for sonar, radar, and medical imaging equipment. The voltage output of the HA-2556 simplifies many designs by eliminating the current-to-voltage conversion stage required for current output multipliers.

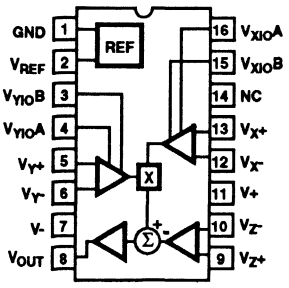
For MIL-STD-883 compliant product consult the HA-2556/883 datasheet.

Ordering Information

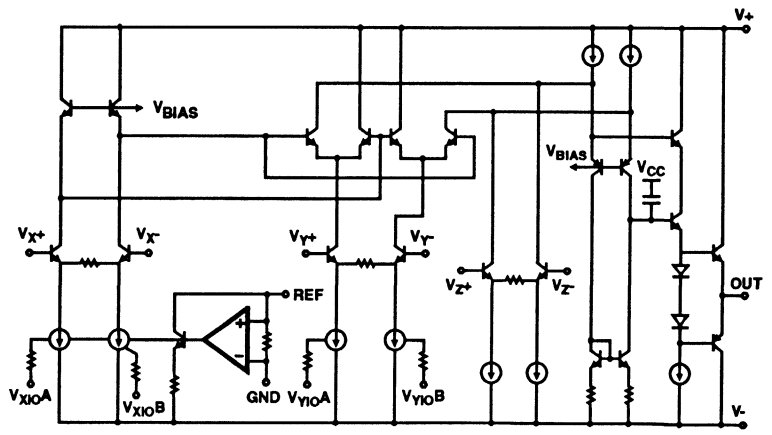
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA3-2556-9	-40°C to +85°C	16 Lead Plastic DIP
HA9P2556-9	-40°C to +85°C	16 Lead SOIC
HA1-2556-9	-40°C to +85°C	16 Lead Ceramic DIP

Pinout

HA-2556
(PDIP, CDIP, 300mil SOIC)
TOP VIEW



Simplified Schematic



Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Output Current ..... ±60mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Packages) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HA-2556-9 ..... $-40°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = 15V, V- = -15V, R_L = 1K, C_L = 20pF, Unless Otherwise Specified

PARAMETER	TEMP	HA-2556-9 MIN	HA-2556-9 TYP	HA-2556-9 MAX	UNITS
MULTIPLIER PERFORMANCE					
Multiplication Error (Note 2)	+25°C	-	1.5	3	%
	Full	-	3.0	6	%
Multiplication Error Drift	Full	-	0.003	-	%/°C
Linearity Error (V_X, V_Y = ±3V)	+25°C	-	0.02	-	%
Linearity Error (V_X, V_Y = ±4V)	+25°C	-	0.05	0.25	%
Linearity Error (V_X, V_Y = ±5V)	+25°C	-	0.2	0.5	%
Differential Gain (Note 3, 8)	+25°C	-	0.1	0.2	%
Differential Phase (Note 3, 8)	+25°C	-	0.1	0.3	Deg.
V_Y 0.2dB Gain Flatness (Note 8)	+25°C	-	8.5	-	MHz
V_X 0.2dB Gain Flatness (Note 8)	+25°C	-	7.0	-	MHz
Scale Factor	+25°C	-	5	-	V
THD + N (Note 4)	+25°C	-	0.03	-	%
Voltage Noise (Note 9)					
f =10Hz	+25°C	-	400	-	$nV/\sqrt{Hz}$
f =100Hz	+25°C	-	150	-	$nV/\sqrt{Hz}$
f =1kHz	+25°C	-	75	-	$nV/\sqrt{Hz}$
SIGNAL INPUT, V_X, V_Y, V_Z					
Input Offset Voltage	+25°C	-	3	10	mV
	Full	-	8	20	mV
Average Offset Voltage Drift	Full	-	45	-	µV/°C
Input Bias Current	+25°C	-	8	15	µA
	Full	-	12	20	µA
Input Offset Current	+25°C	-	0.5	2	µA
	Full	-	1.0	3	µA
Differential Input Resistance	+25°C	-	500	-	MΩ
5MHz Feedthrough	+25°C	-	-50	-	dB
Differential Input Range	+25°C	±5	-	-	V

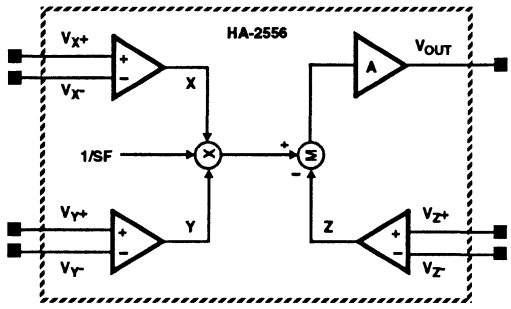
Electrical Specifications V+ = 15V, V- = -15V, R_L = 1K, C_L = 20pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	HA-2556-9			UNITS
		MIN	TYP	MAX	
Common Mode Range (V_X)	+25°C	-	±10	-	V
Common Mode Range (V_Y)	+25°C	-	+9, -10	-	V
CMRR (Within Common Mode Range)	Full	65	78	-	dB
V_X, V_Y, V_Z TRANSIENT RESPONSE					
Slew Rate (Note 5)	+25°C	-	420	-	V/µs
Rise Time (Note 6)	+25°C	-	8	-	ns
Overshoot (Note 6)	+25°C	-	17	-	%
Settling Time (Note 5) 0.1%	+25°C	-	100	-	ns
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 10)	Full	-	±6.05	-	V
Output Current	Full	±20	±45	-	mA
Output Resistance	+25°C	-	1	-	Ω
Small Signal Bandwidth (-3dB)	+25°C	-	65	-	MHz
Full Power Bandwidth (-3dB) ($10V_{P-P}$)	+25°C	-	32	-	MHz
POWER SUPPLY					
+PSRR (Note 7)	Full	-	65	-	dB
-PSRR (Note 7)	Full	-	45	-	dB
Supply Current	Full	-	18	22	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Error is percent of full scale, 1% = 50mV.
3. f = 4.43MHz, $V_Y = 300mV_{P-P}$, 0 to 1Vdc offset, V_X = 5V.
4. f = 10kHz, $V_Y = 1V_{RMS}$, V_X = 5V.
5. V_{OUT} = 0 to ±4V.
6. V_{OUT} = 0 to ± 100mV.
7. V_S = ±12V to ±15V.
8. Guaranteed by characterization and not 100% tested.
9. $V_X = V_Y = 0$.
10. V_X = 5.5V, V_Y = ±5.5

Functional Block Diagram



The transfer equation for the HA-2556 is:
$(V_{X+} - V_{X-})(V_{Y+} - V_{Y-}) = SF(V_{Z+} - V_{Z-})$,
where SF = Scale Factor = 5V V_X, V_Y, V_Z = Differential Inputs.

Applications Information

Operation at Reduced Supply Voltages

The HA-2556 will operate over a range of supply voltages, ±5V to ±15V. Use of supply voltages below ±12V will cause degradation of electrical parameters.

Offset Adjustment

The channel offset voltage may be nulled by using a 20K potentiometer between the V_{YIO} or V_{XIO} adjust pin A and B and connecting the wiper to V-. Reducing the channel offset voltage will reduce AC feedthrough and improve the multiplication error. Output offset voltage can also be nulled by connecting V_{Z-} to the wiper of a potentiometer which is tied between V+ and V-.

Capacitive Drive Capability

When driving capacitive loads >20pF a 50Ω resistor should be connected between V_{OUT} and V_{Z+}, using V_{Z+} as the output (see Figure 1). This will prevent the multiplier from going unstable due to the pole created by the load capacitor and reduce gain peaking at high frequencies.

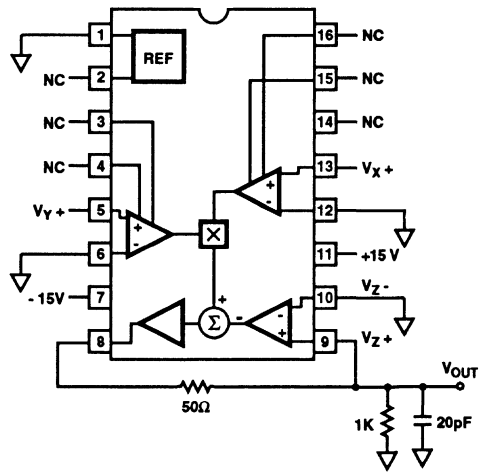


FIGURE 1.

HARRIS SEMICONDUCTOR

HA-2557

Wideband Four Quadrant Current Output Analog Multiplier

March 1993

Features

- Low Multiplication Error 1.5%
- Input Bias Currents 8μA
- Y Input Feedthrough @ 5MHz ..... -50dB
- Wide X and Y Channel Bandwidth 100MHz

Applications

- Military Avionics
- Missile Guidance Systems
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generator

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA3-2557-9	-40°C to +85°C	16 Lead Plastic DIP
HA9P2557-9	-40°C to +85°C	16 Lead Widebody SOIC
HA1-2557-9	-40°C to +85°C	16 Lead Ceramic DIP

Description

The HA-2557 is a monolithic, high speed, four quadrant, analog multiplier constructed in Harris' Dielectrically Isolated High Frequency Process. The high frequency performance of the HA-2557 rivals the best analog multipliers currently available including hybrids.

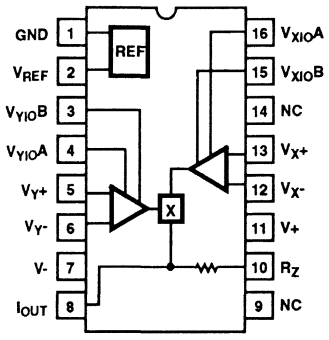
The single-ended current output of the HA-2557 has a 100MHz signal bandwidth (R_L = 50Ω). High bandwidth and low distortion make this part an ideal component in video systems. The suitability for precision video applications is demonstrated further by low multiplication error (1.5%), low feedthrough (-50dB), and differential inputs with low bias currents (8μA). The HA-2557 is also well suited for mixer circuits as well as AGC applications for sonar, radar, and medical imaging equipment.

The current output of the HA-2557 allows it to achieve higher bandwidths than voltage output multipliers. Full scale output current is trimmed to 1.6mA. An internal 2500Ω feedback resistor is also provided to accurately convert the current, if desired, to a full scale output voltage of ±4V. The HA-2557 is not limited to multiplication applications only; frequency doubling and power detection are also possible.

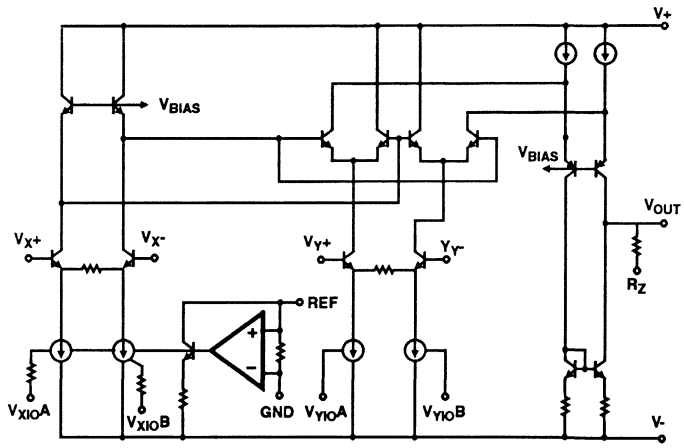
For MIL-STD-883 compliant product consult the HA-2557/883 datasheet.

Pinout

HA-2557
(PDIP, CDIP, 300mil SOIC)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2478.3

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage. 6V
Output Current 3mA
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Packages) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Operating Temperature Range
HA-2557-9 . . . . . $-40°C \le T_A \le +85°C$
Storage Temperature Range . . . . . $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified

PARAMETER	TEMP	HA-2557-9 MIN	HA-2557-9 TYP	HA-2557-9 MAX	UNITS
MULTIPLIER PERFORMANCE					
Multiplication Error (Note 2)	+25°C	-	1.5	3	%FS
	Full	-	3.0	6	%FS
Multiplication Error Drift	Full	-	0.003	-	%/°C
Linearity (V_X, V_Y = ±4V)	+25°C	-	0.1	0.25	%
Scale Factor	+25°C	-	10	-	kV-Ω
THD+N (Note 3)	+25°C	-	0.03	-	%
Output Offset Current	+25°C	-	2.4	6	µA
	Full	-	5.6	8	µA
V_X, V_Y					
Input Offset Voltage	+25°C	-	4	15	mV
	Full	-	8	20	mV
Average Offset Voltage Drift	Full	-	35	-	µV/°C
Input Bias Current	+25°C	-	8	15	µA
	Full	-	12	25	µA
Input Offset Current	+25°C	-	0.5	2	µA
	Full	-	1.0	3	µA
Differential Input Resistance	+25°C	-	720	-	kΩ
Small Signal Bandwidth (-3dB) (Note 5)	+25°C	-	100	-	MHz
Y Input Feedthrough (Note 8)	+25°C	-	-50	-	dB
Differential Input Range	+25°C	±4	-	-	V
Common Mode Range	+25°C	-	±9	-	V
CMRR (Note 6)	Full	65	78	-	dB
V_X, V_Y TRANSIENT RESPONSE (Note 5)					
Rise Time	+25°C	-	5	-	ns
Propagation Delay	+25°C	-	3	-	ns
OUTPUT CHARACTERISTICS					
Full Scale Output Compliance Voltage	Full	-	4	-	V
Full Scale Output Current	+25°C	-	1.6	-	mA
Internal Resistor (R_Z)	+25°C	-	2500	-	Ω
Output Resistance (±10V)	+25°C	1.0	1.5	-	MΩ

Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	HA-2557-9			UNITS
		MIN	TYP	MAX	
Output Capacitance	+25°C	-	6.5	-	pF
POWER SUPPLY					
+PSRR (Note 7)	Full	65	80	-	dB
-PSRR (Note 7) (-)	Full	45	55	-	dB
I_{CC}	Full	-	13	17	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the servicability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Error is percent of full scale, 1% = 16µA.
3. f = 10kHz, V_Y = 1V_{RMS}, V_X = 4V.
4. V_X = 0V, V_Y = 0V.
5. R_L = 50Ω.
6. V_{CM} = 0 to ±9V.
7. V_S = ±12V to ±17V.
8. f = 5MHz. Relative to full scale output.

Test Circuits

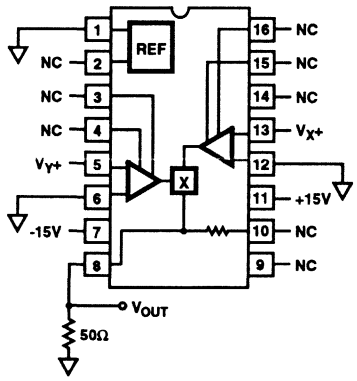
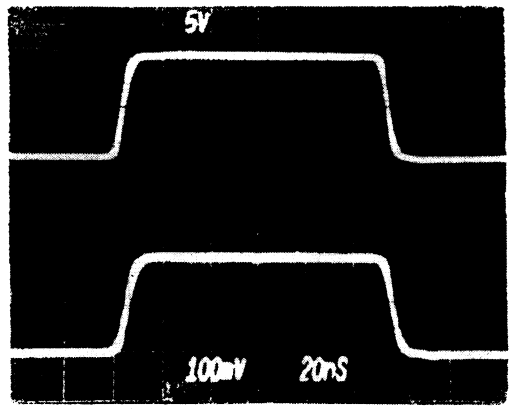


FIGURE 1. AC AND TRANSIENT RESPONSE TEST CIRCUIT

V_Y TRANSIENT RESPONSE
Vertical Scale: Top 5V/Div. Bottom: 100mV/Div.
Horizontal Scale: 20ns/Div.



Applications Information

Operation at Reduced Supply Voltages

The HA-2557 will operate over a range of supply voltages, ±5V to ±15V. Use of supply voltages below ±12V will cause degradation of electrical parameters.

Offset Adjustment

The channel offset voltage may be nulled by using a 20K potentiometer between the V_{YIO} or V_{XIO} adjust pin A and B and connecting the wiper to V-. Reducing the channel offset voltage will reduce AC feedthrough and improve the multiplication error.

HARRIS SEMICONDUCTOR

HA7210

PRELIMINARY

March 1993

Low Power Crystal Oscillator

Features

- Single Supply Operation @ 32kHz ..... 2.0V to 7.0V
- Operating Frequency Range..... 10kHz to 10MHz
- Supply Current at 32kHz 5µA
- Supply Current at 1MHz 130µA
- Drives 2 CMOS Loads
- Only Requires an External Crystal for Operation

Applications

- Battery Powered Circuits
- Remote Metering
- Embedded Microprocessors
- Palm Top/Notebook PC

Description

The HA7210 is a very low power crystal-controlled oscillator that can be externally programmed to operate between 10kHz and 10MHz. For normal operation it requires only the addition of a crystal. The part exhibits very high stability over a wide operating voltage and temperature range.

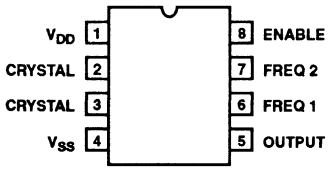
The HA7210 also features a disable mode that switches the output to a high impedance state. This feature is useful for minimizing power dissipation during standby and when multiple oscillator circuits are employed.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA7210IP	-40°C to +85°C	8 Lead Plastic DIP
HA7210IB	-40°C to +85°C	8 Lead SOIC
HA7210Y	-40°C to +85°C	DIE

Pinout

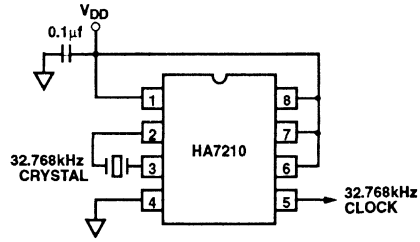
HA7210
TOP VIEW



FREQUENCY SELECTION TRUTH TABLE

ENABLE	FREQ 1	FREQ 2	OUTPUT RANGE
1	1	1	10kHz - 100kHz
1	1	0	100kHz - 1MHz
1	0	1	1MHz - 5MHz
1	0	0	5MHz - 10MHz
0	X	X	High-Z

Typical Application Circuit

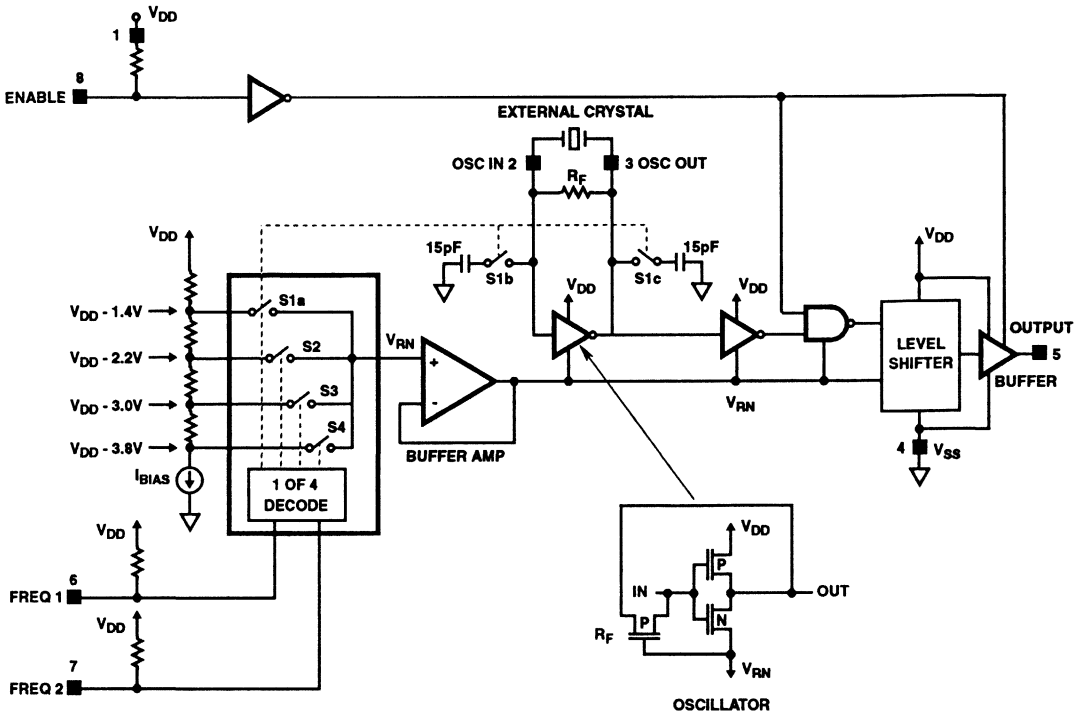


32.768kHz MICROPOWER CLOCK OSCILLATOR

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3389.1

Simplified Block Diagram



ENABLE	FREQ 1	FREQ2	SWITCH	OUTPUT RANGE
1	1	1	S1a, b, c	10kHz - 100kHz
1	1	0	S2	100kHz - 1MHz
1	0	1	S3	1MHz - 5MHz
1	0	0	S4	5MHz - 10MHz+
0	X	X	X	High Impedance

Absolute Maximum Ratings

Supply Voltage 10.0V
Voltage (any pin) ..... V_{SS}-0.3V to V_{DD}+0.3V
Junction Temperature (Plastic Package) ..... +150°C
ESD Rating (Note 2) ..... >4000V
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature (Note 3) ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} = 5V, V_{SS} = GND, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	HA7210I			UNITS
	MIN	TYP	MAX	
V_{DD} Supply Range (f_{OSC} = 32kHz)	2	5	7	V
I_{DD} Supply Current				
f_{OSC} = 32kHz, V_{DD} = 5V, EN = 0 Standby	-	5.0	9.0	µA
f_{OSC} = 32kHz, V_{DD} = 5V, C_L = 10pF (Note 1), EN = 1, Freq1 = 1, Freq2 = 1	-	5.2	10.2	µA
f_{OSC} = 32kHz, V_{DD} = 5V, C_L = 40pF, EN = 1, Freq1 = 1, Freq2 = 1	-	10	15	µA
f_{OSC} = 32kHz, V_{DD} = 3V, C_L = 10pF (Note 1), EN = 1, Freq1 = 1, Freq2 = 1	-	3.6	6.1	µA
f_{OSC} = 32kHz, V_{DD} = 3V, C_L = 40pF, EN = 1, Freq1 = 1, Freq2 = 1	-	6.5	9	µA
f_{OSC} = 1MHz, V_{DD} = 5V, C_L = 10pF (Note 1), EN = 1, Freq1 = 0, Freq2 = 1	-	130	200	µA
f_{OSC} = 1MHz, V_{DD} = 5V, C_L = 40pF, EN = 1, Freq1 = 0, Freq2 = 1	-	270	350	µA
f_{OSC} = 1MHz, V_{DD} = 3V, C_L = 10pF (Note 1), EN = 1, Freq1 = 0, Freq2 = 1	-	90	160	µA
f_{OSC} = 1MHz, V_{DD} = 3V, C_L = 40pF, EN = 1, Freq1 = 0, Freq2 = 1	-	140	250	µA
V_{OH} Output High Voltage (I_{OUT} = -1mA)	4.0	4.9	-	V
V_{OL} Output Low Voltage (I_{OUT} = 1mA)	-	0.07	0.4	V
I_{OH} Output High Current ($V_{OUT} \geq 4V$)	-	-10	-5	mA
I_{OL} Output Low Current ($V_{OUT} \leq 0.4V$)	5.0	10.0	-	mA
I_{IN} Enable, Freq1, Freq2 Input Current (V_{IN} = V_{SS} to V_{DD})	-	0.4	1.0	µA
V_{IH} Input High Voltage Enable, Freq1, Freq2	2.0	-	-	V
V_{IL} Input Low Voltage Enable, Freq1, Freq2	-	-	0.8	V
t_R Output Rise Time (10% - 90%, f_{OSC} = 32kHz, C_L = 40pF)	-	20	40	ns
t_R Output Rise Time (10% - 90%, f_{OSC} = 1MHz, C_L = 40pF)	-	12	-	ns
t_F Output Fall Time (10% - 90%, f_{OSC} = 32kHz, C_L = 40pF)	-	25	50	ns
t_F Output Fall Time (10% - 90%, f_{OSC} = 1MHz, C_L = 40pF)	-	12	-	ns
Duty Cycle (C_L = 40pF) f_{OSC} = 32kHz, Packaged Part Only (Note 4)	40	50	60	%
Frequency Stability vs. Supply Voltage (f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF)	-	1	-	ppm/V
Frequency Stability vs. Temperature (f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF)	-	0.1	-	ppm/°C
Frequency Stability vs. Load (f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF)	-	0.01	-	ppm/pF

NOTES:

1. Calculated using the equation $I_{DD} = I_{DD}$ (No Load) + (V_{DD}) (f_{OSC})(C_L)
2. Human body model.
3. This product is production tested at +25°C only.
4. Duty cycle will vary with supply voltage, oscillation frequency, and parasitic capacitance on the crystal pins.

Die Characteristics

DIE DIMENSIONS:
68 x 64 x 14 ± 1mils

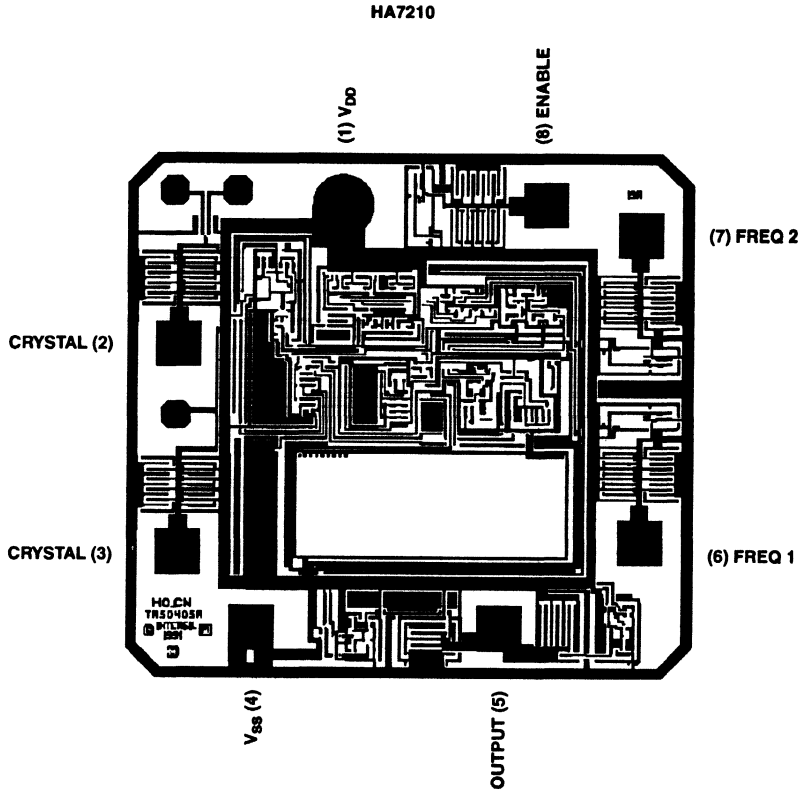
METALLIZATION:
Type: Si - Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride (Si_3N_4) Over Silox (SiO_2, 3% Phos)
Silox Thickness: 7kÅ ± 1kÅ
Nitride Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Silver Epoxy - Plastic DIP and SOIC

SUBSTRATE POTENTIAL: V_{SS}

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HFA5250

PRELIMINARY

March 1993

Ultra High-Speed Monolithic Pin Driver

Features

- High Digital Data Rate 500MHz
- Very Fast Slew Rate 2500V/µs
- Very Fast Rise/Fall Times 600ps
- Wide Output Range ..... +7V to -2V
- Precise 50Ω Output Impedance
- High Impedance, Tri-State Output Control

Applications

- IC Tester Pin Electronics
- Pattern Generators
- Pulse Generators
- Built-In Test Equipment (BITE)
- Level Comparator/Translator

Description

The HFA5250 is the ideal monolithic pin driver solution for high performance test systems. The device will switch at high data rates between two input voltage levels providing variable amplitude pulses. The output impedance is trimmed to achieve a precision 50Ω source for impedance matching. Two differential ECL/TTL compatible inputs control the operation of the HFA5250, one controlling the V_{HIGH}/V_{LOW} switching and the other controlling the output's high-impedance state. The HFA5250's 500MHz data rate makes it compatible with today's high-speed VLSI test systems and the +7V to -2V output swing allows testing of all common logic families.

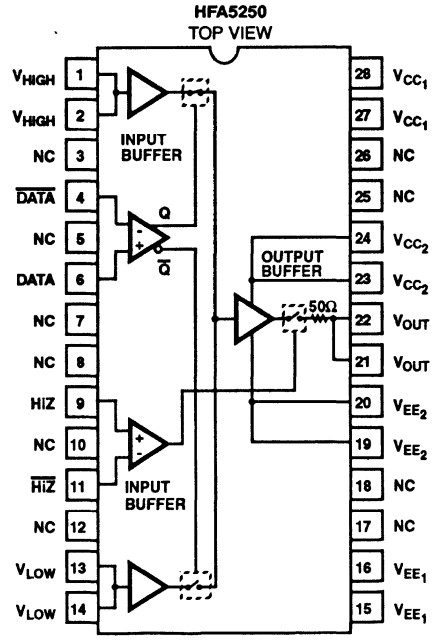
The HFA5250 is manufactured in the Harris proprietary complementary bipolar process and is offered in 28-lead SOIC package.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA5250CB	0°C to +50°C Without Air Flow	28 Lead SOIC
	0°C to +70°C With 400 lfpm Air Flow	

Pinout

HFA5250
TOP VIEW



Switches Shown in the "1" State.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2943.3**

Absolute Maximum Ratings

Supply Voltage 17.0V
Differential Input Voltage. 5.0V
Output Current Continuous. . . . . 160mA (Note 1)
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature. . . . . +175°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C

Thermal Information

Thermal Resistance	θ_{JA}, Still Air	θ_{JA}, 400 lfpm	θ_{JC}
Plastic SOIC Package	70°C/W	53°C/W	21°C/W

Maximum Package Power Dissipation
Plastic SOIC Package with still air at 50°C 1.43W
Plastic SOIC Package with 400 lfpm air at 70°C 1.50W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics V_{CC} = +10V, V_{EE} = -5.2V, Unless Otherwise Specified

PARAMETERS	TEMP	ALL GRADES MIN	ALL GRADES TYP	ALL GRADES MAX	UNITS
INPUT CHARACTERISTICS (V_{HIGH}, V_{LOW})					
V_{HIGH} Input Offset Voltage (V_{HIGH} = 0)	+25°C	-200	-100	30	mV
V_{LOW} Input Offset Voltage (V_{LOW} = 0)	+25°C	-200	-100	30	mV
V_{HIGH} Input Bias Current (V_{HIGH} = 5V)	+25°C	-150	50	250	µA
V_{LOW} Input Bias Current (V_{LOW} = 0V)	+25°C	-350	-100	150	µA
V_{HIGH} Voltage Range	+25°C	-2.6	-	7.5	V
(Note 5)	+25°C	V_{EE}+2.6	-	V_{CC}-2.5	V
V_{LOW} Voltage Range	+25°C	-2.7	-	7.4	V
(Note 5)	+25°C	V_{EE}+2.5	-	V_{CC}-2.6	V
V_{HIGH} to V_{LOW} Differential Voltage Range	+25°C	0.2	-	10.2	V
Input Resistance (V_{IN} = -2V to 7V)	+25°C	-	10	-	kΩ
Input Capacitance	+25°C	-	5	-	pF
Input Noise voltage (10Hz - 1MHz)	+25°C	-	20	-	μV_{P-P}
LOGIC INPUT CHARACTERISTICS (Data, $\overline{Data}$, HiZ, $\overline{HiZ}$)					
Input Offset Voltage	+25°C	-	±250	-	mV
Input Voltage Range	+25°C	-2.0	-	7.0	V
(Note 5)	+25°C	V_{EE}+3.2	-	V_{CC}-3.0	V
Input High Current (V_{IH} = 0V, V_{IL} = -2V)	+25°C	-25	50	200	µA
Input Low Current (V_{IH} = 0V, V_{IL} = -2V)	+25°C	-400	-150	25	µA
Common Mode Input Resistance (V_{CM} = -2V to 7V)	+25°C	-	1	-	MΩ
Differential Input Resistance (V_{DIFF} = 0V to 5V)	+25°C	-	100	-	kΩ
Input Capacitance	+25°C	-	3	-	pF
TRANSFER CHARACTERISTICS					
V_{HIGH}/V_{LOW} Voltage Gain (V_{HIGH}, V_{LOW} = 0V to 5V)	+25°C	0.95	0.97	1.0	V/V
V_{HIGH}/V_{LOW} Linearity Error (V_{HIGH}, V_{LOW} = 0V to 5V, FS = 5V)	+25°C	-0.5	± 0.2	0.5	%
V_{HIGH}/V_{LOW} Linearity Error (V_{HIGH}, V_{LOW} = -2V to 7V, FS = 9V)	+25°C	-1.2	± 0.6	1.2	%
V_{HIGH}/V_{LOW} -3dB Bandwidth (200mV_{P-P})	+25°C	-	500	-	MHz
SWITCHING CHARACTERISTICS (Z_{LOAD} = 10 Inches of RG-58, V_{HIGH} = 3V, V_{LOW} = 0V, V_{DATA} = -1.8V to -1.0V, Measured 50% to 50% pts).					
Propagation Delay (Note 2)	+25°C	-	2	-	ns
Propagation Delay Jitter, 1 Sigma	+25°C	-	30	-	ps
Propagation Delay Match (Rising vs Falling Edge, Note 2)	+25°C	-	150	-	ps

Electrical Characteristics V_{CC} = +10V, V_{EE} = -5.2V, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEMP	ALL GRADES			UNITS
		MIN	TYP	MAX	
Propagation Delay vs Duty Cycle (2.5% to 97.5%, 200ns Period)	+25°C	-	±100	-	ps
Active to HiZ Delay (Measured 50% to 10% Points)	+25°C	-	3.0	-	ns
HiZ to Active Delay (Measured 50% to 10% Points)	+25°C	-	3.5	-	ns
Data Rate (1Vp-p, 50% Duty Cycle, 90% Amplitude)	+25°C	-	500	-	MHz
TRANSIENT RESPONSE (Z_{LOAD} = 16 Inches of RG-58 Terminated with 5pF)					
Slew Rate (-1V to +6V)	+25°C	-	2500	-	V/µs
Rise/Fall Time (1 V_{P-P}, 20%-80%)	+25°C	-	600	-	ps
Rise/Fall Time (3 V_{P-P}, 10%-90%)	+25°C	-	1.2	-	ns
Rise/Fall Time (5 V_{P-P}, 10%-90%)	+25°C	-	1.8	2.25	ns
Rise/Fall Time Match (Note 2)	+25°C	-	-	200	ps
Overshoot/Undershoot/Preshoot (3 V_{P-P})	+25°C	-	5	-	%
Data Settling Time 1% (Note 3)	+25°C	-	7	-	ns
V_{HIGH}/V_{LOW} Settling Time 1% (Note 3)	+25°C	-	12	-	ns
OUTPUT CHARACTERISTICS					
Output Voltage Swing, No Load	+25°C	-2	-	7	V
(Note 5)	+25°C	V_{EE}+3.2	-	V_{CC}-3.0	V
Output Voltage Swing R_L = 50Ω	+25°C	-1	-	3.5	V
Output Resistance - Active (-2V to 7V)	+25°C	49	50	51	Ω
Output Resistance - HiZ (-2V to 7V)	+25°C	-	10	-	MΩ
HiZ Output Voltage Compliance	+25°C	-2	-	7	V
(Note 5)	+25°C	V_{CC}-12.0	-	V_{EE}+12.2	V
Output Leakage - HiZ (-2V to 7V)	+25°C	-1	-	1	µA
Output Capacitance - HiZ	+25°C	-	5		pF
POWER SUPPLY CHARACTERISTICS					
V_{HIGH} Power Supply Rejection Ratio (Note 4)	+25°C	28	-	-	dB
V_{LOW} Power Supply Rejection Ratio (Note 4)	+25°C	28	-	-	dB
Data/HiZ Power Supply Rejection Ratio	+25°C	-	22	-	dB
Total Supply Current	+25°C	85	90	95	mA
I_{CC1}/I_{EE1} Supply Current	+25°C	-	65	-	mA
I_{CC2}/I_{EE2} Supply Current	+25°C	-	25	-	mA
Supply Voltage Range (V_{CC} - V_{EE})	+25°C	10	-	15.2	V
Power Dissipation (V_{CC} = 10V, V_{EE} = -5.2V, No Load)	+25°C	-	-	1.44	W

NOTES:

1. Internal Power Dissipation may limit Output Current below 160mA.
2. 3V Step, 50% duty cycle, 200ns period.
3. 3V Step, measured from 50% of input to ±1% of final value, final value is at 50ns.
4. V_{HIGH} = 2.6V, V_{LOW} = 2.4V, V_{CC} = 9V to 10V, V_{EE} = -4.2V to -5.2V.
5. Operation above total supply voltage of 15.2V is not recommended. See specification under Power Supply Characteristics.

Die Characteristics

DIE DIMENSIONS:
1990µm x 1530µm x 525µm ± 25.4µm

GLASSIVATION:
Nitride, 4kÅ ± 0.5kÅ

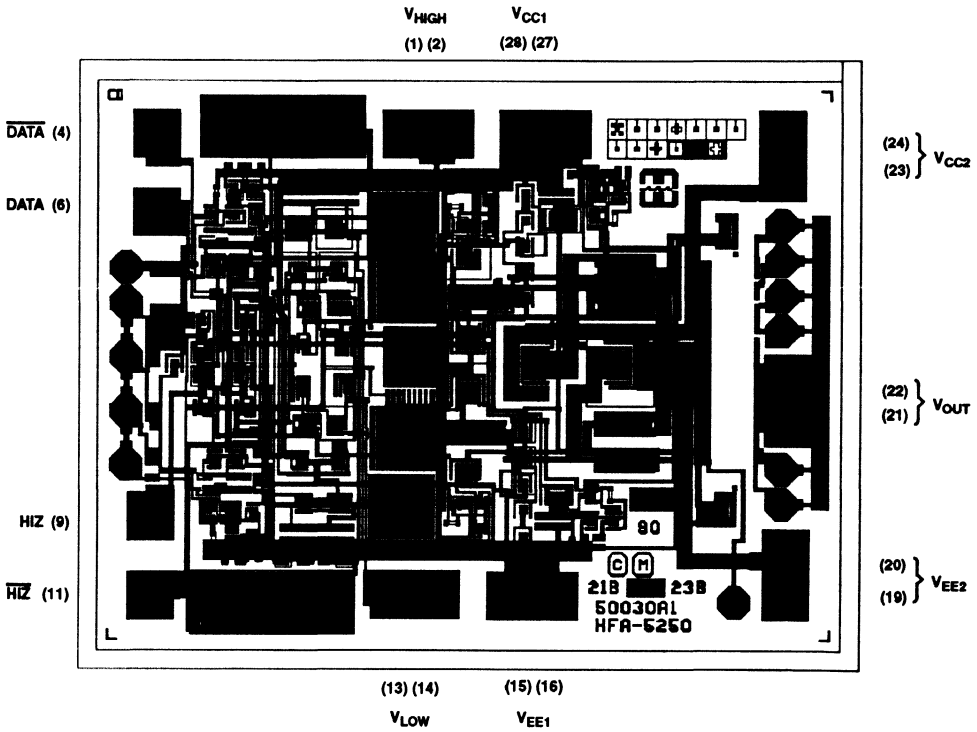
METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

DIE ATTACH:
Material: Epoxy

Metallization Mask Layout

HFA5250



HARRIS SEMICONDUCTOR

ICL8013

March 1993

Four Quadrant Analog Multiplier

Features

- **Accuracy of ±0.5% ("A" Version)**
- **Full ±10V Input Voltage Range**
- **1MHz Bandwidth**
- **Uses Standard ±15V Supplies**
- **Built-In Op Amp Provides Level Shifting, Division and Square Root Functions**

Description

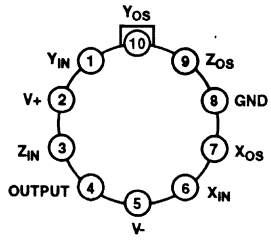
The ICL8013 is a four quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to trim gain accuracy, offset voltage and feedthrough performance. The high accuracy, wide bandwidth, and increased versatility of the ICL8013 make it ideal for all multiplier applications in control and instrumentation systems. Applications include RMS measuring equipment, frequency doublers, balanced modulators and demodulators, function generators, and voltage controlled amplifiers.

Ordering Information

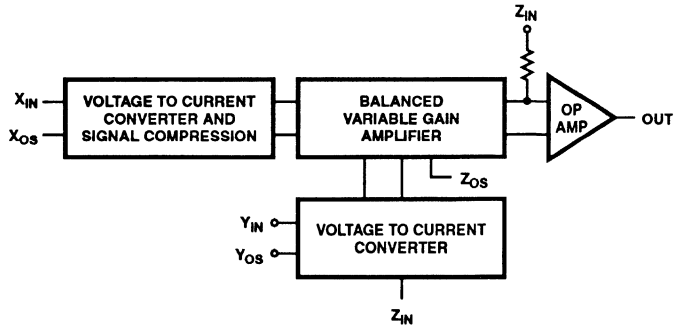
PART NUMBER	MULTIPLICATION ERROR	TEMPERATURE RANGE	PACKAGE
ICL8013AM TX	±0.5%	-55°C to +125°C	10 Pin TO-100 Can
ICL8013BM TX	±1% Max	-55°C to +125°C	10 Pin TO-100 Can
ICL8013CM TX	±2%	-55°C to +125°C	10 Pin TO-100 Can
ICL8013AC TX	±0.5%	0°C to +70°C	10 Pin TO-100 Can
ICL8013BC TX	±1% Max	0°C to +70°C	10 Pin TO-100 Can
ICL8013CC TX	±2%	0°C to +70°C	10 Pin TO-100 Can

Pinout

ICL8013
(TO-100 CAN)
TOP VIEW



Functional Diagram



File Number **2863.1**

Absolute Maximum Ratings

Supply Voltage ..... ±18V
Power Dissipation (Note 1) 500mW
Input Voltages (X_{IN}, Y_{IN}, Z_{IN}, X_{OS}, Y_{OS}, Z_{OS}) ..... V_{SUPPLY}
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
ICL8013XC ..... 0°C to +70°C
ICL8013XM ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, V_{SUPPLY} = ±15V, Gain and Offset Potentiometers Externally Trimmed, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	ICL8013A			ICL8013B			ICL8013C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Multiplier Function			$\frac{XY}{10}$			$\frac{XY}{10}$			$\frac{XY}{10}$		
Multiplication Error	-10 < X < 10 -10 < Y < 10			0.5			1.0			2.0	% Full Scale
Divider Function			$\frac{10Z}{X}$			$\frac{10Z}{X}$			$\frac{10Z}{X}$		
Division Error	X = -10		0.3			0.3			0.3		% Full Scale
	X = -1		1.5			1.5			1.5		% Full Scale
Feedthrough	X = 0, Y = ±10V			50			100			200	mV
	Y = 0, X = ±10V			50			100			150	mV
Non-Linearity X Input	X = $20V_{P-P}$ Y= ±10Vdc		±0.5			±0.5			±0.8		%
Y Input	Y = $20V_{P-P}$ X= ±10Vdc		±0.2			±0.2			±0.3		%
Frequency Response Small Signal Bandwidth (-3dB)			1.0			1.0			1.0		MHz
Full Power Bandwidth			750			750			750		kHz
Slew Rate			45			45			45		V/µs
1% Amplitude Error			75			75			75		kHz
1% Vector Error (0.5° Phase Shift)			5			5			5		kHz
Settling Time (to ±2% of Final Value)	V_{IN} = ±10V		1			1			1		µs
Overload Recovery (to ±2% of Final Value)	V_{IN} = ±10V		1			1			1		µs
Output Noise	5Hz to 10kHz		0.6			0.6			0.6		mVrms
	5Hz to 5MHz		3			3			3		mVrms
Input Resistance X Input	V_{IN} = 0V		10			10			10		MΩ
Y Input			6			6			6		MΩ
Z Input			36			36			36		kΩ
Input Bias Current X or Y Input	V_{IN} = 0V		2	5			7.5			10	µA
Z Input			25			25			25		µA
Power Supply Variation Multiplication Error			0.2			0.2			0.2		%/%
Output Offset				50			75			100	mV/V
Scale Factor			0.1			0.1			0.1		%/%
Quiescent Current			3.5	6.0		3.5	6.0		3.5	6.0	mA

Electrical Specifications T_A= +25°C, V_{SUPPLY} = ±15V, Gain and Offset Potentiometers Externally Trimmed, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	ICL8013A			ICL8013B			ICL8013C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
THE FOLLOWING SPECIFICATIONS APPLY OVER THE OPERATING TEMPERATURE RANGES											
Multiplication Error	-10V < X_{IN} < 10V, -10V < Y_{IN} < 10V		1.5			2			3		% Full Scale
Average Temp. Coefficients											
Accuracy			0.06			0.06			0.06		%/°C
Output Offset			0.2			0.2			0.2		mV/°C
Scale Factor			0.04			0.04			0.04		%/°C
Input Bias Current											
X or Y Input	V_{IN} = 0V			5			5			10	µA
Z Input				25			25			35	µA
Input Voltage (X, Y, or Z)				±10			±10			±10	V
Output Voltage Swing	$R_L \geq 2k\Omega$ $C_L < 1000pF$		±10			±10			±10		V

NOTE: 1. Derate at 6.8mW/°C for operation at ambient temperature above +75°C.

Typical Performance Curves

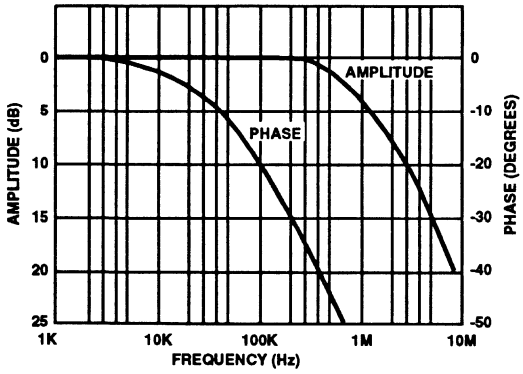


FIGURE 1. AMPLITUDE AND PHASE AS A FUNCTION OF FREQUENCY

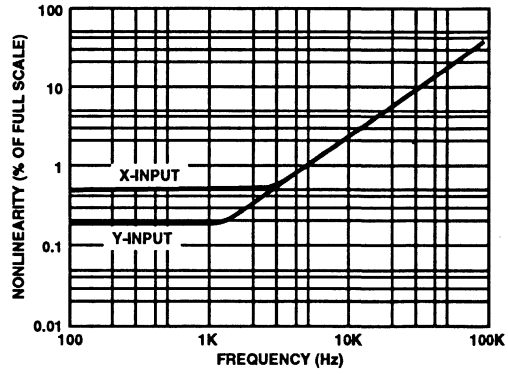


FIGURE 2. NONLINEARITY AS A FUNCTION OF FREQUENCY

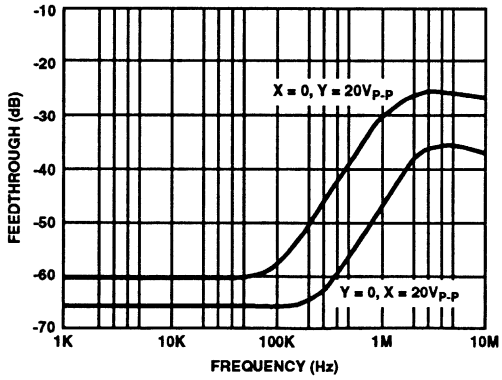


FIGURE 3. FEEDTHROUGH AS A FUNCTION OF FREQUENCY

Detailed Description

The fundamental element of the ICL8013 multiplier is the bipolar differential amplifier of Figure 4.

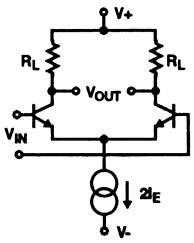


FIGURE 4. DIFFERENTIAL AMPLIFIER

The small signal differential voltage gain of this circuit is given by

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R_L}{r_E}$$

$$\text{Substituting } r_E = \frac{1}{g_M} = \frac{kT}{qI_E}$$

$$V_{OUT} = V_{IN}\left(\frac{R_L}{r_E}\right) = V_{IN} \bullet \frac{qI_E R_L}{kT}$$

The output voltage is thus proportional to the product of the input voltage V_{IN} and the emitter current I_E. In the simple transconductance multiplier of Figure 5, a current source comprising Q_3, D_1, and R_Y is used. If V_Y is large compared with the drop across D_1, then

$$I_D \approx \frac{V_Y}{R_Y} = 2I_E \text{ and}$$

$$V_{OUT} = \frac{qR_L}{kTR_Y}(V_X \bullet V_Y)$$

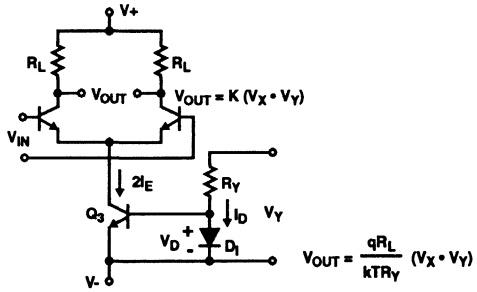


FIGURE 5. TRANSCONDUCTANCE MULTIPLIER

There are several difficulties with this simple modulator:

1. V_Y must be positive and greater than V_D.
2. Some portion of the signal at V_X will appear at the output unless $I_E = 0$.
3. V_X must be a small signal for the differential pair to be linear.
4. The output voltage is not centered around ground.

The first problem relates to the method of converting the V_Y voltage to a current to vary the gain of the V_X differential pair. A better method, Figure 6, uses another differential pair but with considerable emitter degeneration. In this circuit the differential input voltage appears across the common emitter resistor, producing a current which adds or subtracts from the quiescent current in either collector. This type of voltage to current converter handles signals from 0V to ±10V with excellent linearity.

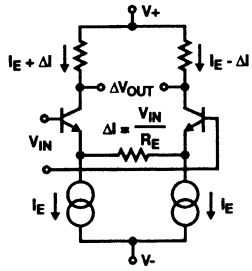


FIGURE 6. VOLTAGE TO CURRENT CONVERTER

The second problem is called feedthrough; i.e. the product of zero and some finite Input signal does not produce zero output voltage. The circuit whose operation is illustrated by Figures 7A, B, and C overcomes this problem and forms the heart of many multiplier circuits in use today.

This circuit is basically two matched differential pairs with cross coupled collectors. Consider the case shown in Figure 7A of exactly equal current sources basing the two pairs. With a small positive signal at V_{IN}, the collector current of Q_1 and Q_4 will increase but the collector currents of Q_2 and Q_3 will decrease by the same amount. Since the collectors are cross coupled the current through the load resistors remains unchanged and independent of the V_{IN} input voltage.

In Figure 7B, notice that with $V_{IN} = 0$ any variation in the ratio of biasing current sources will produce a common mode voltage across the load resistors. The differential output voltage will remain zero. In Figure 7C we apply a differential input voltage with unbalanced current sources. If I_{E1} is twice I_{E2} the gain of differential pair Q_1 and Q_2 is twice the gain of pair Q_3 and Q_4. Therefore, the change in cross coupled collector currents will be unequal and a differential output voltage will result. By replacing the separate biasing current sources with the voltage to current converter of Figure 6 we have a balanced multiplier circuit capable of four quadrant operation (Figure 8).

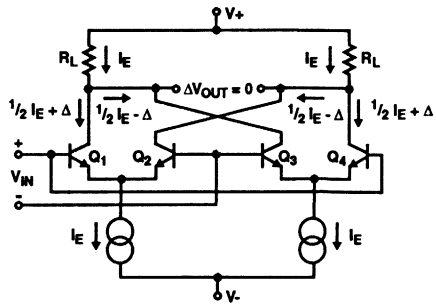


FIGURE 7A. INPUT SIGNAL WITH BALANCED CURRENT SOURCES $\Delta V_{OUT} = 0V$

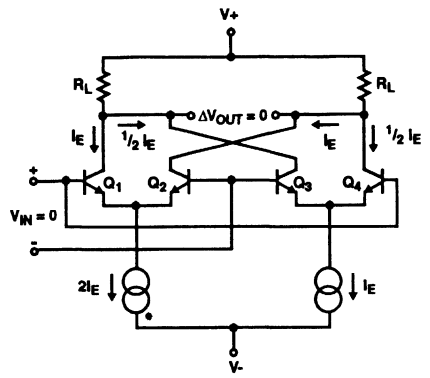


FIGURE 7B. NO INPUT SIGNAL WITH UNBALANCED CURRENT SOURCES $\Delta V_{OUT} = 0V$

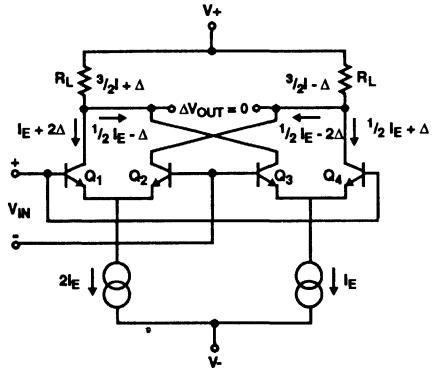


FIGURE 7C. INPUT SIGNAL WITH UNBALANCED CURRENT SOURCES, DIFFERENTIAL OUTPUT VOLTAGE

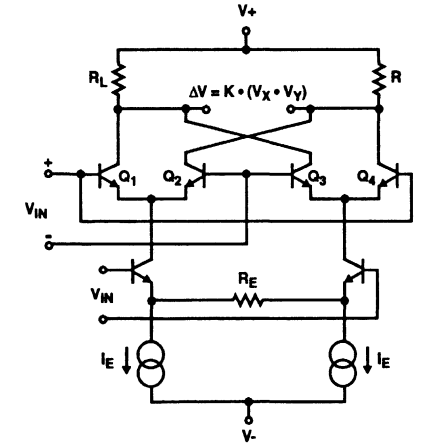


FIGURE 8. TYPICAL FOUR QUADRANT MULTIPLIER-MODULATOR

This circuit of Figure 8 still has the problem that the input voltage V_{IN} must be small to keep the differential amplifier in the linear region. To be able to handle large signals, we need an amplitude compression circuit.

Figure 5 showed a current source formed by relying on the matching characteristics of a diode and the emitter base junction of a transistor. Extension of this idea to a differential circuit is shown in Figure 9A. In a differential pair, the input voltage splits the basing current in a logarithmic ratio. (The usual assumption of linearity is useful only for small signals.) Since the input to the differential pair in Figure 9A is the difference in voltage across the two diodes, which in turn is proportional to the log of the ratio of drive currents, it follows that the ratio of diode currents and the ratio of collector currents are linearly related and independent of amplitude. If we combine this circuit with the voltage to current converter of Figure 6, we have Figure 9B. The output of the differential amplifier is now proportional to the input voltage over a large dynamic range, thereby improving linearity while minimizing drift and noise factors.

The complete schematic is shown in Figure 10. The differential pair Q_3 and Q_4 form a voltage to current converter whose output is compressed in collector diodes Q_1 and Q_2 These diodes drive the balanced cross-coupled differential amplifier Q_7/Q_8 Q_{14}/Q_{15}. The gain of these amplifiers is modulated by the voltage to current converter Q_9 and Q_{10}. Transistors Q_5, Q_6, Q_{11}, and Q_{12} are constant current sources which bias the voltage to current converter. The output amplifier comprises transistors Q_{16} through Q_{27}.

Multiplication

In the standard multiplier connection, the Z terminal is connected to the op amp output. All of the modulator output current thus flows through the feedback resistor R27 and produces a proportional output voltage.

Multiplier Trimming Procedure

1. Set $X_{IN} = Y_{IN} = 0V$ and adjust Z_{OS} for zero Output.
2. Apply a ±10V low frequency (≤100Hz) sweep (sine or triangle) to Y_{IN} with $X_{IN} = 0V$, and adjust X_{OS} for minimum output.
3. Apply the sweep signal of Step 2 to X_{IN} with $Y_{IN} = 0V$ and adjust Y_{OS} for minimum Output.
4. Readjust Z_{OS} as in Step 1, if necessary.
5. With $X_{IN} = 10.0V$ DC and the sweep signal of Step 2 applied to Y_{IN}, adjust the Gain potentiometer for Output = Y_{IN}. This is easily accomplished with a differential scope plug-in (A+B) by inverting one signal and adjusting Gain control for (Output - Y_{IN}) = Zero.

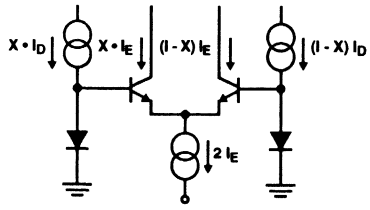


FIGURE 9A. CURRENT GAIN CELL

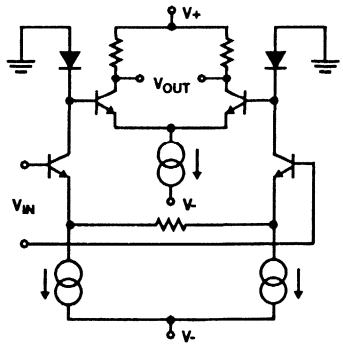


FIGURE 9B. VOLTAGE GAIN WITH SIGNAL COMPRESSION

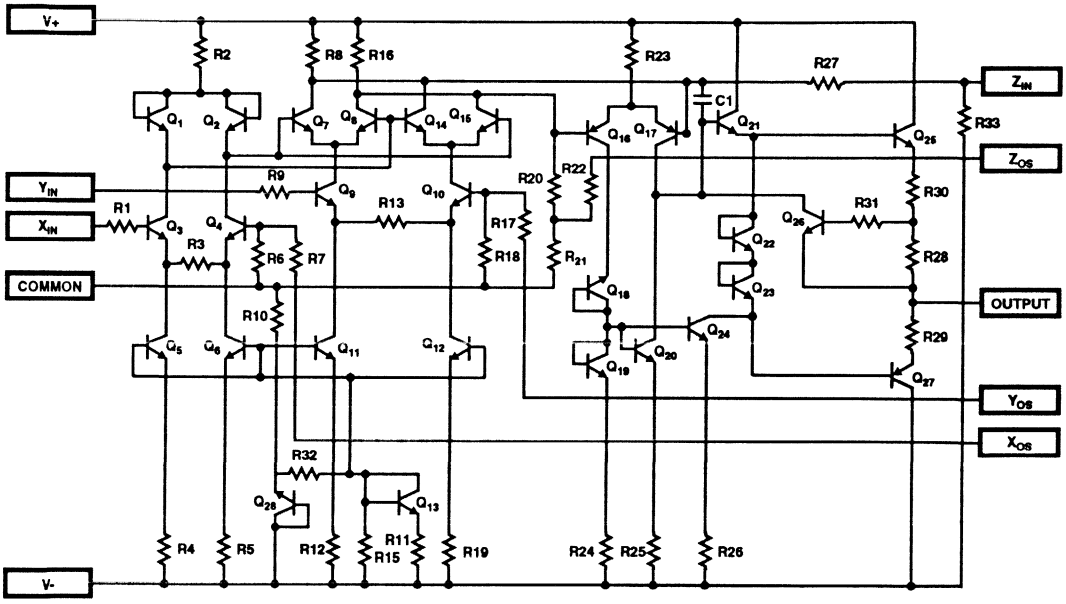


FIGURE 10. SCHEMATIC

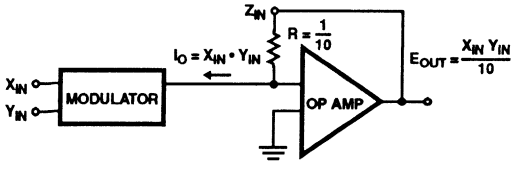


FIGURE 11A. MULTIPLIER BLOCK DIAGRAM

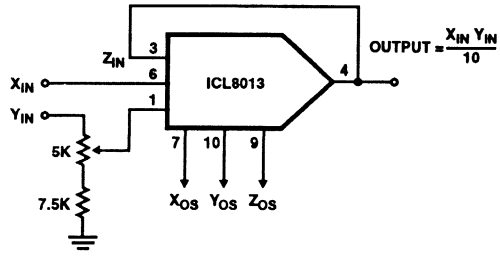


FIGURE 11B. ACTUAL CIRCUIT CONNECTION

Division

If the Z terminal is used as an input, and the output of the op amp connected to the Y input, the device functions as a divider. Since the input to the op amp is at virtual ground, and requires negligible bias current, the overall feedback forces the modulator output current to equal the current produced by Z.

$$\text{Therefore } I_O = X_{IN} \bullet Y_{IN} = \frac{Z_{IN}}{R} = 10Z_{IN}$$

$$\text{Since } Y_{IN} = E_{OUT}, E_{OUT} = \frac{10Z_{IN}}{X_{IN}}$$

Note that when connected as a divider, the X input must be a negative voltage to maintain overall negative feedback.

Divider Trimming Procedure

1. Set trimming potentiometers at mid-scale by adjusting voltage on pins 7, 9 and 10 (X_{OS}, Y_{OS}, Z_{OS}) for zero volts.
2. With Z_{IN} = 0V, trim Z_{OS} to hold the Output constant, as X_{IN} is varied from -10V through -1V.
3. With Z_{IN} = 0V and X_{IN} = -10.0V adjust Y_{OS} for zero Output voltage.
4. With Z_{IN} = X_{IN} (and/or Z_{IN} = -X_{IN}) adjust X_{OS} for minimum worst case variation of Output, as X_{IN} is varied from -10V to -1V.
5. Repeat Steps 2 and 3 if Step 4 required a large initial adjustment.
6. With Z_{IN} = X_{IN} (and/or Z_{IN} = -X_{IN}) adjust the gain control until the output is the closest average around +10.0V (-10V for Z_{IN} = -X_{IN}) as X_{IN} is varied from -10V to -3V.

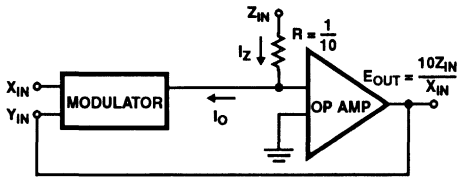


FIGURE 12A. DIVISION BLOCK DIAGRAM

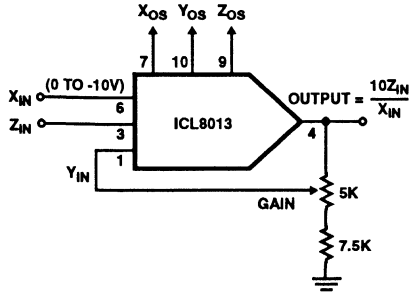


FIGURE 12B. ACTUAL CIRCUIT CONNECTION

Squaring

The squaring function is achieved by simply multiplying with the two inputs tied together. The squaring circuit may also be used as the basis for a frequency doubler since $\cos^2\omega t = {}^1/_2 (\cos 2\omega t + 1)$.

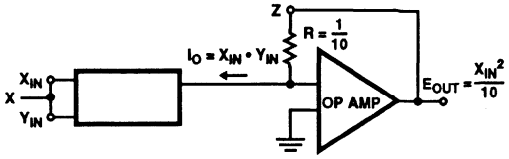


FIGURE 13A. SQUARER BLOCK DIAGRAM

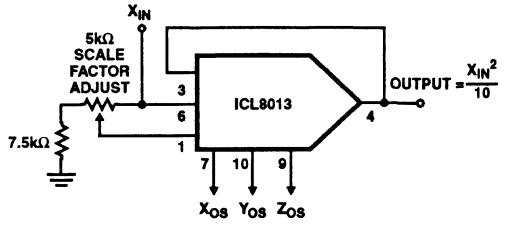


FIGURE 13B. ACTUAL CIRCUIT CONNECTION

Square Root

Tying the X and Y inputs together and using overall feedback from the op amp results in the square root function. The output of the modulator is again forced to equal the current produced by the Z input.

$$I_O = X_{IN} \bullet Y_{IN} = (-E_{OUT})^2 = 10Z_{IN}$$

$$E_{OUT} = -\sqrt{10Z_{IN}}$$

The output is a negative voltage which maintains overall negative feedback. A diode in series with the op amp output prevents the latchup that would otherwise occur for negative input voltages.

Square Root Trimming Procedure

1. Connect the ICL8013 in the Divider configuration.
2. Adjust Z_{OS}, Y_{OS}, X_{OS}, and Gain using Steps 1 through 6 of Divider Trimming Procedure.
3. Convert to the Square Root configuration by connecting X_{IN} to the output and inserting a diode between Pin 4 and the output node.
4. With Z_{IN} = 0V adjust Z_{OS} for zero output voltage.

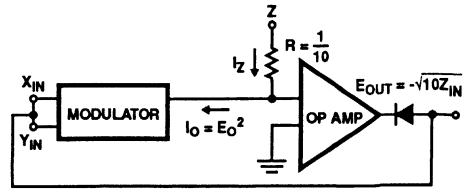


FIGURE 14A. SQUARE ROOT BLOCK DIAGRAM

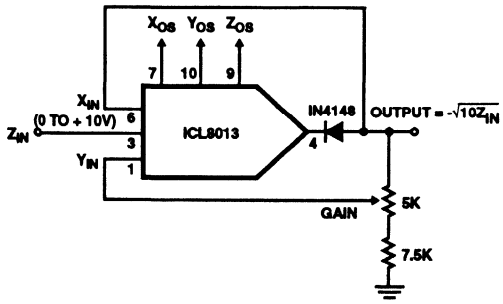


FIGURE 14B. ACTUAL CIRCUIT CONNECTION

Variable Gain Amplifier

Most applications for the ICL8013 are straight forward variations of the simple arithmetic functions described above. Although the circuit description frequently disguises the fact, it has already been shown that the frequency doubler is nothing more than a squaring circuit. Similarly the variable gain amplifier is nothing more than a multiplier, with the input signal applied at the X input and the control voltage applied at the Y input.

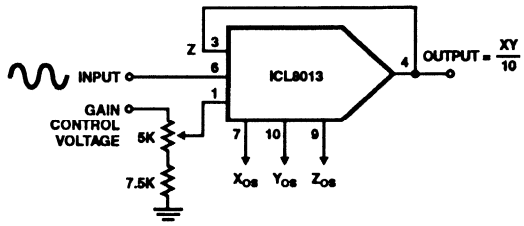


FIGURE 15. VARIABLE GAIN AMPLIFIER

Definition of Terms

Multiplication/Division Error: This is the basic accuracy specification. It includes terms due to linearity, gain, and offset errors, and is expressed as a percentage of the full scale output.

Feedthrough: With either input at zero, the output of an ideal multiplier should be zero regardless of the signal applied to the other input. The output seen in a non-ideal multiplier is known as the feedthrough.

Nonlinearity: The maximum deviation from the best straight line constructed through the output data, expressed as a percentage of full scale. One input is held constant and the other swept through it nominal range. The nonlinearity is the component of the total multiplication/division error which cannot be trimmed out.

Typical Applications

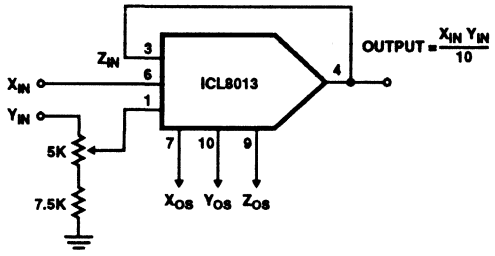


FIGURE 16. MULTIPLICATION

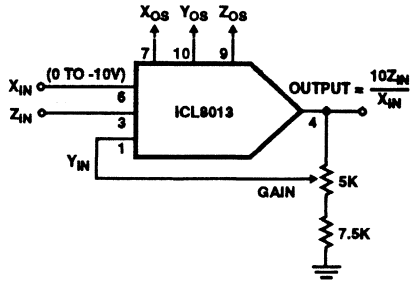


FIGURE 17. DIVISION

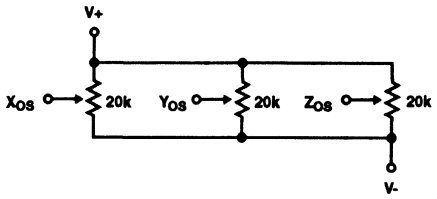


FIGURE 18. POTENTIOMETERS FOR TRIMMING OFFSET AND FEEDTHROUGH

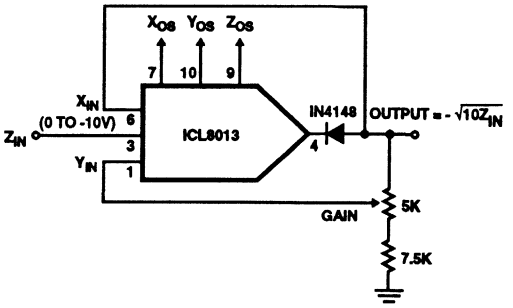


FIGURE 19. SQUARE ROOT

HARRIS SEMICONDUCTOR

ICL8038

Precision Waveform Generator/ Voltage Controlled Oscillator

March 1993

Features

- Low Frequency Drift with Temperature - 250ppm/°C
- Simultaneous Sine, Square, and Triangle Wave Outputs
- Low Distortion - 1% (Sine Wave Output)
- High Linearity - 0.1% (Triangle Wave Output)
- Wide Operating Frequency Range - 0.001Hz to 300kHz
- Variable Duty Cycle - 2% to 98%
- High Level Outputs - TTL to 28V
- Easy to Use - Just a Handful of External Components Required

Description

The ICL8038 waveform generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from 0.001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 250ppm/°C.

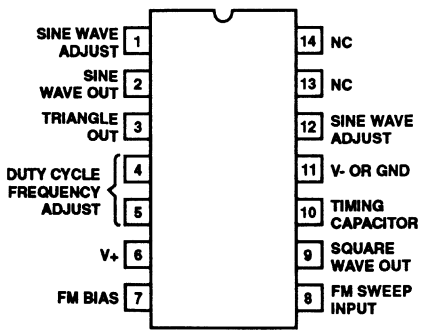
Ordering Information

PART NUMBER	STABILITY	TEMPERATURE RANGE	PACKAGE
ICL8038CCPD	250ppm/°C Typ.	0°C to +70°C	14 Lead Plastic DIP
ICL8038CCJD	250ppm/°C Typ.	0°C to +70°C	14 Lead Ceramic DIP
ICL8038BCJD	180ppm/°C Typ.	0°C to +70°C	14 Lead Ceramic DIP
ICL8038ACJD	120ppm/°C Typ.	0°C to +70°C	14 Lead Ceramic DIP
ICL8038BMJD*	350ppm/°C Max.	-55°C to +125°C	14 Lead Ceramic DIP
ICL8038AMJD*	250ppm/°C Max.	-55°C to +125°C	14 Lead Ceramic DIP

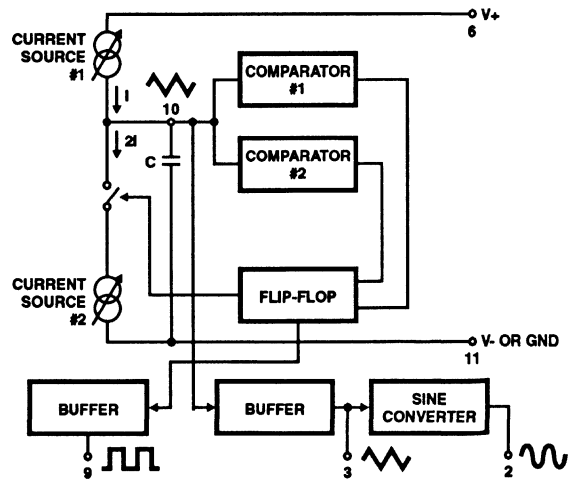
* Add /883B to part number if 883 processing is required.

Pinout

ICL8038
(PDIP, CDIP, SOIC)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2864.1**

Absolute Maximum Ratings

Supply Voltage (V- to V+) 36V
Power Dissipation (Note 1) 750mW
Input Voltage (Any Pin) ..... V- to V+
Input Current (Pins 4 and 5) 25mA
Output Sink Current (Pins 3 and 9) 25mA
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
ICL8038AM, ICL8038BM ..... -55°C to +125°C
ICL8038AC, ICL8038BC, ICL8038CC ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{SUPPLY} = ±10V or +20V, T_A = +25°C, R_L = 10kΩ, Test Circuit Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	ICL8038CC			ICL8038BC(BM)			ICL8038AC(AM)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage Operating Range	V_{SUPPLY}											
Single Supply	V+		+10		+30	+10		30	+10		30	V
Dual Supplies	V+, V-		±5		±15	±5		±15	±5		±5	V
Supply Current	I_{SUPPLY}	V_{SUPPLY} = ±10V (Note 2)										
8038AM 8038BM							12	15		12	15	mA
8038AC, 8038BC, 8038CC				12	20		12	20		12	20	mA
FREQUENCY CHARACTERISTICS (ALL WAVEFORMS)												
Max. Frequency of Oscillation	f_{MAX}		100			100			100			kHz
Sweep Frequency of FM Input	f_{SWEEP}			10			10			10		kHz
Sweep FM Range (Note 3)				35:1			35:1			35:1		
FM Linearity		10:1 Ratio		0.5			0.2			0.2		%
Frequency Drift with Temperature (Note 5)	$\Delta f/\Delta T$											
8038 AC, BC, CC		0°C to +70°C		250			180			120		ppm/°C
8038 AM, BM		-55°C to +125°C						350			250	ppm/°C
Frequency Drift with Supply Voltage	$\Delta f/\Delta V$	Over Supply Voltage Range		0.05			0.05			0.05		%/V
OUTPUT CHARACTERISTICS												
Square Wave												
Leakage Current	I_{OLK}	V_9 = 30V			1			1			1	µA
Saturation Voltage	V_{SAT}	I_{SINK} = 2mA		0.2	0.5		0.2	0.4		0.2	0.4	V
Rise Time	t_R	R_L = 4.7kΩ		180			180			180		ns
Fall Time	t_F	R_L = 4.7kΩ		40			40			40		ns
Typical Duty Cycle Adjust (Note 6)	ΔD		2		98	2		98	2		98	%
Triangle/Sawtooth/Ramp												
Amplitude	$V_{TRIANGLE}$	R_{TRI} = 100kΩ	0.30	0.33		0.30	0.33		0.30	0.33		xV_{SUPPLY}
Linearity				0.1			0.05			0.05		%
Output Impedance	Z_{OUT}	I_{OUT} = 5mA		200			200			200		Ω
Sine Wave												
Amplitude	V_{SINE}	R_{SINE} = 100kΩ	0.2	0.22		0.2	0.22		0.2	0.22		xV_{SUPPLY}
THD	THD	R_S = 1MΩ (Note 4)		2.0	5		1.5	3		1.0	1.5	%
THD Adjusted	THD	Use Figure 14		1.5			1.0			0.8		%

NOTES:

1. Derate ceramic package at 12.5mW/°C for ambient temperatures above 100°C.
2. R_A and R_B currents not included.
3. V_{SUPPLY} = 20V; R_A and R_B = 10kΩ, f ≅ 10kHz nominal; can be extended 1000 to 1. See Figures 15A and 15B.
4. 82kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use R_A and R_B.)
5. Figure 1, pins 7 and 8 connected, V_{SUPPLY} = ±10V. See Typical Curves for T.C. vs V_{SUPPLY}.
6. Not tested, typical value for design purposes only.

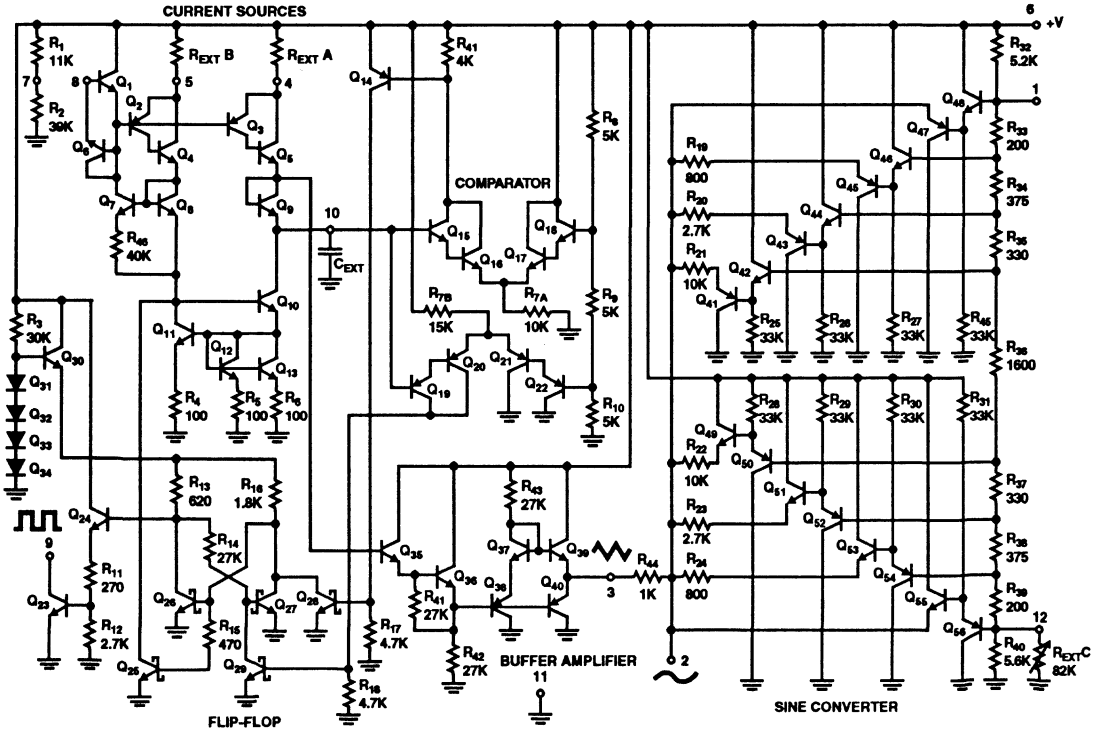
Test Conditions

PARAMETER	R_A	R_B	R_L	C_1	SW_1	MEASURE
Supply Current	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Current Into Pin 6
Sweep FM Range (Note 1)	10kΩ	10kΩ	10kΩ	3.3nF	Open	Frequency at Pin 9
Frequency Drift with Temperature	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 3
Frequency Drift with Supply Voltage (Note 2)	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Output Amplitude (Note 4)						
Sine	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk Output at Pin 2
Triangle	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk Output at Pin 3
Leakage Current (Off) (Note 3)	10kΩ	10kΩ		3.3nF	Closed	Current into Pin 9
Saturation Voltage (On) (Note 3)	10kΩ	10kΩ		3.3nF	Closed	Output (Low) at Pin 9
Rise and Fall Times (Note 5)	10kΩ	10kΩ	4.7kΩ	3.3nF	Closed	Waveform at Pin 9
Duty Cycle Adjust (Note 5)						
Max	50kΩ	~1.6kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Min	~25kΩ	50kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Triangle Waveform Linearity	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 3
Total Harmonic Distortion	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 2

NOTES:

1. The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 (f_{HI}) and then connecting pin 8 to pin 6 (f_{LO}). Otherwise apply Sweep Voltage at pin 8 ($^2/_3$ V_{SUPPLY} +2V) ≤ V_{SWEEP} ≤ V_{SUPPLY} where V_{SUPPLY} is the total supply voltage. In Figure 15B, pin 8 should vary between 5.3V and 10V with respect to ground.
2. 10V ≤ V+ ≤ 30V, or ±5V ≤ V_{SUPPLY} ≤ ±15V.
3. Oscillation can be halted by forcing pin 10 to +5V or -5V.
4. Output Amplitude is tested under static conditions by forcing pin 10 to 5.0V then to -5.0V.
5. Not tested; for design purposes only.

Detailed Schematic



Detailed Description (See Functional Diagram)

An external capacitor C is charged and discharged by two current sources. Current source #2 is switched on and off by a flip-flop, while current source #1 is on continuously. Assuming that the flip-flop is in a state such that current source #2 is off, and the capacitor is charged with a current I, the voltage across the capacitor rises linearly with time. When this voltage reaches the level of comparator #1 (set at 2/3 of the supply voltage), the flip-flop is triggered, changes states, and releases current source #2. This current source normally carries a current 2I, thus the capacitor is discharged with a net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at 1/3 of the supply voltage), the flip-flop is triggered into its original state and the cycle starts again.

Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an asymmetrical sawtooth appears at terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at terminal 9.

The sine wave is created by feeding the triangle wave into a nonlinear network (sine converter). This network provides a decreasing shunt impedance as the potential of the triangle moves toward the two extremes.

Test Circuit

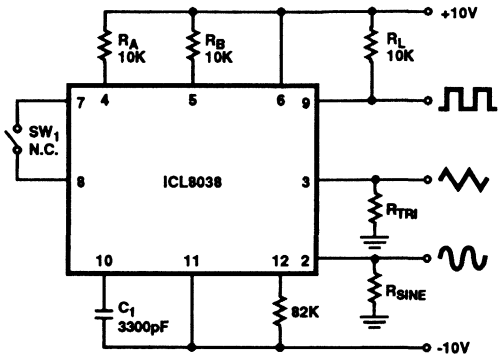


FIGURE 1.

Typical Performance Curves

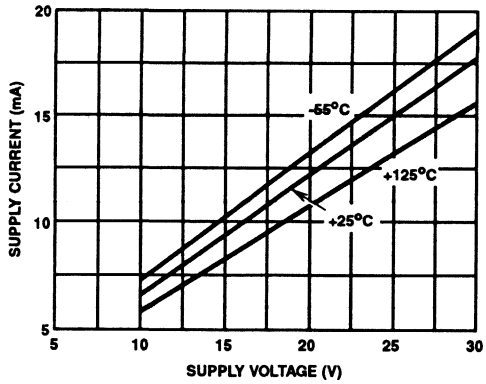


FIGURE 2. SUPPLY CURRENT vs SUPPLY VOLTAGE

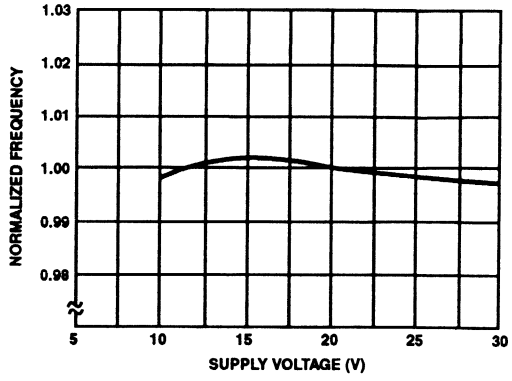


FIGURE 3. FREQUENCY vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

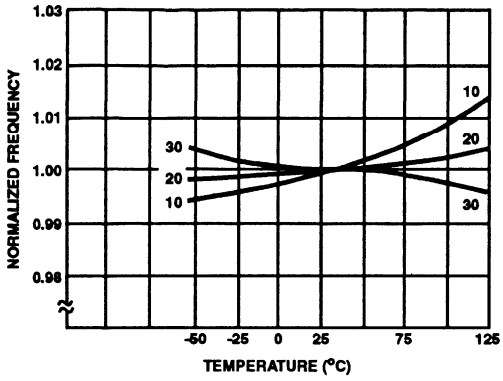


FIGURE 4. FREQUENCY vs TEMPERATURE

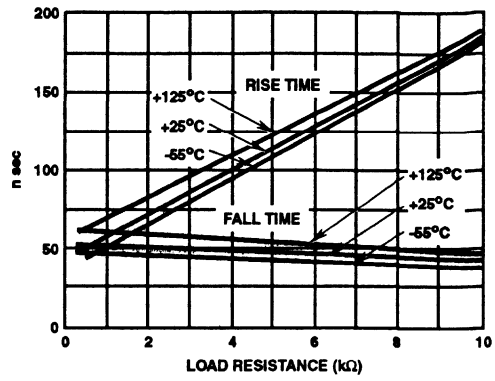


FIGURE 5. SQUARE WAVE OUTPUT RISE/FALL TIME vs LOAD RESISTANCE

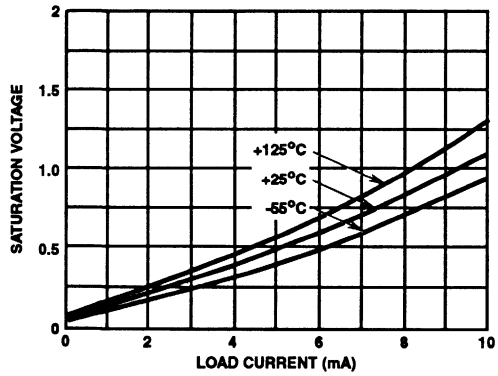


FIGURE 6. SQUARE WAVE SATURATION VOLTAGE vs LOAD CURRENT

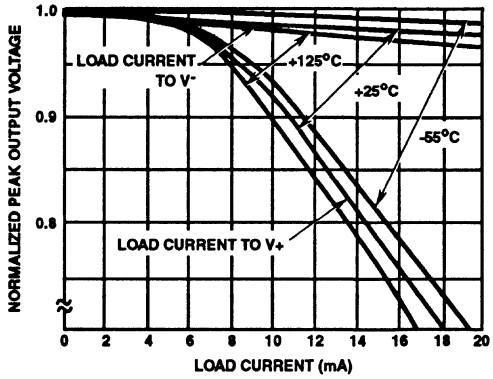


FIGURE 7. TRIANGLE WAVE OUTPUT VOLTAGE vs LOAD CURRENT

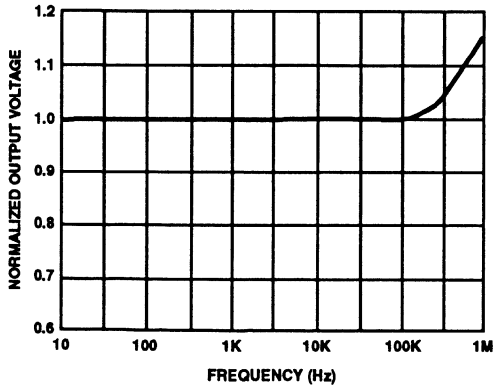


FIGURE 8. TRIANGLE WAVE OUTPUT VOLTAGE vs FREQUENCY

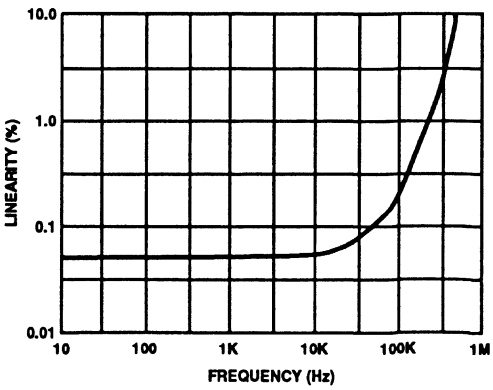


FIGURE 9. TRIANGLE WAVE LINEARITY vs FREQUENCY

Typical Performance Curves (Continued)

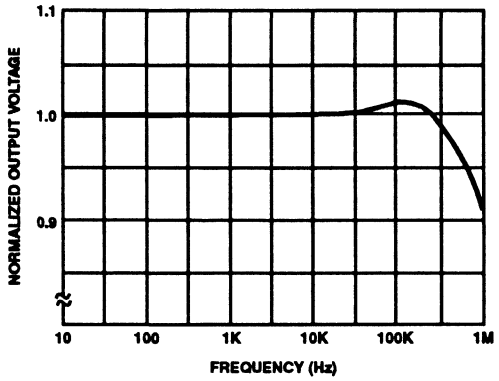


FIGURE 10. SINE WAVE OUTPUT VOLTAGE vs FREQUENCY

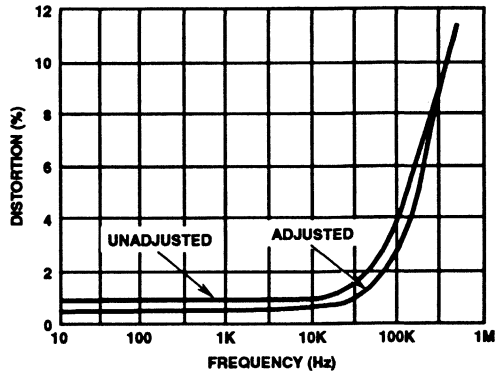


FIGURE 11. SINE WAVE DISTORTION vs FREQUENCY

Waveform Timing

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 13. Best results are obtained by keeping the timing resistors R_A and R_B separate (A). R_A controls the rising portion of the triangle and sine wave and the 1 state of the square wave.

The magnitude of the triangle waveform is set at $^1/_3$ VS_{UPPLY}; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times V}{I} = \frac{C \times 1/3 \times V_{SUPPLY} \times R_A}{0.22 \times V_{SUPPLY}} = \frac{R_A \times C}{0.66}$$

The falling portion of the triangle and sine wave and the 0 state of the square wave is:

$$t_2 = \frac{C \times V}{I} = \frac{C \times 1/3\, V_{SUPPLY}}{2\,(0.22)\,\frac{V_{SUPPLY}}{R_B} - 0.22\,\frac{V_{SUPPLY}}{R_A}} = \frac{R_A R_B C}{0.66\,(2R_A - R_B)}$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

If the duty cycle is to be varied over a small range about 50% only, the connection shown in Figure 13B is slightly more convenient.

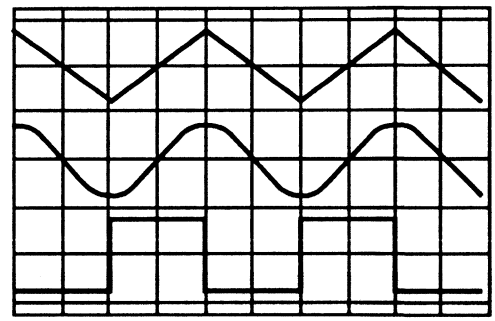
With two separate timing resistors, the frequency is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{R_A C}{0.66}\left(1 + \frac{R_B}{2R_A - R_B}\right)}$$

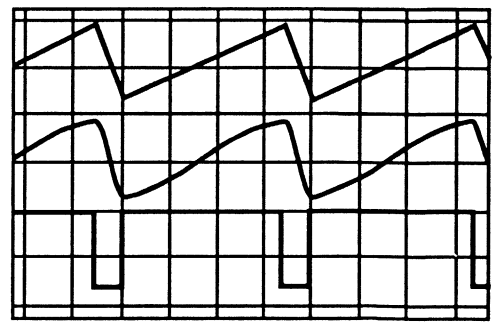
or, if $R_A = R_B = R$

$$f = \frac{0.33}{RC} \text{ (for Figure 13A)}$$

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents *and* thresholds are direct, linear functions of the supply voltage and thus their effects cancel.



SQUARE WAVE DUTY CYCLE - 50%



SQUARE WAVE DUTY CYCLE - 80%

FIGURE 12. PHASE RELATIONSHIP OF WAVEFORMS

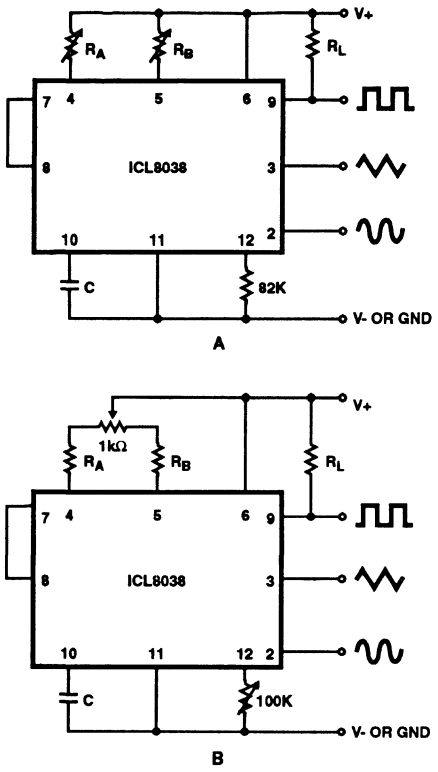


FIGURE 13. POSSIBLE CONNECTIONS FOR THE EXTERNAL TIMING RESISTORS

To minimize sine wave distortion the 82kΩ resistor between pins 11 and 12 is best made variable. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 14; this configuration allows a typical reduction of sine wave distortion close to 0.5%

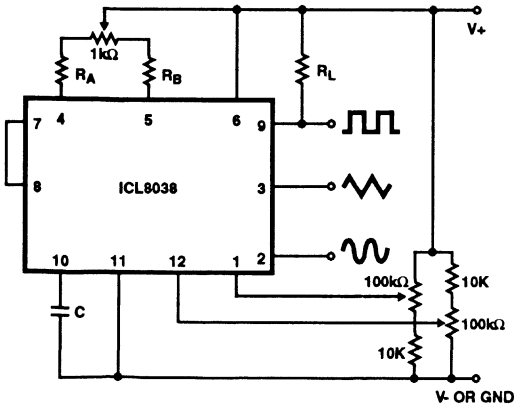


FIGURE 14. CONNECTION TO ACHIEVE MINIMUM SINE WAVE DISTORTION

Selecting R_A, R_B and C

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I > 5mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of 10μA to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to R_A can be calculated from:

$$I = \frac{R_1 \times (V+ - V-)}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{0.22\,(V+ - V-)}{R_A}$$

R_1 and R_2 are shown in the Detailed Schematic.

A similar calculation holds for R_B.

The capacitor value should be chosen at the upper end of its possible range.

Waveform Out Level Control and Power Supplies

The waveform generator can be operated either from a single power supply (10V to 30V) or a dual power supply (±5V to ±15V). With a single power supply the average levels of the triangle and sine wave are at exactly one-half of the supply voltage, while the square wave alternates between V+ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square wave output is not committed. A load resistor can be connected to a different power supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square wave output can be made TTL compatible (load resistor connected to +5V) while the waveform generator itself is powered from a much higher voltage.

Frequency Modulation and Sweeping

The frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from V+). By altering this voltage, frequency modulation is performed. For small deviations (e.g. ±10%) the modulating signal can be applied directly to pin 8, merely providing DC decoupling with a capacitor as shown in Figure 15A. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance from about 8kΩ (pins 7 and 8 connected together), to about (R + 8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 15B). In this way the entire bias for the current sources is created by the modulating signal, and a very large (e.g. 1000:1) sweep range is created (f = 0 at V_{SWEEP} = 0). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on

the supply voltage. The potential on Pin 8 may be swept down from V+ by ($^1/_3$ V_{SUPPLY} - 2V).

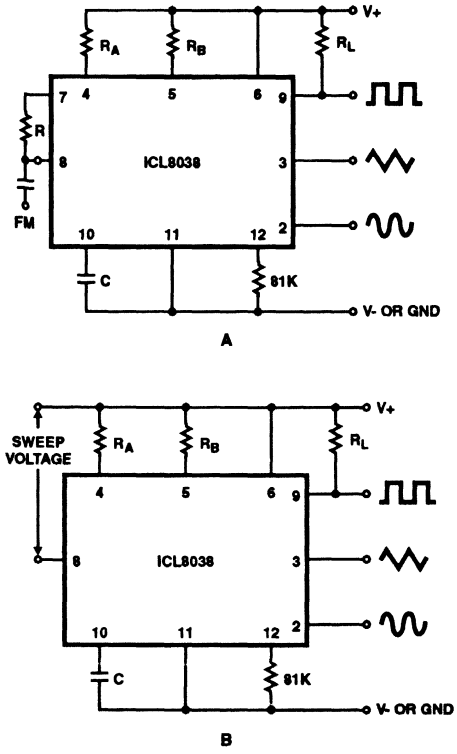


FIGURE 15. CONNECTIONS FRO FREQUENCY MODULATION (A) AND SWEEP (B)

Applications

The sine wave output has a relatively high output impedance (1kΩ Typ). The circuit of Figure 16 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

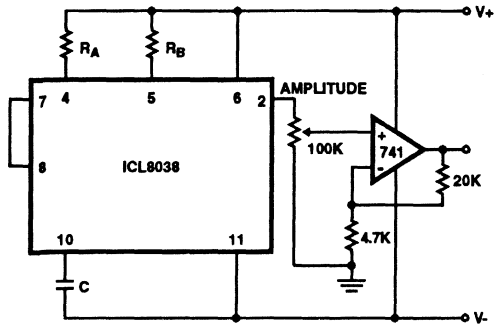


FIGURE 16. SINE WAVE OUTPUT BUFFER AMPLIFIERS

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the ICL8038 oscillation. Figure 17 shows a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.

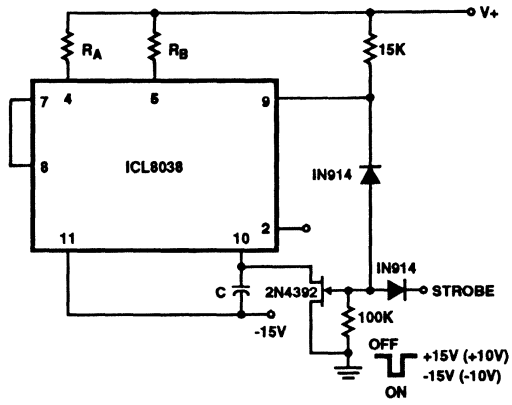


FIGURE 17. STROBE TONE BURST GENERATOR

To obtain a 1000:1 Sweep Range on the ICL8038 the voltage across external resistors R_A and R_B must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of R_A and R_B by a few hundred mV. The Circuit of Figure 18 achieves this by using a diode to lower the effective supply voltage on the ICL8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

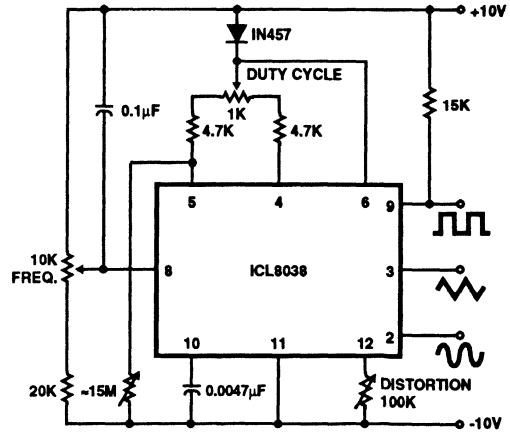


FIGURE 18. VARIABLE AUDIO OSCILLATOR, 20Hz TO 20kHz

The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp a shown in Figure 19.

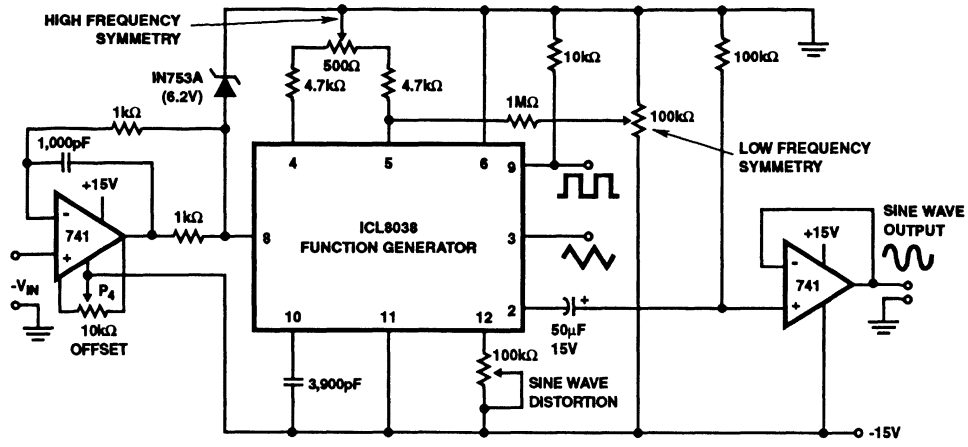


FIGURE 19. LINEAR VOLTAGE CONTROLLED OSCILLATOR

Use in Phase Locked Loops

Its high frequency stability makes the ICL8038 an ideal building block for a phase locked loop as shown in Figure 20. In this application the remaining functional blocks, the phase detector and the amplifier, can be formed by a number of available IC's (e.g. MC4344, NE562, HA2800, HA2820).

In order to match these building blocks to each other, two steps must be taken. First, two different supply voltages are used and the square wave output is returned to the supply of the phase detector. This assures that the VCO input voltage will not exceed the capabilities of the phase detector. If a smaller VCO signal is required, a simple resistive voltage divider is connected between pin 9 of the waveform generator and the VCO input of the phase detector.

Second, the DC output level of the amplifier must be made compatible to the DC level required at the FM input of the waveform generator (pin 8, 0.8V+). The simplest solution here is to provide a voltage divider to V+ (R_1, R_2 as shown) if the amplifier has a lower output level, or to ground if its level is higher. The divider can be made part of the low-pass filter.

This application not only provides for a free-running frequency with very low temperature drift, but is also has the unique feature of producing a large reconstituted sinewave signal with a frequency identical to that at the input.

For further information, see Harris Application Note A013, "Everything You Always Wanted to Know About the ICL8038".

Definition of Terms

Supply Voltage (V_{SUPPLY}). The total supply voltage from V+ to V-.

Supply Current. The supply current required from the power supply to operate the device, excluding load currents and the currents through R_A and R_B.

Frequency Range. The frequency range at the square wave output through which circuit operation is guaranteed.

Sweep FM Range. The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to pin 8. For correct operation, the sweep voltage should be within the range

$$(^2/_3\ V_{SUPPLY} + 2V) < V_{SWEEP} < V_{SUPPLY}$$

FM Linearity. The percentage deviation from the best fit straight line on the control voltage versus output frequency curve.

Output Amplitude. The peak-to-peak signal amplitude appearing at the outputs.

Saturation Voltage. The output voltage at the collector of Q_{23} when this transistor is turned on. It is measured for a sink current of 2mA.

Rise and Fall Times. The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.

Triangle Waveform Linearity. The percentage deviation from the best fit straight line on the rising and falling triangle waveform.

Total Harmonic Distortion. The total harmonic distortion at the sine wave output.

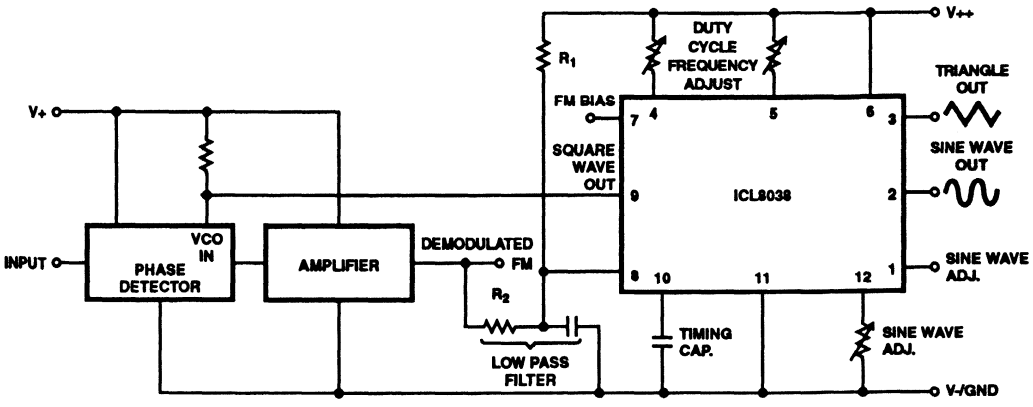


FIGURE 20. WAVEFORM GENERATOR USED AS STABLE VCO IN A PHASE-LOCKED LOOP

HARRIS SEMICONDUCTOR

ICL8048, ICL8049

March 1993

Log/Antilog Amplifiers

Features

- **Full Scale Accuracy 0.5%**
- **Temperature Compensated Operation . . . 0°C to +70°C**
- **Scale Factor, Adjustable 1V/Decade**
- **Dynamic Current Range (ICL8048) 120dB**
- **Dynamic Voltage Range (ICL8048 & ICL8049) 60dB**
- **Dual JFET Input Op Amps**

Description

The ICL8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1V of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

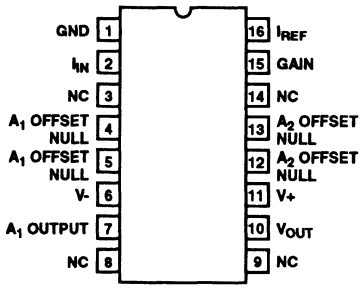
The ICL8049 is the antilogarithmic counterpart of the ICL8048; it nominally generates one decade of output voltage for each 1V change at the input.

Ordering Information

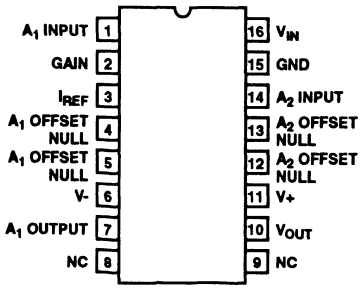
PART NUMBER	ERROR (+25°C)	TEMPERATURE RANGE	PACKAGE
ICL8048BCJE	30mV	0°C to +70°C	16 Lead Ceramic DIP
ICL8048CCJE	60mV	0°C to +70°C	16 Lead Ceramic DIP
ICL8049BCJE	10mV	0°C to +70°C	16 Lead Ceramic DIP
ICL8049CCJE	25mV	0°C to +70°C	16 Lead Ceramic DIP

Pinouts

ICL8048 (CDIP)
TOP VIEW

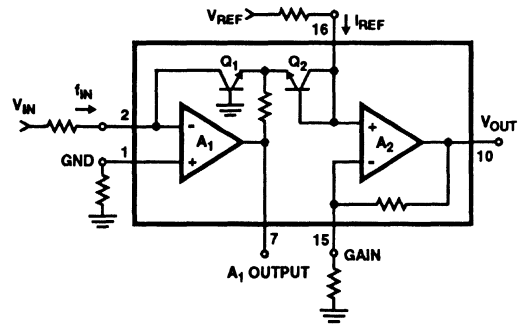


ICL8049 (CDIP)
TOP VIEW

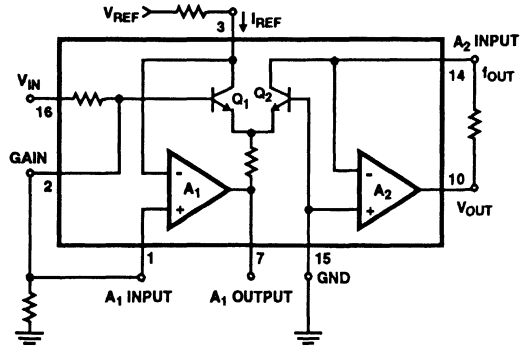


Functional Diagrams

ICL8048



ICL8049



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2865.1**

Specifications ICL8048

Absolute Maximum Ratings

Supply Voltage ..... ±18V
I_{IN} (Input Current) 2mA
I_{REF} (Reference Current) 2mA
Voltage Between Offset Null and V+ ..... ±0.5V
Output Short Circuit Duration ..... Indefinite
Power Dissipation 750mW
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_S = ±15V, T_A = +25°C, I_{REF} = 1mA, Scale Factor Adjusted for 1V/Decade, Unless Otherwise Specified

PARAMETERS	TEST CONDITIONS	ICL4048BC			ICL8048CC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic Range								
I_{IN} (1nA - 1mA)	R_{IN} = 10kΩ	120	-	-	120	-	-	dB
V_{IN} (10mV - 10V)		60	-	-	60	-	-	dB
Error, % of Full Scale	T_A = +25°C, I_{IN} = 1nA to 1mA	-	0.20	0.5	-	0.25	1.0	%
	T_A = 0°C to +70°C, I_{IN} = 1nA to 1mA	-	0.60	1.25	-	0.80	2.5	%
Error, Absolute Value	T_A = +25°C, I_{IN} = 1nA to 1mA	-	12	30	-	14	60	mV
	T_A = 0°C to +70°C, I_{IN} = 1nA to 1mA	-	36	75	-	50	150	mV
Temperature Coefficient of V_{OUT}	I_{IN} = 1nA to 1mA	-	0.8	-	-	0.8	-	mV/°C
Power Supply Rejection Ratio	Referred to Output	-	2.5	-	-	2.5	-	mV/V
Offset Voltage (A_1 & A_2)	Before Nulling	-	15	25	-	15	50	mV
Wideband Noise	At Output, for I_{IN} = 100µA	-	250	-	-	250	-	μV_{RMS}
Output Voltage Swing	R_L = 10kΩ	±12	±14	-	±12	±14	-	V
	R_L = 2kΩ	±10	±13	-	±10	±13	-	V
Power Consumption		-	150	200	-	150	200	mW
Supply Current		-	5	6.7	-	5	6.7	mA

Absolute Maximum Ratings

Supply Voltage ..... ±18V
V_{IN} (Input Current) ..... ±15V
I_{REF} (Reference Current) 2mA
Voltage Between Offset Null and V+ ..... ±0.5V
Output Short Circuit Duration ..... Indefinite
Power Dissipation 750mW
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_S = \pm15V$, $T_A = +25°C$, $I_{REF} = 1mA$, Scale Factor Adjusted for 1 Decade (Out) per Volt (In), Unless Otherwise Specified

PARAMETERS	TEST CONDITIONS	ICL4049BC			ICL8049CC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic Range (V_{OUT})	V_{OUT} = 10mV to 10V	60	-	-	60	-	-	dB
Error, Absolute Value	T_A = +25°C, 0V ≤ V_{IN} ≤ 2V	-	3	15	-	5	25	mV
	T_A = 0°C to +70°C, 0V ≤ V_{IN} ≤ 3V	-	20	75	-	30	150	mV
Temperature Coefficient, Referred to V_{IN}	V_{IN} = 3V	-	0.38	-	-	0.55	-	mV/°C
Power Supply Rejection Ratio	Referred to Input, for V_{IN} = 0V	-	2.0	-	-	2.0	-	µV/V
Offset Voltage (A_1 & A_2)	Before Nulling	-	15	25	-	15	50	mV
Wideband Noise	Referred to Input, for V_{IN} = 0V	-	26	-	-	26	-	μV_{RMS}
Output Voltage Swing	R_L = 10kΩ	±12	±14	-	±12	±14	-	V
	R_L = 2kΩ	±10	±13	-	±10	±13	-	V
Power Consumption		-	150	200	-	150	200	mW
Supply Current		-	5	6.7	-	5	6.7	mA

Typical Performance Curves

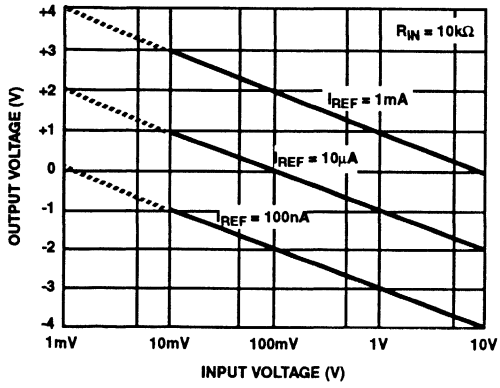


FIGURE 1. TRANSFER FUNCTION FOR VOLTAGE INPUTS (ICL8048 ONLY)

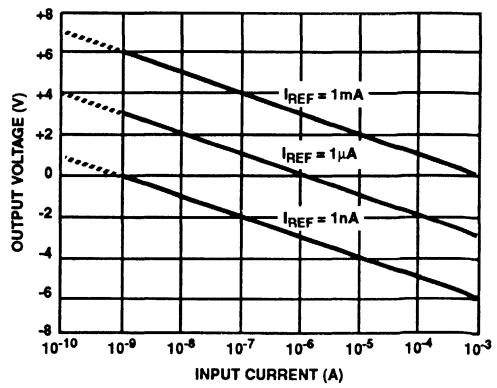


FIGURE 2. TRANSFER FUNCTION FOR CURRENT INPUTS (ICL8048 ONLY)

Typical Performance Curves (Continued)

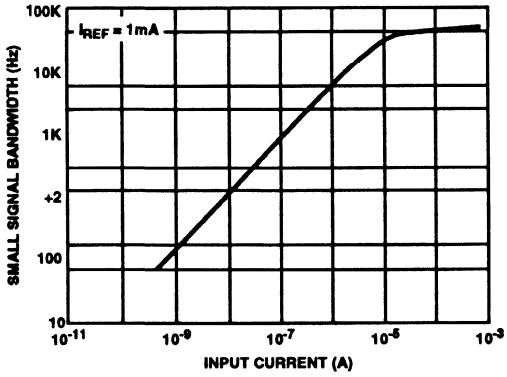


FIGURE 3. SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT CURRENT (ICL8048 ONLY)

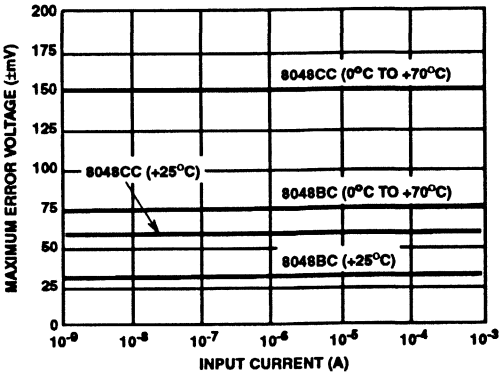


FIGURE 4. MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT CURRENT (ICL8048 ONLY)

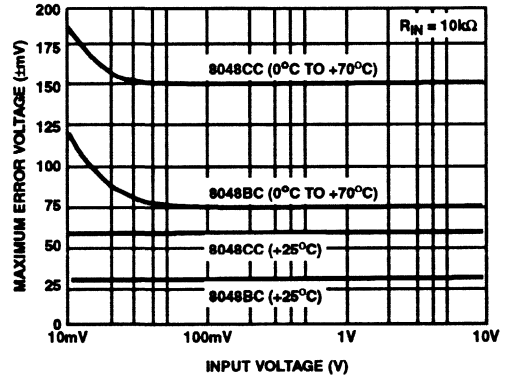


FIGURE 5. MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT VOLTAGE (ICL8048 ONLY)

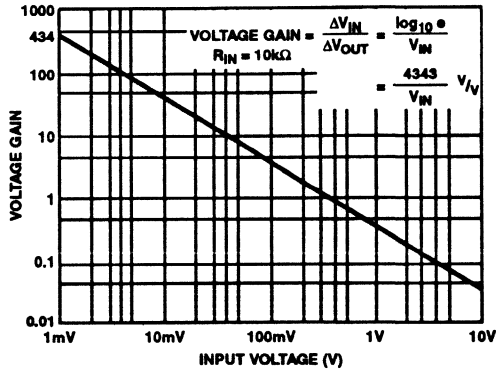


FIGURE 6. SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE FOR R_S = 10kΩ (ICL8048 ONLY)

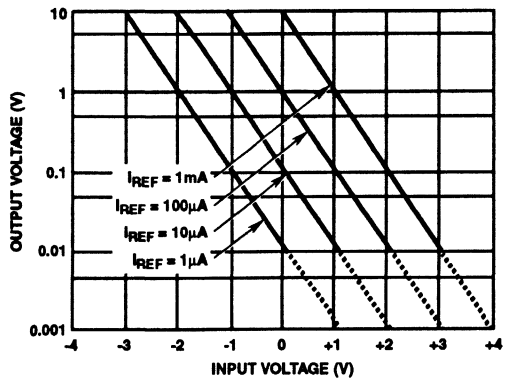


FIGURE 7. TRANSFER FUNCTION (V_{OUT} AS A FUNCTION OF V_{IN}) (ICL8049 ONLY)

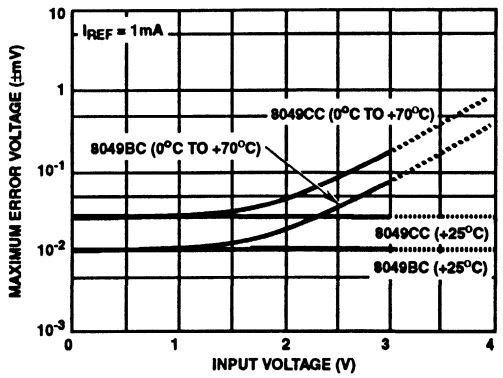


FIGURE 8. MAXIMUM ERROR VOLTAGE REFERRED TO THE INPUT AS A FUNCTION OF V_{IN} (ICL8049 ONLY)

Typical Performance Curves (Continued)

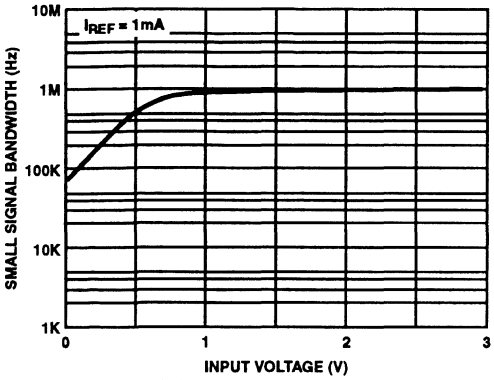


FIGURE 9. SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT VOLTAGE (ICL8049 ONLY)

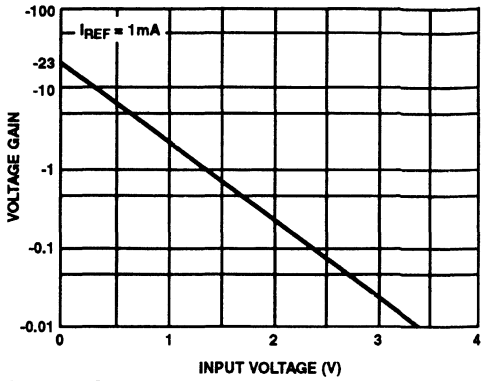


FIGURE 10. SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE (ICL8049 ONLY)

ICL8048 Detailed Description

The ICL8048 relies for its operation on the well known exponential relationship between the collector current and the base emitter voltage of a transistor:

$$I_C = I_S\left[\exp\left(\frac{qV_{BE}}{kT}\right) - 1\right] \quad (1)$$

For base emitter voltages greater than 100mV, Eq. (1) becomes

$$I_C = I_S \exp\left(\frac{qV_{BE}}{kT}\right) \quad (2)$$

From Eq. (2), it can be shown that for two identical transistors operating at different collector currents, the V_{BE} difference (ΔV_{BE}) is given by:

$$\Delta V_{BE} = -2.303 \times \frac{kT}{q} \log_{10}\left[\frac{I_{C1}}{I_{C2}}\right] \quad (3)$$

Referring to Figure 11 it is clear that the potential at the collector of Q_2 is equal to the ΔV_{BE} between Q_1 and Q_2. The output voltage is ΔV_{BE} multiplied by the gain of A_2:

$$V_{OUT} = -2.303\left(\frac{R_1 + R_2}{R_2}\right)\left(\frac{kT}{q}\right)\log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \quad (4)$$

The expression $2.303 \times \frac{kT}{q}$ has a numerical value of 59mV at +25°C; thus in order to generate 1V/decade at the output, the ratio $(R_1 + R_2)/R_2$ is chosen to be 16.9. For this scale factor to hold constant as a function of temperature, the $(R_1 + R_2)/R_2$ term must have a 1/T characteristic to compensate for kT/q.

In the ICL8048 this is achieved by making R1 a thin film resistor, deposited on the monolithic chip. It has a nominal value of 15.9kΩ at +25°C, and its temperature coefficient is carefully designed to provide the necessary compensation. Resistor R_2 is external and should be a low T.C. type; it should have a nominal value of 1kΩ to provide 1V/decade, and must have an adjustment range of ±20% to allow for production variations in the absolute value of R_1.

ICL8048 Offset and Scale Factor Adjustment

A log amp, unlike an op amp, cannot be offset adjusted by simply grounding the input. This is because the log of zero approaches minus infinity; reducing the input current to zero starves Q_1 of collector current and opens the feedback loop around A_1. Instead, it is necessary to zero the offset voltage of A_1 and A_2 separately, and then to adjust the scale factor. Referring to Figure 11, this is done as follows:

1. Temporarily connect a 10kΩ resistor (R_0) between pins 2 and 7. With no input voltage, adjust R_4 until the output of A_2 (pin 7) is zero. Remove R_0.

   Note that for a current input, this adjustment is not necessary since the offset voltage of A_1 does not cause any error for current source inputs.

2. Set $I_{IN} = I_{REF}$ = 1mA. Adjust R_5 such that the output of A_2 (pin 10) is zero.

3. Set I_{IN} = 1µA, I_{REF} = 1mA. Adjust R_2 for V_{OUT} = 3V (for a 1V/decade scale factor) or 6V (for a 2V/decade scale factor).

Step #3 determines the scale factor. Setting I_{IN} = 1µA optimizes the scale factor adjustment over a fairly wide dynamic range, from 1mA to 1nA. Clearly, if the ICL8048 is to be used for inputs which only span the range 100µA to 1mA, it would be better to set I_{IN} = 100µA in Step #3. Similarly, adjustment for other scale factors would require different I_{IN} and V_{OUT} values.

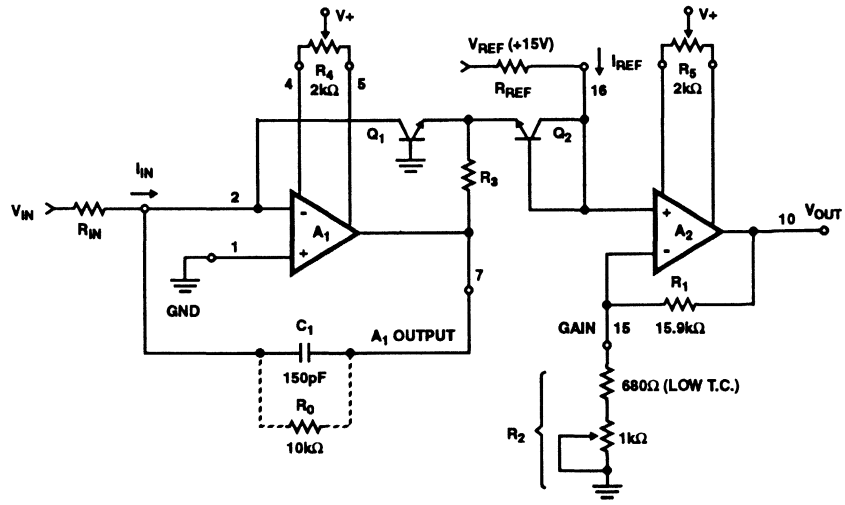


FIGURE 11. ICL8048 OFFSET AND SCALE FACTOR ADJUSTMENT

ICL8049 Detailed Description

The ICL8049 relies on the same logarithmic properties of the transistor as the ICL8048. The input voltage forces a specific ΔV_{BE} between Q_1 and Q_2 (Figure 12). This V_{BE} difference is converted into a difference of collector currents by the transistor pair. The equation governing the behavior of the transistor pair is derived from (2) on the previous page and is as follows:

$$\frac{I_{C1}}{I_{C2}} = \exp\left[\frac{q\Delta V_{BE}}{kT}\right] \quad (5)$$

When numerical values for q/kT are put into this equation, it is found that a ΔV_{BE} of 59mV (at +25°C) is required to change the collector current ratio by a factor of ten. But for ease of application, it is desirable that a 1V change at the input generate a tenfold change at the output. The required input attenuation is achieved by the network comprising R_1 and R_2. In order that scale factors other than one decade per volt may be selected, R_2 is external to the chip. It should have a value of 1kΩ, adjustable ±20%, for one decade per volt. R_1 is a thin film resistor deposited on the monolithic chip; its temperature characteristics are chosen to compensate the temperature dependence of equation 5, as explained on the previous page.

The overall transfer function is as follows:

$$\frac{I_{OUT}}{I_{REF}} = \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{qV_{IN}}{kT}\right] \quad (6)$$

Substituting $V_{OUT} = I_{OUT} \times R_{OUT}$ gives:

$$V_{OUT} = R_{OUT}\, I_{REF} \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{qV_{IN}}{kT}\right] \quad (7)$$

For voltage references equation 7 becomes

$$V_{OUT} = V_{REF} \times \frac{R_{OUT}}{R_{REF}} \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{qV_{IN}}{kT}\right] \quad (8)$$

ICL8049 Offset and Scale Factor Adjustment

As with the log amplifier, the antilog amplifier requires three adjustments. The first step is to null out the offset voltage of A_2. This is accomplished by reverse biasing the base-emitter of Q_2. A_2 then operates as a unity gain buffer with a grounded input. The second step forces V_{IN} = 0; the output is adjusted for V_{OUT} = 10V. This step essentially "anchors" one point on the transfer function. The third step applies a specific input and adjusts the output to the correct voltage. This sets the scale factor. Referring to Figure 12 the exact procedure for 1 decade/volt is as follows:

1. Connect the input (pin #16) to +15V. This reverse biases the base-emitter of Q_2. Adjust R_7 for V_{OUT} = 0V. Disconnect the input from +15V.
2. Connect the input to Ground. Adjust R_4 for V_{OUT} = 10V. Disconnect the input from Ground.
3. Connect the input to a precise 2V supply and adjust R_2 for V_{OUT} = 100mV.

The procedure outlined above optimizes the performance over a 3 decade range at the output (i.e., V_{OUT} from 10mV) to 10V). For a more limited range of output voltages, for example 1V to 10V, it would be better to use a precise 1V supply and adjust for V_{OUT} = 1V. For other scale factors and/or starting points, different values for R_2 and R_{REF} will be needed, but the same basic procedure applies.

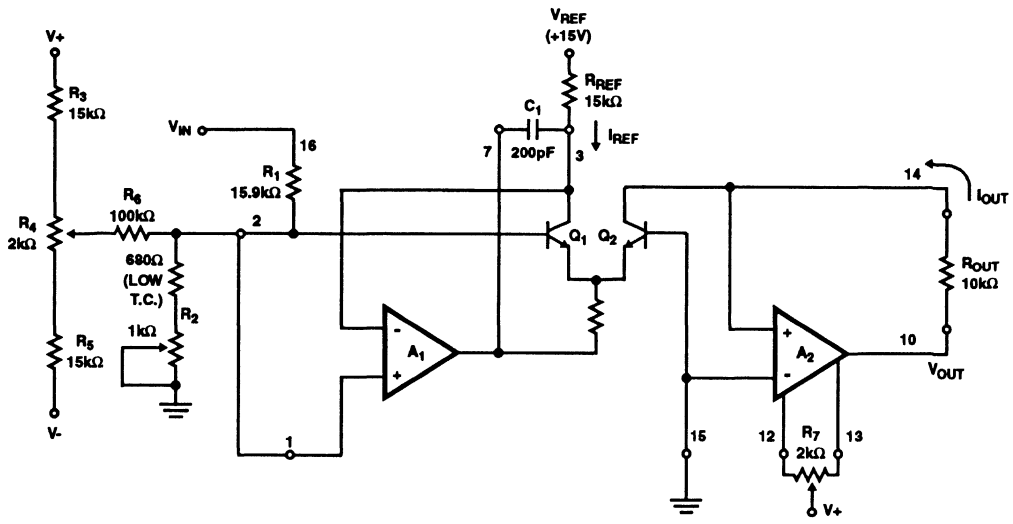


FIGURE 12. ICL8049 OFFSET AND SCALE FACTOR ADJUSTMENT

Applications Information

ICL8048 Scale Factor Adjustment

The scale factor adjustment procedures outlined previously for the ICL8048 and ICL8049, are primarily directed towards setting up 1V (ΔV_{OUT}) per decade (ΔI_{IN} or ΔV_{IN}) for the log amp, or one decade (ΔV_{OUT}) per volt (ΔV_{IN}) for the antilog amp.

This corresponds to K = 1 in the respective transfer functions:

$$\text{Log Amp: } V_{OUT} = -K \log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \quad (9)$$

$$\text{Antilog Amp: } V_{OUT} = R_{OUT} I_{REF} 10^{\left(\frac{-V_{IN}}{K}\right)} \quad (10)$$

By adjusting R_2 (Figure 11 and Figure 12) the scale factor "K" in equation 9 and 10 can be varied. The effect of changing K is shown graphically in Figure 13 for the log amp, and Figure 14 for the antilog amp. The nominal value of R_2 required to give a specific value of K can be determined from equation 11. It should be remembered that R_1 has a ±20% tolerance in absolute value, so that allowance shall be made for adjusting the nominal value of R_2 by ±20%.

$$R_2 = \frac{941}{(K - 0.059)}\Omega \quad (11)$$

ICL8048 Automatic Offset Nulling Circuit

The ICL8048 is fundamentally a logarithmic current amplifier. It can be made to act as a voltage amplifier by placing a resistor between the current input and the voltage source but, since $I_{IN} = (V_{IN} - V_{OFFSET})/R_{IN}$, this conversion is accurate only when V_{IN} is much greater than the offset voltage. A substantial reduction of V_{OFFSET} would allow voltage operation over a 120dB range.

Figure 15 shows the ICL8048 in an automatic offset nulling configuration using the ICL7650S. The extremely low offset voltage of the ICL7650S forces its non-inverting input (and thus pin 2 of the ICL8048) to the same potential as its inverting input by nulling the first stage of the log amp. Since V_{OFFSET} is now within a few µV of ground potential, R_{IN} can perform its voltage to current conversion much more accurately, and without an offset trimmer pot. Step 1 of the offset and scale factor adjustment is eliminated, simplifying calibration.

NOTE: The ICL7650S op amp has a maximum supply voltage of 18V. The ICL8048 will operate at this voltage, but I_{REF} must be limited to 200µA or less for proper calibration and operation. Best performance will be achieved when the ICL7650S has a ±3V to ±8V supply and the ICL8048 is at its recommended ±15V supply. See A053 for a method of powering the ICL7650S from a ±15V source.

Frequency Compensation

Although the op amps in both the ICL8048 and the ICL8049 are compensated for unity gain, some additional frequency compensation is required. This is because the log transistors in the feedback loop add to the loop gain. In the ICL8048, 150pF should be connected between Pins 2 and 7 (Figure 11). In the ICL8049, 200pF between Pins 3 and 7 is recommended (Figure 12).

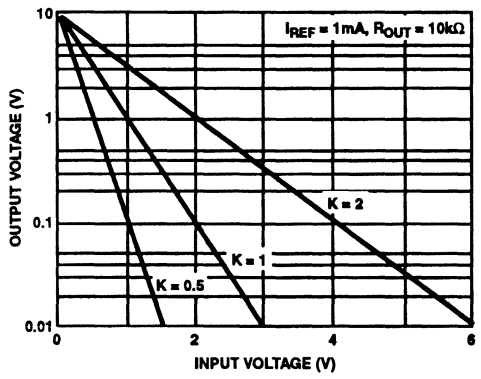


FIGURE 13. EFFECT OF VARYING "K" ON THE ANTILOG AMPLIFIER

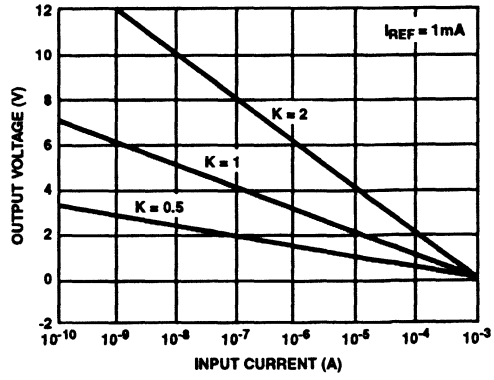


FIGURE 14. EFFECT OF VARYING "K" ON THE LOG AMPLIFIER

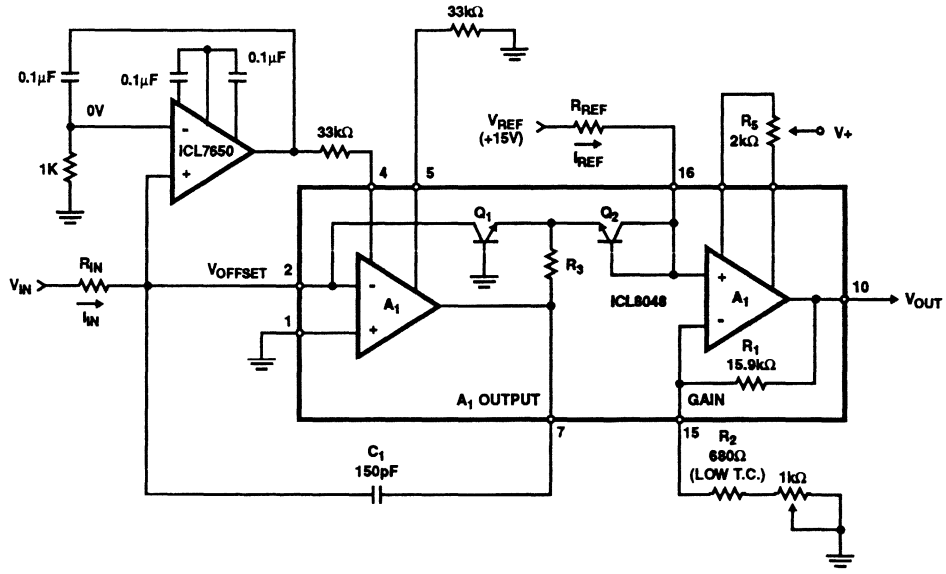


FIGURE 15. ICL8048 OFFSET NULLED BY ICL7650

Error Analysis

Performing a meaningful error analysis of a circuit containing a log and antilog amplifiers is more complex than dealing with a similar circuit involving only op amps. In this data sheet every effort has been made to simplify the analysis task, without in any way compromising the validity of the resultant numbers.

The key difference in making error calculations in log/antilog amps, compared with op amps, is that the gain of the former is a function of the input signal level. Thus, it is necessary, when referring errors from output to input, or vice versa, to check the input voltage level, then determine the gain of the circuit by referring to the graphs given in the Typical Performance Curves section.

The various error terms in the log amplifier, the ICL8048, are Referred To the Output (RTO) of the device. The error terms in the antilog amplifier, the ICL8049, are Referred To the Input (RTI) of the device. The errors are expressed in this way because in the majority of systems a number of log amps interface with an antilog amp, as shown in Figure 16.

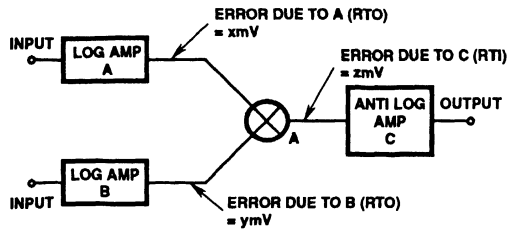


FIGURE 16.

It is very straightforward to estimate the system error at node (A) by taking the square root of the sum-of-the-squares of the errors of each contributing block.

$$\text{Total Error} = \sqrt{x^2 + y^2 + z^2}\ \text{at (A)}$$

If required, this error can be referred to the system output through the voltage gain of the antilog circuit, using the voltage gain versus input voltage plot.

The numerical values of x, y, and z in the above equation are obtained from the maximum error voltage plots. For example, with the ICL8048BC, the maximum error at the output is 30mV at +25°C. This means that the measured output will be within 30mV of the theoretical transfer function, provided the unit has been adjusted per the procedures described previously. Figure 17 illustrates this point.

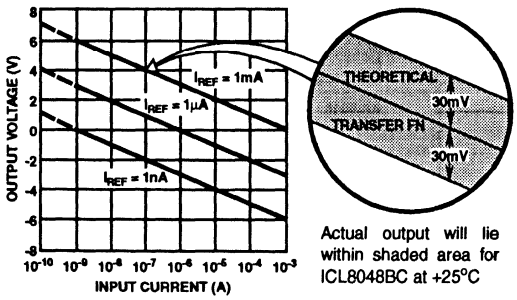


FIGURE 17. TRANSFER FUNCTION FOR CURRENT INPUTS

To determine the maximum error over the operating temperature range, the 0°C to +70°C absolute error values given in the table of electrical specifications should be used. For intermediate temperatures, assume a linear increase in the error between the +25°C value and the +70°C value.

For the antilog amplifier, the only difference is that the error refers to the input, i.e., the horizontal axis. It will be noticed that the maximum error voltage of the ICL8049, over the temperature range, is strongly dependent on the input voltage. This is because the output amplifier, A_2, has an offset voltage drift which is directly transmitted to the output. When this error is referred to the input, it must be divided by the voltage gain, which is input voltage dependent. At V_{IN} = 3V, for example, errors at the output are multiplied by 1/.023 (=43.5) when referred to the input.

It is important to note that both the ICL8048 and the ICL8049 require positive values of I_{REF}, and the input (ICL8048) or output (ICL8049) currents (or voltages) respectively must also be positive. Application of negative I_{IN} to the ICL8048 or negative I_{REF} to either circuit will cause malfunction, and if maintained for long periods, would lead to device degradation. Some protection can be provided by placing a diode between pin 7 and ground.

Setting Up the Reference Current

In both the ICL8048 and ICL8049 the input current reference pin (I_{REF}) is not a true virtual ground. For the ICL8048, a fraction of the output voltage is seen on Pin 16 (Figure 11). This does not constitute an appreciable error provided V_{REF} is much greater than this voltage. A 10V or 15V reference satisfies this condition. For the ICL8049, a fraction of the input voltage appears on Pin 3 (Figure 12), placing a similar restraint on the value of V_{REF}.

Alternatively, I_{REF} can be provided from a true current source. One method of implementing such a current source is shown in Figure 18.

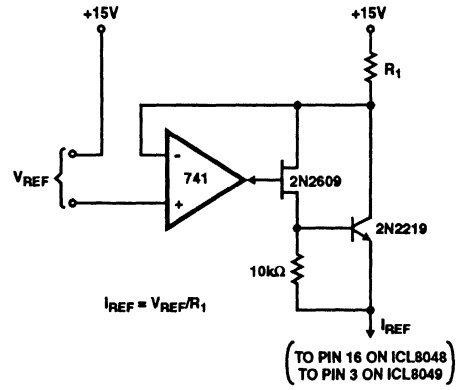


FIGURE 18.

Log of Ratio Circuit, Division

The ICL8048 may be used to generate the log of a ratio by modulating the I_{REF} input. The transfer function remains the same, as defined by equation 9:

$$V_{OUT} = -K\log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \quad (9)$$

Clearly it is possible to perform division using just one ICL8048, followed by an ICL8049. For multiplication, it is generally necessary to use two log amps, summing their outputs into an antilog amp.

To avoid the problems caused by the I_{REF} input not being a true virtual ground (discussed in the previous section), the circuit of Figure 18 is again recommended if the I_{REF} input is to be modulated.

Definition of Terms

In the definitions which follow, it will be noted that the various error terms are referred to the output of the log amp, and to the input of the antilog amp. The reason for this is explained on the previous page.

Dynamic Range. The dynamic range of the ICL8048 refers to the range of input voltages or currents over which the device is guaranteed to operate. For the ICL8049 the dynamic range refers to the range of output voltage over which the device is guaranteed to operate.

Error, Absolute Value. The absolute error is a measure of the deviation from the theoretical transfer function, after performing the offset and scale factor adjustments as outlined, (ICL8048) or (ICL8049). It is expressed in mV and referred to the linear axis of the transfer function plot. Thus, in the case of the ICL8048, it is a measure of the deviation from the theoretical output voltage for a given input current or voltage. For the ICL8049 it is a measure of the deviation from the theoretical input voltage required to generate a specific output voltage.

The absolute error specification is guaranteed over the dynamic range.

Error, % of Full Scale. The error as a percentage of full scale can be obtained from the following relationship:

$$\text{Error, \% of Full Scale} = \frac{100 \times \text{Error, absolute value}}{\text{Full Scale Output Voltage}}$$

Temperature Coefficient of V_{OUT} or V_{IN}. For the ICL8048 the temperature coefficient refers to the drift with temperature of V_{OUT} for a constant input current.

For the ICL8049 it is the temperature drift of the input voltage required to hold a constant value of V_{OUT}.

Power Supply Rejection Ratio. The ratio of the voltage change in the linear axis of the transfer function (V_{OUT} for the ICL8048, V_{IN} for the ICL8049) to the change in the supply voltage, assuming that the log axis is held constant.

Wideband Noise. For the ICL8048, this is the noise occurring at the output under the specified conditions. In the case of the ICL8049, the noise is referred to the input.

Scale Factor. For the log amp, the scale factor (K) is the voltage change at the output for a decade (i.e. 10:1) change at the input. For the antilog amp, the scale factor is the voltage change required at the input to cause a one decade change at the output. See equations 9 and 10.

Application Notes

For further applications assistance, see A007 "The ICL8048/8049 Monolithic Log-Antilog Amplifiers".

HARRIS SEMICONDUCTOR

ICM7242

March 1993

Long Range Fixed Timer

Features

- **Replaces the 2242 in Most Applications**
- **Timing From Microseconds to Days**
- **Cascadeable**
- **Monostable or Astable Operation**
- **Wide Supply Voltage Range: 2V - 16V**
- **Low Supply Current: 115μA at 5V**

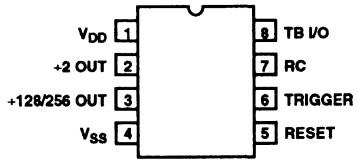
Description

The ICM7242 is a CMOS timer/counter circuit consisting of an RC oscillator followed by an 8-bit binary counter. It will replace the 2242 in most applications, with a significant reduction in the number of external components.

Three outputs are provided. They are the oscillator output, and buffered outputs from the first and eighth counters.

Pinout

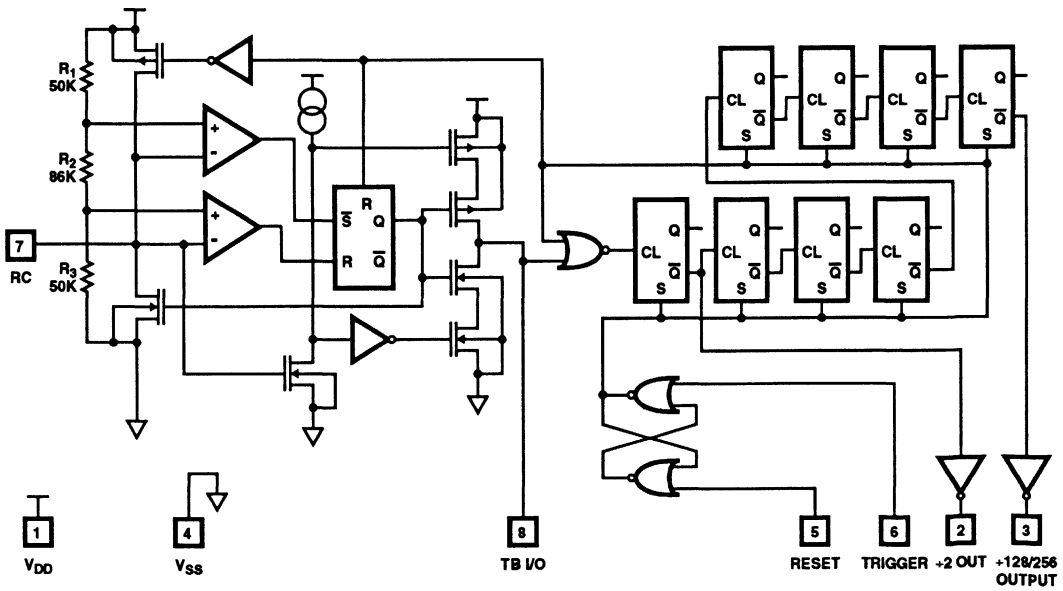
ICM7242
(PDIP, SOIC)
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7242IPA	-25°C to +85°C	8 Lead Plastic DIP
ICM7242CBA	0°C to +70°C	8 Lead SOIC

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2866.1**

Absolute Maximum Ratings

Supply Voltage (V_{DD} to V_{SS}) 18V
Input Voltage (Note 1)
Terminals (Pins 5, 6, 7, 8) ..... (V_{SS} -0.3V) to (V_{DD} +0.3V)
Maximum Continuous Output Current (Each Output) 50mA
Power Dissipation (Note 2) 200mW
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
ICM7242I ..... -25°C to +85°C
ICM7242C ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

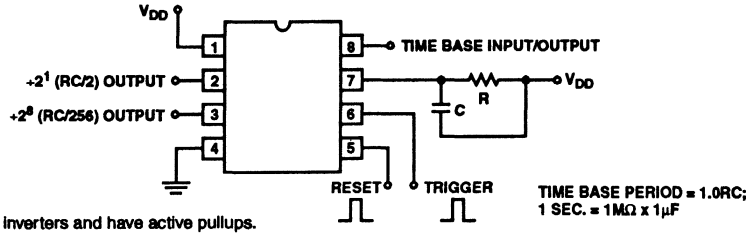
V_{DD} = 5V, T_A = +25°C, R = 10kΩ, C = 0.1µF, V_{SS} = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Guaranteed Supply Voltage	V_{DD}		2	-	16	V
Supply Current	I_{DD}	Reset	-	125	-	µA
		Operating, R = 10kΩ, C = 0.1µF	-	340	800	µA
		Operating, R = 1MΩ, C = 0.1µF	-	220	600	µA
		TB Inhibited, RC Connected to V_{SS}	-	225	-	µA
Timing Accuracy			-	5	-	%
RC Oscillator Frequency Temperature Drift	$\Delta f/\Delta t$	Independent of RC Components	-	250	-	ppm/°C
Time Base Output Voltage	V_{OTB}	I_{SOURCE} = 100µA	-	3.5	-	V
		I_{SINK} = 1.0mA	-	0.40	-	V
Time Base Output Leakage Current	I_{TBLK}	RC = Ground	-	-	25	µA
Trigger Input Voltage	V_{TRIG}	V_{DD} = 5V	-	1.6	2.0	V
		V_{DD} = 15V	-	3.5	4.5	V
Reset Input Voltage	V_{RST}	V_{DD} = 5V	-	1.3	2.0	V
		V_{DD} = 15V	-	2.7	4.0	V
Trigger/Reset Input Current	I_{TRIG}, I_{RST}		-	10	-	µA
Max Count Toggle Rate	f_T	V_{DD} = 2V (Counter/Divider Mode)	-	1	-	MHz
		V_{DD} = 5V (Counter/Divider Mode)	2	6	-	MHz
		V_{DD} = 15V (Counter/Divider Mode)	-	13	-	MHz
		50% Duty Cycle Input with Peak to Peak Voltages Equal to V_{DD} and V_{SS}				
Output Saturation Voltage	V_{SAT}	All Outputs Except TB Output V_{DD} = 5V, I_{OUT} = 3.2mA	-	0.22	0.4	V
Output Sourcing Current	I_{SOURCE}	V_{DD} = 5V Terminals 2 & 3, V_{OUT} = 1V	-	300	-	µA
MIN Timing Capacitor (Note 3)	C_T		10	-	-	pF
Timing Resistor Range (Note 3)	R_T	V_{DD} = 2 - 16V	1K	-	22M	Ω

NOTES:

1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established and, that in multiple supply systems, the supply to the ICM7242 be turned on first.
2. Derate at -2mW/°C above +25°C.
3. For design only, not tested.

Test Circuit



NOTE: $+2^1$ and $+2^8$ outputs are inverters and have active pullups.

FIGURE 1.

Typical Performance Curves

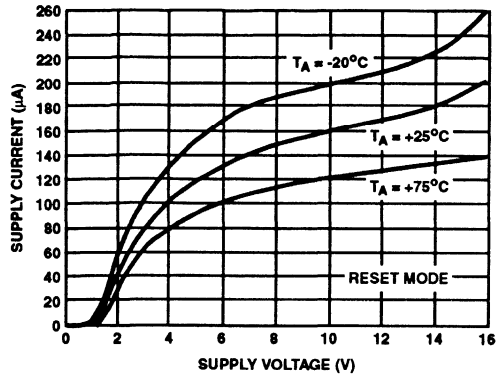


FIGURE 2. SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

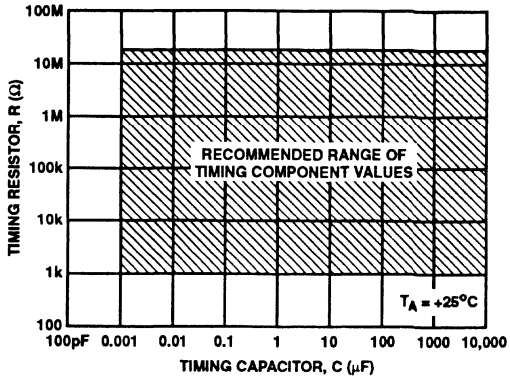


FIGURE 3. RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING

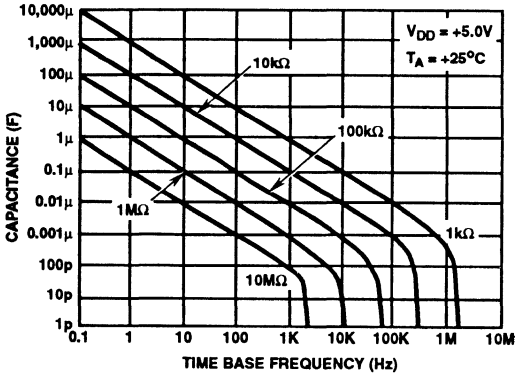


FIGURE 4. TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C

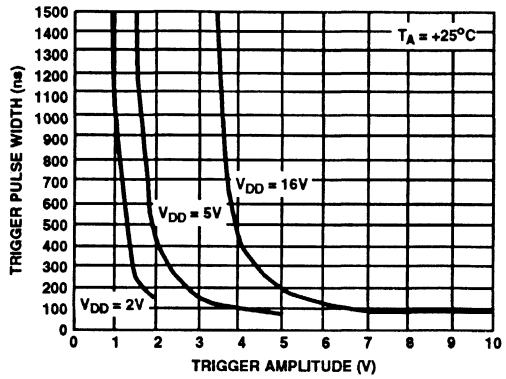


FIGURE 5. MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE

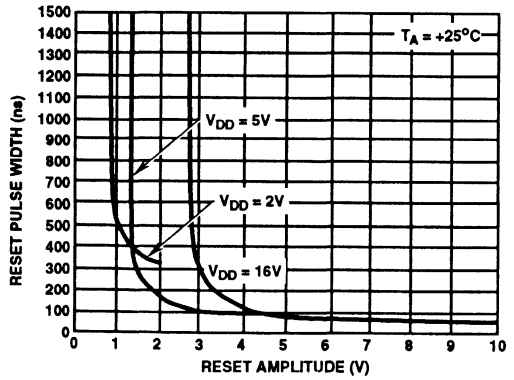


FIGURE 6. MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE

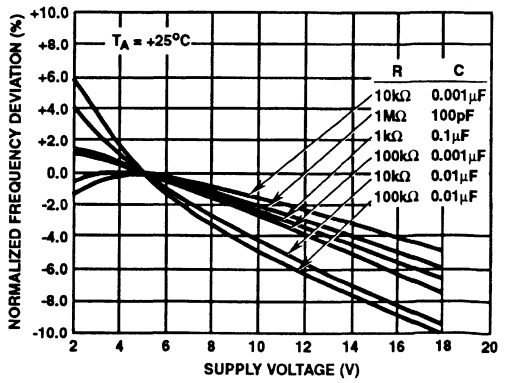


FIGURE 7. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE

Typical Performance Curves (Continued)

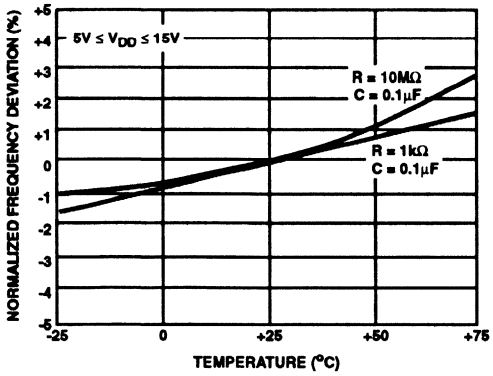


FIGURE 8. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE

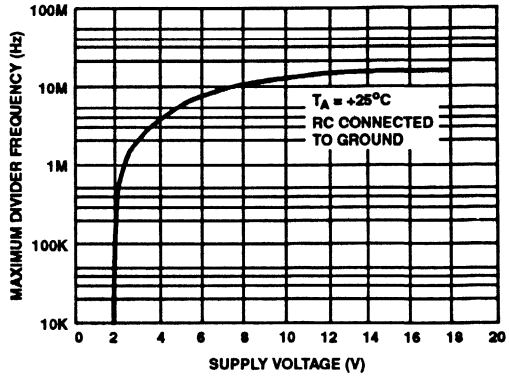


FIGURE 9. MAXIMUM DIVIDER FREQUENCY vs SUPPLY VOLTAGE

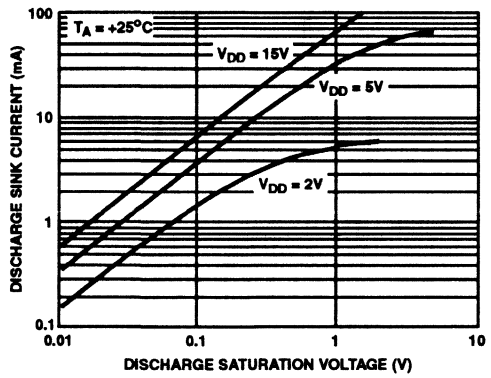


FIGURE 10. DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE

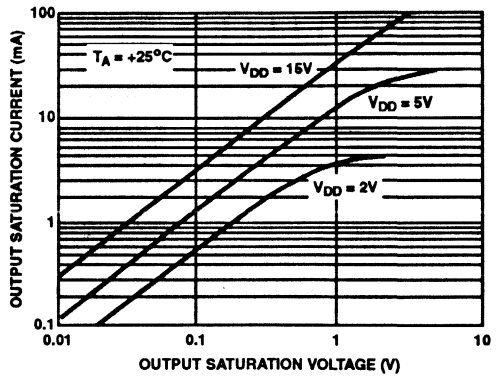


FIGURE 11. OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE

Operating Considerations

Shorting the RC terminal or output terminals to V_{DD} may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

There is a limitation of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in Figure 3. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200kHz.

The timing capacitor should be connected between the RC pin and the positive supply rail, V_{DD}, as shown in Figure 1. When system power is turned off, any charge remaining on the capacitor will be discharged to ground through a large internal diode between the RC node and V_{SS}. Do NOT reference the timing capacitor to ground, since there is no high current path in this direction to safely discharge the capacitor when power is turned off. The discharge current from such a configuration could potentially damage the device.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to the supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform; this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM7242.

The ICM7242 is a non-programmable timer whose principal applications will be very low frequency oscillators and long range timers; it makes a much better low frequency oscilla-

tor/timer than a 555 or ICM7555, because of the on-chip 8-bit counter. Also, devices can be cascaded to produce extremely low frequency signals.

Because outputs will not be AND'd, output inverters are used instead of open drain N-channel transistors, and the external resistors used for the 2242 will not be required for the ICM7242. The ICM7242 will, however, plug into a socket for the 2242 having these resistors.

The timing diagram for the ICM7242 is shown in Figure 12. Assuming that the device is in the RESET mode, which occurs on power up or after a positive signal on the RESET terminal (if TRIGGER is low), a positive edge on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states. Thus, the outputs on terminals 2 and 3 change from high to low states. After 128 negative timebase edges, the $+2^8$ output returns to the high state.

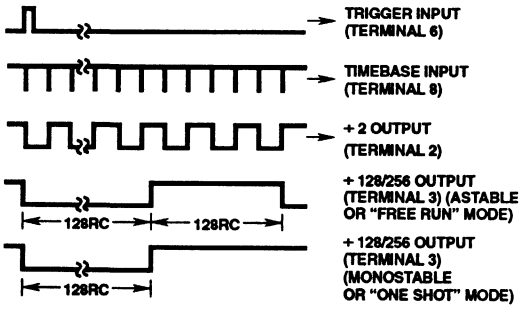


FIGURE 12. TIMING DIAGRAMS OF OUTPUT WAVEFORMS FOR THE ICM7242 (COMPARE WITH FIGURE 16)

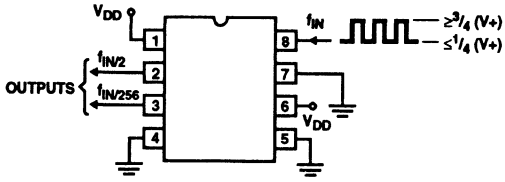


FIGURE 13. USING THE ICM7242 AS A RIPPLE COUNTER (DIVIDER)

To use the 8-bit counter without the timebase, terminal 7 (RC) should be connected to ground and the outputs taken from terminals 2 and 3.

The ICM7242 may be used for a very low frequency square wave reference. For this application the timing components are more convenient than those that would be required by a 555 timer. For very low frequencies, devices may be cascaded (see Figure 14).

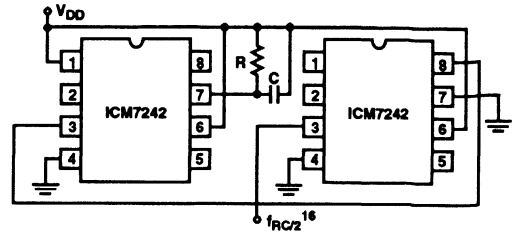


FIGURE 14. LOW FREQUENCY REFERENCE (OSCILLATOR)

For monostable operation the $+2^8$ output is connected to the RESET terminal. A positive edge on TRIGGER initiates the cycle (NOTE: TRIGGER overrides RESET).

The ICM7242 is superior in all respects to the 2242 except for initial accuracy and oscillator stability. This is primarily due to the fact that high value p- resistors have been used on the ICM7242 to provide the comparator timing points.

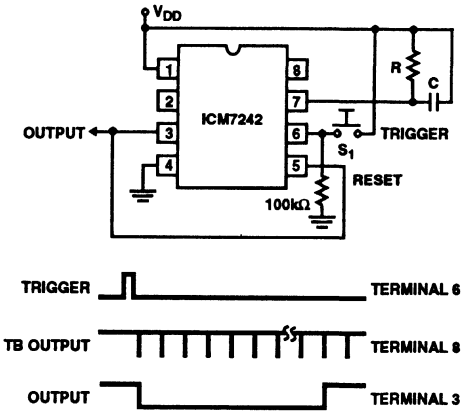


FIGURE 15. MONOSTABLE OPERATION

Comparing the ICM7242 With the 2242

	ICM7242	2242
Operating Voltage	2V - 16V	4V - 15V
Operating Temperature Range	-25°C to +85°C	0°C to +70°C
Supply Current, V_{DD} = 5V	0.7mA Max.	7mA Max.
Pullup Resistors		
TB Output	No	Yes
+2 Output	No	Yes
+256 Output	No	Yes
Toggle Rate	3.0MHz	0.5MHz
Resistor to Inhibit Oscillator	No	Yes
Resistor in Series with Reset for Monostable Operation	No	Yes
Capacitor TB Terminal for HF Operation	No	Sometimes

By selection of R and C, a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as shown in Figure 16.

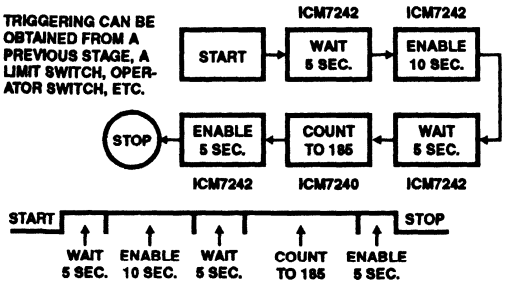
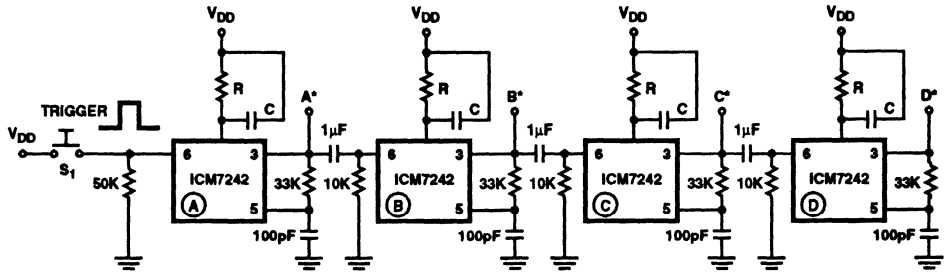


FIGURE 16.

By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

Sequence Timing

- Process Control
- Machine Automation
- Electro-Pneumatic Drivers
- Multi Operation (Serial or Parallel Controlling)



*SELECT RC VALUES FOR DESIRED "ON TIME" FOR EACH ICM7242

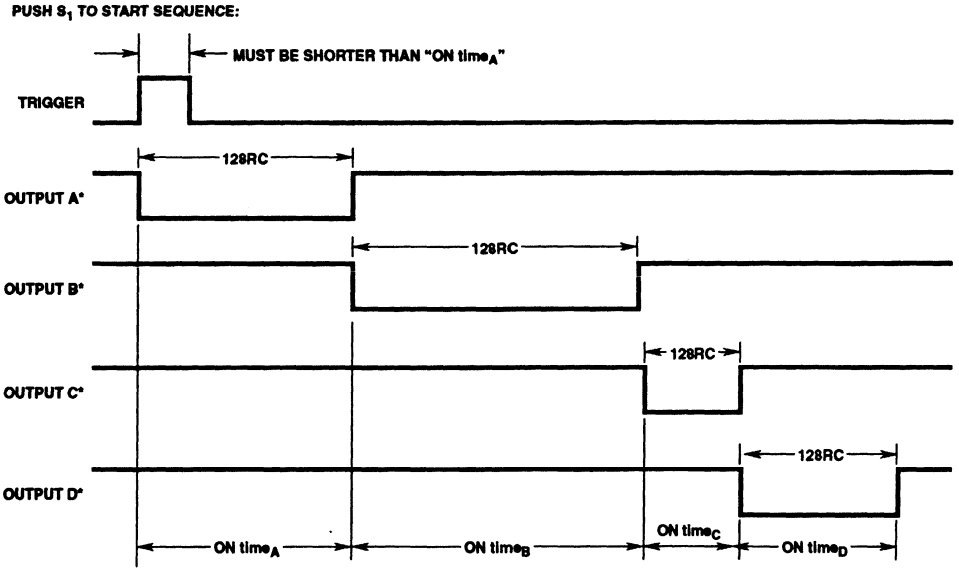


FIGURE 17. SEQUENCE TIMER

HARRIS SEMICONDUCTOR

ICM7555, ICM7556

March 1993

General Purpose Timers

Features

- Exact Equivalent In Most Cases for SE/NE555/556 or TLC555/556
- Low Supply Current - 60μA Typ. (ICM7555) 120μA Typ. (ICM7556)
- Extremely Low Trigger, Threshold and Reset Currents - 20pA Typical
- High Speed Operation - 1MHz Typical
- Wide Operation Supply Voltage Range Guaranteed 2V to 18V
- Normal Reset Function - No Crowbarring of Supply During Output Transition
- Can be Used with Higher Impedance Timing Elements than Regular 555/6 for Longer RC Time Constants
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Output Source/Sink Driver can Drive TTL/CMOS
- Typical Temperature Stability of 0.005% per °C at +25°C
- Outputs have Very Low Offsets, HI and LO

Applications

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

Description

The ICM7555 and ICM7556 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$ and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the ICM7555 and ICM7556 are stable controllers capable of producing accurate time delays or frequencies. The ICM7556 is a dual ICM7555, with the two timers operating independently of each other, sharing only V+ and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555/6 devices, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

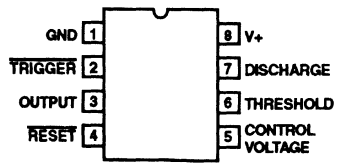
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7555CBA	0°C to +70°C	8 Lead SOIC
ICM7555IBA	-25°C to +85°C	8 Lead SOIC
ICM7555IPA	-25°C to +85°C	8 Lead Plastic DIP
ICM7555ITV	-25°C to +85°C	8 Pin TO-99 Can
ICM7555MTV*	-55°C to +125°C	8 Pin TO-99 Can
ICM7556IPD	-25°C to +85°C	14 Lead Plastic DIP
ICM7556MJD*	-55°C to +125°C	14 Lead Ceramic DIP

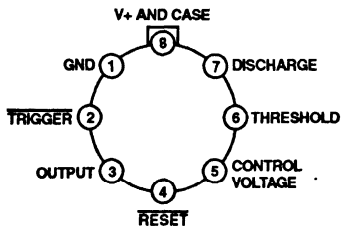
* Add /883B to part number if 883B processing is desired.

Pinouts

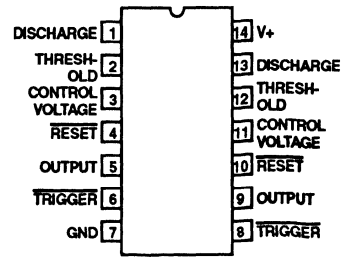
ICM7555 (PDIP, SOIC)
TOP VIEW



ICM7555 (TO-99 CAN)
TOP VIEW



ICM7556 (PDIP, CDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2867.1

Specifications ICM7555

Absolute Maximum Ratings

Supply Voltage ..... +18V
Input Voltage
Trigger, Control Voltage, Threshold,
Reset (Note1) ..... V+ +0.3V to GND -0.3V
Output Current 100mA
Power Dissipation (Note 2), ICM7555 ..... 200mW
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range (Note 2)
ICM7555CX ..... 0°C to +70°C
ICM7555IX ..... -25°C to +85°C
ICM7555MX ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications ICM7555

PARAMETERS	SYMBOL	TEST CONDITIONS	ICM7555C, I, M T_A = +25°C			ICM7555M -55°C ≤ T_A ≤ +125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Static Supply Current	I+	V_{DD} = 5V	-	40	200	-	-	300	µA
		V_{DD} = 15V	-	60	300	-	-	300	µA
Monostable Timing Accuracy		R_A = 10K, C = 0.1µF, V_{DD} = 5V	-	2	-	-	-	-	%
			-	-	-	858	-	1161	µs
Drift with Temp (Note 3)		V_{DD} = 5V	-	-	-	-	150	-	ppm/°C
		V_{DD} = 10V	-	-	-	-	200	-	ppm/°C
		V_{DD} = 15V	-	-	-	-	250	-	ppm/°C
Drift with Supply (Note 3)		V_{DD} = 5V to 15V	-	0.5	-	-	0.5	-	%/V
Astable Timing Accuracy		$R_A = R_B$ = 10K, C = 0.1µF, V_{DD} = 5V	-	2	-	-	-	-	%
			-	-	-	1717	-	2323	µs
Drift with Temp (Note 3)		V_{DD} = 5V	-	-	-	-	150	-	ppm/°C
		V_{DD} = 10V	-	-	-	-	200	-	ppm/°C
		V_{DD} = 15V	-	-	-	-	250	-	ppm/°C
Drift with Supply (Note 3)		V_{DD} = 5V to 15V	-	0.5	-	-	0.5	-	%/V
Threshold Voltage	V_{TH}	V_{DD} = 15V	62	67	71	61	-	72	% V_{DD}
Trigger Voltage	V_{TRIG}	V_{DD} = 15V	28	32	36	27	-	37	% V_{DD}
Trigger Current	I_{TRIG}	V_{DD} = 15V	-	-	10	-	-	50	nA
Threshold Current	I_{TH}	V_{DD} = 15V	-	-	10	-	-	50	nA
Control Voltage	V_{CV}	V_{DD} = 15V	62	67	71	61	-	72	% V_{DD}
Reset Voltage	V_{RST}	V_{DD} = 2V to 15V	0.4	-	1.0	0.2	-	1.2	V
Reset Current	I_{RST}	V_{DD} = 15V	-	-	10	-	-	50	nA
Discharge Leakage	I_{DIS}	V_{DD} = 15V	-	-	10	-	-	50	nA
Output Voltage Drop	V_{OL}	V_{DD} = 15V, I_{SINK} = 20mA	-	0.4	1.0	-	-	1.25	V
		V_{DD} = 5V, I_{SINK} = 3.2mA	-	0.2	0.4	-	-	0.5	V
Output Voltage Drop	V_{OH}	V_{DD} = 15V, I_{SOURCE} = 0.8mA	14.3	14.6	-	14.2	-	-	V
		V_{DD} = 5V, I_{SOURCE} = 0.8mA	4.0	4.3	-	3.8	-	-	V
Discharge Output Voltage Drop	V_{DIS}	V_{DD} = 5V, I_{SINK} = 15mA	-	0.2	0.4	-	-	0.6	V
		V_{DD} = 15V, I_{SINK} = 15mA	-	-	-	-	-	0.4	V
Supply Voltage (Note 3)	V+	Functional Oper.	2.0	-	18.0	3.0	-	16.0	V
Output Rise Time (Note 3)	t_R	R_L = 10M, C_L = 10pF, V_{DD} = 5V	-	75	-	-	-	-	ns
Output Fall Time (Note 3)	t_F	R_L = 10M, C_L = 10pF, V_{DD} = 5V	-	75	-	-	-	-	ns
Oscillator Frequency (Note 3)	f_{MAX}	V_{DD} = 5V, R_A = 470Ω, R_B = 270Ω, C = 200pF	-	1	-	-	-	-	MHz

NOTES:

1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V+ +0.3V or less than V- -0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.
2. Junction temperatures should not exceed +135°C and the power dissipation must be limited to 20mW at +125°C. Below +125°C power dissipation may be increased to 300mW at +25°C. Derating factor is approximately 3mW/°C (7556) or 2mW/°C (7555).
3. These parameters are based upon characterization data and are not tested.

Absolute Maximum Ratings

Supply Voltage ..... +18V
Input Voltage
Trigger, Control Voltage, Threshold,
Reset (Note1) ..... V+ +0.3V to GND -0.3V
Output Current 100mA
Power Dissipation (Note 2), ICM7556 ..... 300mW
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range (Note 2)
ICM7556IX ..... -25°C to +85°C
ICM7556MX ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

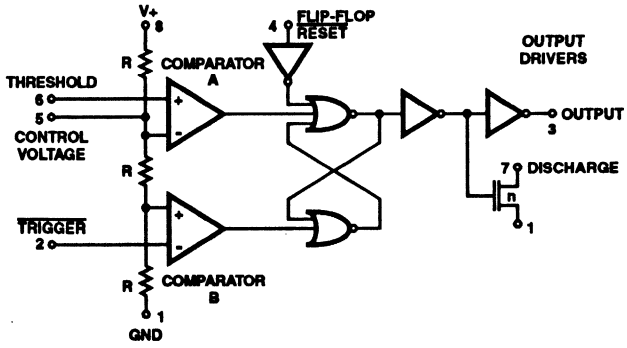
ICM7556, T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	ICM7556I, M T_A = +25°C			ICM7556M -55°C ≤ T_A ≤ +125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Static Supply Current	I+	V_{DD} = 5V	-	80	400	-	-	600	µA
		V_{DD} = 15V	-	120	600	-	-	600	µA
Monostable Timing Accuracy		R_A = 10K, C = 0.1µF, V_{DD} = 5V	-	2	-	-	-	-	%
			-	-	-	858	-	1161	µs
Drift with Temp (Note 3)		V_{DD} = 5V	-	-	-	-	150	-	ppm/°C
		V_{DD} = 10V	-	-	-	-	200	-	ppm/°C
		V_{DD} = 15V	-	-	-	-	250	-	ppm/°C
Drift with Supply (Note 3)		V_{DD} = 5V to 15V	-	0.5	-	-	0.5	-	%/V
Astable Timing Accuracy		R_A = R_B = 10K, C = 0.1µF, V_{DD} = 5V	-	2	-	-	-	-	%
			-	-	-	1717	-	2323	µs
Drift with Temp (Note 3)		V_{DD} = 5V	-	-	-	-	150	-	ppm/°C
		V_{DD} = 10V	-	-	-	-	200	-	ppm/°C
		V_{DD} = 15V	-	-	-	-	250	-	ppm/°C
Drift with Supply (Note 3)		V_{DD} = 5V to 15V	-	0.5	-	-	0.5	-	%/V
Threshold Voltage	V_{TH}	V_{DD} = 15V	62	67	71	61	-	72	% V_{DD}
Trigger Voltage	V_{TRIG}	V_{DD} = 15V	28	32	36	27	-	37	% V_{DD}
Trigger Current	I_{TRIG}	V_{DD} = 15V	-	-	10	-	-	50	nA
Threshold Current	I_{TH}	V_{DD} = 15V	-	-	10	-	-	50	nA
Control Voltage	V_{CV}	V_{DD} = 15V	62	67	71	61	-	72	% V_{DD}
Reset Voltage	V_{RST}	V_{DD} = 2V to 15V	0.4	-	1.0	0.2	-	1.2	V
Reset Current	I_{RST}	V_{DD} = 15V	-	-	10	-	-	50	nA
Discharge Leakage	I_{DIS}	V_{DD} = 15V	-	-	10	-	-	50	nA
Output Voltage Drop	V_{OL}	V_{DD} = 15V, I_{SINK} = 20mA	-	0.4	1.0	-	-	1.25	V
		V_{DD} = 5V, I_{SINK} = 3.2mA	-	0.2	0.4	-	-	0.5	V
Output Voltage Drop	V_{OH}	V_{DD} = 15V, I_{SOURCE} = 0.8mA	14.3	14.6	-	14.2	-	-	V
		V_{DD} = 5V, I_{SOURCE} = 0.8mA	4.0	4.3	-	3.8	-	-	V
Discharge Output Voltage Drop	V_{DIS}	V_{DD} = 5V, I_{SINK} = 15mA	-	0.2	0.4	-	-	0.6	V
		V_{DD} = 15V, I_{SINK} = 15mA	-	-	-	-	-	0.4	V
Supply Voltage (Note 3)	V+	Functional Oper.	2.0	-	18.0	3.0	-	16.0	V
Output Rise Time (Note 3)	t_R	R_L = 10M, C_L = 10pF, V_{DD} = 5V	-	75	-	-	-	-	ns
Output Fall Time (Note 3)	t_F	R_L = 10M, C_L = 10pF, V_{DD} = 5V	-	75	-	-	-	-	ns
Oscillator Frequency (Note 3)	f_{MAX}	V_{DD} = 5V, R_A = 470Ω, R_B = 270Ω, C = 200pF	-	1	-	-	-	-	MHz

NOTES:

1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V+ +0.3V or less than V- -0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.
2. Junction temperatures should not exceed +135°C and the power dissipation must be limited to 20mW at +125°C. Below +125°C power dissipation may be increased to 300mW at +25°C. Derating factor is approximately 3mW/°C (7556) or 2mW/°C (7555).
3. These parameters are based upon characterization data and are not tested.

Functional Diagram



NOTE: This functional diagram reduces the circuitry down to its simplest equivalent components. Tie down unused inputs. R = 100kΩ, ±20% typ.

TRUTH TABLE

THRESHOLD VOLTAGE	$\overline{\text{TRIGGER}}$ VOLTAGE	$\overline{\text{RESET}}$	OUTPUT	DISCHARGE SWITCH
Don't Care	Don't Care	Low	Low	On
$>^2/_3(V+)$	$>^1/_3(V+)$	High	Low	On
$<^2/_3(V+)$	$>^1/_3(V+)$	High	Stable	Stable
Don't Care	$<^1/_3(V+)$	High	High	Off

NOTE: $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

Typical Performance Curves

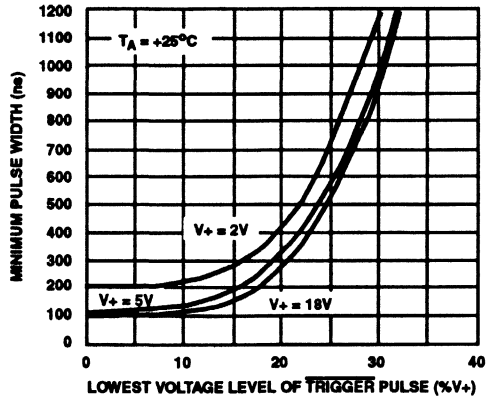


FIGURE 1. MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING

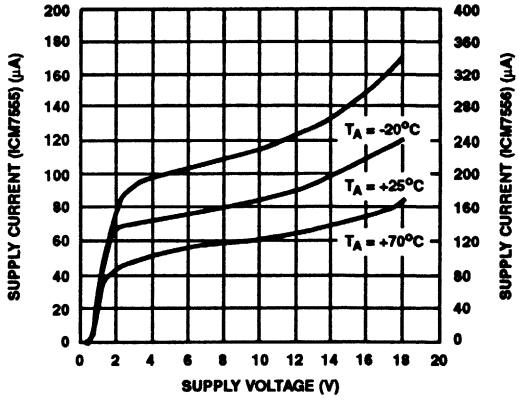


FIGURE 2. SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

Typical Performance Curves (Continued)

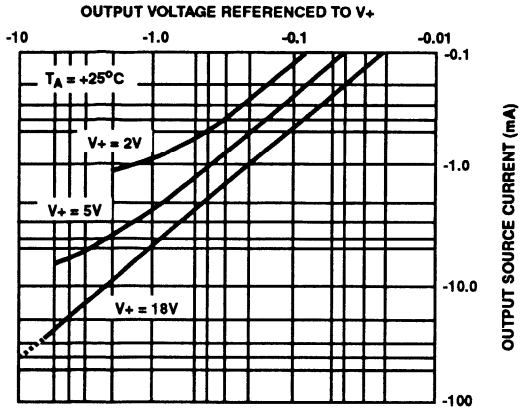


FIGURE 3. OUTPUT SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

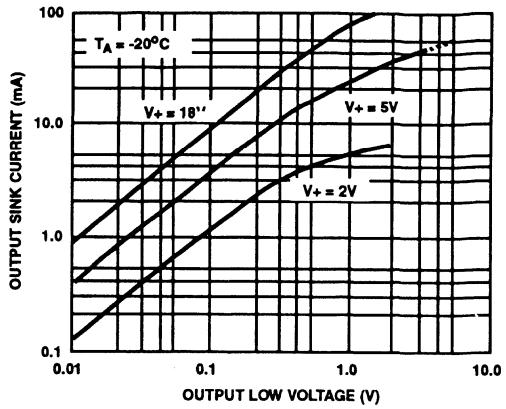


FIGURE 4. OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

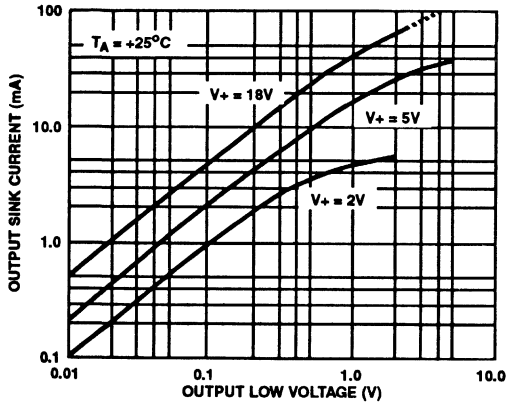


FIGURE 5. OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

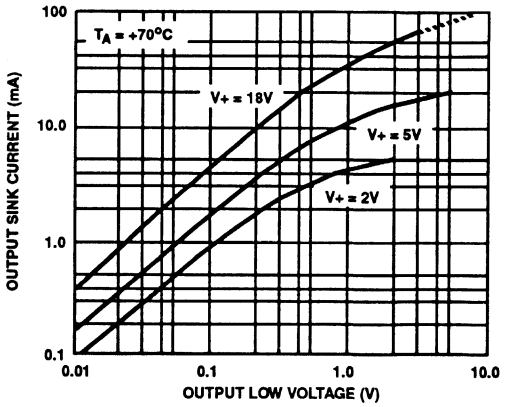


FIGURE 6. OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

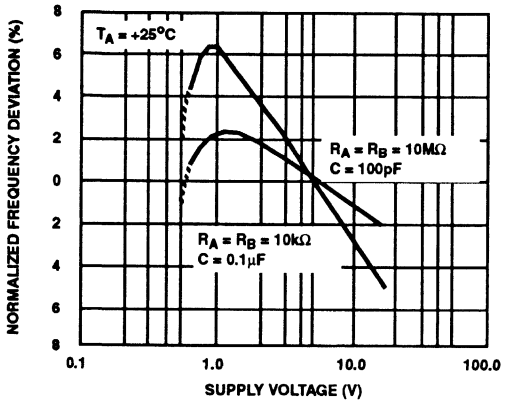


FIGURE 7. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE

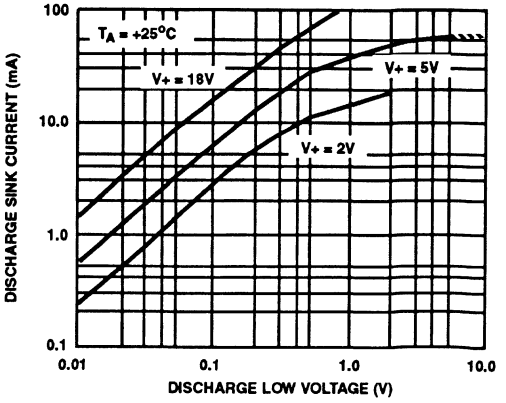


FIGURE 8. DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE

Typical Performance Curves (Continued)

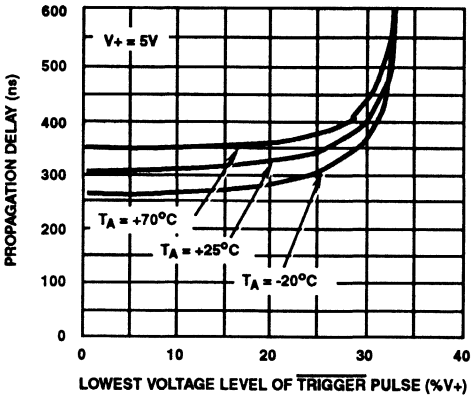


FIGURE 9. PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE

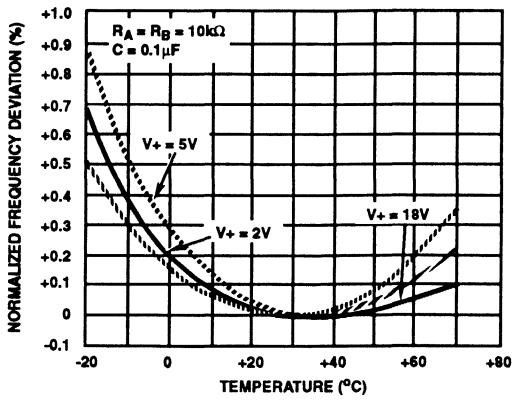


FIGURE 10. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE

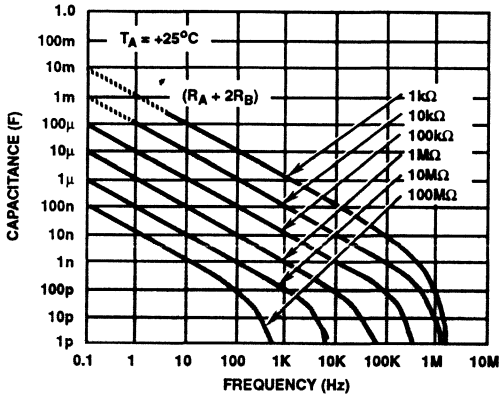


FIGURE 11. FREE RUNNING FREQUENCY AS A FUNCTION OF R_A, R_B AND C

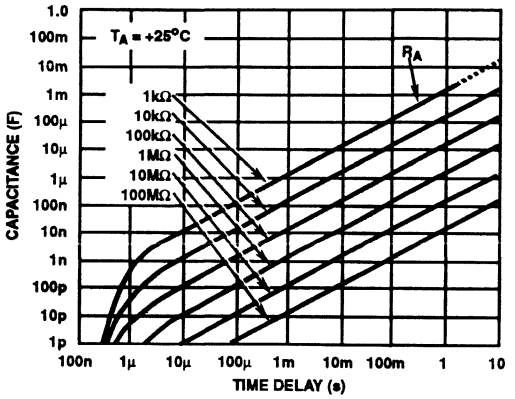


FIGURE 12. TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF R_A AND C

Application Notes

General

The ICM7555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economies in the external component count using the ICM7555/6. Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555/6 devices produce no such transients. See Figure 13.

The ICM7555/6 produces supply current spikes of only 2mA - 3mA instead of 300mA - 400mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using an ICM7555, and 3 capacitors with an ICM7556.

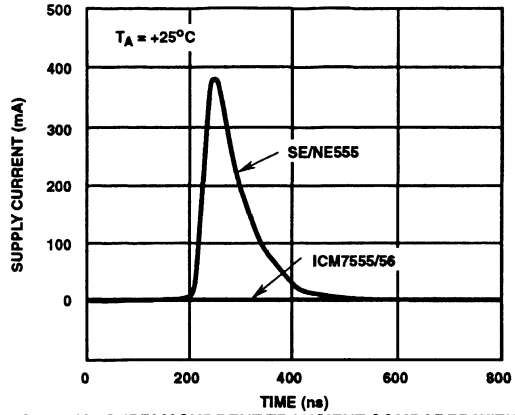


FIGURE 13. SUPPLY CURRENT TRANSIENT COMPARED WITH A STANDARD BIPOLAR 555 DURING AN OUTPUT TRANSITION

Power Supply Considerations

Although the supply current consumed by the ICM7555/6 devices is very low, the total system supply current can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 14 and 15.

Output Drive Capability

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5V or more the ICM7555/6 will drive at least 2 standard TTL loads.

Astable Operation

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 14A. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical). Less than a 1% frequency variation is observed, over a voltage range of +5V to +15V.

$$f = \frac{1}{1.4\,RC}$$

The timer can also be connected as shown in Figure 14B. In this circuit, the frequency is:

$$f = 1.44/(R_A + 2R_B)C$$

The duty cycle is controlled by the values of R_A and R_B, by the equation:

$$D = (R_A + R_B)/(R_A + 2R_B)$$

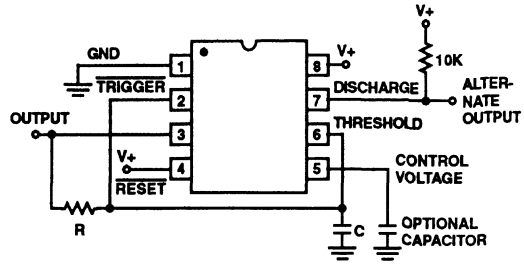


FIGURE 14A. ASTABLE OPERATION

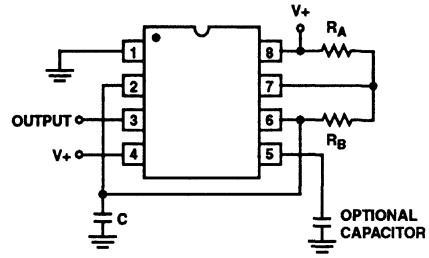
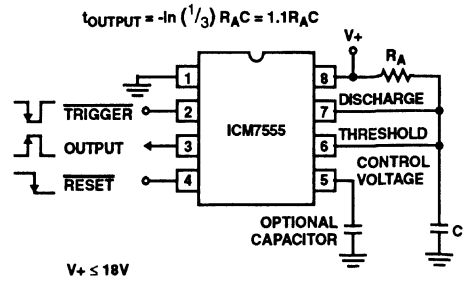


FIGURE 14B. ALTERNATE ASTABLE CONFIGURATION

Monostable Operation

In this mode of operation, the timer functions as a one-shot, see Figure 15. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2, the internal flip-flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant $t = R_AC$. When the voltage across the capacitor equals $^2/_3$ V+, the comparator resets the flip-flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state.

$t_{OUTPUT} = -\ln(^1/_3)\,R_AC = 1.1R_AC$



V+ ≤ 18V

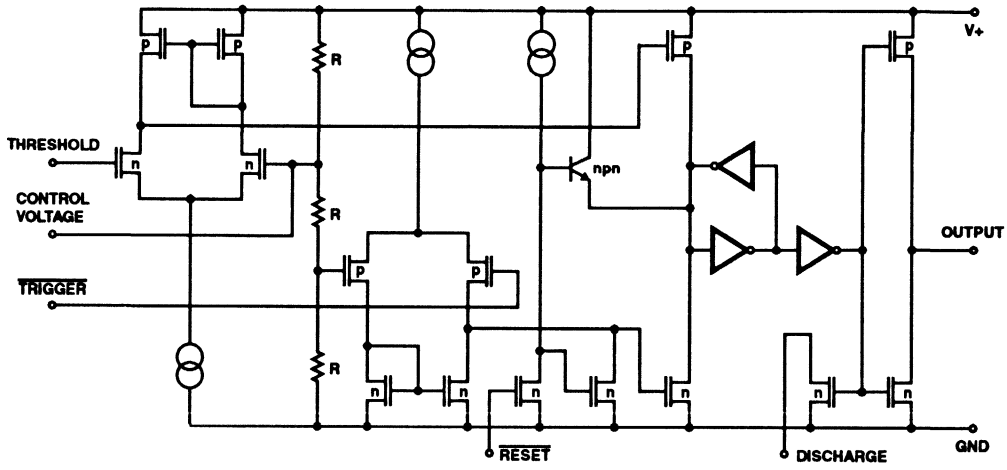
FIGURE 15. MONOSTABLE OPERATION

Control Voltage

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e. 0.6V to 0.7V. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip-flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.



R = 100kΩ ± 20% (TYP)

FIGURE 16. EQUIVALENT CIRCUIT

LINEAR 8

TELECOMMUNICATIONS

NOTE: Bold Type Designates a New Product from Harris.

CD Type Ordering Information

Telecom (CD Series)

Telecom ICs are available in a wide variety of package designs. These packages are identified by suffix letters indicated in the chart below. When ordering Telecom devices, it is important that the appropriate suffix letter be affixed to the type number as indicated on the price schedule.

PACKAGE	CD SERIES
Dual-In-Line Ceramic Sidebraze	D
Dual-In-Line Plastic	E
Frit-Seal Dual-In-Line Ceramic	F
Plastic Lead Chip Carrier	Q
Small Outline (SOIC) Plastic	M

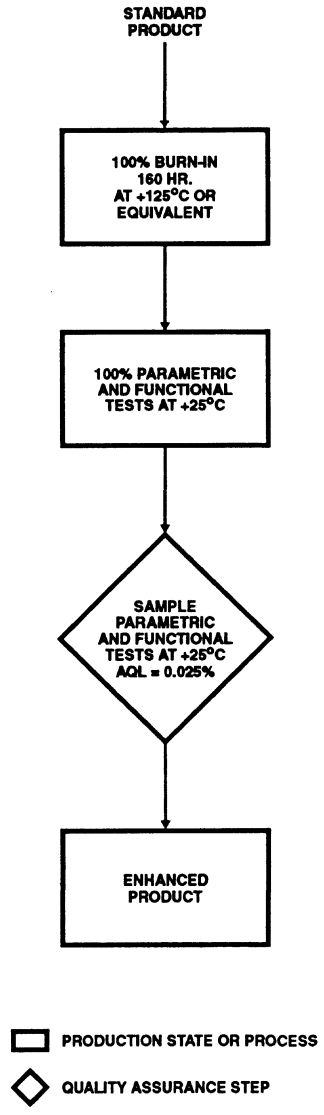
Extra Value Screening

Telecom product with extra value screening has an X added to the standard type number in the price list, and is also branded as such. A white dot will indicate location of Pin 1.

Example:

A CD22100E with Extra Value screening is designated CD22100EX in the price list. It is branded CD22100EX plus a white dot at pin number 1.

PRODUCT FLOW



HARRIS SEMICONDUCTOR

CD22100

CMOS 4 x 4 Crosspoint Switch with Control Memory High-Voltage Type (20V Rating)

March 1993

Features

- Low ON Resistance ..... 75Ω Typ. at V_{DD} = 12V
- "Built-In" Control Latches
- Large Analog Signal Capability ..... $\pm V_{DD}/2$
- 10MHz Switch Bandwidth
- Matched Switch Characteristics ΔR_{ON} = 18Ω Typ. at V_{DD} = 12V
- High Linearity - 0.5% Distortion (Typ.) at f = 1kHz, V_{IN} = $5V_{P-P}$, V_{DD} = 10V, and R_L = 1kΩ
- Standard CMOS Noise Immunity
- 100% Tested for Maximum Quiescent Current at 20V

Description

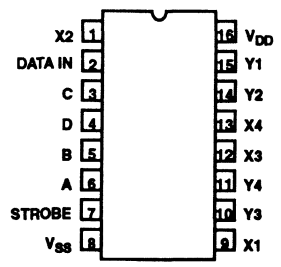
CD22100 combines a 4 x 4 array of crosspoints (transmission gates) with a 4-line to 16-line decoder and 16 latch circuits. Any one of the sixteen transmission gates (crosspoints) can be selected by applying the appropriate four line address. The selected transmission gate can be turned on or off by applying a logical one or zero, respectively, to the data input and strobing the strobe input to a logical one. Any number of the transmission gates can be ON simultaneously. When the required operating power is applied to the CD22100, the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high and data in low, and then addressing all switches in succession.

Ordering Information

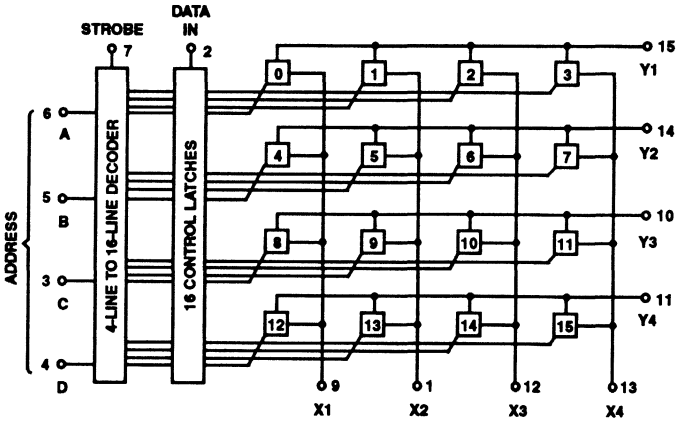
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CD22100D	-55°C to +125°C	16 Lead Ceramic Sidebraze DIP
CD22100E	-40°C to +85°C	16 Lead Plastic DIP
CD22100F	-55°C to +125°C	16 Lead Ceramic Frit Seal DIP

Pinout

CD22100
(PDIP)
TOP VIEW



Functional Diagram



8 TELECOM

File Number 1076.2

Absolute Maximum Ratings

Supply Voltage
(Voltages Referenced to V_{SS} Terminal) .....-0.5 to +20V
Input Voltage (All Inputs) ..... -0.5 to V_{DD} +0.5V
Input Current (Any one input (Note 1)).....±10mA
Power Dissipation
For T_A = -40°C to +60°C (Package Type E) 500mW
For T_A = +60°C to +85°C
(Package Type E) ..... Derate Linearly 12mW/°C to 200mW
For T_A = -55°C to +100°C (Package Type D, F) 500mW
For T_A = +100°C to +125°C
(Package Type D, F) ..... Derate Linearly 12mW/°C to 200mW
Device Dissipation per Transmission Gate
For T_A = Full Package Temperature Range (All Types) 100mW
Junction Temperature..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.)..... +300°C

Recommended Operating Conditions

Operating Temperature Range
Package Type D and F .....-55°C ≤ T_A ≤ +125°C
Package Type E.....-40°C ≤ T_A ≤ +85°C
Storage Temperature Range.....-65°C ≤ T_A ≤ +150°C
Supply Voltage Range
For T_A = Full Package Temperature Range.....+3V to +18V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications

Values at -55°C, +25°C, +125°C Apply to D, F, H Packages
Values at -40°C, +25°C, +85°C Apply to E Package

PARAMETERS	SYMBOL	TEST CONDITIONS	FIG.	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES				+25°C			UNITS
					-55°C	-40°C	+85°C	+125°C	MIN	TYP	MAX	
CROSSPOINTS												
Quiescent Device Current	I_{DD} Max.		1	5	5	5	150	150	-	0.04	5	µA
			1	10	10	10	300	300	-	0.04	10	µA
			1	15	20	20	600	600	-	0.04	20	µA
			1	20	100	100	3000	3000	-	0.08	100	µA
On Resistance	R_{ON} Max.	Any Switch V_{IS} = 0 to V_{DD}	11	5	475	500	725	800	-	225	600	Ω
			12	10	135	145	205	230	-	85	180	Ω
			-	12	100	110	155	175	-	75	135	Ω
			13	15	70	75	110	125	-	65	95	Ω
ΔR_{ON} Resistance	ΔR_{ON}	Between any two switches	-	5	-	-	-	-	-	25	-	Ω
			-	10	-	-	-	-	-	10	-	Ω
			-	12	-	-	-	-	-	8	-	Ω
			-	15	-	-	-	-	-	5	-	Ω
OFF Switch Leakage Current	I_L Max.	All switches OFF, V_{IS} = 18V	3	18	±100		±1000		-	±1	±100 (Note 2)	nA
CONTROLS												
Input Low Voltage	V_{IL} Max.	OFF switch I_L < 0.2µA	-	5	1.5				-	-	1.5	V
			-	10	3				-	-	3	V
			-	15	4				-	-	4	V
Input High Voltage	V_{IH} Min.	ON switch see R_{ON} characteristic	-	5	3.5				3.5	-	-	V
			-	10	7				7	-	-	V
			-	15	11				11	-	-	V
Input Current	I_{IN} Max.	Any control V_{IN} = 0, 18V	2	18	±0.1	±0.1	±1	±1	-	$\pm 10^{-5}$	±0.1	µA

NOTES:

1. Maximum current through transmission gates (switches) = 25mA.
2. Determined by minimum feasible leakage measurement for automatic testing.

Dynamic Electrical Specifications T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS					LIMITS			UNITS
		FIGURE	f_{IS} (kHz)	R_L (kΩ)	V_{IS} (V) (Note 1)	V_{DD} (V)	MIN	TYP	MAX	
CROSSPOINTS										
Propagation Delay Time, (Switch ON) Signal Input to Output	t_{PHL}, t_{PLH}	5	-	10	5	5	-	30	60	ns
					10	10	-	15	30	ns
					15	15	-	10	20	ns
			C_L = 50pF; t_R, t_F = 20ns							
Frequency Response (Any switch ON)	f_{3dB}	16	1	1	5	10	-	40	-	MHz
			Sine wave input, $20 \log \frac{V_{OS}}{V_{IS}}$ = -3dB							
Sine Wave Response (Distortion)	T_{HD}		1	1	5	10	-	0.5	-	%
Feedthrough (All switches OFF)	F_{DT}		1.6	1	5	10	-	-80	-	dB
			Sine wave input							
Frequency for Signal Crosstalk Attenuation of 40dB	F_{CT}	7	-	1	10	10	-	1.5	-	MHz
			Sine wave input							
Attenuation of 110dB							-	0.1	-	kHz
Capacitance:	C_{IS}									
Xn to Ground				-	-	5 - 15	-	18	-	pF
Yn to Ground				-	-	5 - 15	-	30	-	pF
Feedthrough	C_{IOS}			-	-	-	-	0.4	-	pF
CONTROLS										
Propagation Delay Time: Strobe to Output (Switch Turn-ON to High Level)	t_{PZH}	8	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	300	600	ns
						10	-	125	250	ns
						15	-	80	160	ns
Propagation Delay Time: Data-In to Output (Turn-On to High Level)	t_{PZH}	9	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	110	220	ns
						10	-	40	80	ns
						15	-	25	50	ns
Propagation Delay Time: Address to Output (Turn-ON to High Level)	t_{PZH}	10	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	350	700	ns
						10	-	135	270	ns
						15	-	90	180	ns
Propagation Delay Time: Strobe to Output (Switch Turn-OFF)	t_{PHZ}	8	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	165	330	ns
						10	-	85	170	ns
						15	-	70	140	ns
Propagation Delay Time: Data-In to Output (Turn-ON to Low Level)	t_{PZL}	9	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	210	420	ns
						10	-	110	220	ns
						15	-	100	200	ns
Propagation Delay Time: Address to Output (Turn-OFF)	t_{PHZ}	10	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	435	870	ns
						10	-	210	420	ns
						15	-	160	320	ns

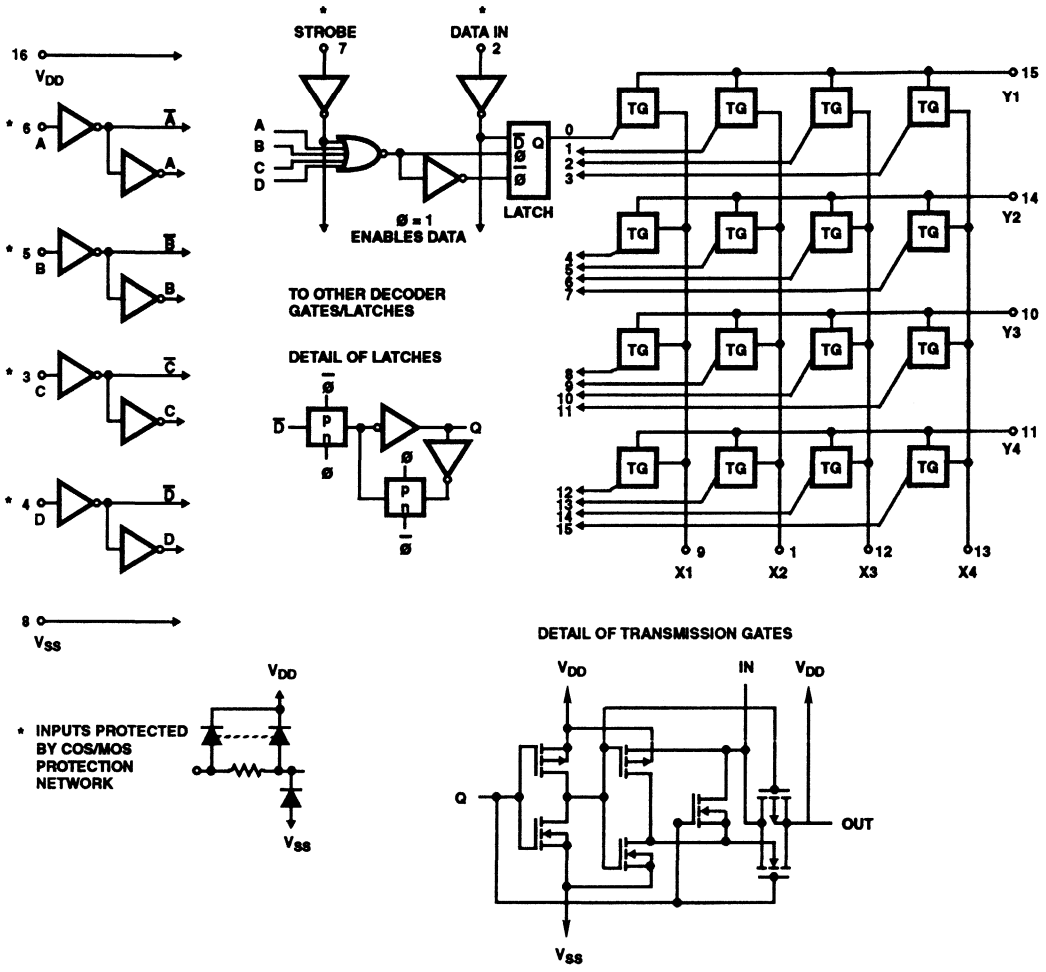
Dynamic Electrical Specifications T_A = +25°C (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS					LIMITS			UNITS
		FIGURE	f_{IS} (kHz)	R_L (kΩ)	V_{IS} (V) (Note 1)	V_{DD} (V)	MIN	TYP	MAX	
Minimum Setup Time Data-In to Strobe, Address	t_S	8, 10	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	95	190	ns
						10	-	25	50	ns
						15	-	15	30	ns
Minimum Hold Time Data-In to Strobe, Address	t_H	8, 10	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	180	360	ns
						10	-	110	220	ns
						15	-	35	70	ns
Maximum Switching Frequency	$f_{Ø}$		R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	0.6	1.2	-	MHz
						10	1.6	3.2	-	MHz
						15	2.5	5	-	MHz
Minimum Strobe Pulse Width	t_W	8				5	-	300	600	ns
						10	-	120	240	ns
						15	-	90	180	ns
Control Crosstalk, Data-In, Address or Strobe to Output		6	Square wave input; t_R, t_F = 20ns			10	-	75	-	mV (peak)
			-	10	10					
Input Capacitance	C_{IN}		Any Control Input			-	-	5	7.5	pF

NOTE:

1. Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$.

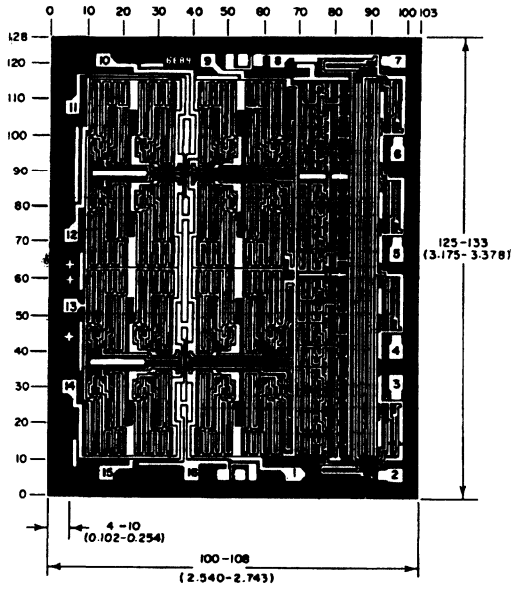
Schematic Diagram



TRUTH TABLE

ADDRESS					ADDRESS				
A	B	C	D	SELECT	A	B	C	D	SELECT
0	0	0	0	X1Y1	0	0	0	1	X1Y3
1	0	0	0	X2Y1	1	0	0	1	X2Y3
0	1	0	0	X3Y1	0	1	0	1	X3Y3
1	1	0	0	X4Y1	1	1	0	1	X4Y3
0	0	1	0	X1Y2	0	0	1	1	X1Y4
1	0	1	0	X2Y2	1	0	1	1	X2Y4
0	1	1	0	X3Y2	0	1	1	1	X3Y4
1	1	1	0	X4Y2	1	1	1	1	X4Y4

Metallization Mask Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Test Circuits and Waveforms

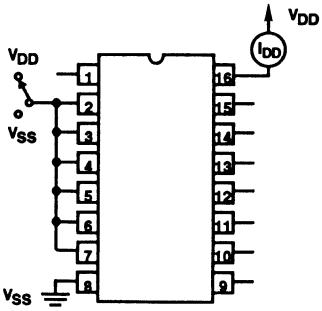
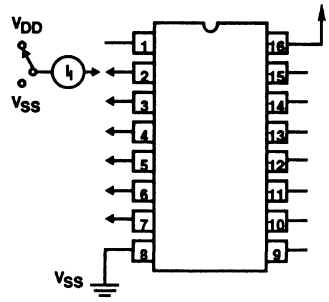


FIGURE 1. QUIESCENT CURRENT TEST CIRCUIT



NOTE:
MEASURE INPUTS SEQUENTIALLY TO BOTH V_{DD} AND V_{SS}
CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}

FIGURE 2. INPUT CURRENT TEST CIRCUIT

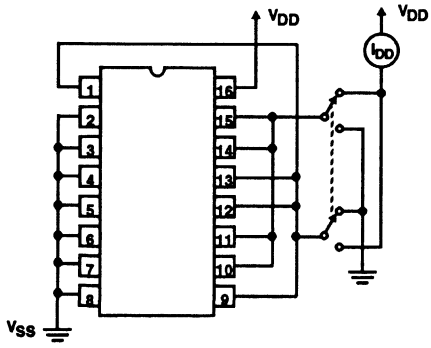
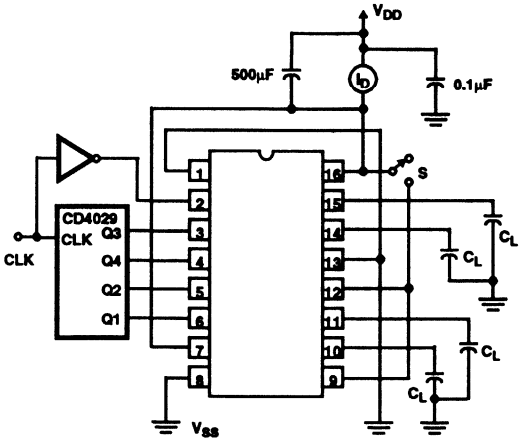


FIGURE 3. OFF SWITCH INPUT OR OUTPUT LEAKAGE CURRENT TEST CIRCUIT

Test Circuits and Waveforms (Continued)



NOTE:
CLOSE SWITCH S AFTER APPLYING V_{DD}

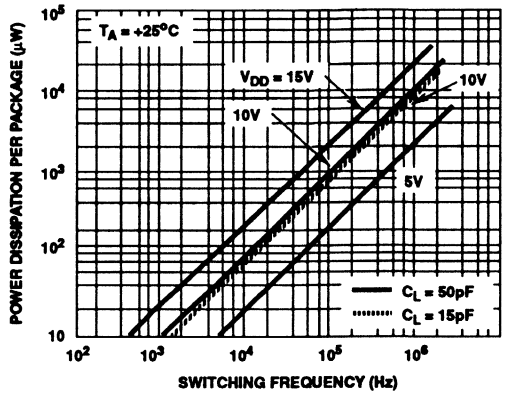
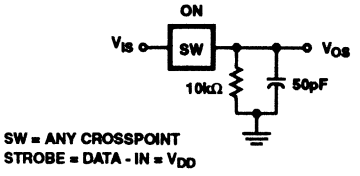


FIGURE 4. DYNAMIC POWER DISSIPATION TEST CIRCUIT AND TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF SWITCHING FREQUENCY



SW = ANY CROSSPOINT
STROBE = DATA - IN = V_{DD}

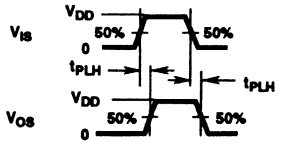


FIGURE 5. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (SIGNAL INPUT TO SIGNAL OUTPUT, SWITCH ON)

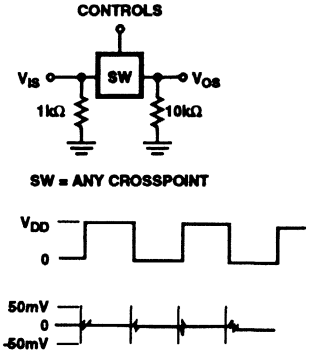
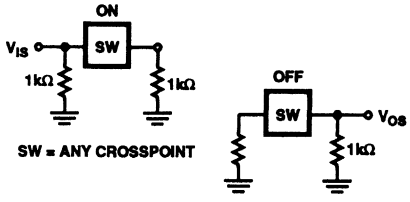


FIGURE 6. TEST CIRCUIT AND WAVEFORMS FOR CROSSTALK (CONTROL INPUT TO SIGNAL OUTPUT)



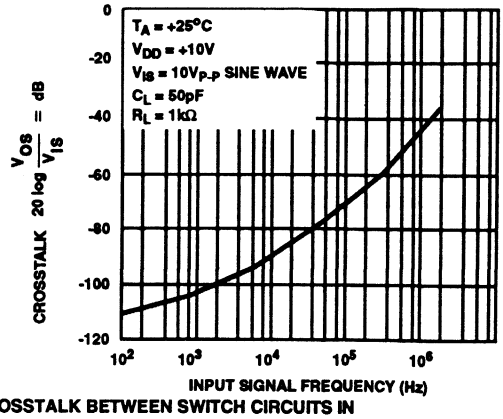


FIGURE 7. TEST CIRCUIT AND TYPICAL CROSSTALK BETWEEN SWITCH CIRCUITS IN THE SAME PACKAGE AS A FUNCTON OF SIGNAL FREQUENCY

Test Circuits and Waveforms (Continued)

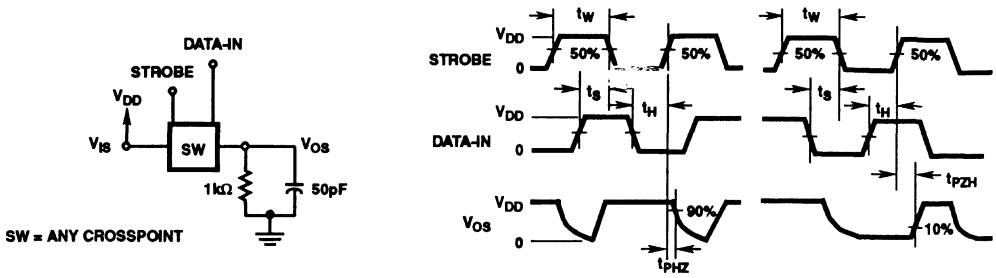


FIGURE 8. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS
(STROBE TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

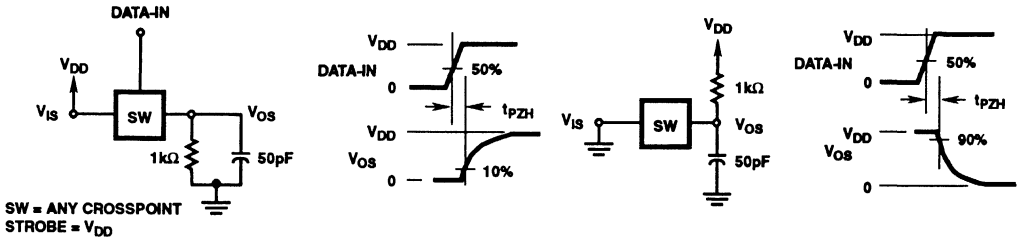


FIGURE 9. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS
(DATA-IN TO SIGNAL OUTPUT, SWITCH TURN-ON TO HIGH OR LOW LEVEL)

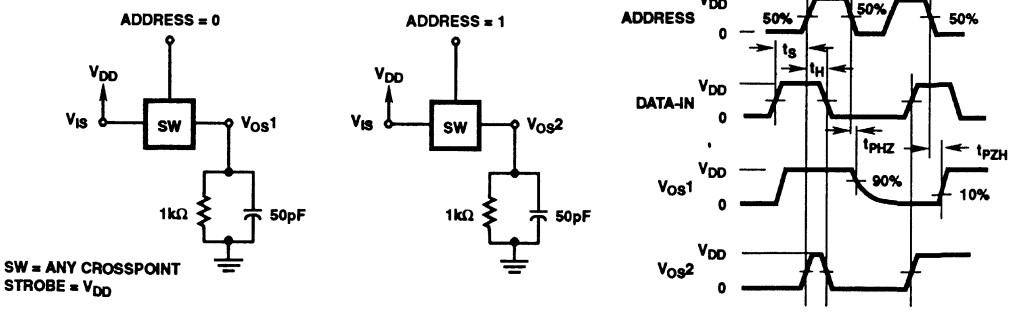


FIGURE 10. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS
(ADDRESS TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

Typical Performance Curves

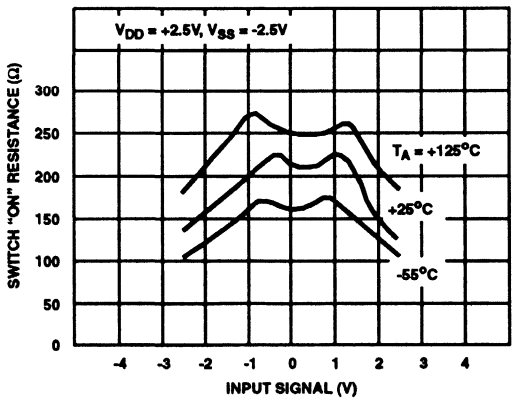


FIGURE 11. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT V_{DD} = -V_{SS} = 2.5V

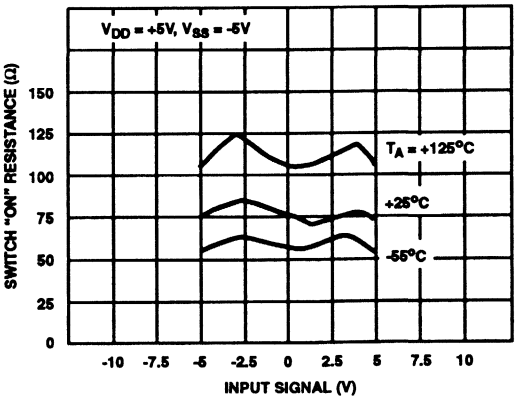


FIGURE 12. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT V_{DD} = -V_{SS} = 5V

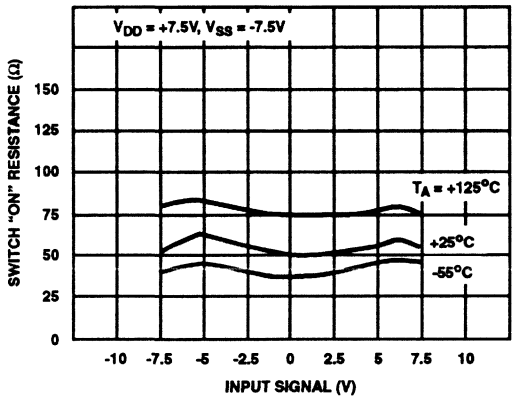


FIGURE 13. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT V_{DD} = -V_{SS} = 7.5V

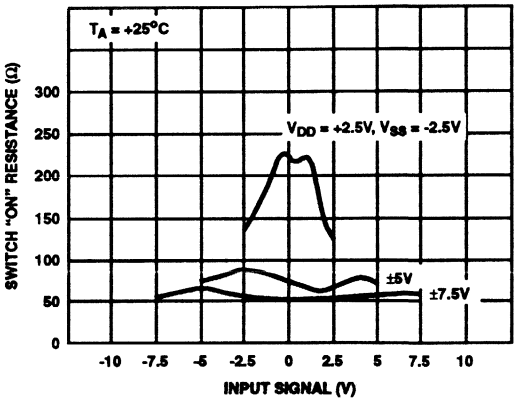


FIGURE 14. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT T_A = +25°C

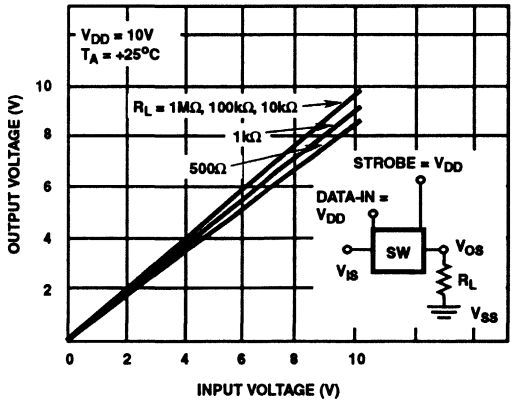


FIGURE 15. TYPICAL SWITCH ON TRANSFER CHARACTERISTICS (1 OF 16 SWITCHES)

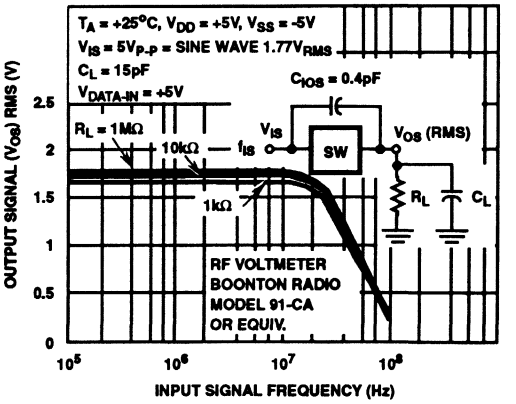


FIGURE 16. TYPICAL SWITCH ON FREQUENCY RESPONSE CHARACTERISTICS

8 TELECOM

HARRIS SEMICONDUCTOR

CD22101, CD22102

CMOS 4 x 4 x 2 Crosspoint Switch with Control Memory

March 1993

Features

- Low ON Resistance . . . . . .75V Typ. at V_{DD} = 12V
- "Built - In" Latched Inputs
- Large Analog Signal Capability . . . . . $\pm V_{DD}/2$
- Switch Bandwidth 10MHz
- Matched Switch Characteristics ΔR_{ON} = 8Ω Typ. at V_{DD} = 12V
- High Linearity - 0.25% Distortion (Typ.) at f = 1kHz, V_{IN} = 5Vp-p, V_{DD} - V_{SS} = 10V, and R_L = 1kΩ
- Standard CMOS Noise Immunity

Applications

- Telephone Systems
- PBX
- Studio Audio Switching
- Multisystem Bus Interconnect

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CD22101E	-40°C to +85°C	24 Lead Plastic DIP
CD22101F	-55°C to +125°C	24 Lead Frit Seal Ceramic DIP
CD22102E	-40°C to +85°C	24 Lead Plastic DIP
CD22102F	-55°C to +125°C	24 Lead Frit Seal Ceramic DIP

Description

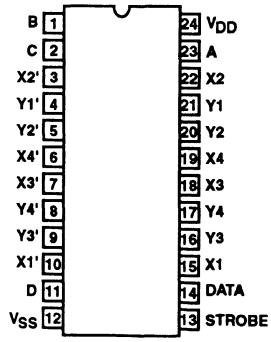
CD22101 and CD22102 crosspoint switches consist of 4 x 4 x 2 arrays of crosspoints (transmission gates) with a 4-line to 16-line decoder and 16 latch circuits. Any one of the sixteen crosspoint pairs can be selected by applying the appropriate four-line address, corresponding crosspoints in each array are turned on and off simultaneously. Any number of crosspoints can be turned on simultaneously.

In the CD22101, the selected crosspoint pair can be turned on or off by applying a logical ONE or ZERO, respectively, to the data input, and applying a ONE to the strobe input. When the device is "powered up", the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high, data-in low, and then addressing all switches in succession.

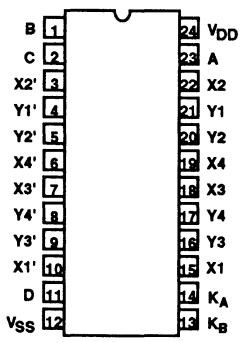
The selected pair of crosspoints in the CD22102 is turned on by applying a logical ONE to the K_A (set) input while a logical ZERO is on the K_B input, and turned off by applying a logical ONE to the K_B (reset) input while a logical ZERO is on the K_A input. In this respect, the control latches of the CD22102 are similar to SET/RESET flip-flops. They differ, however, in that the simultaneous application of ONE's to the K_A and K_B inputs turns off (resets) all crosspoints. All crosspoints in both devices must be turned off as V_{DD} is applied.

Pinouts

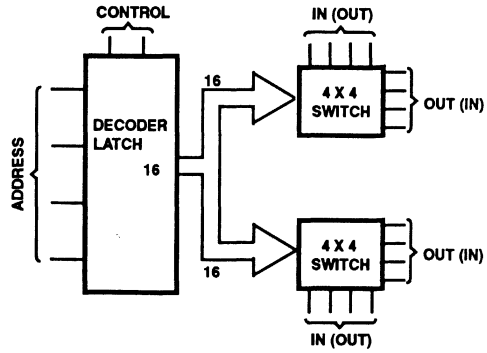
CD22101
24 LEAD (PDIP, CDIP)
TOP VIEW



CD22102
24 LEAD (PDIP, CDIP)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2871.1**

Absolute Maximum Ratings

Supply Voltage (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20V
Input Voltage (All Inputs) ..... -0.5 to V_{DD} +0.5V
Input Current (Any One Input) (Note 1) ..... ±10mA
Power Dissipation
For T_A = -40°C to +60°C (Package Type E) 500mW
For T_A = +60°C to +85°C
Package Type E) ..... Derate Linearly 12mW/°C to 200mW
For T_A = -55°C to +100°C (Package Type D, F) 500mW
For T_A = +100°C to +125°C
(Package Type D, F) ..... Derate Linearly 12mW/°C to 200mW
Device Dissipation per Output Transistor
For T_A = Full Package Temperature Range (All Types) 100mW
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Recommended Operating Conditions

Operating Temperature Range
Package Type D, F, H. ..... -55°C ≤ T_A ≤ +125°C
Package Type E ..... -40°C ≤ T_A ≤ +85°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C
Supply Voltage Range
For T_A = Full Package Temperature Range ..... +3V to +18V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications

Values at -55°C, +25°C, +125°C Apply to D, F, H Packages
Values at -40°C, +25°C, +85°C Apply to E Package

PARAMETERS	SYMBOL	TEST CONDITIONS	FIGURE	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES -55°C	-40°C	+85°C	+125°C	+25°C MIN	+25°C TYP	+25°C MAX	UNITS
CROSSPOINTS												
Quiescent Device Current	I_{DD} Max.		1	5	5	5	150	150	-	0.04	5	µA
			1	10	10	10	300	300	-	0.04	10	µA
			1	15	20	20	600	600	-	0.04	20	µA
			1	20	100	100	3000	3000	-	0.08	100	µA
On Resistance	R_{ON} Max.	Any Switch V_{IS} = 0 to V_{DD}	14	5	475	500	725	800	-	225	600	Ω
			15	10	135	145	205	230	-	85	180	Ω
			-	12	100	110	155	175	-	75	135	Ω
			16	15	70	75	110	125	-	65	95	Ω
Δ_{ON} Resistance	ΔR_{ON}	Between any two switches		5	-	-	-	-	-	25	-	Ω
				10	-	-	-	-	-	10	-	Ω
				12	-	-	-	-	-	8	-	Ω
				15	-	-	-	-	-	5	-	Ω
OFF Leakage Current	I_L Max.	All switches OFF, V_{IS} = 18V	4	18	±1000				-	±1	±100 (Note 2)	nA
CONTROLS												
Input Low Voltage	V_{IL} Max.	OFF switch I_L < 0.2µA		5	1.5				-	-	1.5	V
				10	3				-	-	3	V
				15	4				-	-	4	V
Input High Voltage	V_{IH} Min.	ON switch see R_{ON} characteristic		5	3.5				3.5	-	-	V
				10	7				7	-	-	V
				15	11				11	-	-	V
Input Current	I_{IN} Max.	Any control V_{IN} = 0, 18V	2	18	±0.1	±0.1	±1	±1	-	$±10^{-5}$	±0.1	µA

NOTE:
1. Maximum current through transmission gates (switches) = 25mA.
2. Determined by minimum feasible leakage measurement for automatic testing.

Dynamic Electrical Specifications T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS					LIMITS			UNITS
		FIGURE	f_{IS} (kHz)	R_L (kΩ)	V_{IS} (V) (Note 3)	V_{DD} (V)	MIN	TYP	MAX	
CROSSPOINTS										
Propagation Delay Time, (Switch ON) Signal Input to Output	t_{PHL}, t_{PLH}	5			5	5	-	30	60	ns
			-	10	10	10	-	15	30	ns
					15	15	-	10	20	ns
			C_L = 50pF; t_R, t_F = 20ns							
Frequency Response (Any switch ON)	f_{3dB}	19	1	1	5	10	-	40	-	MHz
			Sine wave input, $20 \log \frac{V_{OS}}{V_{IS}}$ = -3dB							
Sine Wave Response (Distortion)	THD	-	1	1	2.5	5	-	1	-	%
			1	1	5	10	-	0.25	-	%
			1	1	7.5	15	-	0.15	-	%
Feedthrough (All switches OFF)	F_{DT}	13	1.6	0.6	2 (Note 4)	10	-	-96	-	dB
			Sine wave input							
Frequency for Signal Crosstalk	F_{CT}	12	-	0.6	1 (Note 4)	10				
Attenuation of 40dB			Sine wave input				-	2.5	-	MHz
Attenuation of 95dB								0.1		kHz
Capacitance:										
X_N to Ground	C_{IS}			-	-	-	-	25	-	pF
Y_N to Ground				-	-	-	-	60	-	pF
Feedthrough	C_{IOS}			-	-	-	-	0.6	-	pF
CONTROLS										
Propagation Delay Time: High Impedance to High Level or Low Level	t_{PZH}, t_{PZL}	6	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	500	1000	ns
Strobe to Output, CD22101						10	-	230	460	ns
						15	-	170	340	ns
Data-In to Output, CD22101	t_{PZH}, t_{PZL}	7	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	515	1000	ns
						10	-	220	440	ns
						15	-	170	340	ns
K_A to Output, CD22102	t_{PZH}, t_{PZL}	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	500	1000	ns
						10	-	215	430	ns
						15	-	160	320	ns
Address to Output CD22101, CD22102	t_{PZH}, t_{PZL}	8	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	480	960	ns
						10	-	225	450	ns
						15	-	155	300	ns

Dynamic Electrical Specifications T_A = +25°C (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS					LIMITS			UNITS
		FIGURE	f_{IS} (kHz)	R_L (kΩ)	V_{IS} (V) (Note 3)	V_{DD} (V)	MIN	TYP	MAX	
CONTROLS (Continued)										
Propagation Delay Time: High Level or Low Level to High Impedance	t_{PHZ}, t_{PLZ}	6	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	450	900	ns
Strobe to Output, CD22101						10	-	200	400	ns
						15	-	135	270	ns
K_B to Output, CD22102	t_{PHZ}, t_{PLZ}	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	450	900	ns
						10	-	200	400	ns
						15	-	130	260	ns
Data-In to Output, CD22101	t_{PHZ}, t_{PLZ}	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	450	900	ns
						10	-	165	330	ns
						15	-	110	220	ns
K_A • K_B to Output, CD22102	t_{PHZ}, t_{PLZ}	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	280	560	ns
						10	-	130	260	ns
						15	-	90	180	ns
Address to Output CD22101, CD22102	t_{PHZ}, t_{PLZ}	8	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	425	850	ns
						10	-	190	380	ns
						15	-	130	260	ns
Minimum Strobe Pulse Width, CD22101	t_W	6	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	260	500	ns
						10	-	120	240	ns
						15	-	80	160	ns
Address to Strobe Setup or Hold Times, CD22101	t_{SU}, t_H	9	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	-160	0	ns
						10	-	-70	0	ns
						15	-	-50	0	ns
Strobe to Data-In Hold Time, CD22101	t_{HHL}, t_{HLH}	10	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	200	400	ns
						10	-	80	160	ns
						15	-	60	120	ns
Address to K_A and K_B Setup or Hold Times, CD22102	t_{SU}, t_H	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	-160	0	ns
						10	-	-70	0	ns
						15	-	-50	0	ns
Minimum K_A • K_B Pulse Width, CD22102	t_W	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	375	750	ns
						10	-	160	320	ns
						15	-	110	220	ns
Minimum K_A Pulse Width, CD22102	t_W	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	425	850	ns
						10	-	175	350	ns
						15	-	120	240	ns
Minimum K_B Pulse Width, CD22102	t_W	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	200	400	ns
						10	-	90	180	ns
						15	-	70	140	ns

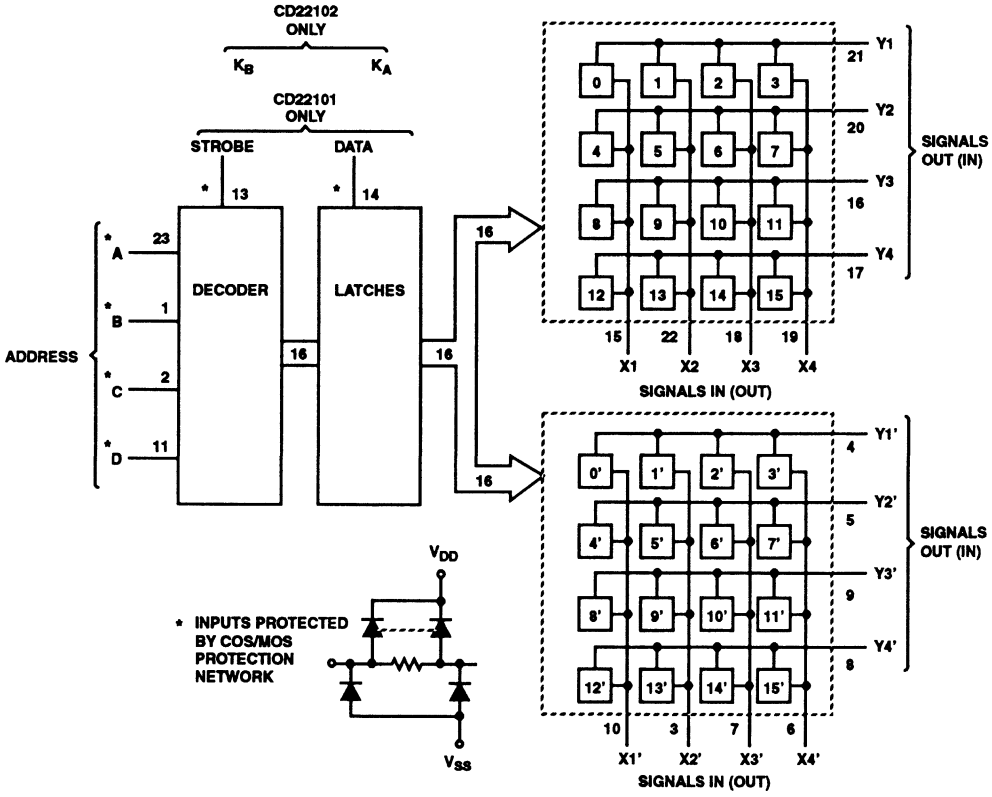
Dynamic Electrical Specifications T_A = +25°C (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS					LIMITS			UNITS
		FIGURE	f_{IS} (kHz)	R_L (kΩ)	V_{IS} (V) (Note 3)	V_{DD} (V)	MIN	TYP	MAX	
CONTROLS (Continued)										
Control Crosstalk, Data-In, Address or Strobe to Output		11	100	10		5	-	75	-	mV (peak)
			Square wave input = 5V, t_R, t_F = 20ns, R_S = 1kΩ							
Input Capacitance	C_{IN}		Any Control Input			-	-	5	7.5	pF

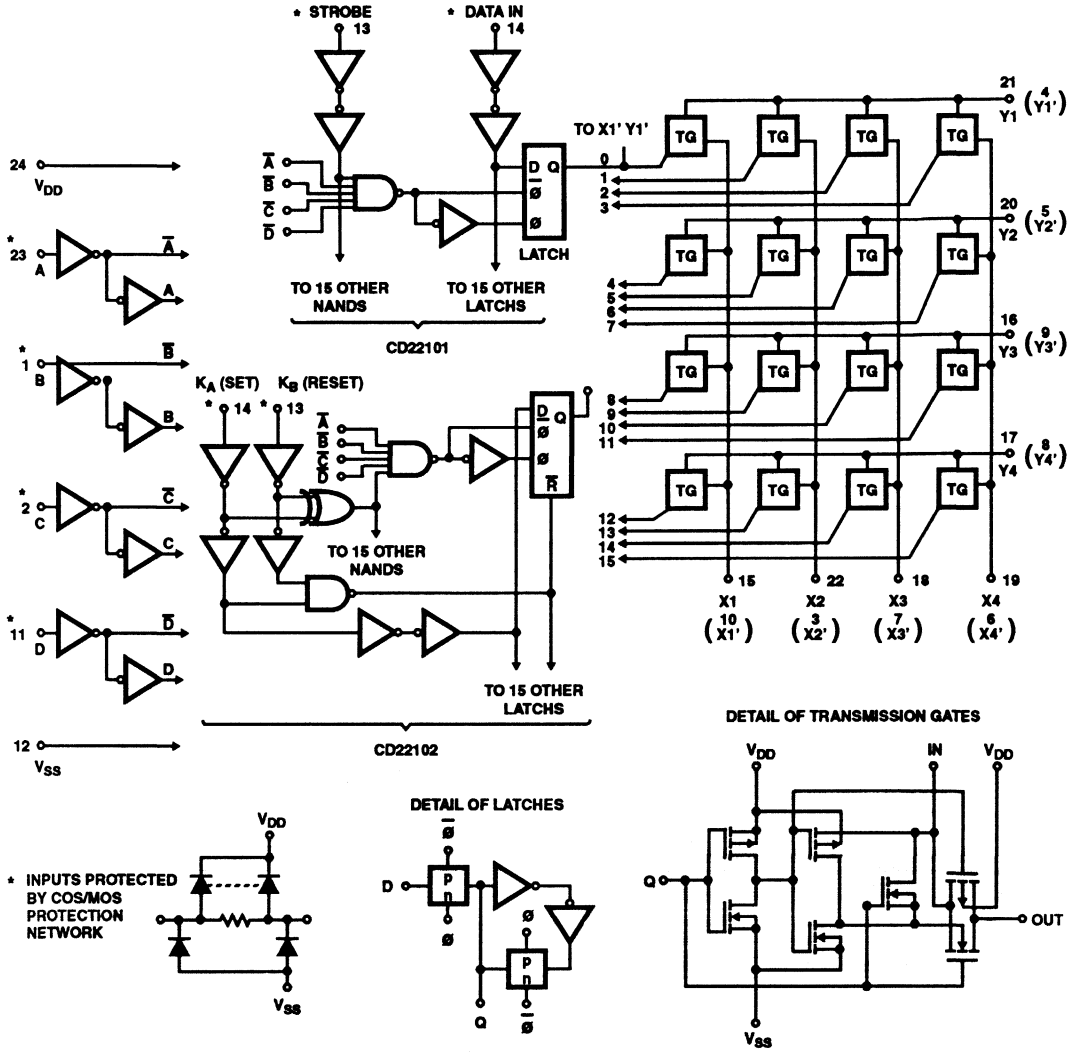
NOTE:

3. Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$, unless otherwise specified.
4. RMS

Functional Block Diagram



Schematic Diagram



DECODER TRUTH TABLE

ADDRESS					ADDRESS				
A	B	C	D	SELECT	A	B	C	D	SELECT
0	0	0	0	X1Y1 and X1'Y1'	0	0	0	1	X1Y3 and X1'Y3'
1	0	0	0	X2Y1 and X2'Y1'	1	0	0	1	X2Y3 and X2'Y3'
0	1	0	0	X3Y1 and X3'Y1'	0	1	0	1	X3Y3 and X3'Y3'
1	1	0	0	X4Y1 and X4'Y1'	1	1	0	1	X4Y3 and X4'Y3'
0	0	1	0	X1Y2 and X1'Y2'	0	0	1	1	X1Y4 and X1'Y4'
1	0	1	0	X2Y2 and X2'Y2'	1	0	1	1	X2Y4 and X2'Y4'
0	1	1	0	X3Y2 and X3'Y2'	0	1	1	1	X3Y4 and X3'Y4'
1	1	1	0	X4Y2 and X4'Y2'	1	1	1	1	X4Y4 and X4'Y4'

CONTROL TRUTH TABLE FOR CD22101

FUNCTION	ADDRESS A	B	C	D	STROBE	DATA	SELECT
Switch On	1	1	1	1	1	1	15 (X4Y4) and 15' (X4'Y4')
Switch Off	1	1	1	1	1	0	15 (X4Y4) and 15' (X4'Y4')
No Change	X	X	X	X	0	X	X X X X

1 = High Level 0 = Low Level X = Don't Care

CONTROL TRUTH TABLE FOR CD22102

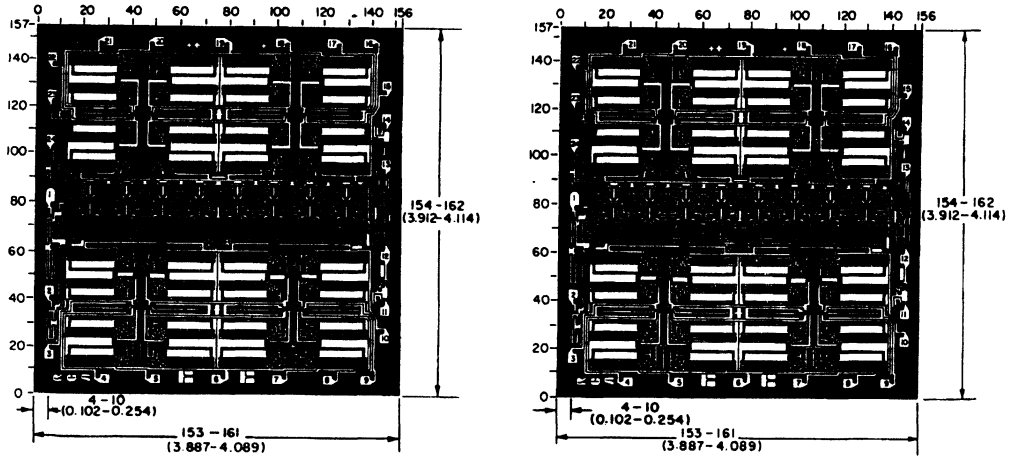
FUNCTION	ADDRESS A	B	C	D	K_A	K_B	SELECT
Switch On	1	1	1	1	1	0	15 (X4Y4) and 15' (X4'Y4')
Switch Off	1	1	1	1	0	1	15 (X4Y4) and 15' (X4'Y4')
All Switches Off (Note 5)	X	X	X	X	1	1	All
No Change	X	X	X	X	0	0	X X X X

1 = High Level 0 = Low Level X = Don't Care

NOTE:

5. In the event that K_A and K_B are changed from levels 1, 1 to 0, 0 K_B should not be allowed to go to 0 before K_A, otherwise a switch which was off will inadvertently be turned on.

Metallization Mask Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Test Circuits and Waveforms

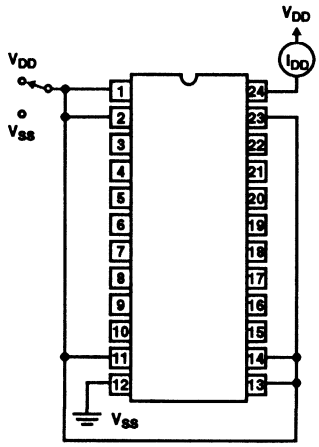
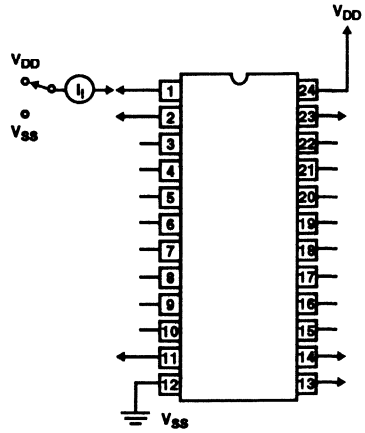
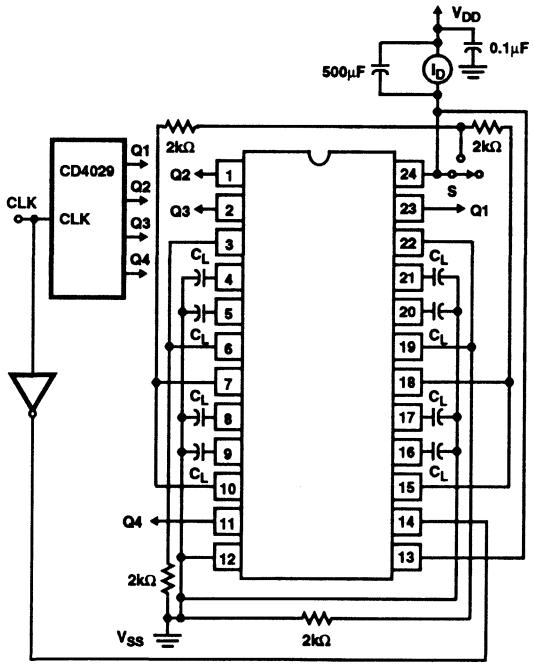


FIGURE 1. QUIESCENT CURRENT TEST CIRCUIT



NOTE:
MEASURE INPUTS SEQUENTIALLY TO BOTH V_{DD} AND V_{SS}
CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}

FIGURE 2. INPUT CURRENT TEST CIRCUIT



NOTE:
CLOSE SWITCH S AFTER APPLYING V_{DD}

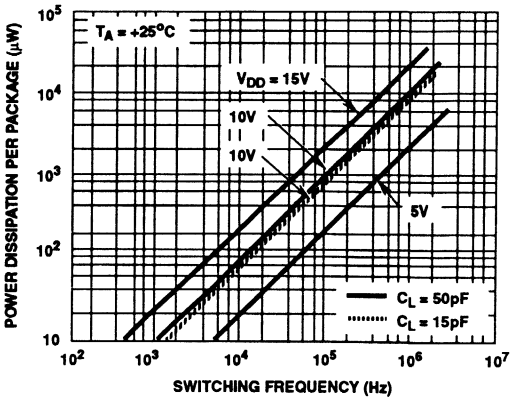


FIGURE 3. DYNAMIC POWER DISSIPATION TEST CIRCUIT FOR CD22101AND TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF SWITCHING FREQUENCY

Test Circuits and Waveforms (Continued)

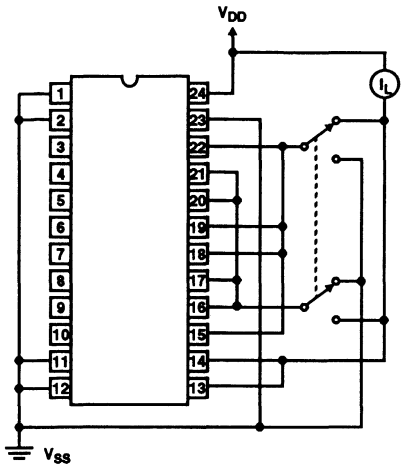


FIGURE 4. OFF SWITCH INPUT OR OUTPUT LEAKAGE CURRENT TEST CIRCUIT (16 OF 32 SWITCHES)

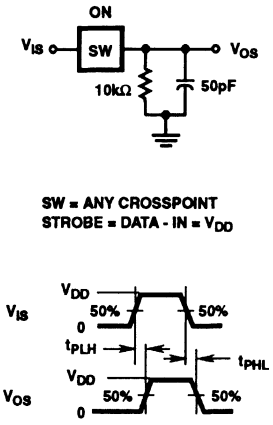


FIGURE 5. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (SIGNAL INPUT TO SIGNAL OUTPUT, SWITCH ON)

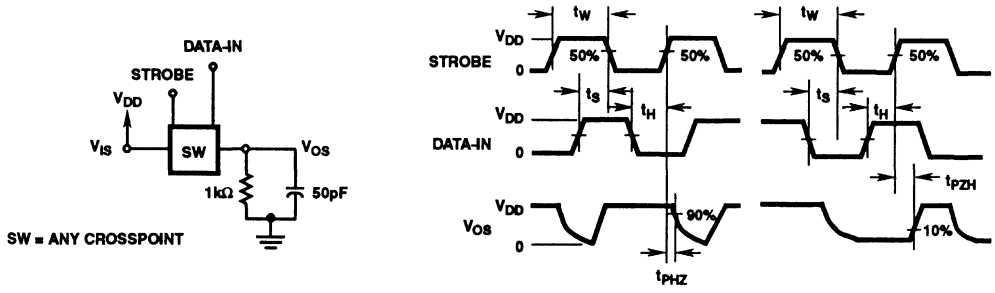


FIGURE 6. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (STROBE TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

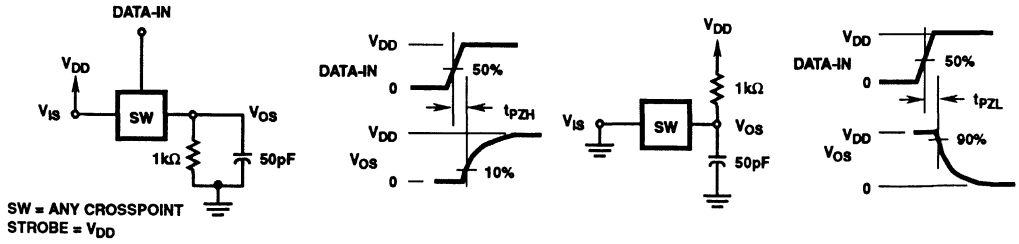


FIGURE 7. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (DATA-IN TO SIGNAL OUTPUT, SWITCH TURN-ON TO HIGH OR LOW LEVEL)

Test Circuits and Waveforms (Continued)

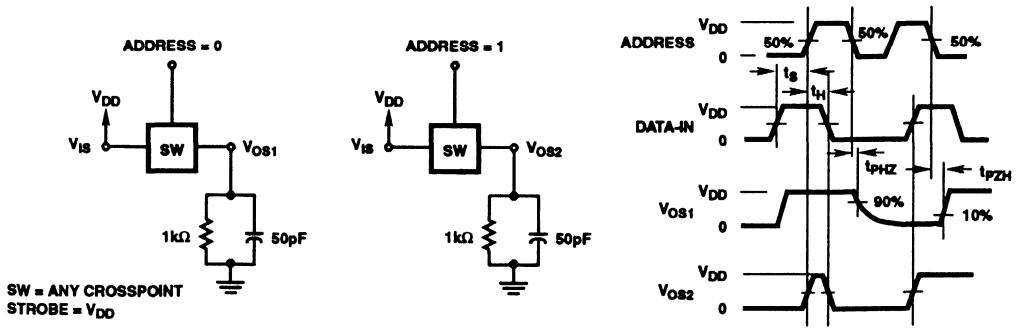
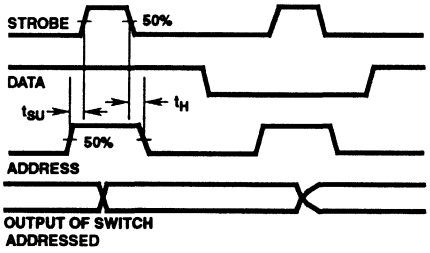
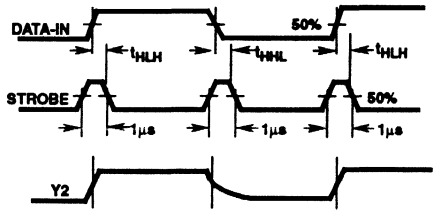


FIGURE 8. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (ADDRESS TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)



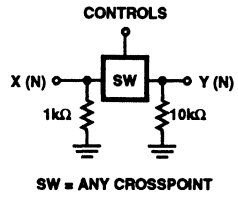
NOTE:
IF SETUP AND HOLD TIMES PROVIDED ARE TOO SHORT, AN UNADDRESSED SWITCH MAY BE TURNED ON OR OFF SIMULTANEOUSLY WITH THE ADDRESSED SWITCH

FIGURE 9. ADDRESS TO STROBE SETUP AND HOLD TIMES



NOTE:
SET ALL SWITCHES TO OFF INITIALLY APPLY VDD TO ALL X INPUTS AND RETURN ALL Y OUTPUTS TO VSS THROUGH 1kΩ. ADDRESS X1Y2 (ABCD) WITH f_{IN} = 10kHz

FIGURE 10. STROBE TO DATA-IN HOLD TIME t_H, FOR CD22101



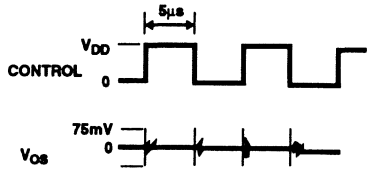
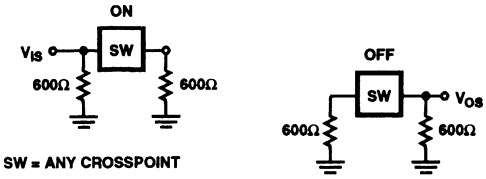


FIGURE 11. TEST CIRCUIT AND WAVEFORMS FOR CROSSTALK (CONTROL INPUT TO SIGNAL OUTPUT)

Test Circuits and Waveforms (Continued)



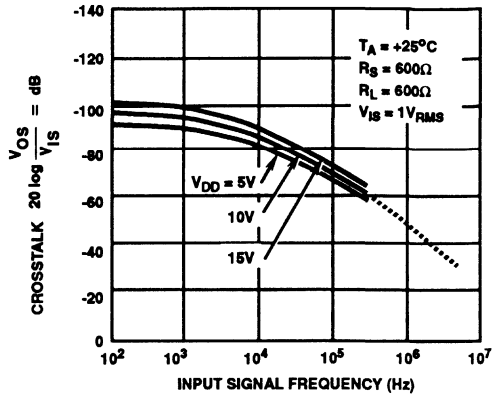
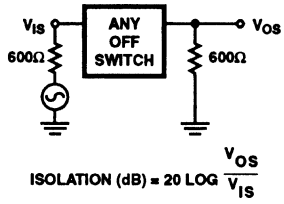


FIGURE 12. TEST CIRCUIT AND TYPICAL CROSSTALK AS A FUNCTION OF FREQUENCY BETWEEN SWITCH CIRCUITS IN THE SAME PACKAGE



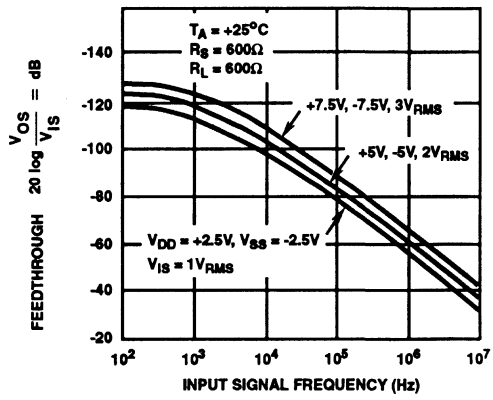


FIGURE 13. TEST CIRCUIT AND TYPICAL FEEDTHROUGH AS A FUNCTION OF FREQUENCY (ANY OFF SWITCH)

Typical Performance Curves

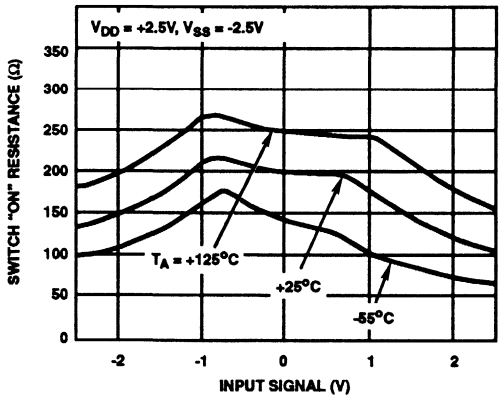


FIGURE 14. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT V_{DD} = -V_{SS} = 2.5V

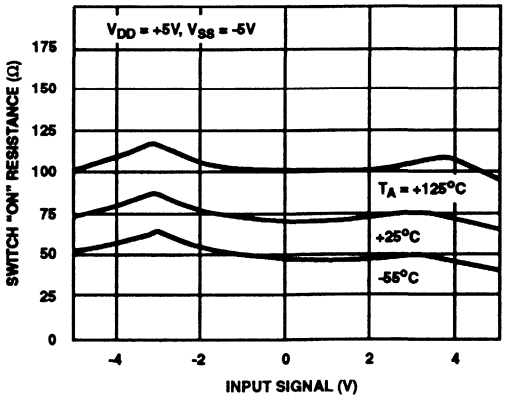


FIGURE 15. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT V_{DD} = -V_{SS} = 5V

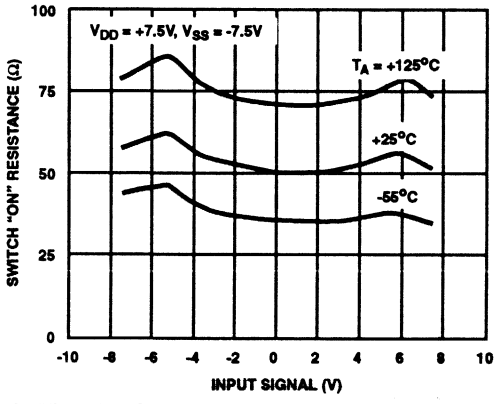


FIGURE 16. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT V_{DD} = -V_{SS} = 7.5V

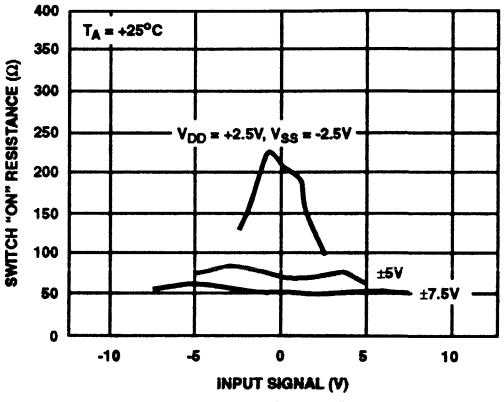


FIGURE 17. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT T_A = +25°C

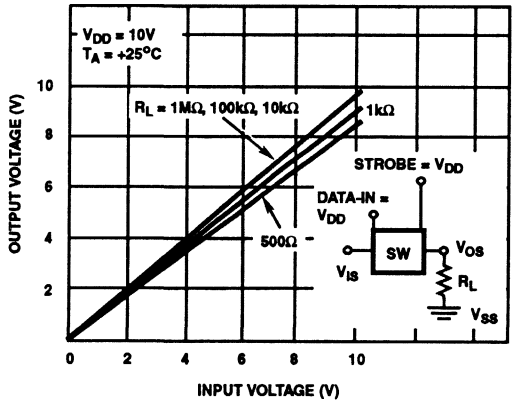


FIGURE 18. TYPICAL SWITCH ON TRANSFER CHARACTERISTICS (1 OF 16 SWITCHES)

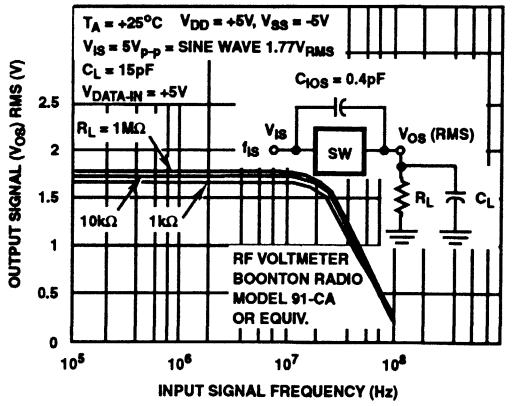


FIGURE 19. TYPICAL SWITCH ON FREQUENCY RESPONSE CHARACTERISTICS

8 TELECOM

HARRIS SEMICONDUCTOR

CD22103A

CMOS HDB3 (High Density Bipolar 3) Transcoder for 2.048/8.448 Mb/s Transmission Applications

March 1993

Features

- **HDB3 Coding and Decoding for Data Rates from 50Kb/s to 10Mb/s in a Manner Consistent with CCITT G703 Recommendations**
- **HDB3/AMI Transmission Coding/Reception Decoding with Code Error Detection is Performed in Independent Coder and Decoder Sections**
- **All Transmitter and Receiver Inputs/Outputs are TTL Compatible**
- **Internal Loop Test Capability**
- **Pin and Functionally Compatible with Type MJ1471**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CD22103AD	-55°C to +125°C	16 Lead Ceramic Side-braze DIP
CD22103AE	-40°C to +85°C	16 Lead Plastic DIP

Description

The CD22103A is an LSI SOS integrated circuit which performs the HDB3 transmission coding and reception decoding functions with error detection. It is used in 2.048Mb/s and 8.448Mb/s transmission applications. The CD22103A performs HDB3 coding and decoding for data rates from 50Kb/s to 10Mb/s in a manner consistent with CCITT G703 recommendations.

HDB3 transmission coding/reception decoding with code error detection is performed in independent coder and decoder sections. All transmitter and receiver inputs/outputs are TTL compatible.

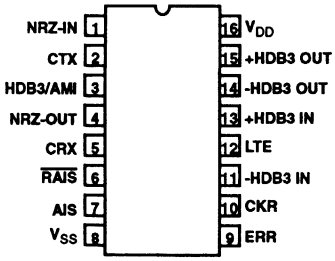
The HDB3 transmitter coder codes an NRZ binary unipolar input signal (NRZ-IN) and a synchronous transmission clock (CTX) into two HDB3 binary unipolar RZ output signals (+HDB3 OUT, -HDB3 OUT). The TTL compatible output signals +HDB3 OUT, -HDB3 OUT are externally mixed to generate ternary bipolar HDB3 signals for driving transmission lines.

The receiver decoder converts binary unipolar inputs (+HDB3 IN, -HDB3 IN), which were externally split from ternary bipolar HDB3 signals, and a synchronous clock signal (CRX) into binary unipolar NRZ signals (NRZ-OUT).

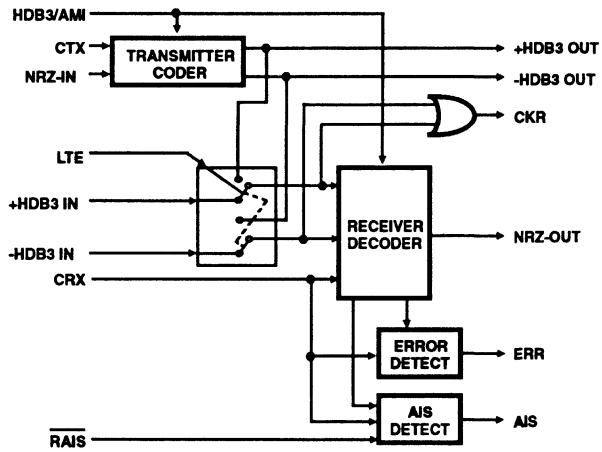
The CD22103A operates with a 5V ±10% power supply voltage over the full military temperature range at data rates from 50Kb/s up to 10Mb/s.

Pinout

CD22103A
(PDIP, CDIP)
TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1310.2**

Absolute Maximum Ratings

Supply Voltage (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +8V
Input Voltage (All Inputs) ..... -0.5 to V_{DD} +0.5V
Input Current (Any One Input) ..... ±10mA
Power Dissipation
For T_A = -40°C to +60°C (Package Type E) 500mW
For T_A = +60°C to +85°C
(Package Type E) ..... Derate Linearly 12mW/°C to 200mW
For T_A = -55°C to +100°C (Package Type D) 500mW
For T_A = +100°C to +125°C
(Package Type D) ..... Derate Linearly 12mW/°C to 200mW
Device Dissipation per Output Transistor
For T_A = Full Package Temperature Range (All Types) 100mW
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Recommended Operating Conditions

Operating Temperature Range
Package Type D ..... -55°C ≤ T_A ≤ +125°C
Package Type E ..... -40°C ≤ T_A ≤ +85°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C
Supply Voltage Range
For T_A = Full Package Temperature Range ..... +4.5V to +5.5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications

V_{DD} = 5V ±10%, T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Quiescent Device Current	I_{DD}		-	-	100	µA
Operating Device Current		f_{CL} = 10MHz	-	-	8	mA
HDB3 Output Low (Sink) Current	I_{OL1}	V_{OL} = 0.5V	1.6	-	-	mA
HDB3 Output High (Source) Current	I_{OH1}	V_{OH} = 2.8V	-10	-	-	mA
All Other Outputs Low (Sink) Current	I_{OL2}	V_{OL} = 0.5V	1.6	-	-	mA
All Other Outputs High (Source) Current	I_{OH2}	V_{OH} = 2.8V	-1.6	-	-	mA
Input Low Current	I_{IL}		-	-	-1	µA
Input High Current	I_{IH}		-	-	1	µA
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2	-	-	V
Input Capacitance	I_{IN}		-	-	5	pF

Dynamic Electrical Specifications

T_A = -40°C to +85°C for Plastic Package; -55°C to +125°C for Ceramic Package; V_{DD} = +4.5V to +5.5V; C_L = 15pF

PARAMETERS	SYMBOL	FIGURE	LIMITS			UNITS
			MIN	TYP	MAX	
INPUT						
CTX, CRX Input Frequency	f_{CTX}, f_{CRX}		0.05	-	10	MHz
CTX, CRX Input Rise Time	t_{RCL}	3	-	-	1	µs
Fall Time	t_{FCL}	3	-	-	1	µs
NRZ-IN to CTX				-		
Data Setup Time	t_S	3	15	-	-	ns
Data Hold Time	t_H	3	15	-	-	ns
HDB3 IN to CRX				-		
Data Setup Time	t_S	4	15	-	-	ns
Data Hold Time	t_H	3	0	-	-	ns

Dynamic Electrical Specifications T_A = -40°C to +85°C for Plastic Package; -55°C to +125°C for Ceramic Package; V_{DD} = +4.5V to +5.5V; C_L = 15pF **(Continued)**

PARAMETERS	SYMBOL	FIGURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
INPUT (Continued)						
CRX to CKR (CRX = 8.448MHz)						
Pretrigger	t_P	5	-	-	20	ns
Delay	t_D	5	-	-	20	ns
OUTPUT						
Transmitter Coder CTX to HDB3 OUT:						
Data Propagation Delay Time	t_{DD}	3	-	-	90	ns
Handling Delay Time	t_{HD}	1	-	4	-	clock period
HDB3 OUT Output Pulse Width (Clock duty cycle = 50%)						
f_{CL} = 2.048MHz	t_W	3	238	-	260	ns
f_{CL} = 8.448MHz	t_W	3	53	-	65	
Receiver Decoder CRX to NRZ OUT:						
Data Propagation Delay Times	t_{DD}	4	-	-	90	ns
Handling Delay Time	t_{HD}	2	-	4	-	clock period
HDB3 IN to CKR HDB3 Propagation Delay Time						
LTE = 0	$t_{IN\ CKR}$	4	-	-	65	ns
LTE = 1		4	-	-	30	ns

Functional Description

The CD22103A is designed to code and decode HDB3 signals which are coded as binary digital signals (NRZ-IN) and (+ HDB3 IN, -HDB3 IN), accompanied by sampling clocks (CTX) and (CRX). The two binary coded HDB3 outputs, (+ HDB3 OUT, -HDB3 OUT) may be externally mixed to create the ternary HDB3 signals (See Figure 1).

The two binary HDB3 input signals have been split from the input ternary HDB3 in an external line receiver.

The receiver decoder converts binary unipolar inputs (+HDB3 IN, -HDB3 IN), which were externally split from ternary bipolar HDB3 signals, and a synchronous clock signal (CRX) into binary unipolar NRZ signals (NRZ-OUT).

Received signals not consistent with HDB3 coding rules are detected as errors. The receiver error output (ERR) is active high during one CRX period of each bit of received data that is inconsistent with HDB3 coding rules.

An input string consisting of all ones (or marks) is detected and signaled by a high level at the Alarm Signal (AIS) output. The AIS output is set to a high level when less than three zeros are received during two consecutive periods of the Reset Alarm Inhibit Signal (RAIS). The AIS output is subsequently reset to a low level when three or more zeros are received during two periods of the reset signal ($\overline{RAIS}$).

A diagnostic Loop-Test Mode may be entered by driving the Loop Test Enable Input (LTE) high. In this mode the HDB3 transmitter outputs (+HDB3 OUT, -HDB3 OUT) are internally connected to the HDB3 receiver inputs, and the external HDB3 receiver inputs, and the external HDB3 receiver inputs (+HDB3 IN, -HDB3 IN) are disabled. The NRZ binary output signal (NRZ - OUT) corresponds to the NRZ binary input signal (NRZ - IN) delayed by approximately 8 clock periods.

The Clock Receiver Output (CKR) is the product of the two HDB3 input signals or-ed together. The CRX clock signal may be derived from the CKR signal with external clock extraction circuitry. In the Loop Test Mode (LTE = 1) CKR is the product of the +HDB3 OUT and -HDB3 OUT signals or-ed together.

The CD22103A may also be used to perform the AMI to NRZ coding/decoding function. To use the CD22103A in this mode, the HDB3/AMI control input is driven low.

Error Detection

Received HDB3/AMI binary input signals are checked for coding violations, and an error signal (ERR) is generated as described below.

Error Detection (Continued)

- **HDB3 Signals HDB3/AMI = High**

The error signal (ERR) is flagged high for one CTX period if a violation pulse (±V) is received of the same polarity as the last received violation pulse.

A violation pulse (±V) is considered a reception error and does not cause replacement of the last string of 4 bits to zeros, if:

The received 4 data bits previous to reception of the violation pulse have not been the sequence BX00 (where X = don't care). The error signal (ERR) remains low.

NOTES:

1. The data sequences B000V and BB00V are valid HDB3 codings of the NRZ binary sequence 10000.
2. The error signal (ERR) count, is the accurate number of all single bit errors.

- **AMI Signals HDB3/AMI = Low**
  - A coding error (ERR) is signaled when a violation pulse (+V) is received.
- **In either the HDB3 or AMI mode:**
  - When high levels appear simultaneously on both HDB3 inputs (+ HDB3 IN, -HDB3 IN) a logical one is assumed in the HDB3/AMI input stream and the error signal (ERR) goes high for the duration of the violation.

Alarm Inhibit Signal

- The alarm output (AIS) is set high if, in two successive periods of the external Reset Alarm Signal ($\overline{RAIS}$), less than three zeros are received.
- The alarm output (AIS) is reset low when three or more zeros are received during two Reset Alarm Signal periods.

Transcoder Operation

Transmitter Coder (See Figure 1)

The HDB3/AMI transmitter coder operates on 4-bit serial strings of NRZ binary data and a synchronous transmitter clock (CTX). NRZ binary data is serially clocked into the transmitter on the negative transition of the (CTX) clock. HDB3/AMI coding is performed on the 4-bit string, and HDB3/AMI binary output data is clocked out to the (+HDB3 OUT, -HDB3 OUT) outputs on the positive transition of the transmitter clock (CTX) 4 clock pulses after the data appeared at the (NRZ-IN) input.

Receiver Decoder (See Figure 2)

The HDB3/AMI receiver decoder operates on 4-bit serial strings of binary coded HDB3/AMI signals, and a synchronous receiver clock (CRX), HDB3/AMI binary data is serially clocked into the receiver on the positive transition of the (CRX) clock. HDB3/AMI decoding is performed on the 4-bit string, and NRZ binary output data is clocked out to the (NRZ-OUT) output on the positive transition of the receiver clock (CRX) 4 clock pulses after the data appeared at the (+HDB3 IN, -HDB3 IN) inputs.

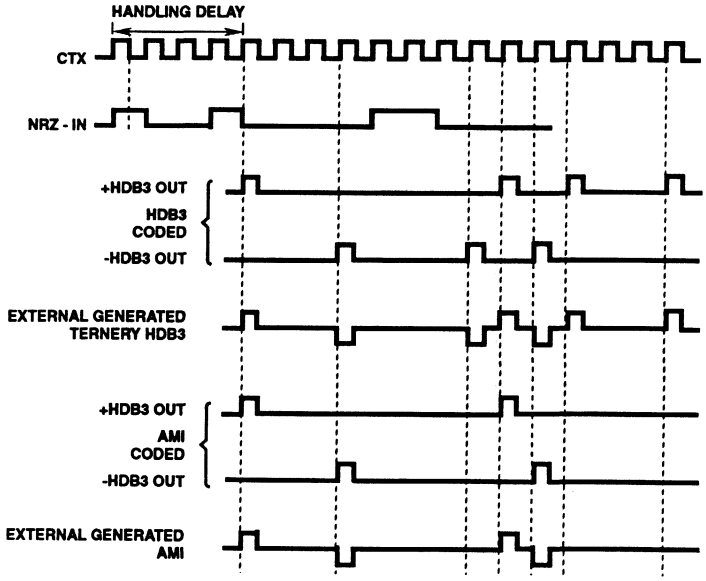


FIGURE 1. TRANSMITTER CODER OPERATION TIMING WAVEFORMS - NRZ TO HDB3/AMI CODING

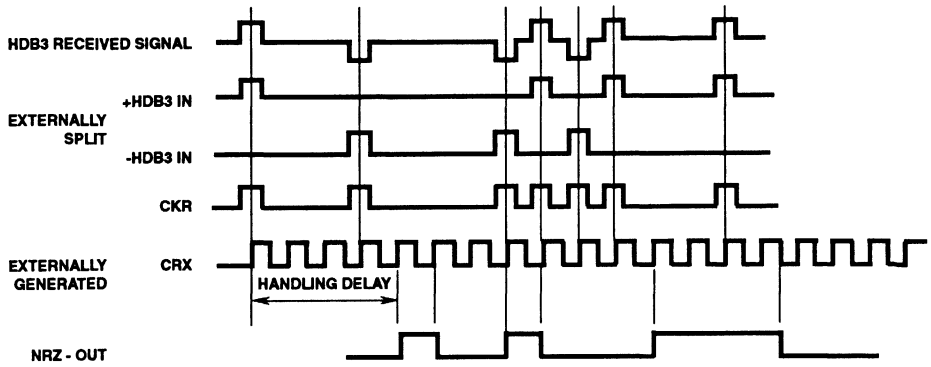


FIGURE 2. RECEIVER DECODER OPERATION TIMING WAVEFORMS - HDB3 TO NRZ DECODING

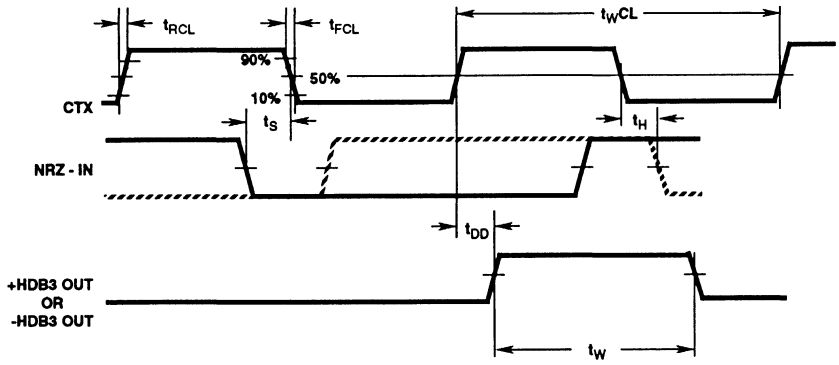


FIGURE 3. TRANSMITTER CODER TIMING WAVEFORMS

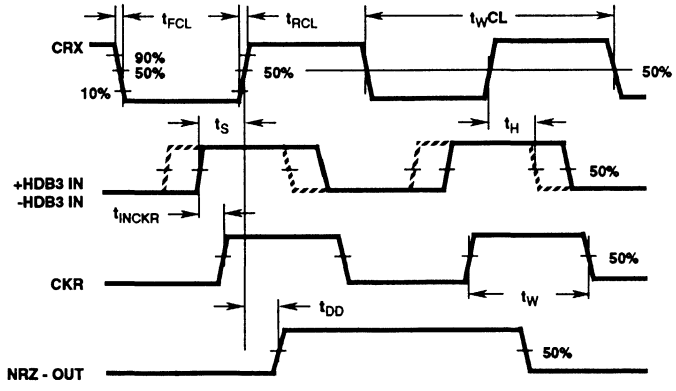


FIGURE 4. INPUT REQUIREMENTS AND OUTPUT CHARACTERISTICS

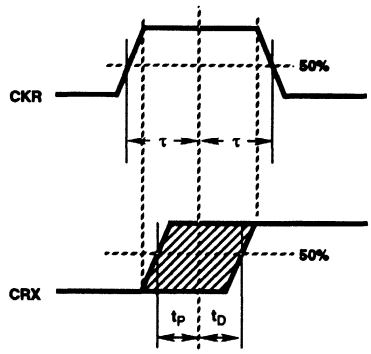


FIGURE 5. CRX RECONSTRUCTION REQUIREMENTS

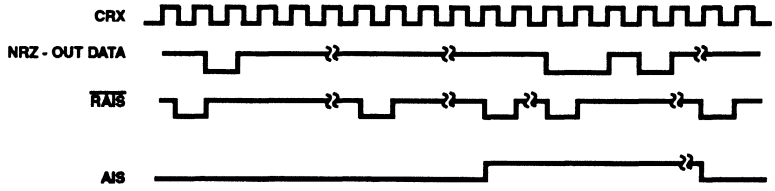


FIGURE 6. RECEIVER ALARM-INHIBIT-SIGNALS TIMING WAVEFORMS

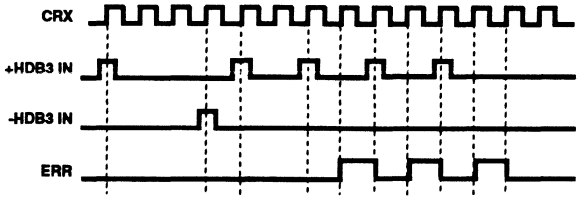


FIGURE 7. RECEIVER ERROR-SIGNALS TIMING WAVEFORMS

Definition of HDB3 Code Used in CD22103A HDB3 Transcoder (As Per CCITRT G703 Annex Recommendations) and Error Detection

Coding Of A Binary Signal Into An HDB3 Signal Is Done According To The Following Rules:

1 HDB3 signal is pseudoternary; the three states are denoted B+, B-, and 0.

2 Spaces (zeros) in the binary NRZ signal are coded as spaces in the HDB3 signal. For strings of four spaces, however, special rules apply (See Item 4 below).

3 Marks (ones) in the binary signal are coded alternately as B+ and B- in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (See Item 4 below).

4 Strings of four spaces in the binary signal are coded according to the followinq rules:

A) The first space of a string is coded as a space if the polarity of the preceding mark of the HDB3 signal has a polarity opposite to the preceding violation and is not a violation by itself; it is coded as a mark, i.e., not a violation (i.e., B+ or B-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.

This rule ensures that successive violations are of alternate polarity so that no dc component is introduced.

B) The second and third spaces of a string are always coded as spaces.

C) The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V+ or V- according to their polarity.

CD22202, CD22203

April 1993

5V Low Power DTMF Receiver

Features

- Central Office Quality
- No Front End Band Splitting Filters Required
- Single, Low Tolerance, 5V Supply
- Detects Either 12 or 16 Standard DTMF Digits
- Uses Inexpensive 3.579545MHz Crystal for Reference
- Excellent Speech Immunity
- Output in Either 4-Bit Hexadecimal Code or Binary Coded 2-of-8
- Synchronous or Handshake Interface
- Three State Outputs
- Excellent Latch-Up Immunity

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CD22202E	0°C to +70°C	18 Lead Plastic DIP
CD22203E	0°C to +70°C	18 Lead Plastic DIP

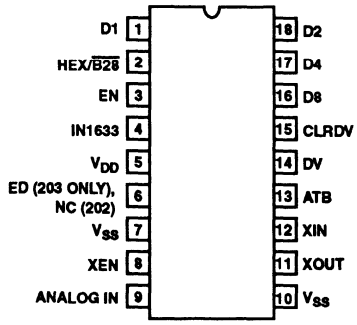
Description

The CD22202 and CD22203 complete dual-tone multiple frequency (DTMF) receivers detect a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.579545MHz TV "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is possible through the use of the clock output of a crystal connected CD22202/CD22203 receiver to drive the time bases of additional receivers. This is a monolithic integrated circuit fabricated with low-power, complementary symmetry CMOS processing. It only requires a single low tolerance power supply.

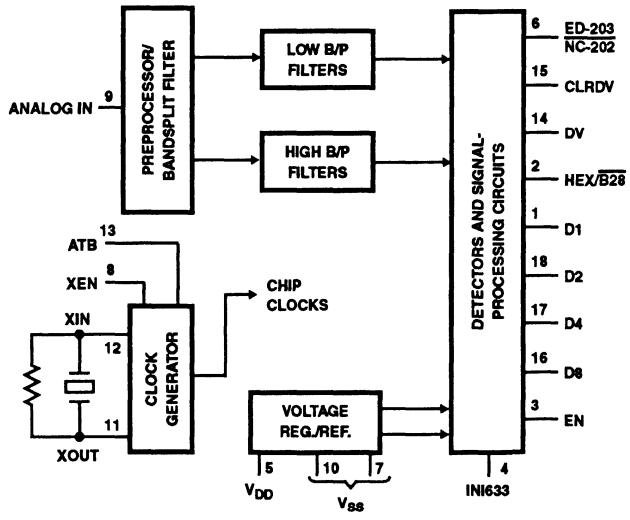
The CD22202 and CD22203 employ state-of-the-art circuit technology to combine the digital and analog functions on the same CMOS chip using a standard digital semiconductor process. The analog input is preprocessed by 60Hz reject and band splitting filters and then hard limited to provide AGC. Eight Bandpass filters detect the individual tones. The digital post processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry and are tri-state enabled to facilitate bus oriented architectures.

Pinout

CD22202, CD22203
(PDIP)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1695.2

Absolute Maximum Ratings

DC Supply Voltage (V_{DD})(Referenced to V_{SS} Terminal) ..... +7V
Power Dissipation
T_A = +25°C (Derate above T_A = +25°C at 6.25mW/°C 65mW
Input Voltage Range
All Inputs Except Analog In ..... (V_{DD} +0.5V) to -0.5V
Analog In Voltage Range ..... (V_{DD} +0.5V) to (V_{DD} -10V)
DC Current into any Input or Output ..... ±20mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Packages) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C

NOTE: Unused inputs must be connected to V_{DD} or V_{SS} as appropriate.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

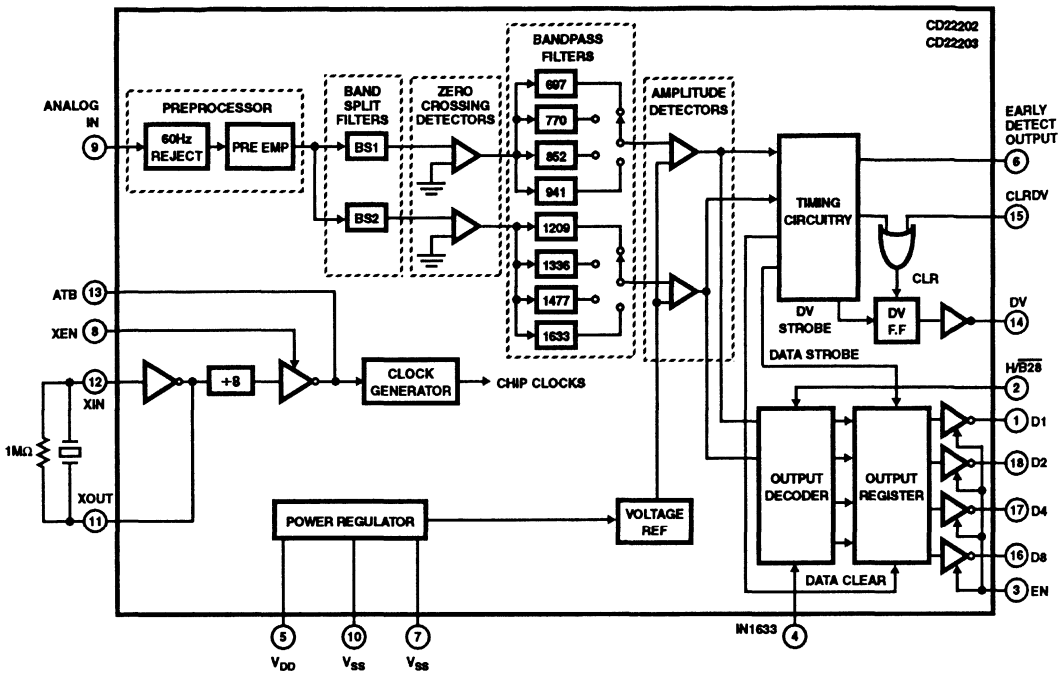
0°C ≤ T_A ≤ +70°C, V_{DD} = 5V ±10%

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		±(1.5 + 2Hz)	±2.3	±3.5	% of f_0
Amplitude for Detection	Each Tone	-32	-	-2	dBm Referenced to 600Ω
Minimum Acceptable Twist	Twist = $\frac{\text{high tone}}{\text{low tone}}$	-10	-	+10	dB
60Hz Tolerance		-	-	0.8	V_{RMS}
Dial Tone Tolerance	"Precise" Dial Tone	-	-	0	dB Referenced to Lower Amplitude Tone
Talk Off	MITEL Tape #CM7291	-	2	-	Hits
Digital Outputs (except XOUT)	"0" Level, 400µA Load	0	-	0.5	V
	"1" Level, 200µA Load	V_{DD} -0.5	-	V_{DD}	V
Digital Inputs	"0" Level	0	-	0.3V_{DD}	V
	"1" Level	0.7V_{DD}	-	V_{DD}	V
Supply Current	T_A = +25°C	-	10	16	mA
Noise Tolerance	MITEL Tape #CM7291 (Note 1)	-	-	-12	dB Referenced to Lowest Amplitude Tone
Input Impedance	$V_{DD} \geq V_{IN} \geq (V_{DD} - 10)$	100kΩ//15pF	300kΩ	-	

NOTE:

1. Bandwidth limited (3kHz) Gaussian noise.

Functional Block Diagram



NOTE: Pin 6: Early detect output on CD22203 only.

System Functions

Analog In

The Analog In pin accepts the analog input. It is internally biased so that the input signal may be either AC or DC coupled, as long as it does not exceed the positive supply voltage. Proper input coupling is illustrated below.

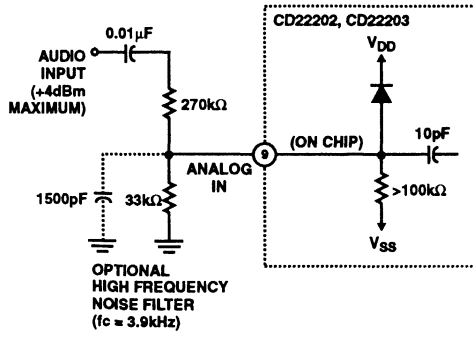


FIGURE 1. ANALOG IN

The CD22202 and CD22203 are designed to accept sinusoidal input waveforms, but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics that are at least 20dB below the fundamental.

Crystal Oscillator

The CD22202 and CD22203 contain an on-board inverter with sufficient gain to provide oscillation when connected to a low cost television "color-burst" (3.579545MHz) crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1MΩ resistor is also connected between these pins in this mode. ATB is a clock frequency output. Other CD22202 and CD22203 devices may use the same frequency reference by tying their ATB pins to the ATB output of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low, respectively. Up to ten devices may be run from a single crystal connected CD22202 and CD22203 as shown in Figure 2.

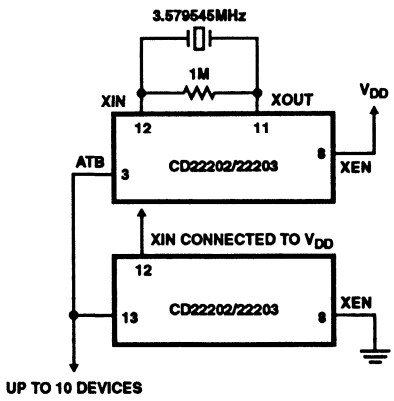


FIGURE 2. CRYSTAL OSCILLATOR

HEX/$\overline{B28}$

This pin selects the format of the digital output code. When HEX/$\overline{B28}$ is tied high, the output is hexadecimal. When tied low, the output is binary coded 2-of-8. The following table describes the two output codes.

TABLE 1. OUTPUT CODES

	HEXADECIMAL				BINARY CODED 2-OF-8			
DIGIT	D8	D4	D2	D1	D8	D4	D2	D1
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0
0	1	0	1	0	1	1	0	1
*	1	0	1	1	1	1	0	0
#	1	1	0	0	1	1	1	0
A	1	1	0	1	0	0	1	1
B	1	1	1	0	0	1	1	1
C	1	1	1	1	1	0	1	1
D	0	0	0	0	1	1	1	1

ED

This pin, on the CD22203 only, indicates the presence of frequencies which are likely to be DTMF digits, but have not yet been verified by a DV signal. It is comparable to a "button-down" output, and it is useful as an EARLY DETECT signal to interrupt a microprocessor for digit storage and validation.

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs or CLRDV is raised high, whichever is sooner. This handshake can save microprocessor time.

DTMF Dialing Matrix

	COL 0 1209Hz	COL 1 1336Hz	COL 2 1477Hz	COL 3 1633Hz
ROW 0 697Hz	1	2	3	A
ROW 1 770Hz	4	5	6	B
ROW 2 852Hz	7	8	9	C
ROW 3 941Hz	*	0	#	D

NOTE: Column 3 is for special applications and is not normally used in telephone dialing.

IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

N/C Pin

This pin has no internal connection and should be left floating.

Digital Inputs and Outputs

All digital inputs and outputs of the DTMF receivers are represented by the schematic below. Only the "analog in" pin is different, and is described above. Care must be exercised not to exceed the voltage or current ratings on these pins as listed in the "maximum ratings" section.

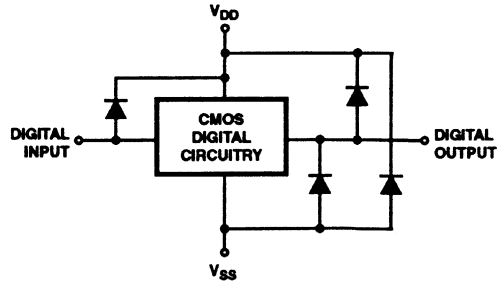


FIGURE 3. DIGITAL INPUTS AND OUTPUTS

Input Filter

The CD22202 and CD22203 will tolerate total input noise of a maximum of 12dB below the lowest amplitude tone. For most telephone applications, the combination of the high frequency attenuation of the telephone line and internal band limiting make special circuitry at the input to these receivers unnecessary. However, noise near the 56kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present

above 28kHz, the simple RC filter shown below may be used to band limit the incoming signal. The cut off frequency is 3.9kHz.

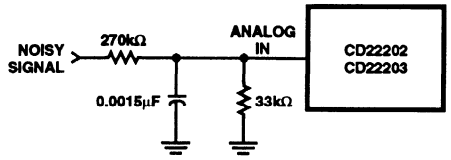
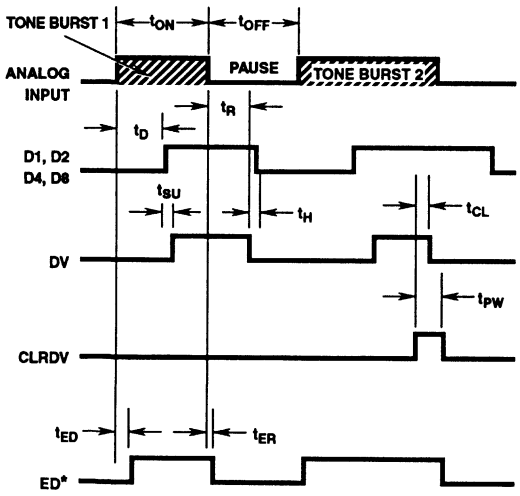


FIGURE 4. FILTER FOR USE IN EXTREME HIGH FREQUENCY INPUT NOISE ENVIRONMENT

Noise will also be reduced by placing a grounded trace around XIN and XOUT pins on the circuit board layout when using a crystal. It is important to note that XOUT is not intended to drive an additional device. XIN may be driven externally; in this case, leave XOUT floating.

Timing Waveforms



* Early Detect output is available only on the CD22203

FIGURE 5.

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS
Tone Time					
For Detection	t_{ON}	40	-	-	ms
For Rejection	t_{ON}	-	-	20	ms
Pause Time					
For Detection	t_{OFF}	40	-	-	ms
For Rejection	t_{OFF}	-	-	20	ms
Detect Time	t_D	25	-	46	ms
Release Time	t_R	35		50	ms
Data Setup Time	t_{SU}	7	-	-	μs
Data Hold Time	t_H	4.2	-	5	ms
DV Clear Time	t_{CL}	-	160	250	ns
CLRDV Pulse Width	t_{PW}	200	-	-	ns
ED Detect Time	t_{ED}	7	-	22	ms
ED Release Time	t_{ER}	2	-	18	ms
Output Enable Time C_L = 50pF, R_L = 1kΩ	-	-	200	300	ns
Output Disable Time C_L = 35pF, R_L = 500Ω	-	-	150	200	ns
Output Rise Time C_L = 50pF	-	-	200	300	ns
Output Fall Time C_L = 50pF	-	-	160	250	ns

Guard Time

Whenever the DTMF receiver is continually monitoring a voice channel containing distorted or musical voices or tones, additional guard time may be added in order to prevent false decoding. This may be done in software by verifying that both ED and DV are present simultaneously for about 55ms. An appropriate guard time should be selected to balance the fastest expected dialing speed against the rejection of distorted or musical voices or tones (most autodialers operate in the 65ms to 75ms range although a few generate 50ms tones). A hardware guard time circuit is shown in Figure 6. R3 and R4 should keep the voice amplitude as low as practical, while R2 and R5 adjust detection speed.

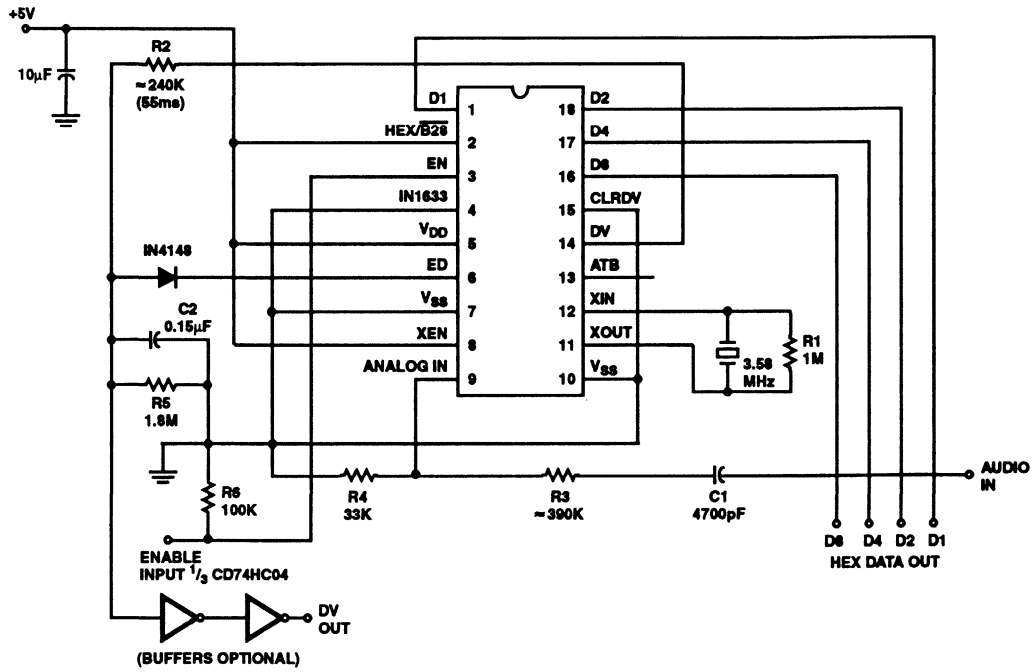


FIGURE 6. CD22203 DTMF RECEIVER WITH GUARD TIME CIRCUIT TO PROVIDE EXCEPTIONAL TALK-OFF PERFORMANCE

Operating and Handling Considerations

Handling

All inputs and outputs of CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits".

Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turnoff transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} - V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 20mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

HARRIS SEMICONDUCTOR

CD22204

5V Low Power Subscriber DTMF Receiver

March 1993

Features

- No Front End Band Splitting Filters Required
- Single Low Tolerance 5V Supply
- Three-State Outputs for Microprocessor Based Systems
- Detects all 16 Standard DTMF Digits
- Uses Inexpensive 3.579545MHz Crystal
- Excellent Speech Immunity
- Output in 4-Bit Hexadecimal Code
- Excellent Latch-Up Immunity

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
CD22204E	0°C to +70°C	14 Lead Plastic DIP
CD22204M	0°C to +70°C	24 Lead SOIC

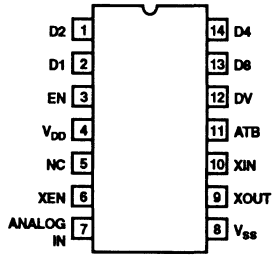
Description

The CD22204 complete dual tone multiple frequency (DTMF) receiver detects a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.579545MHz TV "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is possible through the use of the Alternate Time Base (ATB) output of a crystal connected CD22204 receiver to drive the time bases of up to 10 additional receivers. This is a monolithic integrated circuit fabricated with low power, complementary symmetry CMOS processing. It only requires a single power supply.

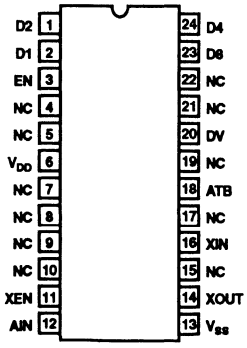
The CD22204 employs state-of-the-art "switched-capacitor" filter technology, resulting in approximately 40 poles of filtering and digital circuitry on the same CMOS chip. The analog input is preprocessed by 60Hz reject and bandsplitting filters and then zero-cross detected to provide AGC. Eight bandpass filters detect the individual tones. Digital processing is used to measure the tone and pause durations and provides the correctly coded and timed digital outputs. The outputs interface directly to standard CMOS circuitry and are tri-state enabled to facilitate bus oriented architectures.

Pinouts

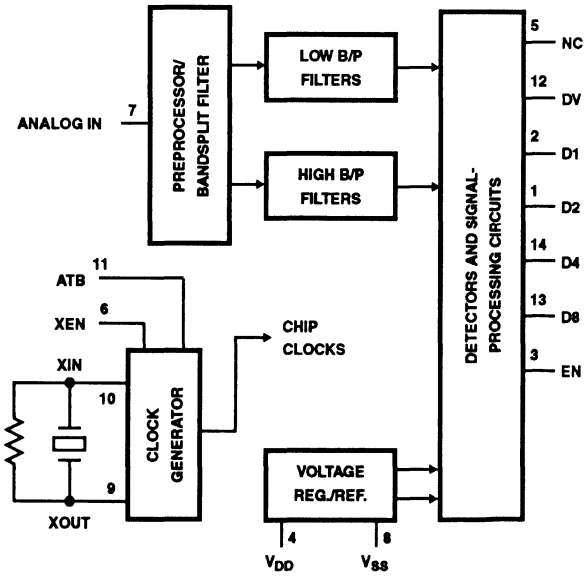
CD22204 (PDIP)
TOP VIEW



CD22204 (SOIC)
TOP VIEW



Functional Diagram



NOTE: Pin numbers are for plastic DIP.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1696.2

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{DD})(Referenced to V_{SS} Terminal) ..... +7V
Power Dissipation
T_A = +25°C (Derate above T_A = +25°C at 6.25mW/°C 65mW
Input Voltage Range
All Inputs Except Analog In ..... (V_{DD} +0.5V) to -0.5V
Analog In Voltage Range ..... (V_{DD} +0.5V) to (V_{DD} -10V)
DC Current into any Input or Output ..... ±20mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Packages) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

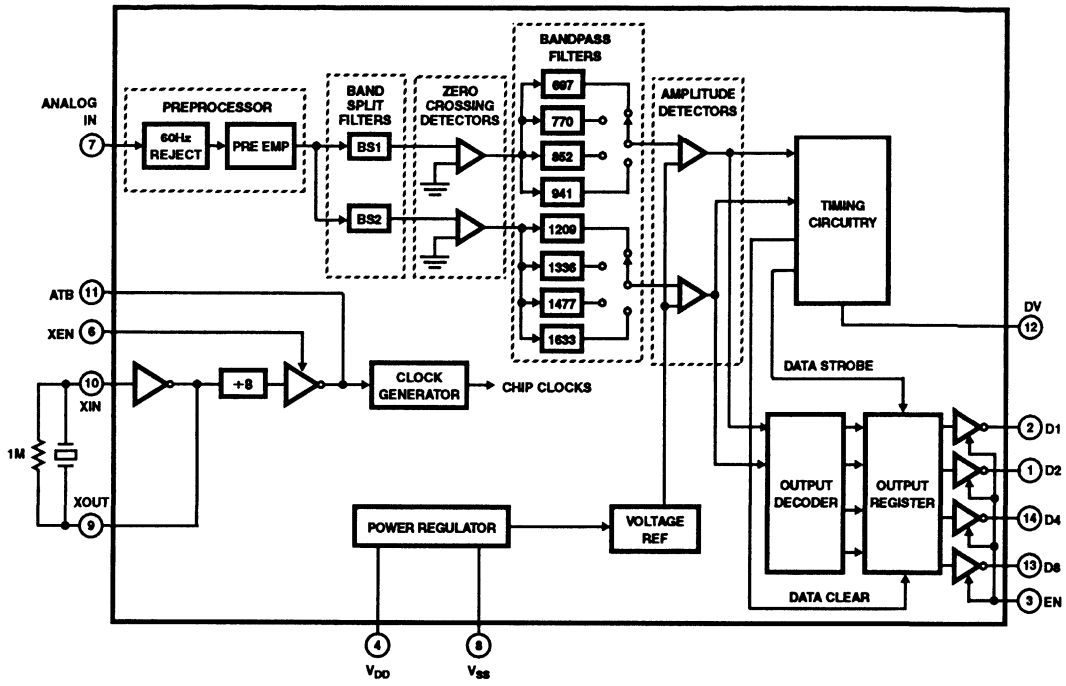
0°C ≤ T_A ≤ +70°C, V_{DD} = 5V ±10%

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		±(1.5 + 2Hz)	±2.3	±3.5	% of f_O
Amplitude for Detection	Each Tone	-32 (Note 3)	-	-2	dBm Referenced to 600Ω
Minimum Acceptable Twist	Twist = $\frac{\text{high tone}}{\text{low tone}}$	-8	-	+4	dB
60Hz Tolerance		-	-	0.8	V_{RMS}
Dial Tone Tolerance	"Precise" Dial Tone	-	-	0	dB Referenced to Lower Amplitude Tone
Talk Off	MITEL Tape #CM7291	-	2	-	Hits
Digital Outputs (except XOUT)	"0" Level, 400µA Load	0	-	0.5	V
	"1" Level, 200µA Load	V_{DD} -0.5	-	V_{DD}	V
Digital Inputs	"0" Level	0	-	$0.3V_{DD}$	V
	"1" Level	$0.7V_{DD}$	-	V_{DD}	V
Supply Current	T_A = +25°C	-	10	20	mA
Noise Tolerance	MITEL Tape #CM7291 (Note 2)	-	-	-12	dB Referenced to Lowest Amplitude Tone
Input Impedance	$V_{DD} \geq V_{IN} \geq (V_{DD} - 10)$	100kΩ//15pF	300kΩ	-	

NOTES:

1. Unused inputs must be connected to V_{DD} or V_{SS} as appropriate.
2. Bandwidth limited (3kHz) Gaussian noise.
3. Lower minimum available, please contact sales office.

Functional Block Diagram



NOTE: Pin numbers are for plastic DIP.

System Functions

Analog In

The Analog In pin accepts the analog input. It is internally biased so that the input signal may be either AC or DC coupled, as long as it does not exceed the positive supply voltage. Proper input coupling is illustrated below.

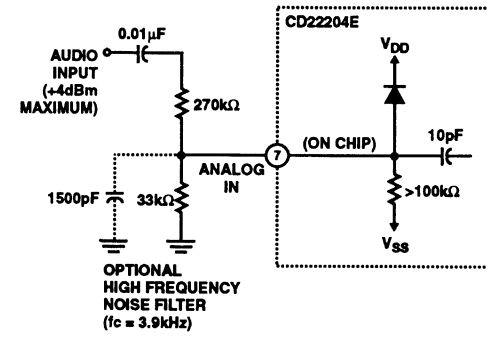


FIGURE 1. ANALOG IN

The CD22204 is designed to accept sinusoidal input waveforms, but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics that are at least 20dB below the fundamental.

Crystal Oscillator

The CD22204 contains an on-board inverter with sufficient gain to provide oscillation when connected to a low cost television "color-burst" (3.579545MHz) crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1MΩ resistor is also connected between these pins in this mode. ATB is a clock frequency output. Other CD22204 devices may use the same frequency reference by tying their ATB pins to the ATB output of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low, respectively. Up to ten devices may be run from a single crystal connected CD22204 as shown in Figure 2.

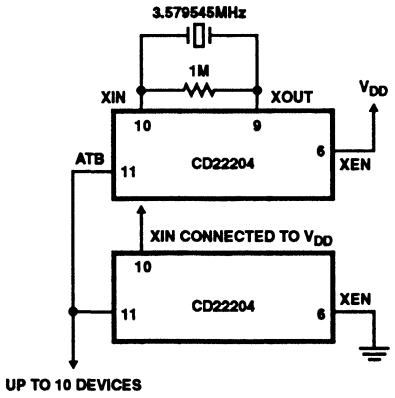


FIGURE 2. CRYSTAL OSCILLATOR

Outputs D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the hexadecimal code corresponding to the detected digit. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed. The table below describes the hexadecimal codes.

TABLE 1. OUTPUT CODES

DIGIT	D8	D4	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

DV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs.

N/C Pin

This pin has no internal connection and should be left floating.

DTMF Dialing Matrix

	COL 0 1209Hz	COL 1 1336Hz	COL 2 1477Hz	COL 3 1633Hz
ROW 0 697Hz	1	2	3	A
ROW 1 770Hz	4	5	6	B
ROW 2 852Hz	7	8	9	C
ROW 3 941Hz	*	0	#	D

NOTE: Column 3 is for special applications and is not normally used in telephone dialing.

Digital Inputs and Outputs

All digital inputs and outputs of the DTMF receivers are represented by the schematic below. Only the "analog in" pin is different, and is described above. Care must be exercised not to exceed the voltage or current ratings on these pins as listed in the "maximum ratings" section.

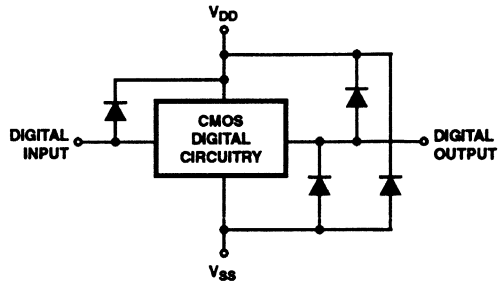


FIGURE 3. DIGITAL INPUTS AND OUTPUTS

Input Filter

The CD22204 will tolerate total input noise of a maximum of 12dB below the lowest amplitude tone. For most telephone applications, the combination of the high frequency attenuation of the telephone line and internal band limiting make special circuitry at the input to these receivers unnecessary. However, noise near the 56kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present above 28kHz, the simple RC filter shown below may be used to band limit the incoming signal. The cut off frequency is 3.9kHz.

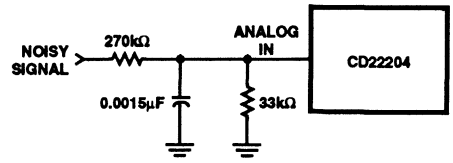


FIGURE 4. FILTER FOR USE IN EXTREME HIGH FREQUENCY INPUT NOISE ENVIRONMENT

Noise will also be reduced by placing a grounded trace around XIN and XOUT pins on the circuit board layout when using a crystal. It is important to note that XOUT is not intended to drive an additional device. XIN may be driven externally; in this case, leave XOUT floating.

Timing Waveforms

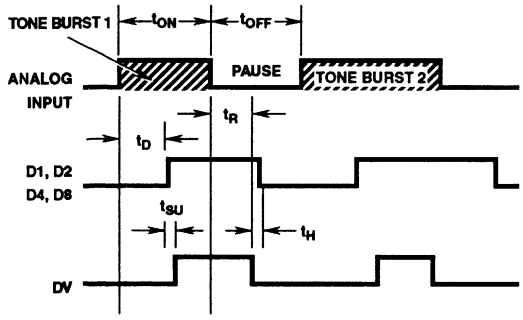


FIGURE 5.

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS
Tone Time					
For Detection	t_{ON}	40	-	-	ms
For Rejection	t_{ON}	-	-	20	ms
Pause Time					
For Detection	t_{OFF}	40	-	-	ms
For Rejection	t_{OFF}	-	-	20	ms
Detect Time	t_D	25	-	46	ms
Release Time	t_R	35		50	ms
Data Setup Time	t_{SU}	7	-	-	µs
Data Hold Time	t_H	4.2	-	5	ms
Output Enable Time C_L = 50pF, R_L = 1kΩ	-	-	200	300	ns
Output Disable Time C_L = 35pF, R_L = 500Ω	-	-	150	200	ns
Output Rise Time C_L = 50pF	-	-	200	300	ns
Output Fall Time C_L = 50pF	-	-	160	250	ns

HARRIS SEMICONDUCTOR

CD22301

March 1993

Monolithic PCM Repeater

Features

- Automatic Line Buildout
- Supply Voltage 5.1V
- Buffered Output

Applications

- Bipolar Carrier System T1 1.544Mbits/s
- Ternary Carrier System T148 2.37Mbits/s

Description

The CD22301 monolithic PCM repeater circuit is designed for T1 carrier systems operating with a bipolar pulse train of 1.544Mbits/s. It can also be used in the T148 carrier system operating with a ternary pulse train of 2.37Mbits/s. The circuit operates from a 5.1V ±5% externally regulated supply.

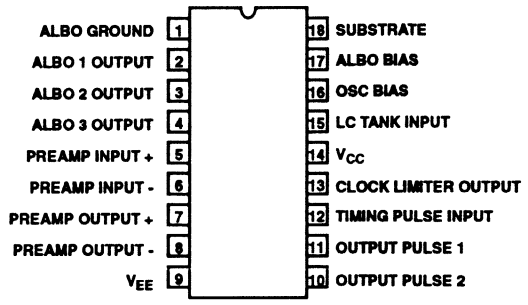
The CD22301 provides active circuitry to perform all functions of signal equalization and amplification, automatic line buildout (ALBO), threshold detection, clock extraction, pulse timing and buffered output formation.

Ordering Information

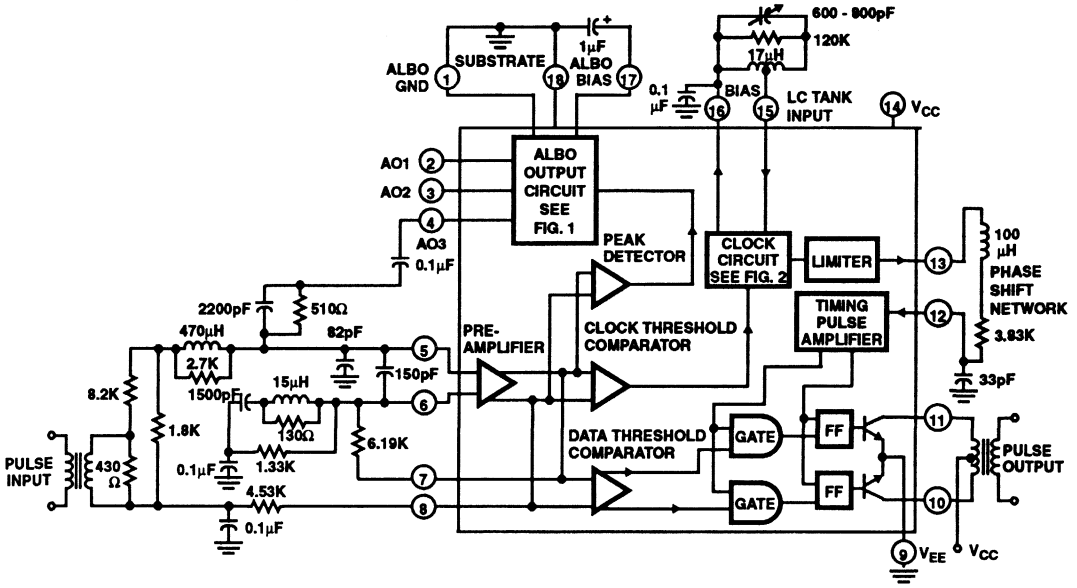
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CD22301E	-40°C to +85°C	18 Lead Plastic DIP

Pinout

CD22301, (PDIP)
TOP VIEW



Typical 1.544MHz T1 Repeater System



8 TELECOM

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1368.2

Absolute Maximum Ratings

Supply Voltage 10V
Input Current (Into Pin 9 or 10) 25mA
Peak Current (Into Pin 9 or 10) 100mA
Input Surge Voltage (Between Pins 5 and 6, t = 10ms) 50V
Output Surge Voltage (Between Pins 10 and 11, t = 1ms) 50V
Power Dissipation
For T_A = -40°C to +60°C 500mW
For T_A = +60°C to +85°C .. Derate Linearly 12mW/°C to 200mW
Device Dissipation per Output Transistor
For T_A = Full Package Temperature Range (All Types) 100mW
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Recommended Operating Conditions

Operating Temperature Range ..... -40°C ≤ T_A ≤ +85°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications T_A = +25°C, V_{CC} = 5.1V ± 5% (See Figure 4)

PARAMETERS	LIMITS			UNITS
	MIN	TYP	MAX	
DC VOLTAGES				
ALBO Pins (Pins 2, 3, 4 and 17)	-	0	0.1	V
Pre Amp Inputs and Outputs (Pins 5, 6, 7 and 8)	2.4	2.9	3.4	V
Output Pulse 1, 2 (Pins 10 and 11)	-	5.1	-	V
Oscillator/Clock (Pins 12, 13, 15 and 16)	3.1	3.6	4.1	V
DC CURRENTS				
I_{CC}	-	22	30	mA
Output Pulse 1, 2 (Pins 10 and 11)	-	0	100	µA

Dynamic Electrical Specifications T_A = +25°C , V_{CC} = 5.1V ± 5%

PARAMETERS	SYMBOL	FIGURE	NOTE	LIMITS			UNITS
				MIN	TYP	MAX	
Preamplifier Input Impedance	Z_{IN}	7		20	-	-	kΩ
Preamplifier Output Impedance	Z_{OUT}	7		-	-	2	kΩ
Preamplifier Gain at 2.37MHz	A_O	7		47	50	-	dB
Preamplifier Output Offset Voltage	ΔV_{OUT}	7	1	-50	0	50	mV
Clock Limiter Input Impedance	$Z_{IN}(CL)$	5	2	10	-	-	kΩ
ALBO Off Impedance	$Z_{ALBO}(off)$	5	3	20	-	-	kΩ
ALBO On Impedance	$Z_{ALBO}(on)$	5	4	-	-	10	Ω
DATA Threshold Voltage	$V_{TH}(D)$	6	5, 8	0.62	0.7	0.78	V
CLOCK Threshold Voltage	$V_{TH}(CL)$	6	6, 8	0.92	1.1	1.28	V
ALBO Threshold	$V_{TH}(AL)$	6	7, 8	1.4	1.5	1.6	V
$V_{TH}(D)$ as % of $V_{TH}(AL)$				44	47	49	%
$V_{TH}(CL)$ as % of $V_{TH}(AL)$				66	73	80	%
Buffer Gate Voltage (low)	V_{OL}	4	9	0.65	0.8	0.95	V
Differential Buffer Gate Voltage	ΔV_{OL}	4	9	-0.15	0	0.15	V
Output Pulse Rise Time	t_R	4, 8	9, 10	-	-	40	ns

Dynamic Electrical Specifications $T_A = +25°C$, $V_{CC} = 5.1V \pm 5\%$

PARAMETERS	SYMBOL	FIGURE	NOTE	LIMITS			UNITS
				MIN	TYP	MAX	
Output Pulse Fall Time	t_F	4, 8	9, 10	-	-	40	ns
Output Pulse Width	t_W	4, 8	9, 10	290	324	340	ns
Pulse Width Differential	Δt_W	4, 8	9, 10	-10	0	10	ns
Clock Drive Current	I_{CL}			-	2	-	mA

NOTES:

1. No signal input. Measure voltage between pins 7 and 8.
2. Measure clock limiter input impedance at pin 15. See Figure 5.
3. Adjust potentiometer for 0V (See Figure 5). Measure ALBO off impedances from pins 2, 3 and 4 to pin 1.
4. Increase potentiometer until voltage at pin 17 = 2V (See Figure 5). Measure ALBO on impedances from pins 2, 3 and 4 to pin 1.
5. Adjust potentiometer for $\Delta V = 0V$ (See Figure 6). Then slowly increase ΔV in the positive direction until pulses are observed at the DATA terminal.
6. Continue increasing ΔV until the DC level at the clock terminal drops to 4V (See Figure 6).
7. Continue increasing ΔV until the ALBO terminal rises to 1V (See Figure 6).
8. Turn potentiometer in the opposite direction and measure negative threshold voltages by repeating tests outlined in notes 5, 6 and 7.
9. Set $e_{IN} = 2.75mV_{RMS}$ at f = 1.185MHz. Adjust frequency until maximum amplitude is obtained at pin 15. Observe output pulses at pins 10 and 11.
10. Adjust input signal amplitude until pulses just appear in outputs. Increase input amplitude by three dB.

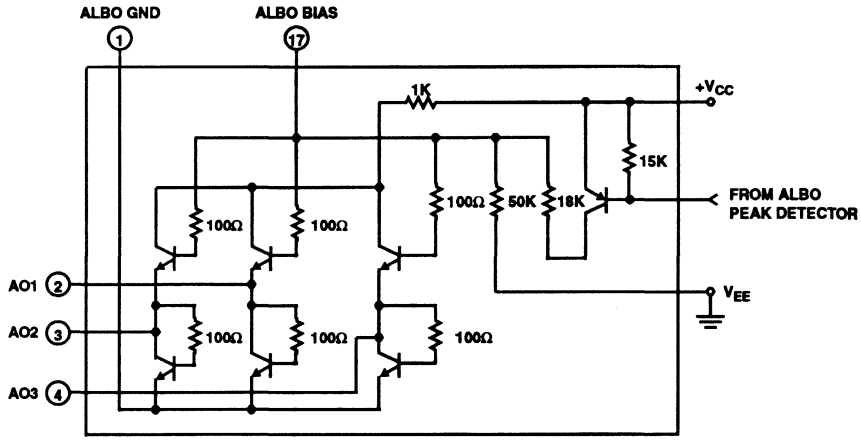


FIGURE 1. ALBO OUTPUT CIRCUIT

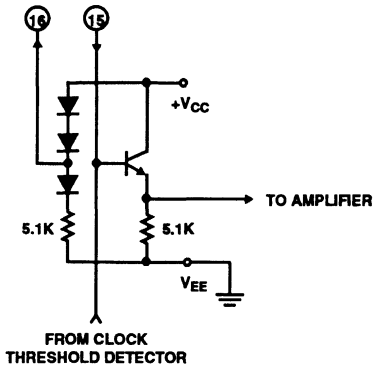


FIGURE 2. CLOCK INTERFACE CIRCUIT

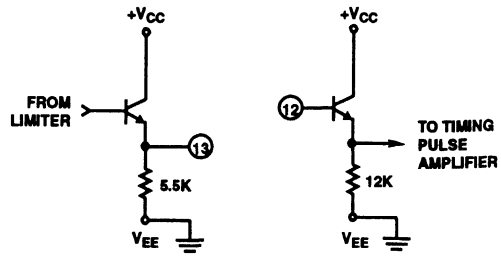


FIGURE 3. PHASE-SHIFT INTERFACE CIRCUITS

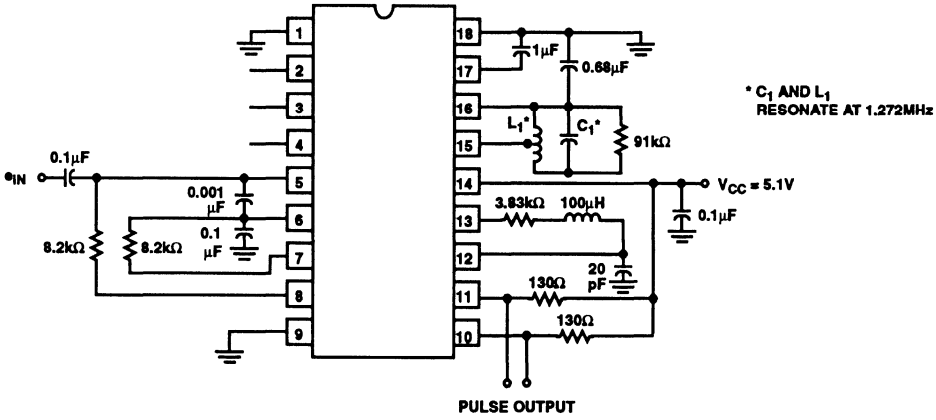


FIGURE 4. DC AND OUTPUT PULSE TEST CIRCUIT

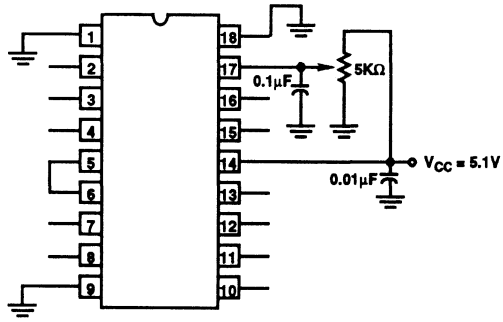


FIGURE 5. TEST CIRCUIT FOR IMPEDANCE MEASUREMENT

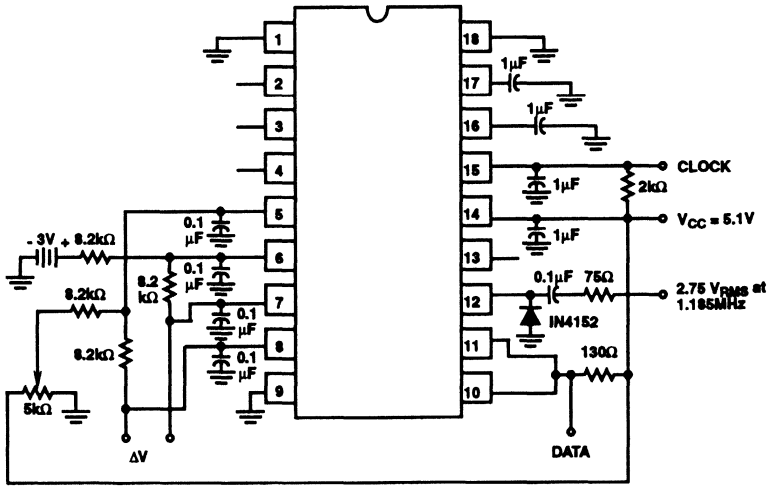


FIGURE 6. TEST CIRCUIT FOR THRESHOLD VOLTAGE MEASUREMENT

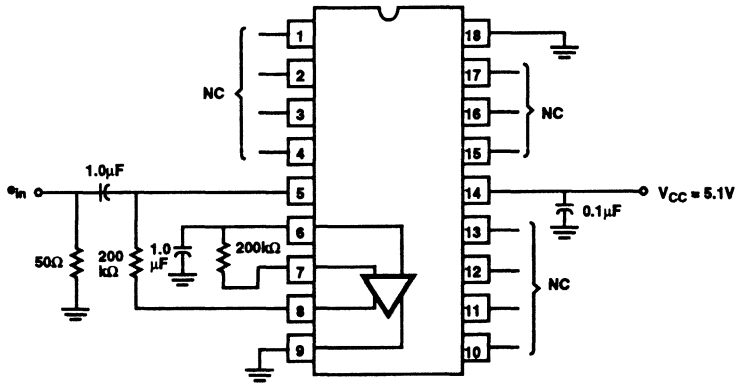


FIGURE 7. PREAMPLIFIER GAIN AND IMPEDANCE MEASUREMENT CIRCUIT

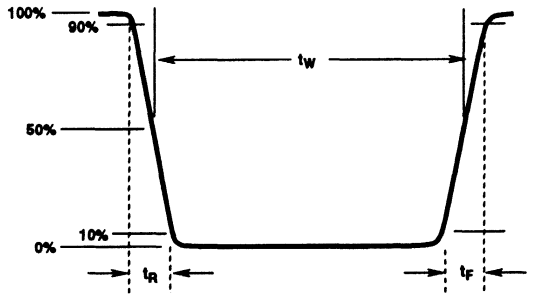


FIGURE 8. OUTPUT PULSE WAVEFORM

HARRIS SEMICONDUCTOR

CD22354A
CD22357A

CMOS Single-Chip, Full-Feature PCM CODEC

March 1993

Features

- Meets or Exceeds All AT&T D3/D4 Specifications and CCITT Recommendations
- Complete CODEC and Filtering Systems: No External Components for Sample-and-Hold and Auto-Zero Functions. Receive Output Filter with (SIN X)/X Correction and Additional 8kHz Suppression
- Variable Data Clocks - From 64kHz 2.1MHz
- Receiver Includes Power-Up Click Filter
- TTL or CMOS-Compatible Logic
- ESD Protection on All Inputs and Outputs

Applications

- PABX
- Central Office Switching Systems
- Accurate A/D and D/A Conversions
- Digital Telephones
- Cellular Telephone Switching Systems
- Voice Scramblers - Descramblers
- T1 Conference Bridges
- Voice Storage and Retrieval Systems
- Sound Based Security Systems
- Computerized Voice Analysis
- Mobile Radio Telephone Systems
- Microwave Telephone Networks
- Fiber-Optic Telephone Networks

Description

The CD22354A and CD22357A are monolithic silicon-gate, double-poly CMOS integrated circuits containing the band-limiting filters and the companding A/D and D/A conversion circuits that conform to the AT&T D3/D4 specifications and CCITT recommendations. The CD22354A provides the AT&T μ-law and the CD22357A provides the CCITT A-law companding characteristic.

The primary applications for the CD22354A and CD22357A are in telephone systems. These circuits perform the analog and digital conversions between the subscriber loop and the PCM highway in a digital switching system. The functional block diagram is shown below.

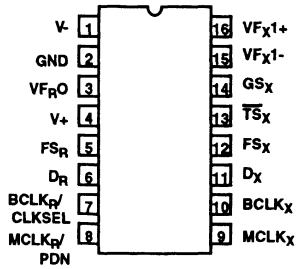
With flexible features, including synchronous and asynchronous operations and variable data rates, the CD22354A and CD22357A are ideally suited for PABX, central office switching system, digital telephones as well as other applications that require accurate A/D and D/A conversions and minimal conversion time.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CD22354AE	-40°C to +80°C	16 Lead Plastic DIP
CD22357AE	-40°C to +80°C	16 Lead Plastic DIP

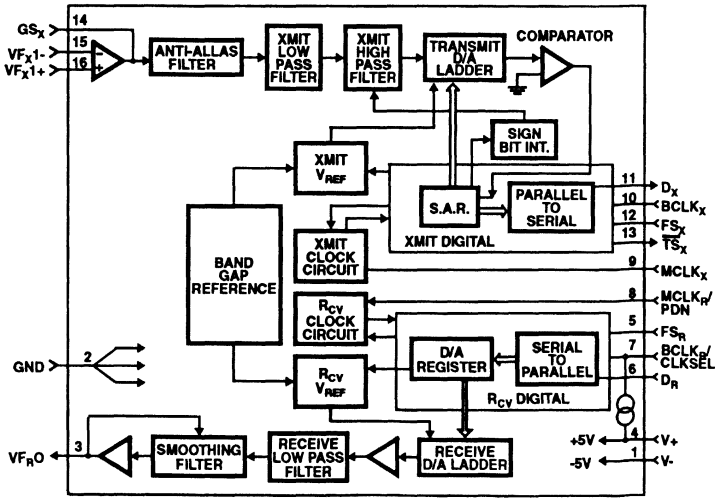
Pinout

CD22354A, CD22357A
(PDIP)
TOP VIEW



Functional Block Diagram

FULL-FEATURE PCM CODEC



File Number 1682.2

Absolute Maximum Ratings

DC Supply-Voltage, (V+) ..... -0.5 to +7V
DC Supply-Voltage, (V-) ..... +0.5 to -7V
DC Input Diode Current,
I_{IK} (V_I < V- -0.5V or V_I > V+ +0.5V) ..... ±20mA
DC Output Diode Current,
I_{OK} (V_I < V- -0.5V or V_O > V+ +0.5V) ..... ±20mA
DC Drain Current, Per Output
I_O (V- -0.5V < V_O < V+ +0.5V) ..... ±25mA
DC Supply/Ground Current ..... ±50mA
Power Dissipation Per Package (P_D):
For T_A = -40°C to +60°C 500mW
For T_A = +60°C to +85°C ..... Derate Linearly at 8mW/°C to 300mW
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Reliability Information

Operating-Temperature Range (T_A) ..... -40°C to +80°C
Storage Temperature (T_{STG}) ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications At T_A = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Positive Power Supply	V+		4.75	5	5.25	V
Negative Power Supply	V-		-4.75	-5	-5.25	V
Power Dissipation (Operating)	P_{OPR}	V+ = 5V	-	75	90	mW
Power Dissipation (Standby)	P_{STBY}	V- = -5V	-	9	15	mW

Static Electrical Specification At T_A = 0°C to 70°C; V+ = 5V ±5%, V- = -5V ±5%

PARAMETER	SYMBOL		LIMITS			UNITS
			MIN	TYP	MAX	
Analog Input Resistance	R_{INA}		10	-	-	MΩ
Input Capacitance	C_{IN}	All Logic and Analog Inputs	-	5	-	pF
Input Leakage Current, Digital	I_I	V_I = 0V or V+	-10	-	10	µA
Low Level Input Voltage	V_{IL}	I_{IL} = ±10µA max	-	-	0.8	V
High Level Input Voltage	V_{IH}	I_{IH} = ±10µA max	2	-	-	V
Low Level Output Voltage	V_{OL}	I_{OL} = 3.2mA	-	-	0.4	V
High Level Output Voltage	V_{OH}	I_{OH} = 1.0mA	2.4	-	-	V
Open State Output Current	I_{OZ}	GND < D_X < V+	-10	-	10	µA
Input Leakage Current, Analog	I_I	-2.5V ≤ $VF_X1±$ ≤ 2.5V	-200	-	200	nA

Transmit and Receive Filter Transfer Characteristics

V+ = 5V ±5%, V- = -5V ± 5%, $BCLK_R = BCLK_X = MCLK_X = 1.544MHz$, V_{IN} = 0dBm0, T_A = 0°C to 70°C

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Transmit Gain (Relative to Gain at 1020Hz) Input Amplifier Set to Unity Gain	G_{RX}	f = 16Hz	-	-	-40	dB
		f = 50Hz	-	-	-30	dB
		f = 60Hz	-	-	-26	dB
		f = 200Hz	-1.8	-	-0.1	dB
		f = 300 to 3000Hz	-0.15	-	0.15	dB
		f = 3300Hz	-0.35	-	0.05	dB
		f = 3400Hz	-0.7	-	0	dB
		f = 4000Hz	-	-	-14	dB
		f ≥ 4600Hz, Measure 0 - 4kHz Response	-	-	-32	dB
Receive Gain (Relative to Gain at 1020Hz) (Includes (SIN X)/X Compensation)	G_{RR}	f = 0Hz to 3000Hz	-0.15	-	0.15	dB
		f = 3300Hz	-0.35	-	0.05	dB
		f = 3400Hz	-0.7	-	0	dB
		f = 4000Hz	-	-	-14	dB

A.C. Specifications

Unless otherwise specified, the following conditions apply:

V+ = 5V ± 5%, V- = -5V ± 5%
GND_A, GND_D = 0V, F_{FX} = 1020Hz at 0dBm0
Transmit input amplifier operating in a unity gain configuration
Temperature . . . . . 0°C to 70°C
Receive output is measured single-ended. All output levels are (SIN X)/X corrected.

Definition

AMPLITUDE RESPONSE
Absolute Levels Definition:
V_{REF} = -2.5V
Nominal 0 dBm0 level . . . . . 4dBm into 600Ω
$1.2276V_{RMS}$
Maximum Overload Level:
Voltage reference (V_{REF}) of -2.5V . . . . . 2.5V μ-Law
2.49V A-Law

A.C. Specifications: Encoding Format at D_X Output

	CD22357A μ-LAW								CD22354A A-LAW (INCLUDES EVEN BIT INVERSION)							
V_{IN} (at GS_X) = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} (at GS_X) = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} (at GS_X) = -Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

A.C. Distortion Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Signal to Total Distortion Xmit or R_{CV}	STD_X, STD_R	Level = +3dBm0	33	-	-	dBC
		Level = 0 to -30dBm0	36	-	-	dBC
		Level = -40dBm0	30	-	-	dBC
		Level = -55dBm0, XMT	14	-	-	dBC
		Level = -55dBm0, R_{CV}	15	-	-	dBC
Single Frequency Distortion Xmit or R_{CV}	SFD_X, SFD_R		-	-	-46	dBC
Intermodulation (End-to-End Measurement) 2-Tone	IMD	V_{FX} = -4dBm0 to -21dBm0 f1, f2 from 300 to 3400Hz	-	-	-41	dB
Transmit Delay, Absolute	t_{DAX}	f = 1600Hz	-	280	315	µs
Transmit Envelope Delay Relative to t_{DAX}	t_{DEX}	f = 500-600Hz	-	170	220	µs
		f = 600-1000Hz	-	70	145	µs
		f = 1000-2600Hz	-	40	75	µs
		f = 2600-2800Hz	-	90	105	µs
Receive Delay, Absolute	t_{DAR}	f = 1600Hz	-	180	200	µs
Receive Envelope Delay Relative to t_{DAR}	t_{DER}	f = 500-600Hz	-40	-25	-	µs
		f = 600-1000Hz	-40	-25	-	µs
		f = 1000-2600Hz	-	60	90	µs
		f = 2600-2800Hz	-	110	125	µs

A.C. Specifications: Gain Tracking

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Transmit Gain Tracking Error	GTX	+3 to -40dBm0	-	-	±0.2	dB
		-40 to -50dBm0	-	-	±0.4	dB
		-50 to -55dBm0	-	-	±1.2	dB
Receive Gain Tracking Error	GTR	+3 to -40dBm0	-	-	±0.2	dB
		-40 to -50dBm0	-	-	±0.4	dB
		-50 to -55dBm0	-	-	±1.2	dB

A.C. Specifications: Gain Tracking (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Transmit Input Amplifier Gain, Open Loop	A_{OL}	$R_L \geq 1M\Omega$ at GS_X	68	-	-	dB
Transmit Input Amplifier Gain, Unity	A_{CL}	Unity Gain Configuration Inverting or Non-Inverting $R_L \geq 10K$, $C_L \leq 50pF$	-0.01	-	0.01	dB
Transmit Gain, Absolute	G_{XA}	$R_L \geq 10K$, $C_L \leq 50pF$	-0.15	-	0.15	dB
Receive Gain, Absolute	G_{RA}	$R_L \geq 600V$, $C_L \leq 500pF$	-0.15	-	0.15	dB

A.C. Noise Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Transmit Noise	N_X	VF_XI- = GND	-	12	15	dBrnc0
		VF_XI+ = GND	-	-74	-67	dBrn0p
Receive Noise	N_R	PCM Code Equivalent to Zero Volts	-	7	11	dBrnc0
			-	-83	-79	dBrn0p
V+ Power Supply Rejection Transmit	PSRR	VF_XI+ = 0V V+ = 5V + ($100mV_{RMS}$) f = 0 to 50kHz	40	-	-	dBC
V- Power Supply Rejection Transmit	PSRR	VF_XI- = 0V V- = -5V + ($100mV_{RMS}$) f = 0 to 50kHz	40	-	-	dBC
V+ Power Supply Rejection Receive	PSRR	PCM Code = All 1 Code V+ = 5V + ($100mV_{RMS}$) f = 0 to 4kHz	40	-	-	dBC
		f = 4k to 25kHz	37	-	-	dB
		f = 25k to 50kHz	36	-	-	dB
V- Power Supply Rejection Receive	PSRR	PCM Code = All 1 Code V- = -5V + ($100mV_{RMS}$) f = 0 to 4kHz	40	-	-	dBC
		f = 4k to 25kHz	40	-	-	dB
		f = 25k to 50kHz	36	-	-	dB
Cross Talk Transmit to Receive	CT_{XR}	VF_XI- = 0dBm0 at 1020Hz	-	-80	-70	dB
Cross Talk Receive to Transmit	CT_{RX}	D_R = 0dBm0 at 1020Hz, VF_XI- = 0V	-	-76	-70	dB

A.C. Timing Specifications

PARAMETER	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Frequency of Master Clocks	$1/t_{PM}$	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin	-	1.536	-	MHz
			-	1.544	-	MHz
		$MCLK_X$ and $MCLK_R$	-	2.048	-	MHz
Width of Master Clock High	t_{WMH}	$MCLK_X$ and $MCLK_R$	160	-	-	ns
Width of Master Clock Low	t_{WML}	$MCLK_X$ and $MCLK_R$	160	-	-	ns
Rise Time of Master Clock	t_{RM}	$MCLK_X$ and $MCLK_R$	-	-	50	ns
Fall Time of Master Clock	t_{FM}	$MCLK_X$ and $MCLK_R$	-	-	50	ns
Set-up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	t_{SBFM}	First Bit Clock after the Leading Edge of FS_X	100	-	-	ns
Period of Bit Clock	t_{PB}		485	488	15,725	ns
Width of Bit Clock High	t_{WBH}	V_{IH} = 2.2V	160	-	-	ns
Width of Bit Clock Low	t_{WBL}	V_{IL} = 0.6V	160	-	-	ns
Rise Time of Bit Clock	t_{RB}	t_{PB} = 488ns	-	-	50	ns
Fall Time of Bit Clock	t_{FB}	t_{PB} = 488ns	-	-	50	ns
Hold Time from Bit Clock Low to Frame Sync	t_{HBF}	Long Frame Only	0	-	-	ns
Hold Time from Bit Clock High to Frame Sync	t_{HOLD}	Short Frame Only	0	-	-	ns
Set-up Time from Frame Sync to Bit Clock Low	t_{SFB}	Long Frame Only	80	-	-	ns
Delay Time from $BCLK_X$ High to Data Valid	t_{DBD}	Load = 150pF plus 2 LSTTL Loads	0	-	180	ns
Delay Time to $\overline{TS}_X$ Low	t_{XDP}	Load = 150pF plus 2 LSTTL Loads	-	-	140	ns
Delay Time from $BCLK_X$ Low or FS_X Low to Data Output Disabled	t_{DZC}		50	-	165	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	t_{DZF}	C_L = 0pF to 150pF	20	-	165	ns
Set-up Time from D_R Valid to $BCLK_{R/X}$ Low	t_{SDB}		50	-	-	ns
Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	t_{HBD}		50	-	-	ns
Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	t_{SF}	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	50	-	-	ns
Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	t_{HF}	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	100	-	-	ns

A.C. Timing Specifications (Continued)

PARAMETER	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	t_{HBFI}	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100	-	-	ns
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64K Bit/s Operating Mode	160	-	-	ns

NOTE:

1. For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

Pin Function and Description

PIN NO.	SYMBOL	DESCRIPTION
1	V-	Negative power supply, V- = -5V ± 5%.
2	GND	Analog and digital ground. All signals referenced to this pin.
3	VF_RO	Analog output of RECEIVE FILTER.
4	V+	Positive power supply, V+ = +5V ± 5%.
5	FS_R	Receive Frame Sync Pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8kHz PULSE TRAIN.
6	D_R	Receive Data Input. PCM data is shifted into D_R following the FS_R leading edge.
7	$BCLK_R$/CLKSEL	The Receive Bit Clock, which shifts data into D_R after the frame sync leading edge, may vary from 64kHz to 2.048MHz. Alternatively, the leading edge may be a logic input which selects either 1.536MHz/ 1.544MHz or 2.048MHz for Master Clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions.
8	$MCLK_R$/PDN	Receive Master Clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_X$, but best performance is realized from synchronous operation. When this pin is continuously connected low, $MCLK_X$ is selected for all internal timing. When this pin is continuously connected high, the device is powered down.
9	$MCLK_X$	Transmit Master Clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_R$, but best performance is realized from synchronous operation.
10	$BCLK_X$	The Bit Clock which shifts out the PCM Data on D_X. May vary from 64kHz to 2.048MHz, but must be synchronous with $MCLK_X$.
11	D_X	The TRI-STATE PCM Data Output which is enabled by FS_X.
12	FS_X	Transmit Frame Sync Pulse input which enables $BCLK_X$ to shift out the data on D_X. FS_X is an 8kHz PULSE TRAIN.
13	$\overline{TS}_X$	Open drain output which pulses low during the encoder time slot.
14	GS_X	Transmit gain adjust.
15	VF_XI-	Inverting input of the transmit input amplifier.
16	VF_XI+	Non-inverting input of the transmit input amplifier.

Functional Description

Power-Up

When power is first applied, the Power-On reset circuitry initializes the CODEC and places it in a Power-Down mode. When the CODEC returns to an active state from the Power-Down mode, the receive output is muted briefly to minimize turn-on "click".

To power up the device, there are two methods available.

1. A logical zero at $MCLK_R$/PDN will power up the device, provided FS_X or FS_R pulses are present.
2. Alternatively, a clock ($MCLK_R$) must be applied to $MCLK_R$/PDN and FS_X or FS_R pulses must be present.

Power-Down

Two power-down modes are available.

1. A logical 1 at $MCLK_R$/PDN, after approximately 0.5ms, will power down the device.
2. Alternatively, hold both FS_X and FS_R continuously low, the device will power down approximately 0.5ms after the last FS_X or FS_R pulse.

Synchronous Operation (Transmit and Receive Sections use the Same Master Clock)

The same master clock and bit-clock should be used for the receive and transmit sections. $MCLK_X$ (pin 9) is used to provide the master clock for the transmit section; the receive section will use the same master clock if the $MCLK_R$/PDN (pin 8) is grounded (synchronous operation), or at V+ (power-down mode). $MCLK_R$/PDN may be clocked only if a clock is provided at $BCLK_R$/CLKSEL (pin 7) as in asynchronous operation.

The $BCLK_X$ (pin 10) is used to provide the bit clock to the transmit section. In synchronous operation, this bit clock is also used for the receive section if $MCLK_R$/PDN (pin 8) is grounded. $BCLK_R$/CLKSEL (pin 7) is then used to select the proper internal frequency division for 1.544MHz, 1.536MHz or 2.048MHz operation (see Table below). For 1.544MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the leading edge of $BCLK_X$. After 8 bit-clock periods, the tristate D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of the $BCLK_X$. FS_X and FS_R must be synchronous with $MCLK_X$.

CLOCKING OPTIONS

MODE	$BCLK_R$/CLKSEL (PIN 7)	MASTER CLOCK FREQUENCY SELECTED	
		CD22354A (μ)	CD22357A (A)
Asynchronous or Synchronous	Clocked	1.536MHz or 1.544MHz	2.048MHz
Synchronous	0	2.048MHz	1.536MHz or 1.544MHz
Synchronous	1(or open circuit)	1.536MHz or 1.544MHz	2.048MHz

Asynchronous Operation (Transmit and Receive Sections use Separate Master Clocks)

For the CD22357A, the $MCLK_X$ and $MCLK_R$ must be 2.048MHz and for the CD22354A must be 1.536MHz or 1.544MHz. These clocks need not be synchronous. However, for best transmission performance, it is recommended that $MCLK_X$ and $MCLK_R$ be synchronous.

For 1.544MHz operation the device automatically compensates for the 193rd clock pulse each frame. FS_X starts the encoding operation and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts the decoding operation and must be synchronous with $BCLK_R$. $BCLK_R$ must be clocked in asynchronous operation. $BCLK_X$ and $BCLK_R$ may be between 64kHz - 2.04MHz.

Short-Frame Sync Mode

When the power is first applied, the power initialization circuitry places the CODEC in a short-frame sync mode. In this mode both frame sync pulses must be 1 bit-clock period long, with the timing relationship shown in Figure 1.

With FS_X high during the falling edge of the $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X tristate output buffer, which will output the sign bit. The following rising seven edges clock out the remaining seven bits upon which the next falling edge will disable the D_X output.

With FS_R high during the falling edge of the $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven edges latch in the seven remaining bits.

Long-Frame Sync Mode

In this mode of operation, both of the frame sync pulses must be three or more bit-clock periods long with the timing relationship shown in Figure 2.

Based on the transmit frame sync FS_X, the CODEC will sense whether short or long-frame sync pulses are being used.

For 64kHz operation the frame sync pulse must be kept low for a minimum of 160ns.

The D_X tristate output buffer is enabled with the rising edge of FS_X or the rising edge of the $BCLK_X$, whichever comes later and the first bit clocked out is the sign bit. The following seven rising edges of the $BCLK_X$ clock out the remaining seven bits. The D_X output is disabled by the next falling edge of the $BCLK_X$ following the 8th rising edge or by FS_X going low whichever comes later.

A rising edge on the receive frame sync, FS_R, will cause the PCM data at D_R to be latched in on the next falling edge of the $BCLK_R$. The remaining seven bits are latched on the successive seven falling edges of the bit-clock ($BCLK_X$ in synchronous mode).

Transmit Section

The transmit section consists of a gain-adjustable input op-amp, an anti-aliasing filter, a low-pass filter, a high-pass filter and a compressing A/D converter. The input op-amp drives a

RC active anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides 30-dB attenuation (minimum) at the sampling frequency. From this filter the signal enters a 5th order low-pass filter clocked at 128kHz, followed by a 3rd order high-pass filter clock at 32kHz. The output of the high-pass filter directly drives the encoder capacitor ladder at an 8kHz sampling rate. A precision voltage reference is trimmed in manufacturing to provide an input overload of nominally 2.5 V_{PEAK}. Transmit frame sync pulse FS_X controls the process. The 8-bit PCM data is clocked out at D_X by the $BCLK_X$. $BCLK_X$ can be varied from 64kHz to 2.048MHz.

Receive Section

The receive section consists of an expanding D/A converter and a low-pass filter which fulfills both the AT&T D3/D4 specifications and CCITT recommendations. PCM data enters the receive section at D_R upon the occurrence of FS_R, Receive Frame sync pulse. $BCLK_R$, Receive Data Clock, which can range from 64kHz to 2.048MHz, clocks the 8-bit PCM data into the receive data register. A D/A conversion is performed on the 8-bit PCM data and the corresponding analog signal is held on the D/A capacitor ladder. This signal is transferred to a switched capacitor low-pass filter clocked at 128kHz to smooth the sample-and-hold signal as well as to compensate for the (SIN X)/X distortion.

The filter is then followed by a second order Sallen and Key active filter capable of driving a 600Ω load to a level of 7.2dBm.

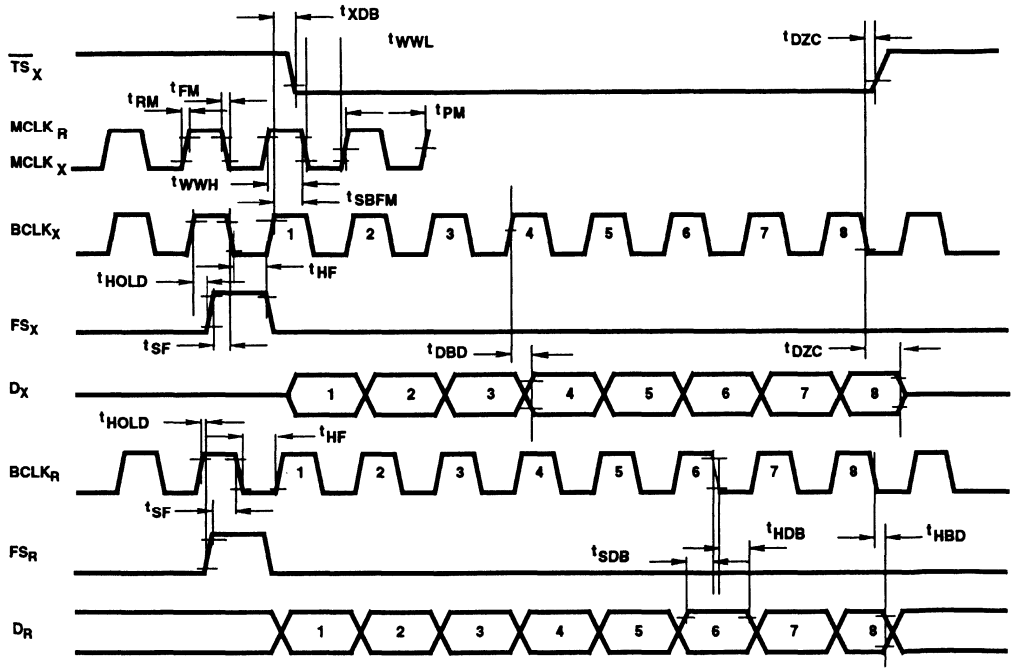


FIGURE 1. SHORT FRAME-SYNC TIMING

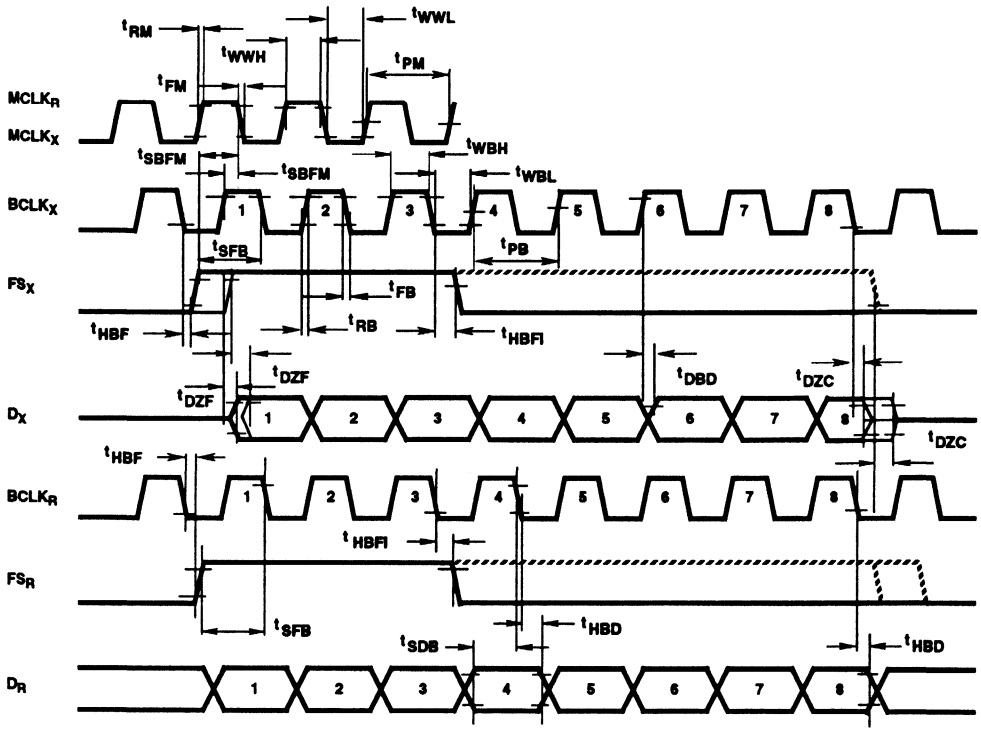


FIGURE 2. LONG FRAME-SYNC TIMING

HARRIS SEMICONDUCTOR

CD22M3493

12 x 8 x 1 BiMOS-E Crosspoint Switch

March 1993

Features

- 96 Analog Switches
- Low R_{ON}
- Guaranteed R_{ON} Matching
- Analog Signal Input Voltage Equal To The Supply Voltage
- Wide Operating Voltage: 4V To 16V
- Parallel Input Addressing
- High Latch Up Current: 50mA Minimum
- Very Low Crosstalk
- Pin And Functionally Compatible With The Following Types: SGS M3493, SGS M093, SSI 78A093A, and Mitel MT8812

Applications

- PBX Systems
- Instrumentation
- Analog And Digital Multiplexers
- Video Switching Networks

Description

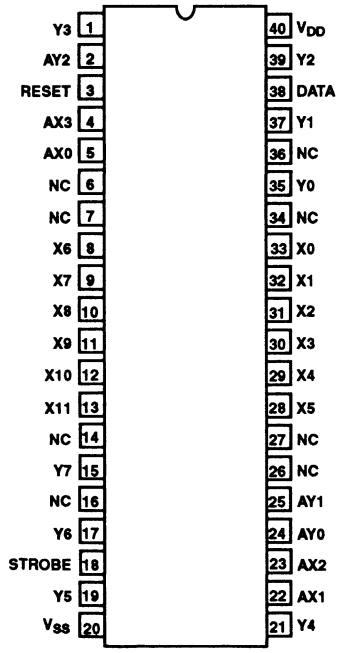
The Harris CD22M3493 is an array of 96 analog switches capable of handling signals from DC to video. Because of the switch structure, input signals may swing through the total supply voltage range, V_{DD} to V_{SS}. Each of the 96 switches may be addressed via the ADDRESS input to the 7 to 96 line decoder. The state of the addressed switch is established by the signal to the DATA input. A low or logic zero input will open the switch, while a high logic level or a one will result in closure of the addressed switch when the STROBE input goes high from its normally low state. Any number or combination of connections may be active at one time. Each connection, however, must be made or broken individually in the manner previously described. All switches may be reset by taking the RESET input from a zero state to a one state and then returning it to its normal low state.

Ordering Information

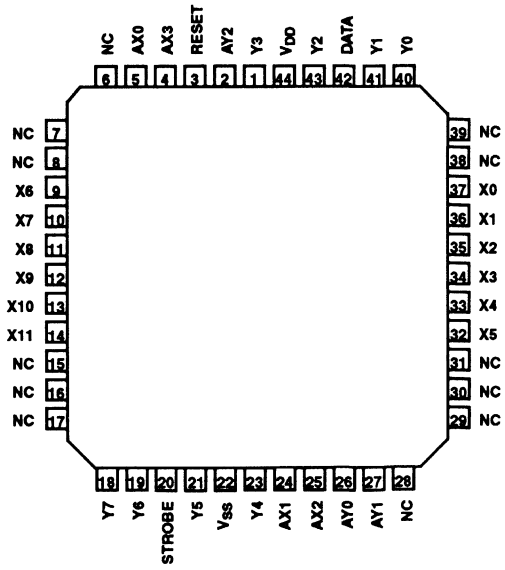
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CD22M3493E	-40°C to +85°C	40 Lead Plastic DIP
CD22M3493Q	-40°C to +85°C	44 Lead PLCC

Pinouts

CD22M3493 (PDIP)
TOP VIEW



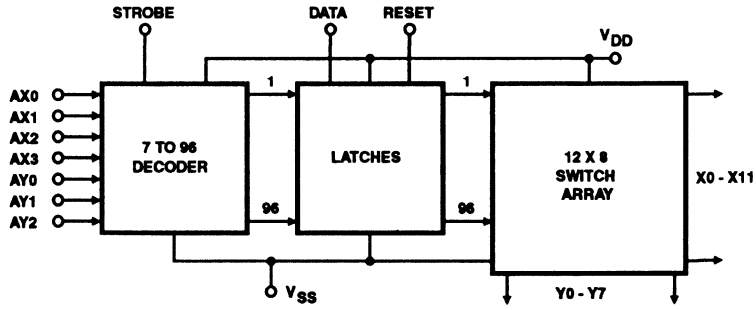
CD22M3493 (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2491.2**

Block Diagram



Pin Descriptions

SYMBOL	40 LEAD PLASTIC DIP	44 LEAD PLCC	DESCRIPTION
POWER SUPPLIES			
V_{DD}	40	44	Positive Supply
V_{SS}	20	22	Negative Supply
ADDRESS			
AX0 - AX3	5, 22, 23, & 4	5, 24, 25, & 4	X Address Lines. These pins select one of the 12 rows of switches. See the Truth Table for the valid addresses.
AY0 - AY2	24, 25, & 2	26, 27,& 2	Y Address Lines. These pins select one of the 8 columns of switches. See the Truth Table for the valid addresses.
CONTROL			
DATA	38	42	DATA Input determines the state of the addressed switch. A high or one will close the switch. A low or zero will open the switch.
STROBE	18	20	STROBE Input enables the action defined by the DATA and ADDRESS Inputs. A low or zero results in no action. The ADDRESS Input must be stable before the STROBE Input goes to the active high level. The DATA Input must be stable on the failing edge of the STROBE.
RESET	3	3	MASTER RESET. A high or one on this line opens all switches.
INPUTS/OUTPUTS			
X0 - X5 I/O X6 - X11	33 - 28 8 - 13	37 - 32 9 - 14	Analog or Digital Inputs/Outputs. These pins are the rows X0 - X11.
Y0 - Y7 I/O	35, 37, 39, 1, 21, 19, 17 & 15	40, 41, 43, 1, 23, 21, 19 & 18	Analog or Digital Inputs/Outputs. These pins are the columns Y0 - Y7.

Absolute Maximum Ratings

DC Supply Voltage (V_{DD}):
(Voltages Referenced to V_{SS}) ..... -0.5 to +17V
DC Input Diode Current, I_{IN} ..... ±20mA
(For $V_I < V_{SS}$ -0.5V or $V_I > V_{DD}$ +0.5V)
DC Output Diode Current, I_{OK} ..... ±20mA
(For $V_O < V_{SS}$ -0.5V or $V_O > V_{DD}$ +0.5V)
DC Transmission Gate Current ..... ±25mA
Power Dissipation Per Package (Po):
For T_A = -40°C to +85°C 500mW
(Package Type E, 40 Pin Plastic DIP)
For T_A = -40°C to +85°C 600mW
(Package Type Q, 44 Pin PLCC)

Operating Temperature Range (T_A):
Package Type E and Q ..... -40°C to +85°C
Storage Temperature Range (T_{STG}) ..... -65°C to +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Recommended Operating Conditions

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

PARAMETERS	LIMITS MIN	LIMITS MAX	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range) V_{SS} = 0V V_{DD}	4	16	V
DC Input or Output Voltage V_I or V_O Digital Input Voltage	V_{SS} V_{SS}	V_{DD} V_{DD}	V V

Dynamic Electrical Specifications (T_A = -40°C to +85°C) V_{SS} = 0V, V_{DD} = 14V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONTROLS CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{DD}	V_{DD} = 5V Logic Inputs = V_{DD}	-	-	2	mA
		V_{DD} = 16V Logic Inputs = V_{DD}	-	-	5	mA
High-Level Input Voltage	V_{IH}		2.4	-	-	V
Low-Level Input Voltage	V_{IL}		-	-	0.8	V
Input Leakage Current, Digital	I_{IN}	Reset = Low (Note 1)	-	-	±10 (Note 2)	µA

PARAMETERS	SYMBOL	CROSSPOINTS CONDITIONS	MIN	TYP	MAX	UNITS
ON Resistance	R_{ON}	T_A = +25°C, V_{DD} = 5V $V_{IN} = V_{DD}/2$ VX - VY = 0.25V V_{DD} = 14V	-	40	70	Ω
			-	22	45	Ω
ON Resistance	R_{ON}	T_A = -40°C to +85°C V_{DD} = 5V $V_{IN} = V_{DD}/2$ VX - VY = 0.25V V_{DD} = 14V	-	-	80	Ω
			-	-	55	Ω
Difference in ON Resistance between any two switches	ΔR_{ON}	T_A = +25°C $V_{IN} = V_{DD}/2$ VX - VY = 0.25V V_{DD} = 14V	-	4	10	Ω
Difference in ON Resistance between any two switches	ΔR_{ON}	T_A = -40°C to +85°C $V_{IN} = V_{DD}/2$ VX - VY = 0.25V V_{DD} = 14V	-	-	10	Ω
OFF-State Leakage Current	I_L	|VX - VY| = 14V	-	-	±10 (Note 2)	µA

NOTES:
1. Reset I_{IH} < 2mA, Reset = V_{DD} = 16V
2. At +25°C Limit is ±100nA

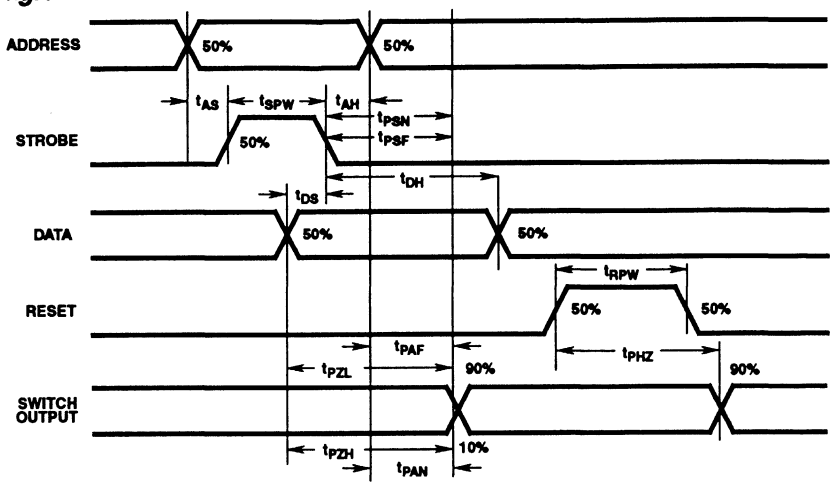
Dynamic Electrical Specifications (T_A = +25°C), V_{SS} = 0V, V_{DD} = 14V, C_L = 50pF, Unless Otherwise Specified

PARAMETERS	CROSSPOINTS CONDITIONS	MIN	TYP	MAX	UNITS
Switch I/O Capacitance	V_{IN} = 7V, f = 1MHz	-	20	-	pF
Switch Feedthrough Capacitance	V_{IN} = 7V, f = 1MHz	-	0.2	-	pF
Propagation Delay Time (switch ON) Signal Input to Output, t_{PHL} or t_{PLH}		-	30	100	ns
Frequency Response Channel ON f = 20log (VX/VY) = -3dB	C_L = 3pF, R_L = 75Ω, V_{IN} = $2V_{P-P}$	-	50	-	MHz
Total Harmonic, T_{HD}	V_{IN} = $2V_{P-P}$, f = 1kHz	-	0.01	-	%
Feedthrough Channel OFF Feedthrough = 20log (VX/VY) = F_{DT}	V_{IN} = $2V_{P-P}$, f = 1kHz	-	-95	-	dB
Frequency for Signal Crosstalk, f_{CT}	40dB, V_{IN} = $2V_{P-P}$, R_L = 75Ω	-	10	-	MHz
Attenuation of:	110dB, V_{IN} = $2V_{P-P}$, R_L = 1kΩ ‖ 10pF	-	5	-	kHz
Control Crosstalk DATA-Input, ADDRESS, or STROBE to Output	Control Input = $3V_{P-P}$ Square Wave, t_R = t_F = 10ns R_{IN} = 1K, R_{OUT} = 10kΩ ‖ 10pF	-	75	-	mVPK

Dynamic Electrical Specifications (T_A = +25°C), V_{SS} = 0V, V_{DD} = 14V, R_L = 1kΩ ‖ 50pF, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONTROLS CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input Capacitance	C_{IN}	V_{IN} = 5V, f = 1MHz	-	5	-	pF
Propagation Delay Time STROBE to Output						
(Switch turn-ON)	t_{PSN}		-	30	100	ns
(Switch turn-OFF)	t_{PSF}		-	40	100	ns
DATA-in to Output						
(Turn-ON to high level)	t_{PZH}		-	30	100	ns
(Turn-ON to low level)	t_{PZL}		-	30	100	ns
ADDRESS to Output						
(Turn-ON to high level)	t_{PAN}		-	30	100	ns
(Turn-OFF to low level)	t_{PAF}		-	25	100	ns
Set-up Time						
DATA-in to STROBE	t_{DS}		20	-	-	ns
ADDRESS to STROBE	t_{AS}		20	-	-	ns
Hold Time						
STROBE to DATA-in	t_{DH}		20	-	-	ns
STROBE to ADDRESS	t_{AH}		10	-	-	ns
Pulse Width						
STROBE	t_{SPW}		30	-	-	ns
RESET	t_{RPW}		50	-	-	ns
RESET Turn OFF to Output Delay	t_{PHZ}		-	100	200	ns

Timing Diagram



TRUTH TABLE X AXIS

X ADDRESS					
AX3	AX2	AX1	AX0	NOTE	X SWITCH
0	0	0	0		X0
0	0	0	1		X1
0	0	1	0		X2
0	0	1	1		X3
0	1	0	0		X4
0	1	0	1		X5
0	1	1	0	1	No Connect
0	1	1	1	1	No Connect
1	0	0	0		X6
1	0	0	1		X7
1	0	1	0		X8
1	0	1	1		X9
1	1	0	0		X10
1	1	0	1		X11
1	1	1	0	1	No Connect
1	1	1	1	1	No Connect

NOTE: 1. When X switch addresses are in these states, no change in status will occur in switches between any X and Y points.

TRUTH TABLE Y AXIS

Y ADDRESS			
AY2	AY1	AY0	Y SWITCH
0	0	0	Y0
0	0	1	Y1
0	1	0	Y2
0	1	1	Y3
1	0	0	Y4
1	0	1	Y5
1	1	0	Y6
1	1	1	Y7

To make a connection (close switch) between any two points, specify an "X" address, a "Y" address, set "Data" high, and switch "Strobe" from low to high. To break a connection, follow this same procedure with "Data" low.:

Example:

	DATA	X ADDRESS				Y ADDRESS		
		AX3	AX2	AX1	AX0	AY2	AY1	AY0
To connect switch X3 to switch Y4:	1	0	0	1	1	1	0	0
To connect switch X6 to switch Y7:	1	1	0	0	0	1	1	1
To break connection from X3 to Y4:	0	0	0	1	1	1	0	0

HARRIS SEMICONDUCTOR

CD22M3494

16 x 8 x 1 BiMOS-E Crosspoint Switch

March 1993

Features

- 128 Analog Switches
- Low R_{ON}
- Guaranteed R_{ON} Matching
- Analog Signal Input Voltage Equal to the Supply Voltage
- Wide Operating Voltage: 4V to 15V
- Parallel Input Addressing
- High Latch Up Current: 50mA Minimum
- Very Low Crosstalk
- Pin And Functionally Compatible with the Following Types: SGS M3494 and Mitel MT8816

Applications

- PBX Systems
- Instrumentation
- Analog And Digital Multiplexers
- Video Switching Networks

Description

The Harris CD22M3494 is an array of 128 analog switches capable of handling signals from DC to video. Because of the switch structure, input signals may swing through the total supply voltage range, V_{DD} to V_{EE}. Each of the 128 switches may be addressed via the ADDRESS input to the 7 to 128 line decoder. The state of the addressed switch is established by the signal to the DATA input. A low or zero input will open the switch, while a high logic level or a one will result in closure of the addressed switch when the STROBE input goes high from its normally low state. Any number or combination of connections may be active at one time. Each connection, however, must be made or broken individually in the manner previously described. All switches may be reset by taking the RESET input from a zero state to a one state and then returning it to its normal low state.

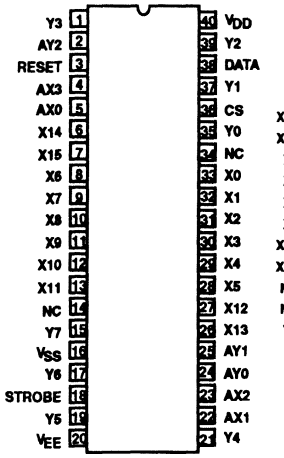
CS allows crosspoint array to be cascaded for matrix expansion.

Ordering Information

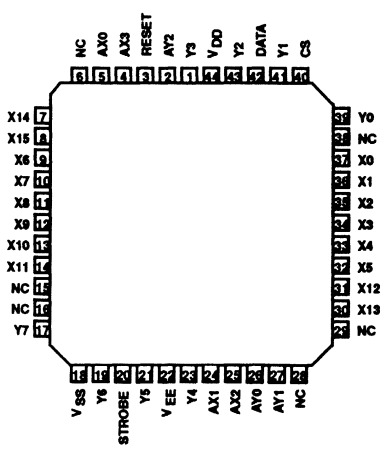
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CD22M3494E	-40°C to +85°C	40 Lead Plastic DIP
CD22M3494MQ	-40°C to +85°C	44 Lead PLCC (Mitel Lead Compatible)
CD22M3494SQ	-40°C to +85°C	44 Lead PLCC (SGS Lead Compatible)

Pinouts

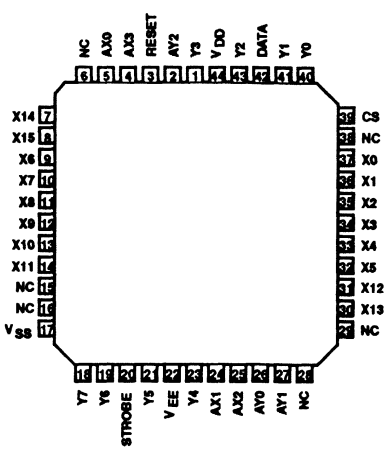
CD22M3494E (PDIP) TOP VIEW



CD22M3494MQ (PLCC) (MITEL LEAD COMPATIBLE) TOP VIEW



CD22M3494SQ (PLCC) (SGS LEAD COMPATIBLE) TOP VIEW

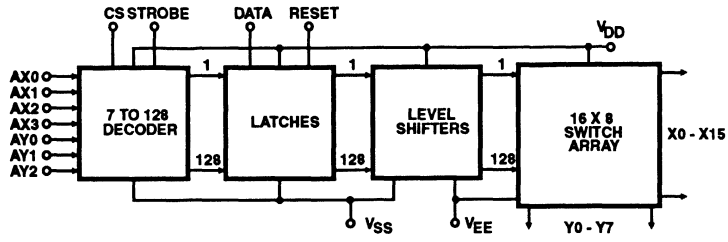


8 TELECOM

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2793.2**

Block Diagram



Pin Descriptions

SYMBOL	40 LEAD PLASTIC DIP	44 LEAD PLCC MQ	44 LEAD PLCC SQ	DESCRIPTION
POWER SUPPLIES				
V_{DD}	40	44	44	Positive Supply
V_{SS}	16	18	17	Negative Supply (Digital)
V_{EE}	20	22	22	Negative Supply (Analog)
ADDRESS				
AX0 - AX3	5, 22, 23, & 4	5, 24, 25, & 4		X Address Lines. These pins select one of the 16 rows of switches. See the Truth Table for the valid addresses.
AY0 - AY2	24, 25, & 2	26, 27,& 2		Y Address Lines. These pins select one of the 8 columns of switches. See the Truth Table for the valid addresses.
CONTROL				
DATA	38	42		DATA Input determines the state of the addressed switch. A high or one will close the switch. A low or zero will open the switch.
STROBE	18	20		STROBE Input enables the action defined by the DATA and ADDRESS Inputs. A low or zero results in no action. The ADDRESS Input must be stable before the STROBE Input goes to the active high level. The DATA Input must be stable on the failing edge of the STROBE.
RESET	3	3		MASTER RESET. A high or one on this line opens all switches.
CS	36	40	39	CHIP SELECT. Device is selected when CS is at a high level, allows the crosspoint array to be cascaded for matrix expanion.
INPUTS/OUTPUTS				
X0 - X5 X6 - X11 X12 - X15	33 - 28 8 - 13 27, 26, 6, 7	37 - 32 9 - 14 31, 30, 7, 8		Analog or Digital Inputs/Outputs. These pins are the rows X0 - X15.
Y0 - Y7 I/O	35, 37, 39, 1, 21, 19, 17 & 15	40, 41, 43, 1, 23, 21, 19 & 18		Analog or Digital Inputs/Outputs. These pins are the columns Y0 - Y7.

Absolute Maximum Ratings

DC Supply Voltage (V_{DD}):
(Voltages Referenced to V_{EE}) ..... -0.5 to +16V
DC Supply Voltage (V_{DD}):
(Voltages Referenced to V_{SS}) ..... -0.5, +16V
DC Input Diode Current, I_{IN} ..... ±20mA
(For V_I, Digital < V_{SS} -0.5V or V_I, Analog < V_{EE} -0.5V or V_I > V_{DD} +0.5V)
DC Output Diode Current, I_{OK} ..... ±20mA
(For V_O, Digital < V_{SS} -0.5V or V_O, Analog < V_{EE} -0.5V
or V_O > V_{DD} +0.5V)
DC Transmission Gate Current ..... ±25mA
Power Dissipation Per Package (Po):
For T_A = -40°C to +85°C 500mW
(Package Type E, 40 Pin Plastic DIP)
For T_A = +60°C to +85°C Derate Lineary ..... 12mW/°C to 200mW
For T_A = -40°C to +85°C 600mW
(Package Type Q, 44 Lead PLCC)
Operating Temperature Range (T_A):
Package Type E and Q ..... -40°C to +85°C
Storage Temperature Range (T_{STG}) ..... -65°C to +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Recommended Operating Conditions

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

PARAMETERS	LIMITS		UNITS
	MIN	MAX	
Supply Voltage Range (For T_A = Full Package Temperature Range) V_{SS} = 0V, V_{EE} = 0V, V_{DD}	4	15	V
DC Input or Output Voltage V_I or V_O Digital Input Voltage	V_{EE} V_{SS}	V_{DD} V_{DD}	V V

Static Electrical Specifications (T_A = -40°C to +85°C) V_{DD} = 5V, V_{SS} = 0V, V_{EE} = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONTROLS CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{DD}	V_{DD} = 5V Logic Inputs = V_{DD}	-	-	2	mA
		V_{DD} = 15V Logic Inputs = V_{DD}	-	-	5	mA
High-Level Input Voltage	V_{IH}		2.4	-	-	V
Low-Level Input Voltage	V_{IL}		-	-	0.8	V
Input Leakage Current, Digital	I_{IN}	Reset = Low (Note 1)	-	-	±10 (Note 2)	µA

Static Electrical Specifications (T_A = -40°C to +85°C) V_{DD} = 12V, V_{SS} = 0V, V_{EE} = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CROSSPOINTS CONDITIONS	MIN	TYP	MAX	UNITS
ON Resistance	R_{ON}	V_{SS} = V_{EE} = 0V V_{DD} = 10V	-	40	75	Ω
		T_A = +25°C, V_{IN} = V_{DD}/2 VX - VY = 0.2V V_{DD} = 12V	-	36	65	Ω
ON Resistance	R_{ON}	T_A = -40°C to +85°C V_{DD} = 10V V_{IN} = V_{DD}/2	-	50	75	Ω
		VX - VY = 0.2V V_{DD} = 12V V_{SS} = V_{EE} = 0V	-	45	65	Ω
Difference in ON Resistance between any two switches	ΔR_{ON}	T_A = +25°C V_{IN} = V_{DD}/2 VX - VY = 0.2V V_{DD} = 12V V_{SS} = V_{EE} = 0V	-	6	10	Ω

8 TELECOM

Static Electrical Specifications (T_A = -40°C to +85°C) V_{DD} = 12V, V_{SS} = 0V, V_{EE} = 0V, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	CROSSPOINTS CONDITIONS	MIN	TYP	MAX	UNITS
Difference in ON Resistance between any two switches	ΔR_{ON}	T_A = -40°C to +85°C $V_{IN} = V_{DD}/2$ VX - VY = 0.2V V_{DD} = 12V $V_{SS} = V_{EE}$ = 0V	-	-	10	Ω
OFF-State Leakage Current	I_L	IVX - VYI = 12V	-	-	±10 (Note 2)	µA

NOTE:

1. Reset I_{IH} < 20µA, Reset = V_{IH}
2. At +25°C Limit is ±100nA

Dynamic Electrical Specifications (T_A = +25°C), V_{SS} = 0V, V_{EE} = 0V, V_{DD} = 14V, C_L = 50pF, Unless Otherwise Specified

PARAMETERS	CROSSPOINTS CONDITIONS	MIN	TYP	MAX	UNITS
Switch I/O Capacitance	$V_{IN} = V_{DD}/2$, f = 1MHz	-	-	20	pF
Switch Feedthrough Capacitance	$V_{IN} = V_{DD}/2$, f = 1MHz	-	0.3	-	pF
Propagation Delay Time (switch ON) Signal Input to Output, t_{PHL} or t_{PLH}		-	30	100	ns
Frequency Response Channel ON f = 20log (VX/VY) = -3dB	C_L = 3pF, R_L = 75Ω, $V_{IN} = 2V_{P-P}$	-	50	-	MHz
Total Harmonic, T_{HD}	$V_{IN} = 2V_{P-P}$, f = 1kHz	-	0.01	-	%
Feedthrough Channel OFF Feedthrough = 20log (VX/VY) = F_{DT}	$V_{IN} = 2V_{P-P}$, f = 1kHz	-	-95	-	dB
Frequency for Signal Crosstalk, f_{CT}	40dB, $V_{IN} = 2V_{P-P}$, R_L = 75Ω	-	10	-	MHz
Attenuation of:	110dB, $V_{IN} = 2V_{P-P}$, R_L = 1kΩ II 10pF	-	5	-	kHz
Control Crosstalk DATA-Input, ADDRESS, or STROBE to Output	Control Input = 3VP-P Square Wave, $t_R = t_F$ = 10ns R_{IN} = 1K, R_{OUT} = 10kΩ II 10pF	-	75	-	mV_{PK}

Dynamic Electrical Specifications

(T_A = +25°C), V_{SS} = 0V, V_{EE} = 0V, V_{DD} = 14V, R_L = 1kΩ II 50pF, Unless Otherwise Specified

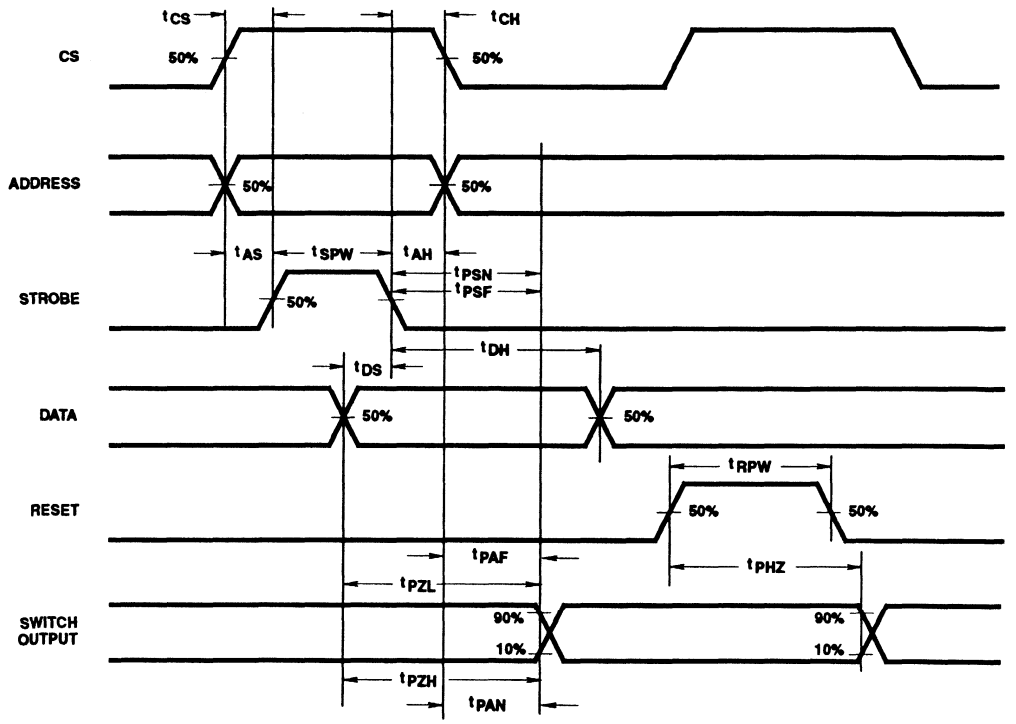
PARAMETERS	SYMBOL	CONTROLS CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input Capacitance	C_{IN}	V_{IN} = 5V, f = 1MHz	-	5	-	pF
Propagation Delay Time STROBE to Output						
(Switch turn-ON)	t_{PSN}		-	50	100	ns
(Switch turn-OFF)	t_{PSF}		-	50	100	ns
DATA-in to Output						
(Turn-ON to high level)	t_{PZH}		-	60	100	ns
(Turn-ON to low level)	t_{PZL}		-	70	100	ns
ADDRESS to Output						
(Turn-ON to high level)	t_{PAN}		-	70	-	ns
(Turn-OFF to low level)	t_{PAF}		-	70	-	ns

Dynamic Electrical Specifications

(T_A = +25°C), V_{SS} = 0V, V_{EE} = 0V, V_{DD} = 14V, R_L = 1kΩ || 50pF, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	CONTROLS CONDITIONS	MIN	TYP	MAX	UNITS
Set-up Time						
CS to STROBE	t_{CS}		10	-	-	ns
DATA-In to STROBE	t_{DS}		10	-	-	ns
ADDRESS to STROBE	t_{AS}		10	-	-	ns
Hold Time						
STROBE to CS	t_{CH}		10	-	-	
ADDRESS to CS			10	-	-	
STROBE to DATA-in	t_{DH}		20	-	-	ns
STROBE to ADDRESS	t_{AH}		10	-	-	ns
DATA-In to CS				20	-	-
Pulse Width						
STROBE	t_{SPW}		20	-	-	ns
RESET	t_{RPW}		20	-	-	ns
RESET Turn OFF to Output Delay	t_{PHZ}		-	70	100	ns

Timing Diagram



TRUTH TABLE X AXIS

X ADDRESS				
AX3	AX2	AX1	AX0	X SWITCH
0	0	0	0	X0
0	0	0	1	X1
0	0	1	0	X2
0	0	1	1	X3
0	1	0	0	X4
0	1	0	1	X5
0	1	1	0	X12
0	1	1	1	X13
1	0	0	0	X6
1	0	0	1	X7
1	0	1	0	X8
1	0	1	1	X9
1	1	0	0	X10
1	1	0	1	X11
1	1	1	0	X14
1	1	1	1	X15

TRUTH TABLE Y AXIS

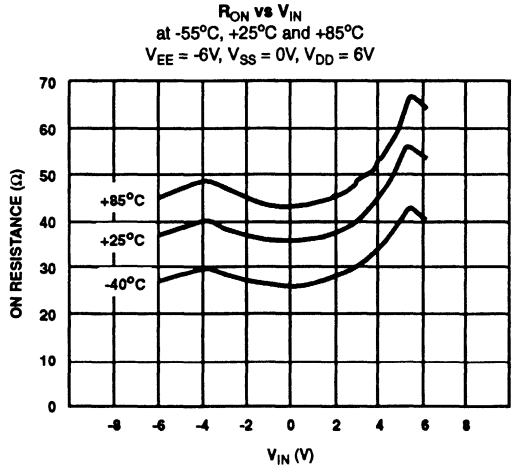
Y ADDRESS			
AY2	AY1	AY0	Y SWITCH
0	0	0	Y0
0	0	1	Y1
0	1	0	Y2
0	1	1	Y3
1	0	0	Y4
1	0	1	Y5
1	1	0	Y6
1	1	1	Y7

To make a connection (close switch) between any two points, specify an "X" address, a "Y" address, set "Data" high, and switch "Strobe" from low to high. To break a connection, follow this same procedure with "Data" low.

Example:

	DATA	X ADDRESS AX3	AX2	AX1	AX0	Y ADDRESS AY2	AY1	AY0
To connect switch X3 to switch Y4:	1	0	0	1	1	1	0	0
To connect switch X6 to switch Y7:	1	1	0	0	0	1	1	1
To break connection from X3 to Y4:	0	0	0	1	1	1	0	0

Voltage and Resistance



HARRIS SEMICONDUCTOR

CD22859

Monolithic Silicon COS/MOS Dual-Tone Multifrequency Tone Generator

March 1993

Features

- **Mute Drivers On-Chip**
- **Device Power can Either be Regulated DC or Telephone Loop Current**
- **Use of an Inexpensive 3.579545MHz TV Crystal Provides High Accuracy and Stability for all Frequencies**

Applications

- **For Use in Dual-tone Telephone Dialing Systems**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CD22859E	-40°C to +85°C	16 Pin Plastic DIP

Description

The CD22859 is a CMOS dual-tone multifrequency (DTMF) tone generator for use in dual-tone telephone dialing systems. The device can easily be interfaced to a standard push-button telephone keyboard to provide enabling operation directly with the telephone lines.

The CD22859 generates standard DTMF sinusoidal dialing tones from an on-chip reference crystal oscillator. The reference oscillator uses an inexpensive 3.579545MHz color TV crystal to create highly stable and accurate tones. The sinusoidal tones are digitally synthesized by a stair-step approximation.

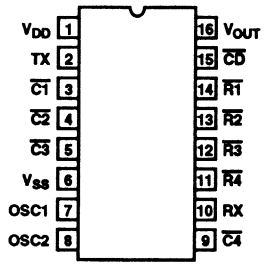
One of four low-frequency band row tones and one of four high-frequency band column tones are selected by driving one of the four row inputs and one of the four column inputs low. Simultaneous selection of more than one row input and/or more than one column input will inhibit tone generation, or generate a single-tone sinusoid. These operating modes are described in the functional truth table.

Control logic is included to allow easy interface to standard K500-type telephones. Two CMOS outputs (T_X, R_X) capable of driving external pnp receiver and transmitter muting transistors are provided. A low input to the $\overline{CD}$ pin inhibits tone generation, turns off the reference oscillator and causes T_X and R_X outputs to go to logic '0'. During tone generation mode, $\overline{CD}$ = 1 and T_X, R_X = logic 1.

The row, column and $\overline{CD}$ inputs are provided with pull-up resistors to allow the use of SPST switch matrixes.

Pinout

CD22859
PDIP
TOP VIEW



8 TELECOM

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1257.2**

Absolute Maximum Ratings

Supply Voltage (V_{DD} - V_{SS}) ..... -0.5 to +12V
Input Voltage ..... -0.5V to V_{DD} +0.5V
Power Dissipation, P_D
T_A = -40°C to +60°C 500mW
T_A = +60°C to +85°C .... Derate Linearly at 1.2mW/°C to 200mW
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Power Dissipation Per Output 100mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Dynamic Electrical Specifications

T_A = -25°C to +60°C, All Voltages Referenced to V_{SS} = 0V

PARAMETER	V_{DD} (V)	LIMITS MIN	LIMITS MAX	UNITS
DC SUPPLY VOLTAGE				
Tone Generation Mode with Valid Input (Note 1)		2.5	10	V
Non-Tone Generation (Note 2)		1.7	10	V
OPERATING CURRENT				
Tone Generation Mode (Outputs Unloaded)	3.7	-	2.7	mA
	9.3	-	13	mA
No Keydown Mode	3.7	-	100	µA
	9.3	-	200	µA
Input Pull-Up Current	3 - 10	-	400	µA
Input Low Voltage (V_{IL}) Maximum	3 - 10	-	0.2 V_{DD}	V
Input Low Voltage (V_{IH}) Minimum	3 - 10	-	0.8 V_{DD}	V

Static Electrical Specifications

T_A = -25°C to +60°C

PARAMETER	V_{DD} (V)	V_O (V)	LIMITS MIN	LIMITS MAX	UNITS
TONE OUTPUTS (R_L = 82Ω)					
V_O; Dual-Tone Output	3.7 - 9.3	-	350	700	mV_{RMS}
V_O (C_L); Single-Tone Output, Column (Note 3)	3.7 - 9.3	-	300	-	mV_{RMS}
V_O (R_L); Single-Tone Output, Row (Note 4)	3.7 - 9.3	-	260	-	mV_{RMS}
Distortion (Note 5)	3.9 - 9.3	-	-	10	%
Rise and Fall Time (Dual-Tone Out) (Note 6)	3.9 - 9.3	-	-	5	ms
Pre-Emphasis (Note 7)	3.9 - 9.3	-	1	3	dB
Output Frequency (Note 8)	3.9 - 9.3	-	(Nom. -1%)	(Nom. +1%)	Hz

Static Electrical Specifications T_A = -25°C to +60°C **(Continued)**

PARAMETER	V_{DD} (V)	V_O (V)	LIMITS MIN	LIMITS MAX	UNITS
MUTE OUTPUT CURRENT					
Transmitter	1.7	1.2	-0.5	-	mA
I_{OH} (Source)	10	9.5	-3.4	-	mA
I_{OL} (Sink)	10	2.5	-	10	µA
Receiver	1.7	1.2	-0.5	-	mA
I_{OH} (Source)	10	9.5	-3.4	-	mA
I_{OL} (Sink)	10	2.5	-	10	µA

NOTES:

1. All logic and counters functional.
2. Mute switches remain open.
3. Two or more row inputs low and one column input low.
4. Two or more column inputs low and one row input low.
5. Distortion is defined as: The ratio of all extraneous frequency components generated in the voiceband 0.5kHz to 3kHz, to the power of the dual-tone signal, measure across R_L.

$$\text{Distortion} = \frac{\sqrt{(V_1{}^2 + V_2{}^2 + \ldots + V_n{}^2)}}{\sqrt{V_L{}^2 + V_H{}^2}}$$

   where V_1, V_2 . . . . V_n are extraneous frequency components in the voiceband 0.5kHz to 3kHz, V_L is the low-band frequency tone, and V_H is the high-band frequency tone.
6. Tone rise time is defined as the time for each of the 2 DTMF frequencies to attain 90% of full amplitude, measured from the time when a row and column signal are driven low.
7. Pre-emphasis is the ratio of the high-group level to the low-group level.
8. Refer to Figure 1 for standard DTMF frequencies.
9. Corresponds to normal dual-tone operation.
10. Corresponds to single-tone generation mode.

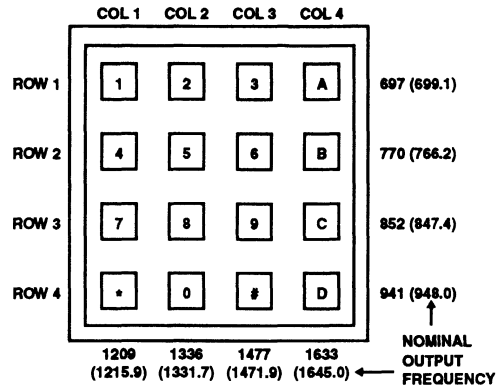


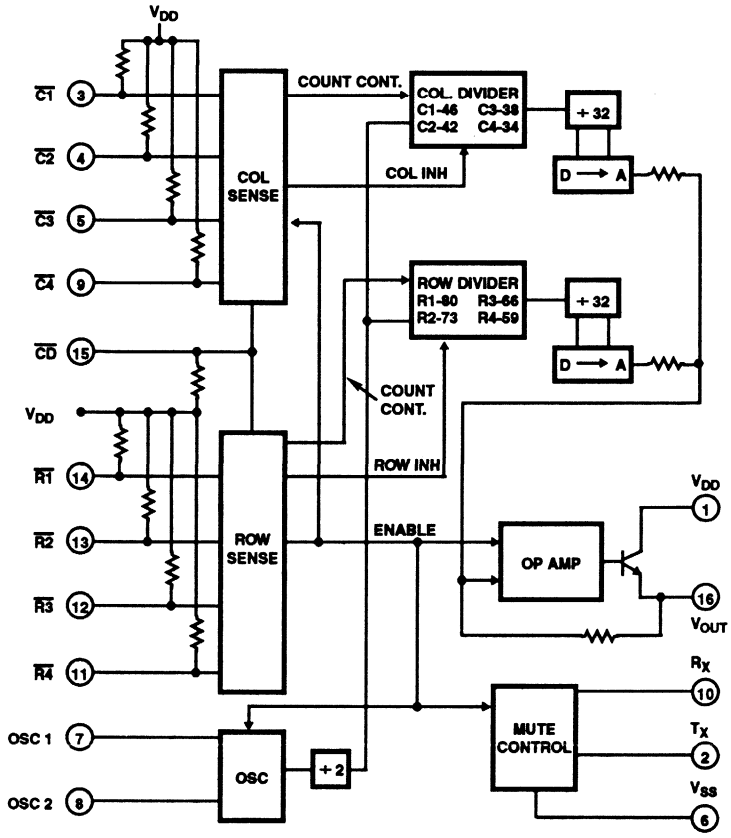
FIGURE 1. BELL AND NOMINAL OUTPUT FREQUENCIES (IN PARENTHESIS) FOR 3.579545MHz CRYSTAL

DTMF GENERATOR FUNCTIONAL TRUTH TABLE

	INPUTS			OUTPUTS			
KEYBOARD MODE	NUMBER OF COLUMN INPUTS ACTIVATED "LOW"	NUMBER OF ROW INPUTS ACTIVATED "LOW"	$\overline{CD}$	TONE	OSC RUNNING	R_X	T_X
X	X	X	"0"	None	No	"0"	"0"
No Key Depressed	0	0	"1"	None	No	"0"	"0"
	0	1	"1"	Dual Tone R_A, C_1	Yes	"1"	"1"
	1, 2, 3, or 4	0	"1"	None	No	"0"	"0"
Normal Dialing One Key Depressed (Note 9)	1	1	"1"	Dual Tone R_A, C_B	Yes	"1"	"1"
Two or More Keys In Same Row (Note 10)	2, 3, or 4	1	"1"	Single Row Tone R_A	Yes	"1"	"1"
Two or More Keys In Same Column	1	2, 3, or 4	"1"	Single Column Tone C_B	Yes	"1"	"1"
Two or More Keys In Different Rows and Columns	2, 3, or 4	2, 3, or 4	"1"	None	Yes	"1"	"1"

Where:
X = Do Not Care
R_A refers to Tone Output frequencies corresponding to Row 1, Row 2, Row 3, Row 4; C_B refers to Tone Output frequencies corresponding to Column 1, Column 2, Column 3, Column 4.
A = 1, 2, 3, 4 B = 1, 2, 3, 4 A = B, or $A \neq B$

Functional Diagram



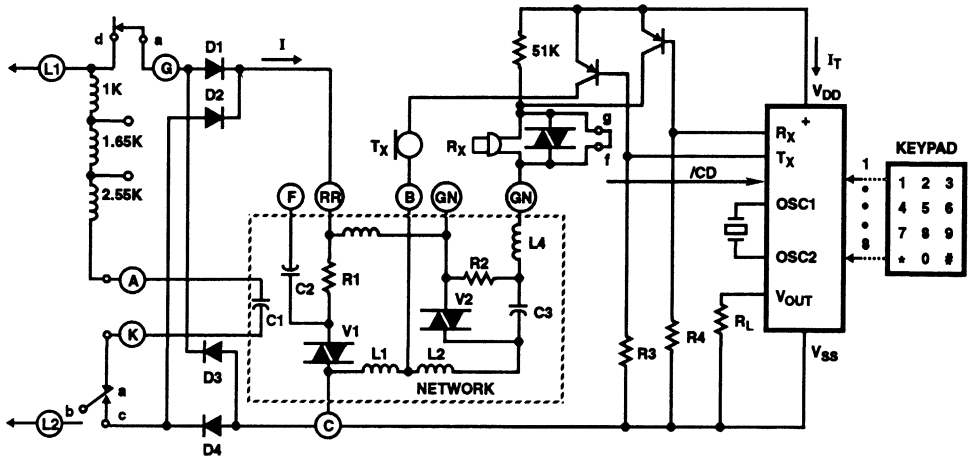


FIGURE 2. INTERFACE WITH STANDARD K500 TELEPHONE NETWORK

HARRIS SEMICONDUCTOR

CD74HC22106
CD74HCT22106

QMOS 8 x 8 x 1 Crosspoint Switch with Memory Control

April 1993

Features

- 64 Analog Switches In an 8 x 8 x 1 Array
- On-Chip Line Decoder and Control Latches
- Automatic Power-Up Reset by Using a 0.1μF Capacitor at the MR Pin
- R_{ON} Resistanced 95Ω at V_{CC} = 4.5V
- Analog Signal Capability: $V_{DD}/2$
- Wide Operating Temp. Range: -40°C to +85°C

Family Features

- CD74HC Types
  - 2V to 10V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{DD}; at V_{DD} = 5V and 10V
- CD74HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility: V_{IL} = 0.8V Max, V_{IH} = 2V Min
  - CMOS Input Compatibility: I_I < 1μA at V_{OL}, V_{OH}

Description

The CD74HC22106 and CD74HCT22106 are digitally controlled analog switches which utilize silicon-gate CMOS technology. The CD74HC22106 type features CMOS input-voltage-level compatibility and the CD74HCT22106 features LSTTL input-voltage-level compatibility.

The Master Reset has an internal pull-up resistor and is normally used with a 0.1μF capacitor. During power up all switches are automatically reset. The crosspoint switches will reset with MR = 0 even if CE is high. A 6-bit address through a 6 line to 64 line decoder selects the transmission gate which can be turned on by applying a logical ONE to the DATA input and logical ZERO to the STROBE. Similarly, any transmission gate can be turned OFF by applying a logical ZERO to the DATA input while strobing the STROBE with a logical ZERO.

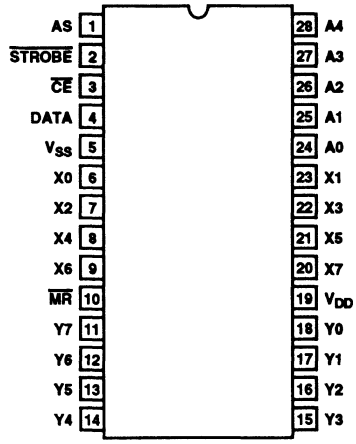
The CE pin allows the crosspoint array to be cascaded for matrix expansion in both the X and Y directions.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CD74HC22106E	-40°C to +85°C	28 Lead Plastic DIP
CD74HCT22106E	-40°C to +85°C	28 Lead Plastic DIP

Pinout

CD74HC22106, CD74HCT22106
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1719.2

Absolute Maximum Ratings

DC Supply Voltage (V_{DD})
Voltage Reference to V_{SS} Terminal ..... -0.5V to +11V
DC Input Diode Current
I_{IK} (for V_I < -0.5 or V_I > V_{DD} +0.5V ..... ±20mA
DC Output Diode Current
I_{OK} (For V_O < -0.5 or V_O > V_{DD} +0.5V ..... ±20mA
DC Transmission Gate Current ..... ±25mA
Power Dissipation per Package (P_D)
For T_A = -40°C to +60°C (Package Type E) 500mW
For T_A = -60°C to +85°C (Package Type E) ..... Derate Linearily at 12mW/°C to 200mW
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range (T_A)
Package Type E ..... -40°C to +85°C
Storage Temperature Range ..... -65°C ≤T_A ≤+150°C
Supply Voltage Range (for T_A = Full Package Temp. Range) V_{DD}
CD74HC22106 ..... 2V to 10V
CD74HCT22106 ..... 4.5V to 5.5V
DC Input or Output Voltage V_I, V_O ..... 0V to V_{DD}

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications V_{SS} = GND

PARAMETERS	CD74HC22106							CD74HCT22106							UNITS
	TEST CONDITIONS		+25°C			-40°C to +85°C		TEST CONDITIONS		+25°C			-40°C to +85°C		
	V_{IS} (V)	V_{DD} (V)	MIN	TYP	MAX	MIN	MAX	V_{IS} (V)	V_{DD} (V)	MIN	TYP	MAX	MIN	MAX	
High-Level Input Voltage V_{IH}	-	2	1.5	-	-	1.5	-	-	4.5 to 5.5	2	-	-	2	-	V
	-	4.5	3.15	-	-	3.5	-	-							
	-	9	6.3	-	-	6.3	-	-							
Low-Level Input Voltage V_{IL}	-	2	-	-	0.5	-	0.5	-	4.5 to 5.5	-	-	0.8	-	0.8	V
	-	4.5	-	-	1.35	-	1.35	-							
	-	9	-	-	2.7	-	2.7	-							
Input Leakage Current (Any Control) I_L	V_{DD} or GND	10	-	-	±0.1	-	±1	Any Voltage Between V_{DD} & GND	5.5	-	-	±0.1	-	±1	µA
Quiescent Device Current, I_{CC} (with $\overline{MR}$ = 1)	V_{DD} or GND	10	-	-	5	-	50	V_{DD} or GND	5.5	-	-	2	-	20	µA
Off Leakage Current, I_L (with $\overline{MR}$ = 1)	All Switches OFF	10	-	-	0.1	-	1	-	5.5	-	-	0.1	-	1	µA
"On" Resistance R_{ON}	V_{DD} to GND Figures 8, 9	2	-	470	700	-	875	Figure 8	4.5	-	64	95	-	120	Ω
		4.5	-	64	95	-	120								
		9	-	45	70	-	90								
	V_{DD}/2	-	-	-	-	-	-	-	4.5	-	58	85	-	110	Ω
		4.5	-	58	85	-	110								
		9	-	40	60	-	80								
"On" Resistance Between Any Two Channels ΔR_{ON}	V_{DD} to GND	-	-	-	-	-	-	V_{DD} to GND	4.5	-	25	-	-	-	Ω
		4.5	-	25	-	-	-								
		9	-	23	-	-	-								

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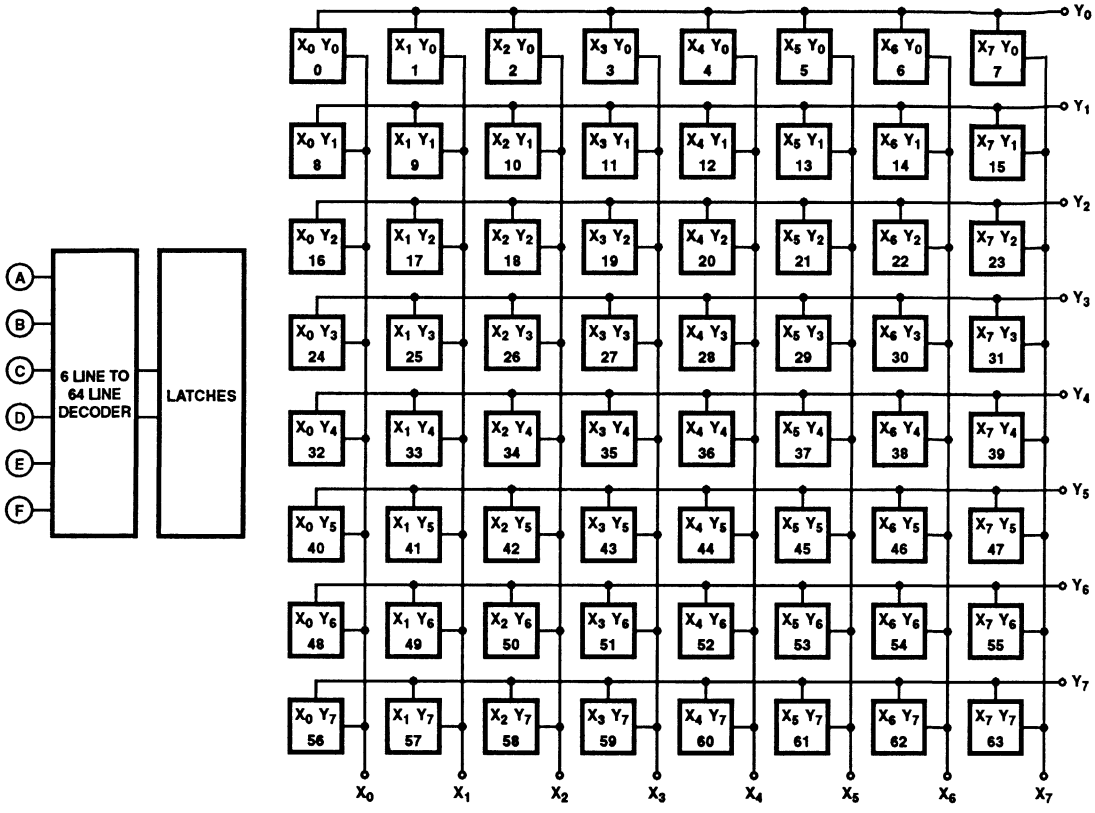
Dynamic Electrical Specifications V_{SS} = 0V

PARAMETERS	SYMBOL	TEST CONDITIONS	FIG.	V_{DD} (V)	LIMITS +25°C HC MIN	HC MAX	HCT MIN	HCT MAX	-40°C to +85°C HC MIN	HC MAX	HCT MIN	HCT MAX	UNITS
CONTROLS													
Propagation Delay Time:	t_{PZH}	R_L = 10kΩ	1	2	-	370	-	-	-	385	-	-	ns
Strobe to Output (Switch Turn-On to High Level)		C_L = 50pF		4.5	-	110	-	120	-	125	-	135	ns
		t_R, t_F = 6ns		9	-	65	-	-	-	70	-	-	ns
Data-In to Output (Turn-On to High Level)	t_{PZH}		2	2	-	240	-	-	-	255	-	-	ns
				4.5	-	75	-	85	-	85	-	95	ns
				9	-	50	-	-	-	55	-	-	ns
Address to Output (Turn-On to High Level)	t_{PZH}		3	2	-	380	-	-	-	400	-	-	ns
				4.5	-	110	-	120	-	125	-	135	ns
				9	-	65	-	-	-	75	-	-	ns
Propagation Delay Time:	t_{PHZ}		1	2	-	400	-	-	-	420	-	-	ns
Strobe to Output				4.5	-	135	-	150	-	155	-	170	ns
				9	-	90	-	-	-	100	-	-	ns
Data-In to Output (Turn-On to Low Level)	t_{PZL}		2	2	-	240	-	-	-	255	-	-	ns
				4.5	-	75	-	85	-	85	-	95	ns
				9	-	50	-	-	-	55	-	-	ns
Address to Output (Turn-Off)	t_{PHZ}		3	2	-	420	-	-	-	440	-	-	ns
				4.5	-	140	-	150	-	155	-	170	ns
				9	-	95	-	-	-	100	-	-	ns
Minimum Set-Up Time (Data-In to Strobe Address)	t_{SU}		-	2	35	-	-	-	40	-	-	-	ns
				4.5	20	-	20	-	20	-	20	-	ns
				9	15	-	-	-	15	-	-	-	ns
Minimum Hold Time (Data-In to Strobe Address)	t_H		-	2	85	-	-	-	90	-	-	-	ns
				4.5	25	-	25	-	25	-	25	-	ns
				9	20	-	-	-	20	-	-	-	ns
Minimum Strobe Pulse Width	t_W		-	2	200	-	-	-	210	-	-	-	ns
				4.5	45	-	55	-	55	-	65	-	ns
				9	25	-	-	-	30	-	-	-	ns
Maximum Switching Frequency	F_O		-	2	0.7	-	-	-	0.6	-	-	-	MHz
				4.5	3.0	-	2.8	-	2.8	-	2.6	-	MHz
				9	7	-	-	-	6.5	-	-	-	MHz
Input (Control) Capacitance	C_I		-	-	-	10	-	10	-	10	-	10	pF

Dynamic Electrical Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	V_{IS} (V_{P-P})	V_{SS} (V)	V_{DD} (V)	LIMITS +25°C HC MIN	LIMITS +25°C HC MAX	LIMITS +25°C HCT MIN	LIMITS +25°C HCT MAX	LIMITS -40°C to +85°C HC MIN	LIMITS -40°C to +85°C HC MAX	LIMITS -40°C to +85°C HCT MIN	LIMITS -40°C to +85°C HCT MAX	UNITS
Propagation Delay Time, Signal Input to Output	t_{PLH}, t_{PHL}	R_L = 10kΩ, C_L = 50pF, t_R, t_F = 6ns	-	0	2	-	30	-	-	-	33	-	-	ns
			-	0	4.5	-	20	-	20	-	22	-	22	ns
			-	-	9	-	15	-	-	-	17	-	-	ns
						HC Typical		HCT Typical						
Switch Frequency Response at -3dB	f_{3dB}	R_S = R_L = 600Ω	2	-2.25	2.25	5		5		-	-	-	-	MHz
			2	-4.5	4.5	6		6		-	-	-	-	MHz
Crosstalk Between Any Two Channels	F_{CT}	R_S = R_L = 600Ω, f = 1kHz	2	-2.25	2.25	-110		-110		-	-	-	-	dB
		R_S = R_L = 600Ω, f = 1MHz	2	-2.25	2.25	-53		-53		-	-	-	-	dB
			2	-4.5	4.5	-55		-55		-	-	-	-	dB
Switch "OFF" -40dB Feed Through Frequency	F_{DT}	R_S = R_L = 600Ω	2	-2.25	2.25	7		7		-	-	-	-	MHz
			2	-4.5	4.5	8		8		-	-	-	-	MHz
Total Harmonic Distortion	THD	R_L = 10kΩ, f = 1kHz sine-wave	4	-2.25	2.25	0.05		0.05		-	-	-	-	%
			8	-4.5	4.5	0.05		0.05		-	-	-	-	%
		R_L = 600Ω, f = 1kHz sine-wave	4	-2.25	2.25	0.25		0.25		-	-	-	-	%
			7	-4.5	4.5	0.12		0.12		-	-	-	-	%
Control to Switch Feed-Through Noise (DATA IN, Strobe, Address)		R_L = 10kΩ, t_R, t_F = 6ns	V_{DD}	0	5	35		35		-	-	-	-	mV
			V_{DD}	0	10	65		65		-	-	-	-	mV
Capacitance, Xn to GND	C_{IS}	f = 1MHz	-	0	10	48		48		-	-	-	-	pF
Yn to GND			-	0	10	44		44		-	-	-	-	pF

Functional Diagram



TRUTH TABLE

A_5	A_4	A_3	A_2	A_1	A_0	SWITCH SELECT	A_5	A_4	A_3	A_2	A_1	A_0	SWITCH SELECT
0	0	0	0	0	0	X_0 Y_0	1	0	0	0	0	0	X_0 Y_4
0	0	0	0	0	1	X_1 Y_0	1	0	0	0	0	1	X_1 Y_4
0	0	0	0	1	0	X_2 Y_0	1	0	0	0	1	0	X_2 Y_4
0	0	0	0	1	1	X_3 Y_0	1	0	0	0	1	1	X_3 Y_4
0	0	0	1	0	0	X_4 Y_0	1	0	0	1	0	0	X_4 Y_4
0	0	0	1	0	1	X_5 Y_0	1	0	0	1	0	1	X_5 Y_4
0	0	0	1	1	0	X_6 Y_0	1	0	0	1	1	0	X_6 Y_4
0	0	0	1	1	1	X_7 Y_0	1	0	0	1	1	1	X_7 Y_4
0	0	1	0	0	0	X_0 Y_1	1	0	1	0	0	0	X_0 Y_5
0	0	1	0	0	1	X_1 Y_1	1	0	1	0	0	1	X_1 Y_5
0	0	1	0	1	0	X_2 Y_1	1	0	1	0	1	0	X_2 Y_5
0	0	1	0	1	1	X_3 Y_1	1	0	1	0	1	1	X_3 Y_5
0	0	1	1	0	0	X_4 Y_1	1	0	1	1	0	0	X_4 Y_5
0	0	1	1	0	1	X_5 Y_1	1	0	1	1	0	1	X_5 Y_5
0	0	1	1	1	0	X_6 Y_1	1	0	1	1	1	0	X_6 Y_5
0	0	1	1	1	1	X_7 Y_1	1	0	1	1	1	1	X_7 Y_5
0	1	0	0	0	0	X_0 Y_2	1	1	0	0	0	0	X_0 Y_6
0	1	0	0	0	1	X_1 Y_2	1	1	0	0	0	1	X_1 Y_6
0	1	0	0	1	0	X_2 Y_2	1	1	0	0	1	0	X_2 Y_6
0	1	0	0	1	1	X_3 Y_2	1	1	0	0	1	1	X_3 Y_6
0	1	0	1	0	0	X_4 Y_2	1	1	0	1	0	0	X_4 Y_6
0	1	0	1	0	1	X_5 Y_2	1	1	0	1	0	1	X_5 Y_6
0	1	0	1	1	0	X_6 Y_2	1	1	0	1	1	0	X_6 Y_6
0	1	0	1	1	1	X_7 Y_2	1	1	0	1	1	1	X_7 Y_6
0	1	1	0	0	0	X_0 Y_3	1	1	1	0	0	0	X_0 Y_7
0	1	1	0	0	1	X_1 Y_3	1	1	1	0	0	1	X_1 Y_7
0	1	1	0	1	0	X_2 Y_3	1	1	1	0	1	0	X_2 Y_7
0	1	1	0	1	1	X_3 Y_3	1	1	1	0	1	1	X_3 Y_7
0	1	1	1	0	0	X_4 Y_3	1	1	1	1	0	0	X_4 Y_7
0	1	1	1	0	1	X_5 Y_3	1	1	1	1	0	1	X_5 Y_7
0	1	1	1	1	0	X_6 Y_3	1	1	1	1	1	0	X_6 Y_7
0	1	1	1	1	1	X_7 Y_3	1	1	1	1	1	1	X_7 Y_7

Test Circuits and Waveforms

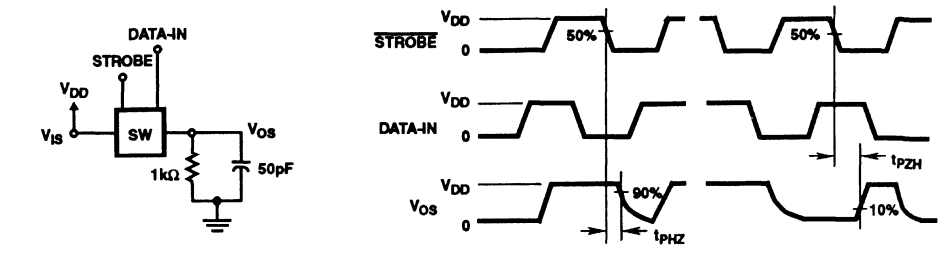


FIGURE 1. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (STROBE TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-0FF)

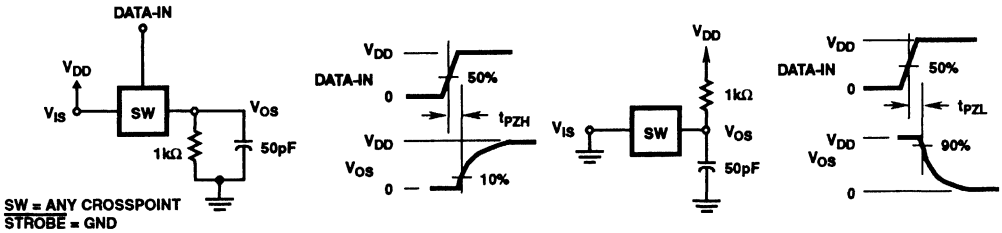


FIGURE 2. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (DATA-IN TO SIGNAL OUTPUT, SWITCH TURN-ON TO HIGH OR LOW LEVEL)

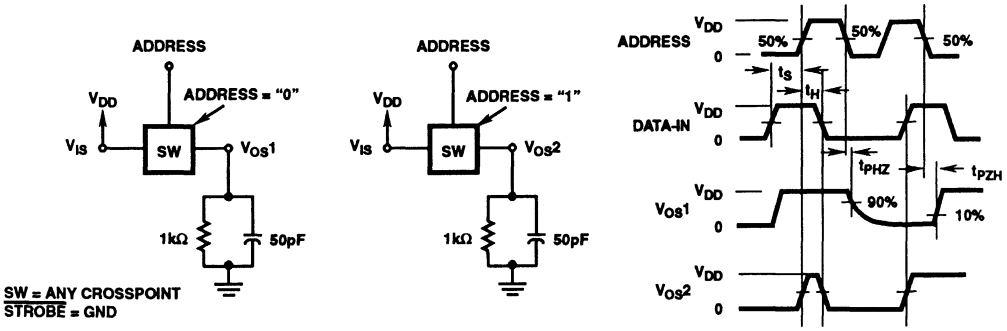


FIGURE 3. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (ADDRESS TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-0FF)

Typical Application Information

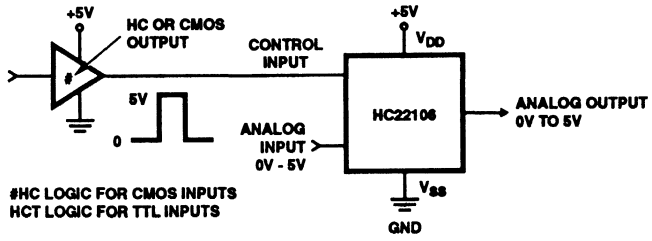


FIGURE 4. TYPICAL SINGLE SUPPLY CONNECTION FOR HC22106

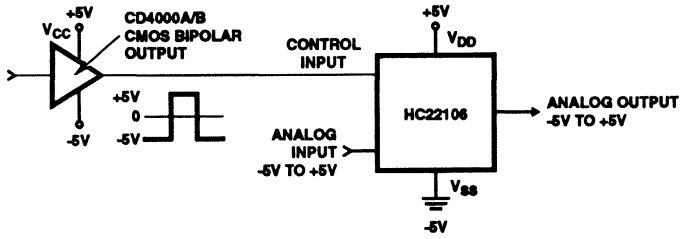


FIGURE 5. TYPICAL DUAL SUPPLY CONNECTION FOR HC22106

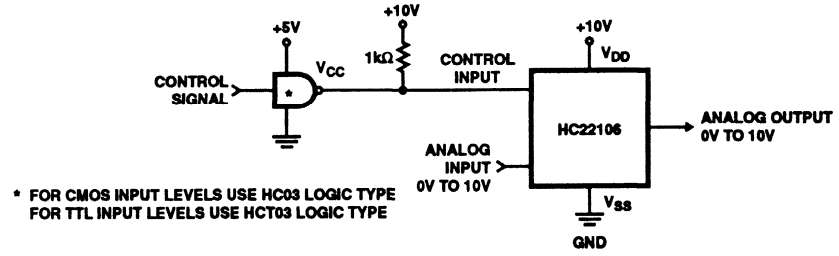


FIGURE 6. USE OF HC/HCT03 WHEN CONTROL IS 0V - 5V AND ANALOG SIGNAL IS 0V - 10V

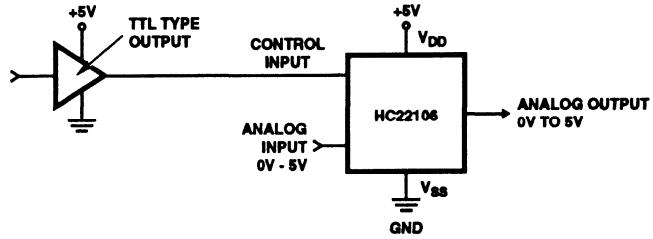


FIGURE 7. TYPICAL SINGLE SUPPLY CONNECTION FOR HCT22106 WITH TTL INPUT

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Typical Performance Curves

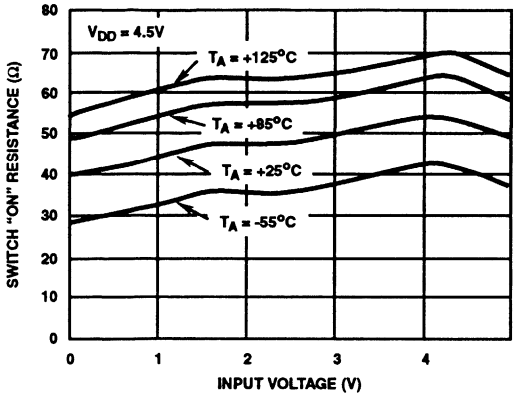


FIGURE 8. TYPICAL "ON" RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE vs TEMPERATURE

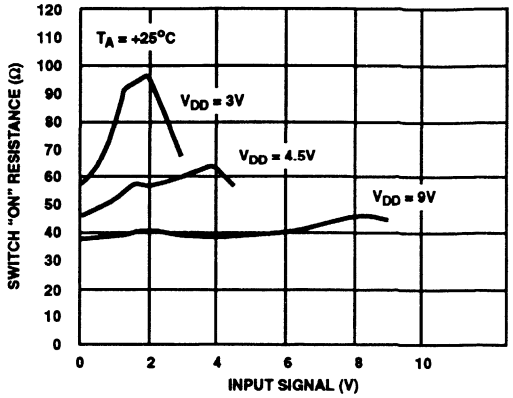


FIGURE 9. TYPICAL "ON" RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE vs V_{DD}

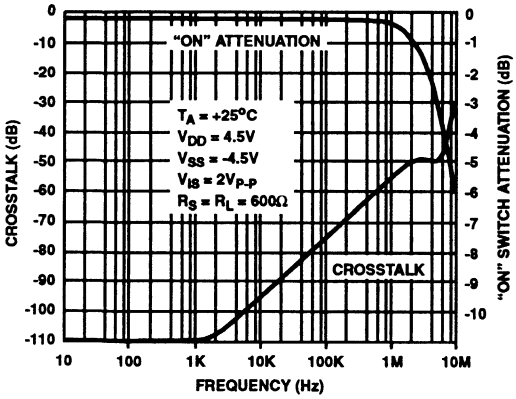


FIGURE 10. TYPICAL "ON" SWITCH ATTENUATION AND CROSSTALK AS A FUNCTION OF FREQUENCY

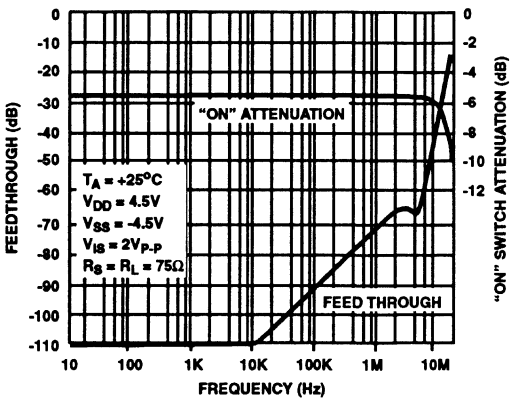


FIGURE 11. TYPICAL "ON" SWITCH ATTENUATION AND "OFF" SWITCH FEED THROUGH AS A FUNCTION OF FREQUENCY

HARRIS SEMICONDUCTOR

HC-5502B

SLIC
Subscriber Line Interface Circuit

March 1993

Features

- Pin For Pin Replacement For The HC-5502A
- Capable of +12V or +5V (VB+) Operation
- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (30mA)
- Internal Ring Relay Driver
- Low Power Consumption During Standby
- Switch Hook, Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBX's

Description

The Harris SLIC incorporates many of the BORSHT function on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Harris dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

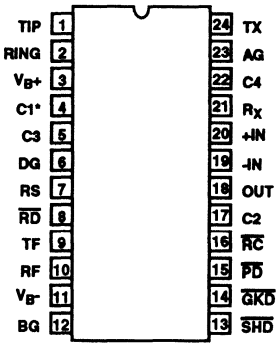
The Harris SLIC is ideally suited for the design of new digital PBX systems, by eliminating bulky hybrid transformers.

Ordering Information

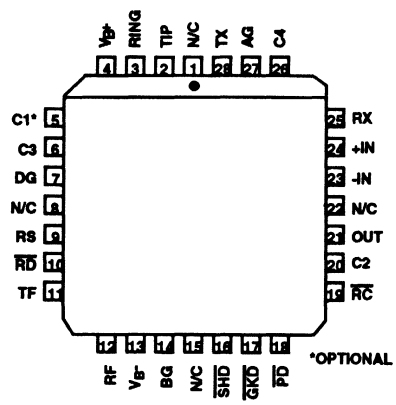
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HC1-5502B-5	0°C to +75°C	24 Lead Ceramic DIP
HC1-5502B-9	-40°C to +85°C	24 Lead Ceramic DIP
HC3-5502B-5	0°C to +75°C	24 Lead Plastic DIP
HC3-5502B-9	-40°C to +85°C	24 Lead Plastic DIP
HC4P5502B-5	0°C to +75°C	28 Lead PLCC
HC4P5502B-9	-40°C to +85°C	28 Lead PLCC
HC9P5502B-5	0°C to +75°C	24 Lead SOIC
HC9B5502B-9	-40°C to +85°C	24 Lead SOIC

Pinouts

HC-5502B
(PDIP, CDIP, SOIC)
TOP VIEW



HC-5502B
(PLCC)
TOP VIEW



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CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2884.1**

Absolute Maximum Ratings (Note 1)

Supply Voltage
- (V_{B-}) ..... -60 to +0.5V
- (V_{B+}) ..... -0.5 to +15V
- (V_{B+} - V_{B-}) ..... +75V

Relay Drive Voltage (V_{RD}) ..... -0.5 to +15V
Junction Temperature (Ceramic) ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Relay Driver Voltage (V_{RD}) ..... +5V to +12V
Positive Supply Voltage (V_{B+}) ..... 4.75V to 5.25V or 10.8V to 13.2V
Negative Supply Voltage (V_{B-}) ..... -42V to -58V
High Level Logic Input Voltage 2.4V
Low Level Logic Input Voltage 0.6V
Loop Resistance (R_L) ..... 200 to 1200Ω
Operating Temperature Range
- HC-5502B-5 ..... 0°C to +75°C
- HC-5502B-9 ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Unless Otherwise Specified, V_{B-} = -48V, V_{B+} = +12V and +5V, AG = BG = DG = 0V, Typical Parameters T_A = +25°C. Min-Max Parameters are Over Operating Temperature Range.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I_{Long}* = 0, V_{B+} = +12V	-	135	235	mW
Off Hook Power Dissipation	R_L = 600Ω, I_{Long}* = 0, V_{B+} = +12V	-	450	690	mW
Off Hook IB+	R_L = 600Ω, I_{Long}* = 0, T_A = -40°C	-	-	6.0	mA
Off Hook IB+	R_L = 600Ω, I_{Long}* = 0, T_A = +25°C	-	-	5.3	mA
Off Hook IB-	R_L = 600Ω, I_{Long}* = 0	-	-	39	mA
Off Hook Loop Current	R_L = 1200Ω, I_{Long}* = 0	-	21	-	mA
Off Hook Loop Current	R_L = 1200Ω, V_{B-} = -42V, I_{Long}* = 0, T_A = +25°C	17.5	-	-	mA
Off Hook Loop Current	R_L = 200Ω, I_{Long}* = 0	25.5	30	34.5	mA
Fault Currents					
TIP to Ground		-	14	-	mA
RING to Ground		-	47	-	mA
TIP to RING		-	30	-	mA
TIP and RING to Ground		-	47	-	mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	V_{RD} = +12V, $\overline{RC}$ = 1 = HIGH, T_A = +25°C	-	-	100	µA
Ring Trip Detection Period	R_L = 600Ω, T_A = +25°C	-	2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD}$ = V_{OL}	10	-	-	mA
	$\overline{SHD}$ = V_{OH}	-	-	5	mA
Ground Key Detection Threshold	$\overline{GKD}$ = V_{OL}	20	-	-	mA
	$\overline{GKD}$ = V_{OH}	-	-	10	mA
Loop Current During Power Denial	R_L = 200Ω	-	±2	-	mA
Dial Pulse Distortion		0	-	5	ms
Receive Input Impedance	(Note 2)	-	110	-	kΩ
Transmit Output Impedance	(Note 2)	-	10	20	Ω

Electrical Specifications Unless Otherwise Specified, V_{B}- = -48V, V_{B}+ = +12V and +5V, AG = BG = DG = 0V, Typical Parameters T_A = +25°C. Min-Max Parameters are Over Operating Temperature Range. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Two Wire Return Loss	Referenced to 600Ω +2.16μF (Note 2)				
SRL LO		-	15.5	-	dB
ERL		-	24	-	dB
SRL HI		-	31	-	dB
Longitudinal Balance	$1V_{RMS}$ 200Hz - 3400Hz, (Note 2)				
2 Wire Off Hook	IEEE Method $0°C \le T_A \le +75°C$	58	65	-	dB
2 Wire On Hook		60	63	-	dB
4 Wire Off Hook		50	58	-	dB
Low Frequency Longitudinal Balance	R.E.A. Method, (Note 2) R_L = 600Ω, $0°C \le T_A \le +75°C$	-	-	23	dBrnC
		-	-	-67	dBm0p
Insertion Loss 2 Wire - 4 Wire, 4 Wire - 2 Wire	at 1kHz, 0dBm Input Level, Referenced 600Ω	-	±0.05	±0.2	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 2)	-	±0.02	±0.05	dB
Idle Channel Noise 2 Wire - 4 Wire, 4 Wire - 2 Wire	(Note 2)	-	1	5	dBrnC
		-	-89	-85	dBm0p
Absolute Delay 2 Wire - 4 Wire, 4 Wire - 2 Wire	(Note 2)	-	-	2	μs
Trans Hybrid Loss	Balance Network Set Up for 600Ω Termination at 1kHz	36	40	-	dB
Overload Level 2 Wire - 4 Wire, 4 Wire - 2 Wire	V_{B}+ = +5V	1.5			V_{PEAK}
	V_{B}+ = +12V	1.75	-	-	V_{PEAK}
Level Linearity	at 1kHz, (Note 2) Referenced to 0dBm Level				
2 Wire - 4 Wire, 4 Wire - 2 Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
Power Supply Rejection Ratio	(Note 2) 30 - 60Hz R_L = 600Ω				
V_{B}+ to 2 Wire		15	-	-	dB
V_{B}+ to Transmit		15	-	-	dB
V_{B}- to 2 Wire		15	-	-	dB
V_{B}- to Transmit		15	-	-	dB
V_{B}+ to 2 Wire	200 - 16kHz R_L = 600Ω	30	-	-	dB
V_{B}+ to Transmit		30	-	-	dB
V_{B}- to 2 Wire		30	-	-	dB
V_{B}- to Transmit		30	-	-	dB
Logic Input Current (RS, $\overline{RC}$, $\overline{PD}$)	$0V \le V_{IN} \le +5V$	-	-	±100	μA

Electrical Specifications Unless Otherwise Specified, V_{B}- = -48V, V_{B}+ = +12V and +5V, AG = BG = DG = 0V, Typical Parameters T_A = +25°C. Min-Max Parameters are Over Operating Temperature Range. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Inputs					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} 800µA, V_{B}+ = +12V, +5V	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} 80µA, V_{B}+ = +12V	2.7	5.0	5.5	V
	I_{LOAD} 40µA, V_{B}+ = +5V	2.7	-	5.0	V

* I_{Long} = Longitudinal Current

Uncommitted Op Amp Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Input Bias Current		-	20	-	nA
Differential Input Resistance	(Note 2)	-	1	-	MΩ
Output Voltage Swing	R_L = 10kΩ, V_{B}+ = +12V	-	±5	-	V_{PEAK}
	R_L = 10kΩ, V_{B}+ = +5V	-	±3	-	V_{PEAK}
Output Resistance	A_{VCL} = 1 (Note 2)	-	10	-	Ω
Small Signal GBW	(Note 2)	-	1	-	MHz

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterised upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Pin Descriptions

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
2	1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring process.
3	2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
4	3	V_{B}+	Positive Voltage Source - Most positive supply. V_{B}+ is typically 12V or 5V.

Pin Descriptions (Continued)

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
5	4	C1	Capacitor #1 - Optional Capacitor used to improve power supply rejection. This pin should be left open if unused.
6	5	C3	Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V_B- supply. Typical value is 0.3µF, 30V.
7	6	DG	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC.
9	7	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock should be arranged such that a positive transition occurs on the negative going zero crossing of the ring voltage source, ensuring that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If synchronization is not required, tie to +5V.
10	8	$\overline{RD}$	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
11	9	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
12	10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signal to the telephone set, and sink longitudinal current.
13	11	V_B-	Negative Voltage Source - Most negative supply. V_B- is typically -48 volts with an operational range of -42V to -58V. Frequently referred to as "battery".
14	12	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
16	13	$\overline{SHD}$	Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
17	14	$\overline{GKD}$	Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.
18	15	$\overline{PD}$	Power Denial - A low active TTL - Compatible logic input. When enabled the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.
19	16	$\overline{RC}$	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next rising edge of the ring sync ($\overline{RS}$) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off- hook ($\overline{SHD}$ = 0).
20	17	C2	Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15µF, 10V. This capacitor is not used if ground key function is not required.
21	18	OUT	The analog output of the spare operational amplifier.
23	19	-IN	The inverting analog input of the spare operational amplifier.
24	20	+IN	The non-inverting analog input of the spare operational amplifier.
25	21	RX	Receive Input, Four Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed amplifiers, which in turn drive tip and ring through 300Ω of feed resistance on each side of the line.

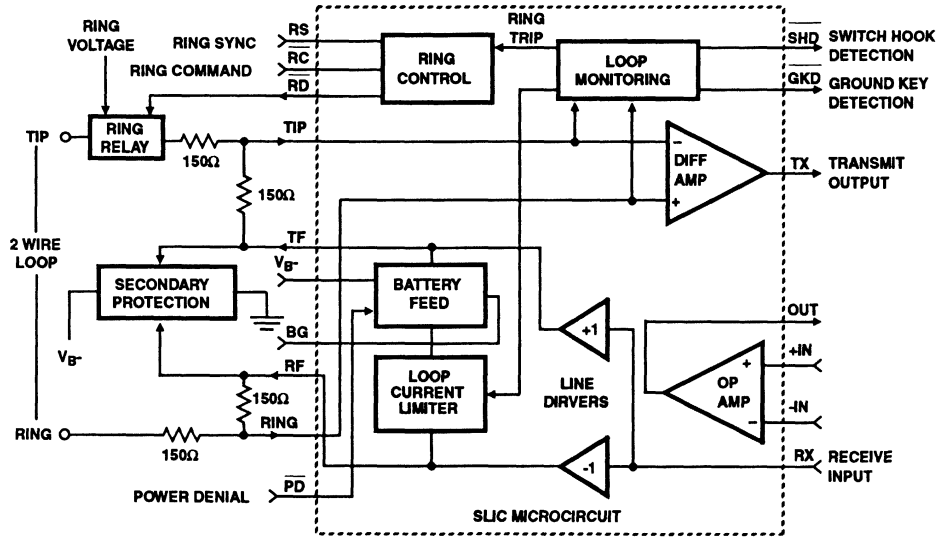
Pin Descriptions (Continued)

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
26	22	C4	Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from nearby power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5µF to 1.0µF, 20V. This capacitor should be nonpolarized.
27	23	AG	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
28	24	TX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
1, 8, 5, 22		NC	No Internal Connection.

NOTE:

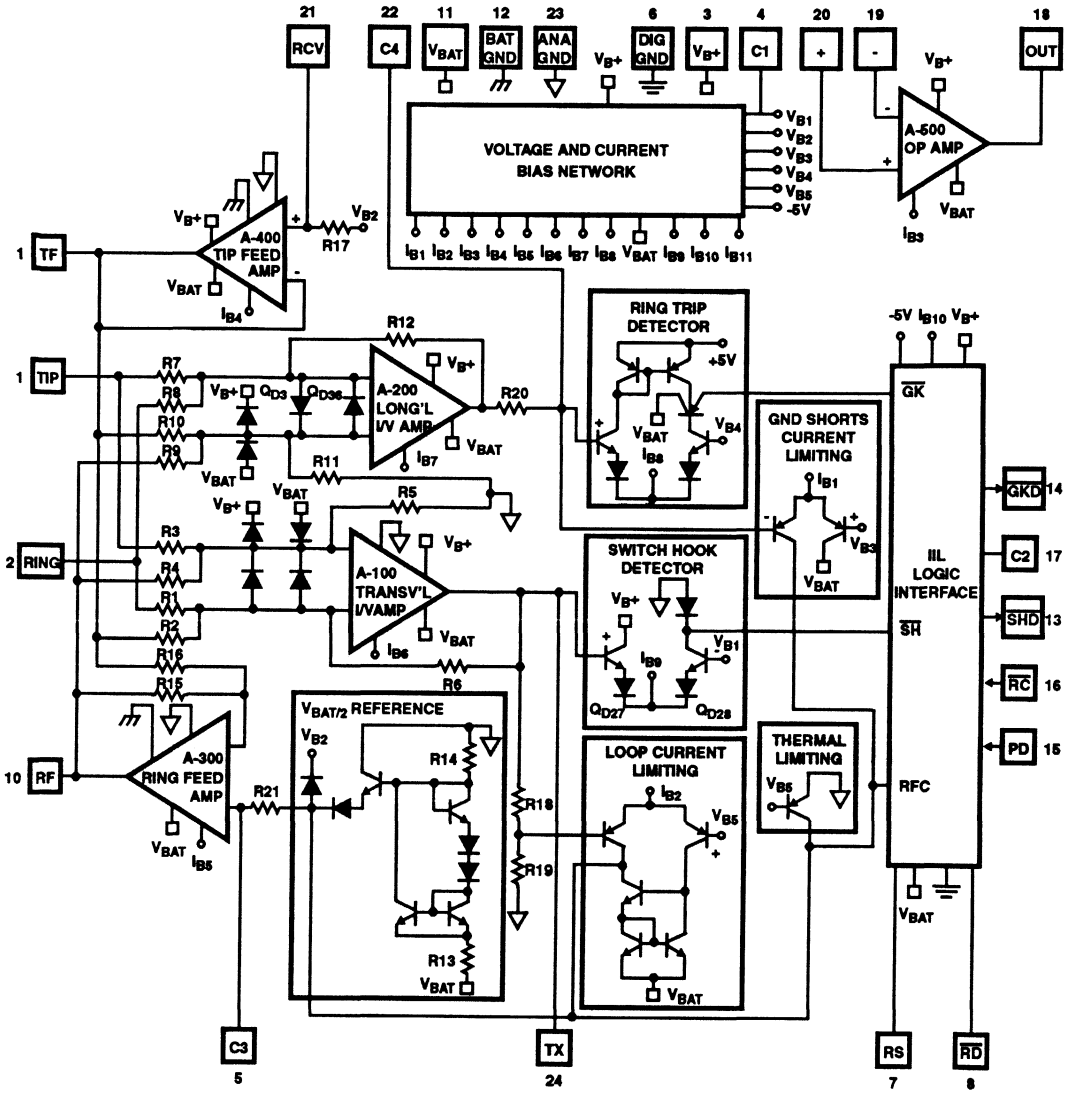
1. All grounds (AG, BG, & DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Functional Diagram



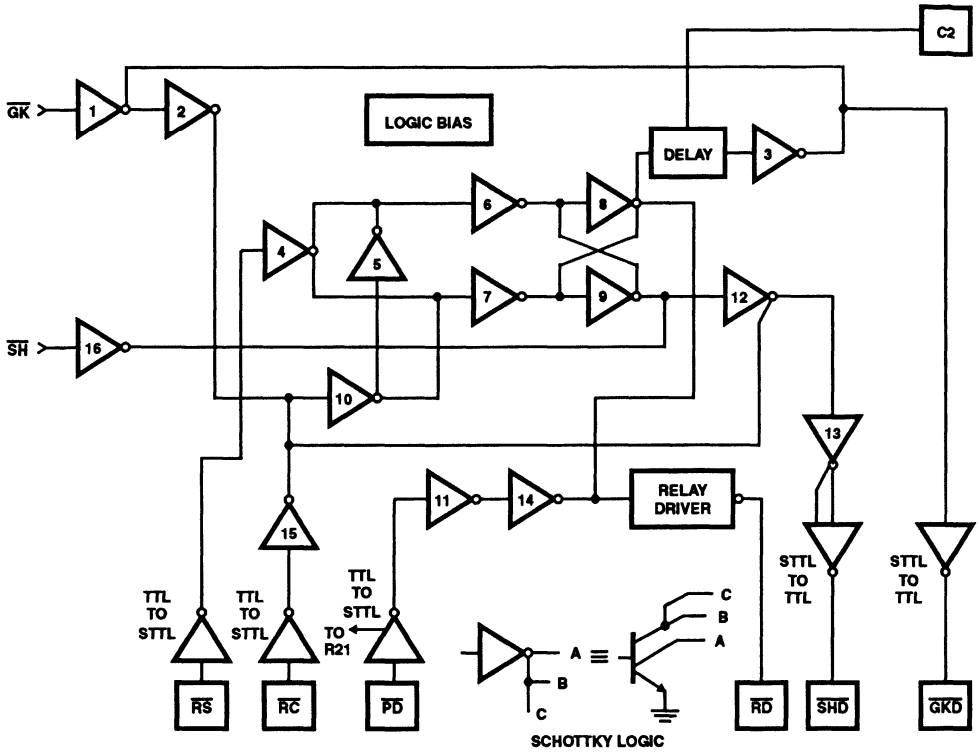
Schematic

HC-5502B SLIC FUNCTIONAL SCHEMATIC
Pin Numbers for DIP/SOIC Package



Logic Diagram

HC-5502B LOGIC GATE SCHEMATIC



Die Characteristics

Transistor Count		183
Diode Count		33
Die Dimensions		137 x 102 mils
Substrate Potential		V_B-
Process		Bipolar-DI
Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	52	15
Plastic DIP	52	22
PLCC	67	29
SOIC	76	24

Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or $30mA_{RMS}$, $15mA_{RMS}$ per leg, without any performance degradation.

TABLE 1

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/	±1000 (Plastic)	V_{PEAK}
	1000µs Fall	±500 (Ceramic)	V_{PEAK}
Metallic Surge	10µs Rise/	±1000 (Plastic)	V_{PEAK}
	1000µs Fall	±500 (Ceramic)	V_{PEAK}
T/GND	10µs Rise/	±1000 (Plastic)	V_{PEAK}
R/GND	1000µs Fall	±500 (Ceramic)	V_{PEAK}
50/60Hz Current			
T/GND	11 Cycles	700 (Plastic)	V_{RMS}
R/GND	Limited to 10Arms	350 (Ceramic)	V_{RMS}

Applications Diagram

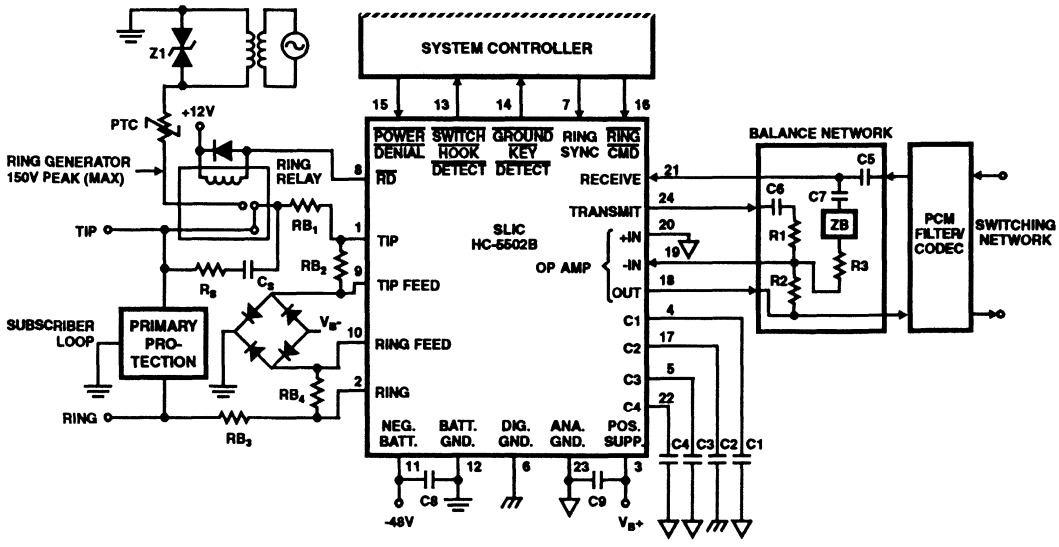


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values

C1 = 0.5µF (Note 1)

C2 = 0.15µF, 10V

C3 = 0.3µF, 30V

C4 = 0.5µF to 1.0µF, 10%, 20V (Should be nonpolarized)

C5 = 0.5µF, 20V

C6 = C7 = 0.5µF (10% Match Required) (Note 2), 20V

C8 = 0.01µF, 100V

C9 = 0.01µF, 20V, ±20%

R1 = R2 = R3 = 100kΩ (0.1% Match Required, 1% absolute value), ZB = 0 for 600Ω Terminations (Note 2)

$RB_1 = RB_2 = RB_3 = RB_4 = 150\Omega$ (0.1% Match Required, 1% absolute value)

R_S = 1kΩ, C_S = 0.1µF, 200V typically, depending on V_{RING} and line length.

Z1 = 150V to 200V transient protection. PTC used as ring generator ballast.

NOTES:

1. C1 is an optional capacitor used to improve V_B+ supply rejection. This pin must be left open if unused.
2. To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 are 1µF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -22V step when the loop is closed. Too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

   A 0.5µF and 100kΩ gives a time constant of 50msec. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.
3. Secondary protection diode bridge recommended is a 2A, 200V type.
4. All grounds (AG, BG, & DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first
5. Pin numbers given for DIP/SOIC package.

Additional information is contained in Application Note 549, "The HC-550X Telephone SLICs" By Geoff Phillips.

HARRIS SEMICONDUCTOR

HC-5504B

SLIC
Subscriber Line Interface Circuit

March 1993

Features

- Pin for Pin Replacement for the HC-5504
- Capable of +5V or +12V (V_B+) Operation
- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (41mA)
- Internal Ring Relay Driver
- Allows Interfacing With Negative Superimposed Ringing Systems
- Low Power Consumption During Standby
- Switch Hook Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBXs

Description

The Harris SLIC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Harris dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

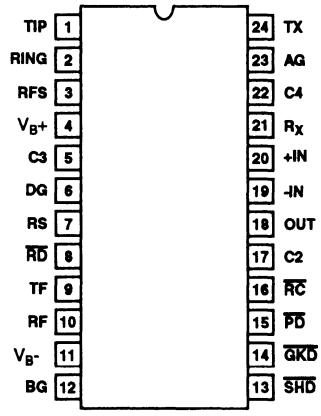
The Harris SLIC is ideally suited for the design of new digital PBX systems by eliminating bulky hybrid transformers.

Ordering Information

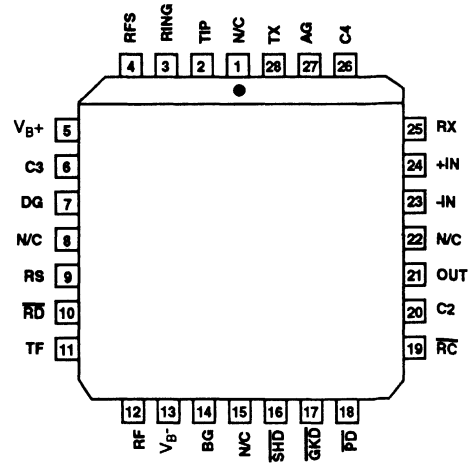
PART #	TEMP. RANGE	PACKAGE
HC1-5504B-5	0° to +75°C	24 Lead Ceramic DIP
HC1-5504B-9	-40° to +85°C	24 Lead Ceramic DIP
HC3-5504B-5	0° to +75°C	24 Lead Plastic DIP
HC3-5504B-9	-40° to +85°C	24 Lead Plastic DIP
HC4P5504B-5	0° to +75°C	28 Lead PLCC
HC4P5504B-9	-40° to +85°C	28 Lead PLCC
HC9P5504B-5	0° to +75°C	24 Lead SOIC
HC9P5504B-9	-40° to +85°C	24 Lead SOIC

Pinouts

HC-5504B (PDIP, CDIP, SOIC)
TOP VIEW



HC-5504B (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2886.1**

Absolute Maximum Ratings (Note 1)

Maximum Continuous Supply Voltages
- (V_{B-}) ..... -60 to +0.5 V
- (V_{B+}) ..... -0.5 to +15 V
- (V_{B+} - V_{B-}) ..... +75V

Relay Drive Voltage (V_{RD}) ..... -0.5 to +15V
Junction Temperature Ceramic ..... +175°C
Junction Temperature Plastic ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
- HC-5504B-5 ..... 0°C to +75°C
- HC-5504B-9 ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to 150°C
Relay Driver Voltage (V_{RD}) ..... +5 to +12V
Positive Supply Voltage (V_{B+}) ..... 4.75 to 5.25 or 10.8 to 13.2V
Negative Supply Voltage (V_{B-}) ..... -36 to -58V
High Level Logic Input Voltage 2.4V
Low Level Logic Input Voltage 0.6V
Loop Resistance (R_L) ..... 200 to 1200Ω

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Unless Otherwise Specified, V_{B-} = -48V, V_{B+} = +12V and +5V, AG = BG = DG = 0V, Typical Parameters T_A = +25°C. Min-Max Parameters are Over Operating Temperature Range.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I_{LONG}* = 0, V_{B+} = +12V	-	170	235	mW
Off Hook Power Dissipation	R_L = 600Ω, I_{LONG}* = 0, V_{B+} = +12V	-	425	550	mW
Off Hook IB+	R_L = 600Ω, I_{LONG}* = 0, T_A = -40°C	-	-	6.0	mA
Off Hook IB+	R_L = 600Ω, I_{LONG}* = 0, T_A = +25°C	-	-	5.3	mA
Off Hook IB-	R_L = 600Ω, I_{LONG}* = 0	-	35	41	mA
Off Hook Loop Current	R_L = 1200Ω, I_{LONG}* = 0	-	21	-	mA
Off Hook Loop Current	R_L = 1200Ω, V_{B-} = -42V, I_{LONG}* = 0 T_A = +25°C	17.5	-	-	mA
Off Hook Loop Current	R_L = 200Ω, I_{LONG}* = 0	36	41	48	mA
Fault Currents					
TIP to Ground		-	14	-	mA
RING to Ground		-	55	-	mA
TIP to RING		-	41	-	mA
TIP and RING to Ground		-	55	-	mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	V_{RD} = +12V, $\overline{RC}$ = 1 = HIGH, T_A = +25°C	-	-	100	µA
Ring Trip Detection Period	R_L = 600Ω	-	2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD}$ = V_{OL}	10	-	-	mA
	$\overline{SHD}$ = V_{OH}	-	-	5	mA
Ground Key Detection Threshold	$\overline{GKD}$ = V_{OL}	20	-	-	mA
	$\overline{GKD}$ = V_{OH}	-	-	10	mA
Loop Current During Power Denial	R_L = 200Ω	-	±2	-	mA
Dial Pulse Distortion		0	-	5	ms
Receive Input Impedance	(Note 2)	-	110	-	kΩ
Transmit Output Impedance	(Note 2)	-	10	20	Ω
Two Wire Return Loss	(Referenced to 600Ω + 2.16µF), (Note 2)				
SR_L LO		-	15.5	-	dB
ER_L		-	24	-	dB
SR_L HI		-	31	-	dB
Longitudinal Balance	$1V_{RMS}$ 200Hz - 3400Hz, (Note 2) IEEE Method				
2 Wire Off Hook	0°C ≤ T_A ≤ +75°C	58	65	-	dB
2 Wire On Hook		60	63	-	dB
4 Wire Off Hook		50	58	-	dB

Electrical Specifications Unless Otherwise Specified, V_B- = -48V, V_B+ = +12V and +5V, AG = BG = DG = 0V, Typical Parameters T_A = +25°C. Min-Max Parameters are Over Operating Temperature Range. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Low Frequency Longitudinal Balance	R.E.A. Method, (Note 2), R_L = 600Ω	-	-	23	dBrnC
	0°C ≤ T_A ≤ +75°C	-	-	-67	dBm0p
Insertion Loss	at 1kHz, 0dBm Input Level, Referenced 600Ω				
2 Wire - 4 Wire, 4 Wire - 2 Wire		-	±0.05	±0.2	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 2)	-	±0.02	±0.05	dB
Idle Channel Noise	(Note 2)				
2 Wire - 4 Wire, 4 Wire - 2 Wire		-	1	5	dBrnC
		-	-89	-85	dBm0p
Absolute Delay	(Note 2)				
2 Wire - 4 Wire, 4 Wire - 2 Wire		-	-	2	ms
Trans Hybrid Loss	Balance Network Set Up for 600Ω Termination at 1kHz	36	40	-	dB
Overload Level	V_B+ = +5V	1.5	-	-	Vpeak
2 Wire - 4 Wire, 4 Wire - 2 Wire	V_B+ = +12V	1.75	-	-	Vpeak
Level Linearity	At 1kHz, (Note 2) Referenced to 0dBm Level				
2 Wire - 4 Wire, 4 Wire - 2 Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
Power Supply Rejection Ratio	(Note 2)				
V_B+ to 2 Wire	30 - 60Hz, R_L = 600Ω	15	-	-	dB
V_B+ to Transmit		15	-	-	dB
V_B- to 2 Wire		15	-	-	dB
V_B- to Transmit		15	-	-	dB
V_B+ to 2 Wire	200 - 16kHz, R_L = 600Ω	30	-	-	dB
V_B+ to Transmit		30	-	-	dB
V_B- to 2 Wire		30	-	-	dB
V_B- to Transmit		30	-	-	dB
Logic Input Current (RS, $\overline{RC}$, $\overline{PD}$)	0V ≤ V_{IN} ≤ + 5V	-	-	±100	µA
Logic Inputs					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} 800µA, V_B+ = +12V, +5V	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} 80µA, V_B+ = +12V	2.7	5.0	5.5	V
	I_{LOAD} 40µA, V_B+ = +5V	2.7	-	5.0	V

* I_{LONG} = Longitudinal Current

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Uncommitted Op Amp Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Input Bias Current		-	20	-	nA
Differential Input Resistance	(Note 2)	-	1	-	MΩ
Output Voltage Swing	R_L = 10K, V_{B+} = +12V	-	±5	-	Vpeak
	R_L = 10K, V_{B+} = +5V	-	±3	-	Vpeak
Output Resistance	A_{VCL} = 1 (Note 2)	-	10	-	Ω
Small Signal GBW	(Note 2)	-	1	-	MHz

Pin Descriptions

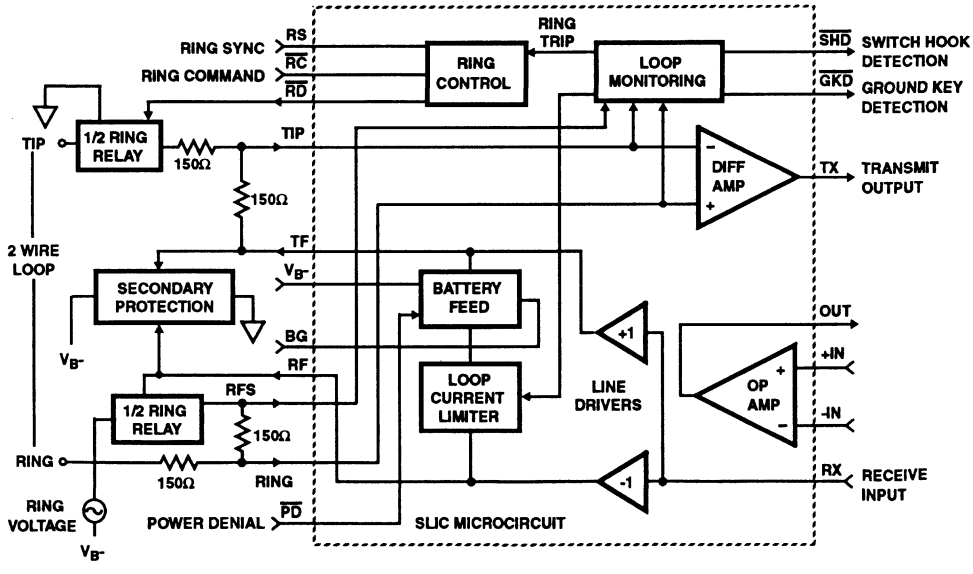
28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
2	1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring purposes.
3	2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
4	3	RFS	Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.
5	4	V_{B+}	Positive Voltage Source - Most positive supply. V_{B+} is typically 12V or 5V.
6	5	C3	Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V_{B-}. Typical value is 0.3µF, 30V.
7	6	DG	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
9	7	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock should be arranged such that a positive pulse transition occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring relay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5V.
10	8	$\overline{RD}$	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
11	9	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
12	10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
13	11	V_{B-}	Negative Voltage Source - Most negative supply. V_{B-} is typically -48V with an operational range of -42V to -58V. Frequently referred to as "battery".
14	12	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
16	13	$\overline{SHD}$	Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
17	14	$\overline{GKD}$	Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.
18	15	$\overline{PD}$	Power Denial - A low active TTL - Compatible logic input. When enabled, the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.

Pin Descriptions (Continued)

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
19	16	$\overline{RC}$	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off- hook ($\overline{SHD}$ = 0).
20	17	C2	Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15µF, 10V. This capacitor is not used if ground key function is not required and (Pin 17) may be left open or connected to digital ground.
21	18	OUT	The analog output of the spare operational amplifier. The output voltage swing is typically ±5V.
23	19	-IN	The inverting analog input of the spare operational amplifier.
24	20	+IN	The non-inverting analog input of the spare operational amplifier.
25	21	RX	Receive Input, Four Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed terminals, which in turn drive tip and ring through 300Ω of feed resistance on each side of the line.
26	22	C4	Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near by power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5µF, to 1.0µF, 20V. This capacitor should be nonpolarized.
27	23	AG	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
28	24	TX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
1,8,15,22		NC	No Internal Connection.

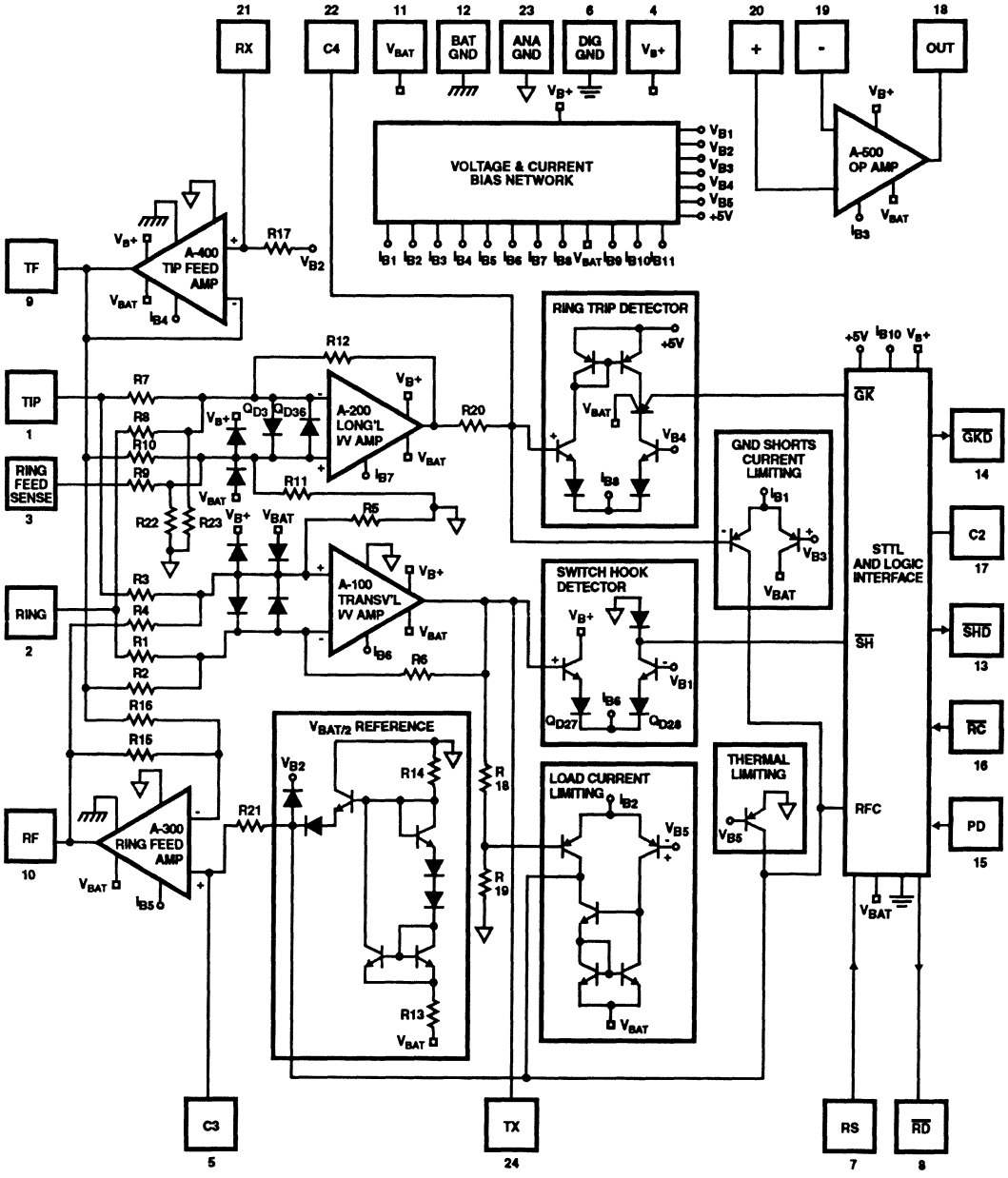
NOTE: All grounds (AG, BG, & DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Functional Diagram



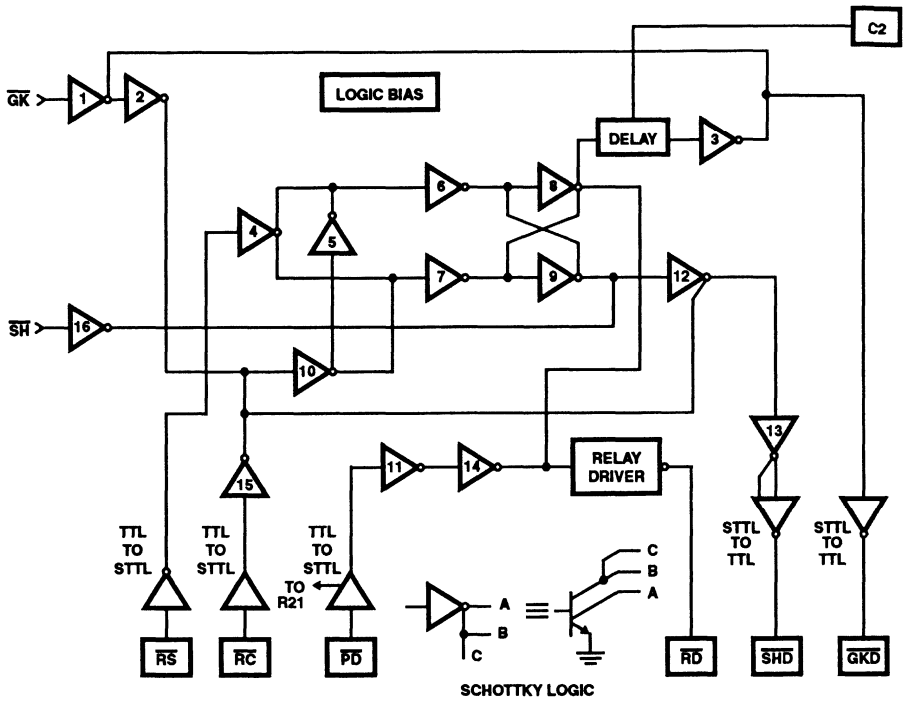
Schematic

SLIC FUNCTIONAL SCHEMATIC
(DIP/SOIC PIN NUMBERS SHOWN)



Schematic (Continued)

LOGIC GATE SCHEMATIC



Die Characteristics

Transistor Count 185
Diode Count 36
Die Dimensions ..... 137 x 102
Substrate Potential ..... Connected
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	52	15
Plastic DIP	52	22
PLCC	67	29
SOIC	76	29

Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or 30mArms, 15mArms per leg, without any performance degradation.

TABLE 1

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
50/60Hz Current T/GND R/GND	11 Cycles Limited to 10Arms	700 (Plastic)	V_{RMS}
		350 (Ceramic)	V_{RMS}

Applications Diagram

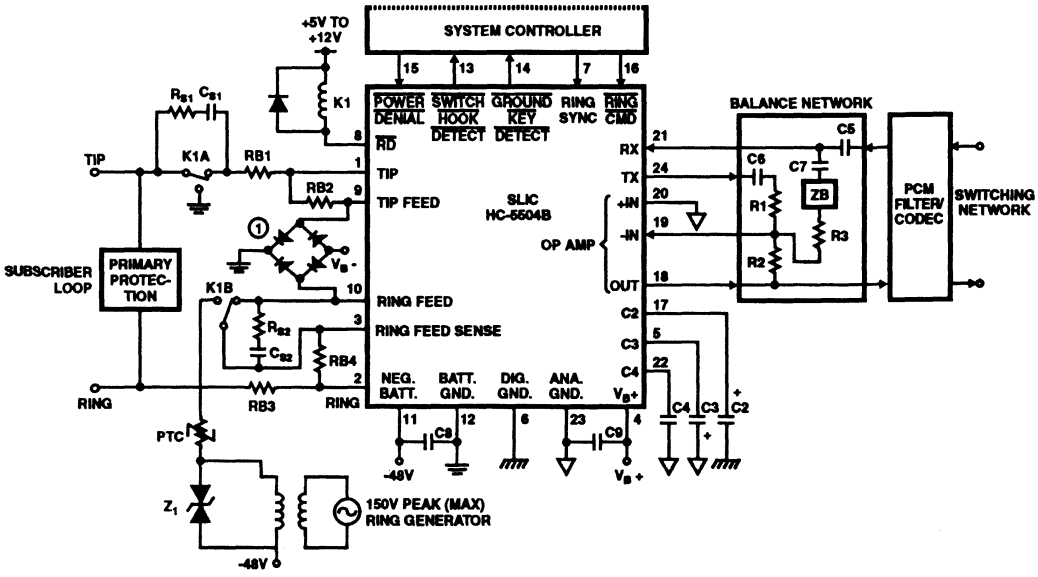


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values

C2 = 0.15µF, 10V

C3 = 0.3µF, 30V

C4 = 0.5µF to 1.0µF, 10%, 20V (Should be nonpolarized)

C5 = 0.5µF, 20V

C6 = C7 = 0.5µF (10% Match Required) (Note 2)

C8 = 0.01µF, 100V

C9 = 0.01µF, 20V, ±20%

R1 = R2 = R3 = 100k (0.1% Match Required, 1% absolute value) ZB = 0 for 600Ω Terminations (Note 2)

$RB_1 = RB_2 = RB_3 = RB_4 = 150\Omega$ (0.1% Match Required, 1% absolute value)

$R_{S1} = R_{S2} = 1k\Omega$, typically.

$C_{S1} = C_{S2} = 0.1\mu F$, 200V typically, depending on V_{RING} and line length.

Z_1 = 150V to 200V transient protection.

PTC used as ring generator ballast.

NOTES:

1. Secondary protection diode bridge recommended is a 2A, 200V type.
2. To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 are 1µF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -22V step when the loop is closed. Too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

   A 0.5µF and 100kΩ gives a time constant of 50msec. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.
3. All grounds (AG, BG, & DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first
4. Application shows Ring Injected Ringing, Balanced or Tip injected configuration may be used.
5. Pin numbers given for DIP/SOIC package.

Additional information is contained in Application Note 549, "The HC-550X Telephone SLICs" By Geoff Phillips

HARRIS SEMICONDUCTOR

HC-5504DLC

SLIC
Subscriber Line Interface Circuit

March 1993

Features

- Pin for Pin Replacement for the HC-5504
- Capable of +5V or +12V (V_{B+}) Operation
- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (41mA)
- Internal Ring Relay Driver
- Allows Interfacing With Negative Superimposed Ringing Systems
- Low Power Consumption During Standby
- Switch Hook Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBXs
- Allows Multi-Phone Operation

Description

The Harris SLIC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Harris dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

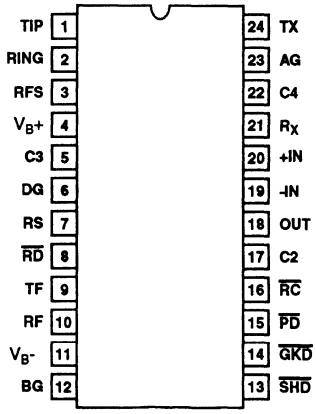
The Harris SLIC is ideally suited for the design of new digital PBX systems by eliminating bulky hybrid transformers.

Ordering Information

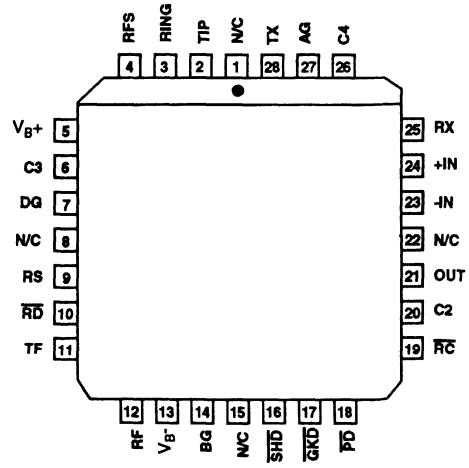
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HC1-5504DLC-5	0° to +75°C	24 Lead Ceramic DIP
HC1-5504DLC-9	-40° to +85°C	24 Lead Ceramic DIP
HC3-5504DLC-5	0° to +75°C	24 Lead Plastic DIP
HC3-5504DLC-9	-40° to +85°C	24 Lead Plastic DIP
HC4P5504DLC-5	0° to +75°C	28 Lead PLCC
HC4P5504DLC-9	-40° to +85°C	28 Lead PLCC
HC9P5504DLC-5	0° to +75°C	24 Lead SOIC
HC9P5504DLC-9	-40° to +85°C	24 Lead SOIC

Pinouts

HC-5504DLC (PDIP, CDIP, SOIC)
TOP VIEW



HC-5504DLC (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2443.2**

Absolute Maximum Ratings (Note 1)

Maximum Continuous Supply Voltages
- (V_{B-}) ..... -60 to +0.5 V
- (V_{B+}) ..... -0.5 to +15 V
- (V_{B+} - V_{B-}) ..... +75V

Relay Drive Voltage (V_{RD}) ..... -0.5 to +15V
Junction Temperature Ceramic ..... +175°C
Junction Temperature Plastic ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
- HC-5504DLC-5 ..... 0°C to +75°C
- HC-5504DLC-9 ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to 150°C
Relay Driver Voltage (V_{RD}) ..... +5 to +12V
Positive Supply Voltage (V_{B+}) ..... 4.75 to 5.25 or 10.8 to 13.2V
Negative Supply Voltage (V_{B-}) ..... -42 to -58V
High Level Logic Input Voltage 2.4V
Low Level Logic Input Voltage 0.6V
Loop Resistance (R_L) ..... 200 to 1200Ω

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Unless Otherwise Specified, V_{B-} = -48V, V_{B+} = +12V and +5V, AG = BG = DG = 0V, Typical Parameters T_A = +25°C. Min-Max Parameters are Over Operating Temperature Range.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I_{LONG}* = 0, V_{B+} = +12V	-	170	235	mW
Off Hook Power Dissipation	R_L = 600Ω, I_{LONG}* = 0, V_{B+} = +12V	-	425	550	mW
Off Hook IB+	R_L = 600Ω, I_{LONG}* = 0, T_A = -40°C	-	-	6.0	mA
Off Hook IB+	R_L = 600Ω, I_{LONG}* = 0, T_A = +25°C	-	-	5.3	mA
Off Hook IB-	R_L = 600Ω, I_{LONG}* = 0	-	35	41	mA
Off Hook Loop Current	R_L = 1200Ω, I_{LONG}* = 0	-	21	-	mA
Off Hook Loop Current	R_L = 1200Ω, V_{B-} = -42V, I_{LONG}* = 0 T_A = +25°C	17.5	-	-	mA
Off Hook Loop Current	R_L = 200Ω, I_{LONG}* = 0	36	41	48	mA
Fault Currents					
TIP to Ground		-	14	-	mA
RING to Ground		-	55	-	mA
TIP to RING		-	41	-	mA
TIP and RING to Ground		-	55	-	mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	V_{RD} = +12V, $\overline{RC}$ = 1 = HIGH, T_A = +25°C	-	-	100	µA
Ring Trip Detection Period	R_L = 600Ω	-	2	3	Ring Cycles
On Hook Ringing Current		-	-	30	mApk
Switch Hook Detection Threshold	$\overline{SHD}$ = V_{OL}	18	-	-	mA
	$\overline{SHD}$ = V_{OH}	-	-	12	mA
Ground Key Detection Threshold	$\overline{GKD}$ = V_{OL}	20	-	-	mA
	$\overline{GKD}$ = V_{OH}	-	-	10	mA
Loop Current During Power Denial	R_L = 200Ω	-	±2	-	mA
Dial Pulse Distortion		0	-	5	ms
Receive Input Impedance	(Note 2)	-	110	-	kΩ
Transmit Output Impedance	(Note 2)	-	10	20	Ω
Two Wire Return Loss	(Referenced to 600Ω + 2.16µF), (Note 2)				
SR_L LO		-	15.5	-	dB
ER_L		-	24	-	dB
SR_L HI		-	31	-	dB
Longitudinal Balance	$1V_{RMS}$ 200Hz - 3400Hz, (Note 2) IEEE Method				
2 Wire Off Hook		58	65	-	dB
2 Wire On Hook		60	63	-	dB
4 Wire Off Hook	0°C ≤ T_A ≤ +75°C	50	58	-	dB

Electrical Specifications Unless Otherwise Specified, V_B- = -48V, V_B+ = +12V and +5V, AG = BG = DG = 0V, Typical Parameters T_A = +25°C. Min-Max Parameters are Over Operating Temperature Range. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Low Frequency Longitudinal Balance	R.E.A. Method, (Note 2), R_L = 600Ω	-	-	23	dBrnC
	0°C ≤ T_A ≤ +75°C	-	-	-67	dBm0p
Insertion Loss	at 1kHz, 0dBm Input Level, Referenced 600Ω				
2 Wire - 4 Wire, 4 Wire - 2 Wire		-	±0.05	±0.2	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 2)	-	±0.02	±0.05	dB
Idle Channel Noise	(Note 2)				
2 Wire - 4 Wire, 4 Wire - 2 Wire		-	1	5	dBrnC
		-	-89	-85	dBm0p
Absolute Delay	(Note 2)				
2 Wire - 4 Wire, 4 Wire - 2 Wire		-	-	2	ms
Trans Hybrid Loss	Balance Network Set Up for 600Ω Termination at 1kHz	36	40	-	dB
Overload Level	V_B+ = +5V	1.5	-	-	Vpeak
2 Wire - 4 Wire, 4 Wire - 2 Wire	V_B+ = +12V	1.75	-	-	Vpeak
Level Linearity	At 1kHz, (Note 2) Referenced to 0dBm Level				
2 Wire - 4 Wire, 4 Wire - 2 Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
Power Supply Rejection Ratio	(Note 2)				
V_B+ to 2 Wire	30 - 60Hz, R_L = 600Ω	15	-	-	dB
V_B+ to Transmit		15	-	-	dB
V_B- to 2 Wire		15	-	-	dB
V_B- to Transmit		15	-	-	dB
V_B+ to 2 Wire	200 - 16kHz R_L = 600Ω	30	-	-	dB
V_B+ to Transmit		30	-	-	dB
V_B- to 2 Wire		30	-	-	dB
V_B- to Transmit		30	-	-	dB
Logic Input Current (RS, $\overline{RC}$, $\overline{PD}$)	0V ≤ V_{IN} ≤ + 5V	-	-	±100	µA
Logic Inputs					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} 800µA, V_B+ = +12V, +5V	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} 80µA, V_B+ = +12V	2.7	5.0	5.5	V
	I_{LOAD} 40µA, V_B+ = +5V	2.7	-	5.0	V

* I_{LONG} = Longitudinal Current

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Uncommitted Op Amp Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Input Bias Current		-	20	-	nA
Differential Input Resistance	(Note 2)	-	1	-	MΩ
Output Voltage Swing	R_L = 10K, V_B+ = +12V	-	±5	-	V_{PEAK}
	R_L = 10K, V_B+ = +5V	-	±3	-	V_{PEAK}
Output Resistance	A_{VCL} = 1 (Note 2)	-	10	-	Ω
Small Signal GBW	(Note 2)	-	1	-	MHz

Pin Descriptions

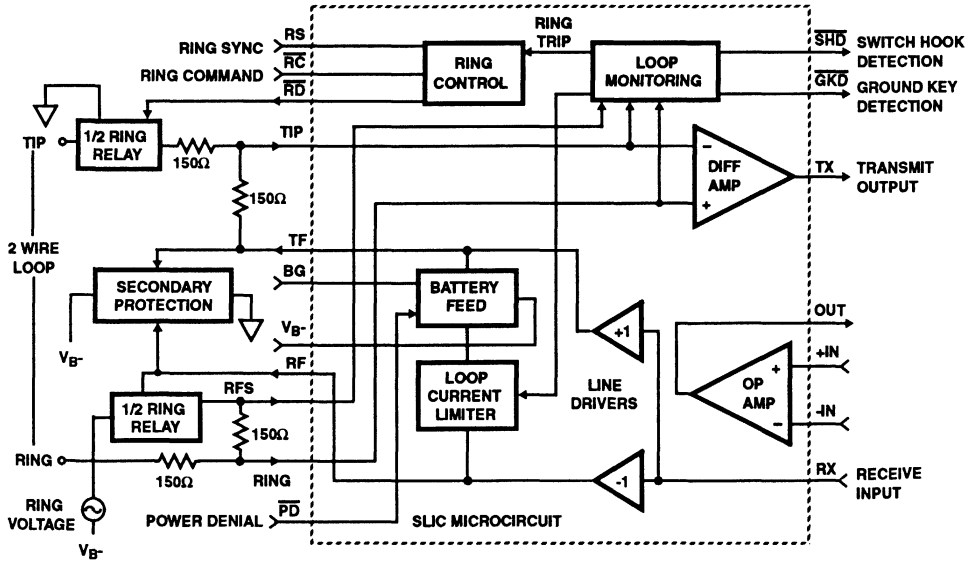
28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
2	1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring purposes.
3	2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
4	3	RFS	Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.
5	4	V_B+	Positive Voltage Source - Most positive supply. V_B+ is typically 12V or 5V.
6	5	C3	Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V_B-. Typical value is 0.3µF, 30V.
7	6	DG	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
9	7	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock should be arranged such that a positive pulse transition occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring relay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5V.
10	8	$\overline{RD}$	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
11	9	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
12	10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
13	11	V_B-	Negative Voltage Source - Most negative supply. V_B- is typically -48V with an operational range of -42V to -58V. Frequently referred to as "battery".
14	12	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
16	13	$\overline{SHD}$	Switch Hook Detection - A low active LS TTL - compatible logic output.
17	14	$\overline{GKD}$	Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is below an internally set threshold.
18	15	$\overline{PD}$	Power Denial - A low active TTL - Compatible logic input. When enabled, the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.
19	16	$\overline{RC}$	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off- hook ($\overline{SHD}$ = 0).

Pin Descriptions (Continued)

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
20	17	C2	Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15µF, 10V. This capacitor is not used if ground key function is not required and (Pin 17) may be left open or connected to digital ground.
21	18	OUT	The analog output of the spare operational amplifier. The output voltage swing is typically ±5V.
23	19	-IN	The inverting analog input of the spare operational amplifier.
24	20	+IN	The non-inverting analog input of the spare operational amplifier.
25	21	RX	Receive Input, Four Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed terminals, which in turn drive tip and ring through 300Ω of feed resistance on each side of the line.
26	22	C4	Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near by power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5µF, to 1.0µF, 20V. This capacitor should be nonpolarized.
27	23	AG	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
28	24	TX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
1,8,15,22		NC	No Internal Connection.

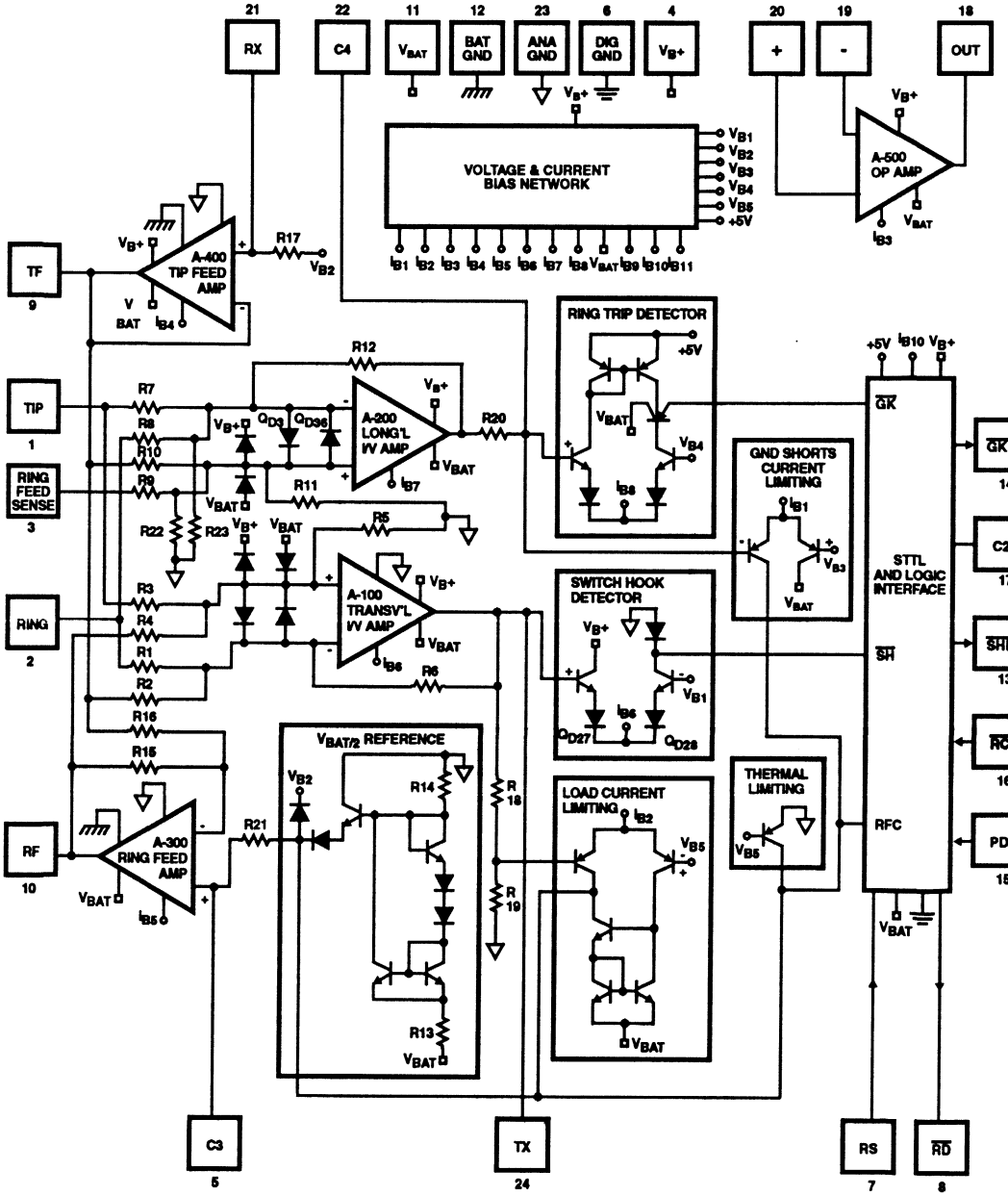
NOTE: All grounds (AG, BG, & DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Functional Diagram



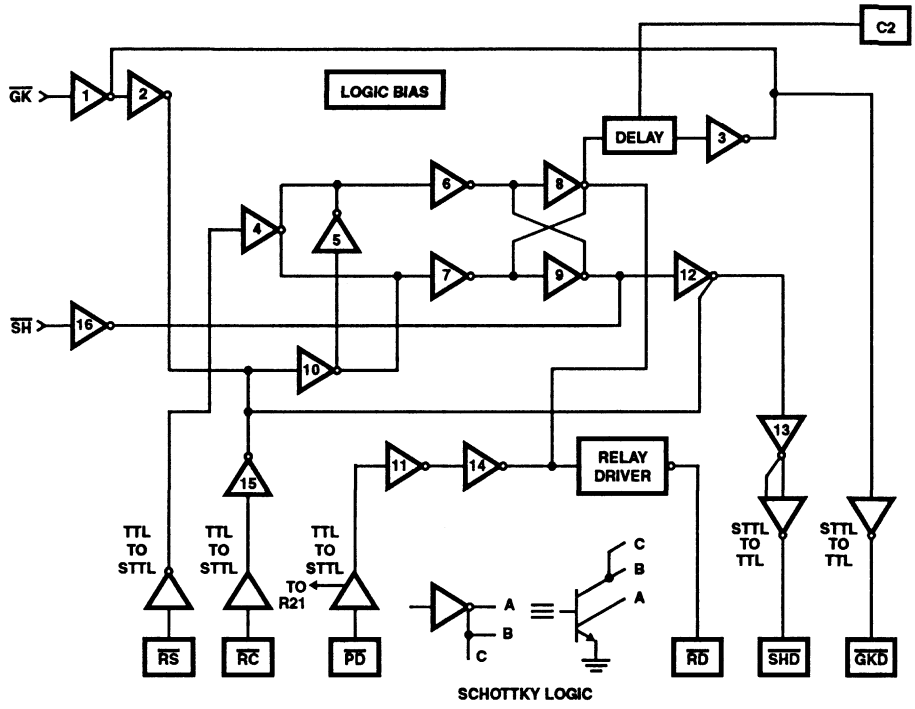
Schematic

SLIC FUNCTIONAL SCHEMATIC
(DIP/SOIC PIN NUMBERS SHOWN)



Schematic (Continued)

LOGIC GATE SCHEMATIC



Die Characteristics

Transistor Count		185
Diode Count		36
Die Dimensions		137 x 102
Substrate Potential		Connected
Process		Bipolar-DI
Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	52	15
Plastic DIP	52	22
PLCC	67	29
SOIC	76	24

Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or 30mArms, 15mArms per leg, without any performance degradation.

TABLE 1

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/	±1000 (Plastic)	V_{PEAK}
	1000µs/Fall	±500 (Ceramic)	V_{PEAK}
Metallic Surge	10µs Rise/	±1000 (Plastic)	V_{PEAK}
	1000µ Fall	±500 (Ceramic)	V_{PEAK}
T/GND	10µs Rise/	±1000 (Plastic)	V_{PEAK}
R/GND	1000µs Fall	±500 (Ceramic)	V_{PEAK}
50/60Hz Current			
T/GND	11 Cycles	700 (Plastic)	V_{RMS}
R/GND	Limited to 10Arms	350 (Ceramic)	V_{RMS}

Applications Diagram

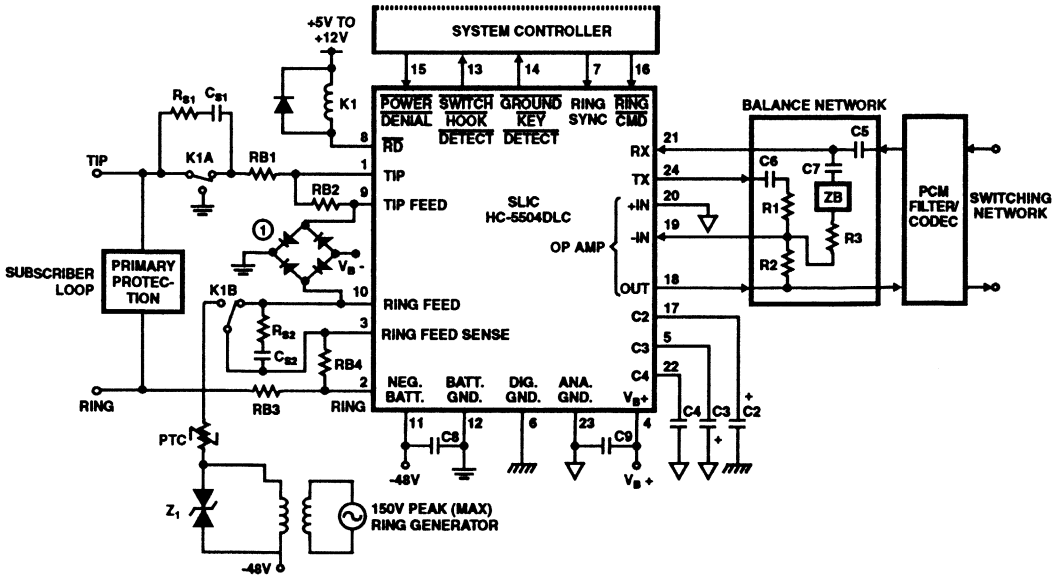


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values

C2 = 0.15µF, 10V

C3 = 0.3µF, 30V

C4 = 0.5µF to 1.0µF, 10%, 20V (Should be nonpolarized)

C5 = 0.5µF, 20V

C6 = C7 = 0.5µF (10% Match Required) (Note 2)

C8 = 0.01µF, 100V

C9 = 0.01µF, 20V, ±20%

R1 = R2 = R3 = 100k (0.1% Match Required, 1% absolute value) ZB = 0 for 600Ω Terminations (Note 2)

$RB_1 = RB_2 = RB_3 = RB_4 = 150\Omega$ (0.1% Match Required, 1% absolute value)

$R_{S1} = R_{S2} = 1k\Omega$, typically.

$C_{S1} = C_{S2} = 0.1\mu F$, 200V typically, depending on V_{RING} and line length.

Z_1 = 150V to 200V transient protection.

PTC used as ring generator ballast.

NOTES:

1. Secondary protection diode bridge recommended is a 2A, 200V type.
2. To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 are 1µF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -22V step when the loop is closed. Too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

   A 0.5µF and 100kΩ gives a time constant of 50msec. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.
3. All grounds (AG, BG, & DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
4. To prevent saturation of longitudinal amplifier during ringing, the ringer current should be limited to less than 30mA peak.
5. Application shows Ring injected ringing, a Balanced or Tip injected configuration may be used.
6. Pin numbers given for DIP/SOIC package.

   Additional information is contained in Application Note 549, "The HC-550X Telephone SLICs" By Geoff Phillips

HARRIS SEMICONDUCTOR

HC-5509A1

PRELIMINARY

March 1993

SLIC
Subscriber Line Interface Circuit

Features

- DI Monolithic High Voltage Process
- Compatible with Worldwide PBX and CO Performance Requirements
- Controlled Supply of Battery Feed Current with Programmable Current Limit
- Operates with 5V Positive Supply (V_{B+})
- Internal Ring Relay Driver and a Utility Relay Driver
- High Impedance Mode for Subscriber Loop
- High Temperature Alarm Output
- Low Power Consumption During Standby Functions
- Switch Hook, Ground Key, and Ring Trip Detection
- Selective Power Denial to Subscriber
- Voice Path Active During Power Denial
- On Chip Op-Amp for 2 Wire Impedance Matching

Applications

- Solid State Line Interface Circuit for PBX or Central Office Systems, Digital Loop Carrier Systems
- Hotel/Motel Switching Systems
- Direct Inward Dialing (DID) Trunks
- Voice Messaging PBX's
- High Voltage 2W/4W, 4W/2W Hybrid

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HC1-5509A1-5	0° to +75°C	28 Lead Ceramic DIP
HC1-5509A1-9	-40° to +85°C	28 Lead Ceramic DIP
HC3-5509A1-5	0° to +75°C	28 Lead Plastic DIP
HC3-5509A1-9	-40° to +85°C	28 Lead Plastic DIP
HC4P5509A1-5	0° to +75°C	44 Lead PLCC
HC4P5509A1-9	-40° to +85°C	44 Lead PLCC
HC9P5509A1-5	0° to +75°C	28 Lead SOIC
HC9P5509A1-9	-40° to +85°C	28 Lead SOIC

Description

The HC-5509A1 telephone Subscriber Line Interface Circuit integrates most of the BORSCHT functions on a monolithic IC. The device is manufactured in a Dielectric Isolation (DI) process and is designed for use as a high voltage interface between the traditional telephone subscriber pair (Tip and Ring) and the low voltage filtering and coding/decoding functions of the line card. Together with a secondary protection diode bridge and "feed" resistors, the device will withstand 1000V lightning induced surges, in plastic packages. The SLIC also maintains specified transmission performance in the presence of externally induced longitudinal currents. The BORSCHT functions that the SLIC provides are:

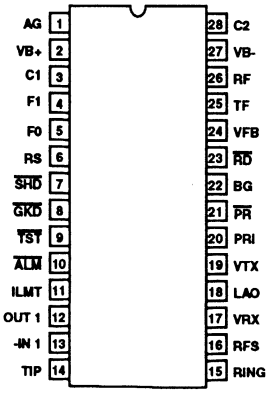
- Battery Feed with Subscriber Loop Current Limiting
- Overvoltage Protection
- Ring Relay Driver
- Supervisory Signaling Functions
- Hybrid Functions (with External Op-Amp)
- Test (or Battery Reversal) Relay Driver

In addition, the SLIC provides selective denial of power to subscriber loops, a programmable subscriber loop current limit from 20 to 60mA, a thermal shutdown with an alarm output and line fault protection. Switch hook detection, ring trip detection and ground key detection functions are also incorporated in the SLIC device.

The HC-5509A1 SLIC is ideally suited for line card designs in PBX and CO systems, replacing traditional transformer solutions.

Pinouts

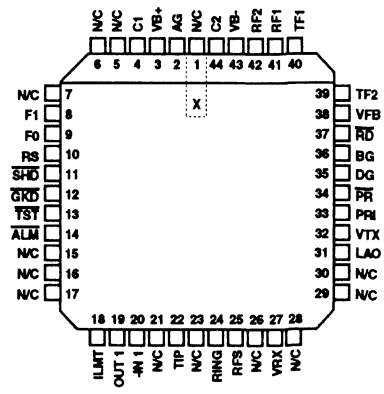
HC-5509A1 (PDIP, CDIP, SOIC)
TOP VIEW



TRUTH TABLE

F1	F0	ACTION
0	0	Normal Loop Feed
0	1	$\overline{RD}$ Active
1	0	Power Down Latch RESET
1	0	Power on RESET
1	1	Loop Power Denial Active

HC-5509A1 (PLCC)
TOP VIEW



File Number **3567**

Absolute Maximum Ratings (Note 1)

Relay Drivers ..... -0.5V to +15V
Maximum Supply Voltages
(V_{B+}) ..... -0.5V to +7V
(V_{B+})-(V_{B-}) ..... +75V
Junction Temperature Ceramic ..... +175°C
Junction Temperature Plastic ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HC-5509A1-5 ..... 0°C to +75°C
HC-5509A1-9 ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Relay Drivers ..... +5V to +12V
Positive Power Supply (V_{B+}) ..... +5V ±5%
Negative Power Supply (V_{B-}) ..... -42V to -58V
Loop Resistance (R_L) ..... 200Ω to 1750Ω (Note 2)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Unless Otherwise Specified, Typical Parameters are at T_A = +25°C, Min-Max Parameters are over Operating Temperature Range, V_{B-} = -48V, V_{B+} = +5V, AG = DG = BG = 0V. All A.C. Parameters are specified at 600Ω 2-Wire terminating impedance.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
A.C. TRANSMISSION PARAMETERS					
RX Input Impedance	300Hz to 3.4kHz (Note 3)	-	100	-	kΩ
TX Output Impedance	300Hz to 3.4kHz (Note 3)	-	-	20	Ω
4W Input Overload Level	300Hz to 3.4kHz R_L = 1200Ω, 600Ω Reference	+1.5	-	-	V_{PEAK}
2W Return Loss	Matched for 600Ω (Note 3)				
SRL LO		26	35	-	dB
ERL		30	40	-	dB
SRL HI		30	40	-	dB
2W Longitudinal to Metallic Balance Off Hook	Per ANSI/IEEE STD 455-1976 (Note 3) 300Hz to 3400Hz	58	63	-	dB
4W Longitudinal Balance Off Hook	300Hz to 3400Hz (Note 3)	50	55	-	dB
Low Frequency Longitudinal Balance	R.E.A. Test Circuit	-	-	-67	dBmp
	I_{LINE} = 40mA T_A = +25°C (Note 3)	-	-	23	dBrnC
Longitudinal Current Capability	I_{LINE} = 40mA T_A = +25°C (Note 3)	-	-	30	mArms
Insertion Loss	0dBm at 1kHz, Referenced 600Ω				
2W/4W		-	±0.05	±0.2	dB
4W/2W		-	±0.05	±0.2	dB
4W/4W		-	-	±0.12	dB
Frequency Response	300Hz to 3400Hz (Note 3) Referenced to Absolute Level at 1kHz, 0dBm Referenced 600Ω	-	±0.02	±0.05	dB
Level Linearity	Referenced to -10dBm (Note 3)				
2W to 4W and 4W to 2W	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB

Electrical Specifications Unless Otherwise Specified, Typical Parameters are at T_A = +25°C, Min-Max Parameters are over Operating Temperature Range, V_{B-} = -48V, V_{B+} = +5V, AG = DG = BG = 0V. All A.C. Parameters are specified at 600Ω 2-Wire terminating impedance. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Delay	(Note 3)				
2W/4W	300Hz to 3400Hz	-	-	1	µs
4W/2W	300Hz to 3400Hz	-	-	1	µs
4W/4W	300Hz to 3400Hz	-	-	1.5	µs
Transhybrid Loss, THL	(Note 3) See Figure 1	-	40	-	dB
Total Harmonic Distortion 2W/4W, 4W/2W, 4W/4W	Reference Level 0dBm at 600Ω 300Hz to 3400Hz (Note 3)	-	-	-52	dB
Idle Channel Noise	(Note 3)				
2W and 4W	C-Message	-	-	5	dBrnC
	Psophometric	-	-	-85	dBmp
	3kHz Flat	-	-	15	dBrn
Power Supply Rejection Ratio	(Note 3) 30Hz to 200Hz, R_L = 600Ω				
V_{B+} to 2W		20	29	-	dB
V_{B+} to 4W		20	29	-	dB
V_{B-} to 2W		20	29	-	dB
V_{B-} to 4W		20	29	-	dB
V_{B+} to 4W	(Note 3) 200Hz to 16kHz, R_L = 600Ω	30	-	-	dB
V_{B-} to 2W		30	-	-	dB
V_{B-} to 4W		20	25	-	dB
V_{B-} to 4W		20	25	-	dB
Ring Sync Pulse Width		50	-	500	µs
D.C. PARAMETERS					
Loop Current Programming					
Limit Range		20	40	60	mA
Accuracy		10	-	-	%
Loop Current During Power Denial	R_L = 200Ω	-	±3	±5	mA
Fault Currents					
TIP to Ground		-	30	-	mA
RING to Ground		-	60	-	mA
TIP and RING to Ground		-	90	-	mA
Switch Hook Detection Threshold		-	12	15	mA
Ground Key Detection Threshold		8	12	16	mA
Thermal $\overline{\text{ALARM}}$ Output	Safe Operating Die Temperature Exceeded	140	-	160	°C

Electrical Specifications Unless Otherwise Specified, Typical Parameters are at T_A = +25°C, Min-Max Parameters are over Operating Temperature Range, V_{B-} = -48V, V_{B+} = +5V, AG = DG = BG = 0V. All A.C. Parameters are specified at 600Ω 2-Wire terminating impedance. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Ring Trip Comparator Threshold	See Typical Applications for more information	9.5	13.5	17.5	mA
Dial Pulse Distortion		-	0.1	0.5	ms
Relay Driver Outputs					
On Voltage V_{OL}	I_{OL} ($\overline{PR}$) = 60mA, I_{OL} ($\overline{RD}$) = 30mA	-	0.2	0.5	V
Off Leakage Current	V_{OH} = 13.2V	-	±10	±100	µA
TTL/CMOS Logic Inputs (F0, F1, RS, $\overline{TEST}$, PRI)					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Input Current (F0, F1, RS, $\overline{TEST}$, PRI)	0V ≤ V_{IN} ≤ 5V	-	-	±100	µA
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} = 800µA	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} = 40µA	2.7	-	-	V
Power Dissipation On Hook	Relay Drivers Off	-	200	-	mW
I_{B+}	V_{B+} = +5.25V, V_{B-} = -58V, R_{LOOP} = ∞	-	-	6	mA
I_{B-}	V_{B+} = +5.25V, V_{B-} = -58V, R_{LOOP} = ∞	-6	-	-	mA
UNCOMMITED OP AMP PARAMETERS					
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Differential Input Resistance	(Note 2)	-	1	-	MΩ
Output Voltage Swing	R_L = 10kΩ	-	±3	-	V_{P-P}
Small Signal GBW	(Note 2)	-	1	-	MHz

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. May Be Extended to 1900Ω With Application Circuit.
3. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Pin Descriptions

DIP/SOIC	PLCC	SYMBOL	DESCRIPTION
1	2	AG	Analog Ground - To be connected to zero potential. Serves as a reference for the transmit output and receive input terminals.
2	3	VB+	Positive Voltage Source - Most Positive Supply.
3	4	C1	Capacitor #C1 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function.
4	8	F1	Function Address #1 - A TTL and CMOS compatible input used with F0 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on page1. F1 should be toggled high after power is applied.
5	9	F0	Function Address #0 - A TTL and CMOS compatible input used with F1 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on page 1.
6	10	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive pulse (50 - 500µs) occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring delay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5.
7	11	$\overline{SHD}$	Switch Hook Detection - An active low LS TTL compatible logic output. A line supervisory output.
8	12	$\overline{GKD}$	Ground Key Detection - An active low LS TTL compatible logic output. A line supervisory output.
9	13	$\overline{TST}$	A TTL logic input. A low on this pin will set a latch and keep the SLIC in a power down mode until the proper F1, F0 state is set and will keep $\overline{ALM}$ low. See Truth Table on page 1.
10	14	$\overline{ALM}$	A LS TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded. When $\overline{TST}$ is forced low by an external control signal, $\overline{ALM}$ is latched low until the proper F1, F0 state and $\overline{TST}$ input is brought high. The $\overline{ALM}$ can be tied directly to the $\overline{TST}$ pin to power down the part when a thermal fault is detected and then reset with F0, F1. See Truth Table on page 1. It is possible to ignore transient thermal overload conditions in the SLIC by delaying the response to the $\overline{TST}$ pin from the $\overline{ALM}$. Care must be exercised in attempting this as continued thermal overstress may reduced component life.
11	18	ILMT	Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions using a resistive voltage divider.
12	19	OUT1	The analog output of the spare operational amplifier.
13	20	-IN1	The inverting analog input of the spare operational amplifier.
14	22	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor and ring relay contact. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purpose.
15	24	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.
16	25	RFS	Ring Feed Sense - Senses RING side of the loop for Ground Key Detection. During Ring injected ringing the ring signal at this node is isolated from RF via the ring relay. For Tip injected ringing, the RF and RFS pins must be shorted.
17	27	VRX	Receive Input, Four Wire Side - A high impedance analog input. AC signals appearing at this input drive the Tip Feed and Ring Feed amplifiers differentially.
18	31	LAO	Longitudinal Amplifier Output - A low impedance output to be connected to C2 through a low pass filter. Output is proportional to the difference in I_{TIP} and I_{RING}.

Pin Descriptions (Continued)

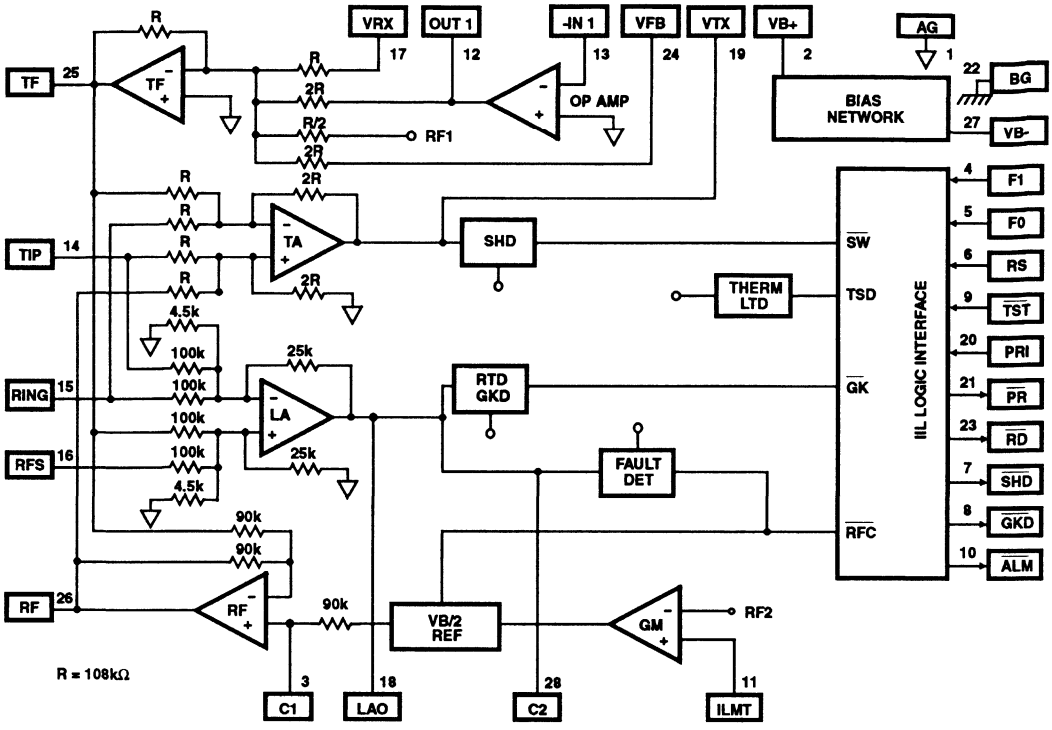
DIP/SOIC	PLCC	SYMBOL	DESCRIPTION
19	32	VTX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Transhybrid balancing must be performed beyond this output to completely implement two to four wire conversion. This output is referenced to analog ground. Since the D.C. level of this output varies with loop current, capacitive coupling to the next stage is necessary.
20	33	PRI	A TTL compatible input used to control $\overline{PR}$. PRI active High = $\overline{PR}$ active low.
21	34	$\overline{PR}$	An active low open collector output. Can be used to drive a Polarity Reversal Relay.
NA	35	DG	Digital Ground - To be connected to zero potential - serves as reference for all digital inputs and outputs on the SLIC.
22	36	BG	Battery Ground - Tube connected to zero potential. All loop current and some quiescent current flows into this terminal.
23	37	$\overline{RD}$	Ring Relay Driver - An active low open collector output. Used to drive a relay that switches ringing signals onto the 2-Wire line.
24	38	VFB	Feedback input to the tip feed amplifier; may be used in conjunction with transmit output signal and the spare op-amp to accommodate 2W line impedance matching.
25	39	TF2	Tip Feed - A low impedance analog output connected to the TIP terminal through a feed resistor. Functions with the RF terminal to provide loop current, and to feed voice signals to the telephone set and to sink longitudinal currents. Must be tied to TF1.
NA	40	TF1	Tie directly to TF2 in the PLCC application.
26	41	RF1	Ring Feed - A low impedance analog output connected to the RING terminal through a feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and to sink longitudinal currents. Tie directly to RF2.
NA	42	RF2	Tie directly to RF1 in the PLCC application.
27	43	VB-	The battery voltage source. The most negative supply.
28	44	C2	Capacitor #2 - An external capacitor to be connected between this terminal and ground. It prevents false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from power lines and other noise sources. This capacitor should be nonpolarized.
	1, 5, 6, 7, 15, 16, 17, 21, 23, 26, 28, 29, 30	NC	No internal connection.

NOTE:

1. All grounds (AG, BG, DG) must be applied before V_{B+} or V_{B-}. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Functional Diagram

DIP OR SOIC



Die Characteristics

Transistor Count 224
Diode Count 28
Die Dimensions ..... 174 x 120
Substrate Potential ..... Connected
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	48	12
Plastic DIP	51	21
PLCC	47	17
SOIC	72	22

Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

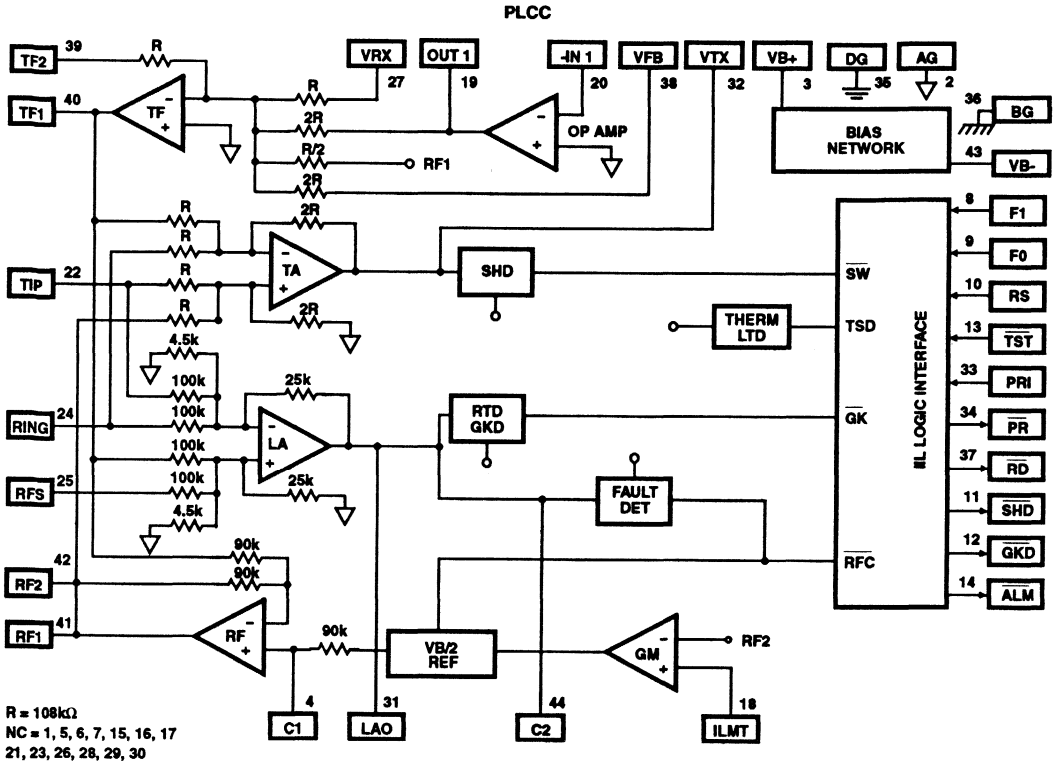
High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or 30mArms, 15mArms per leg, without any performance degradation

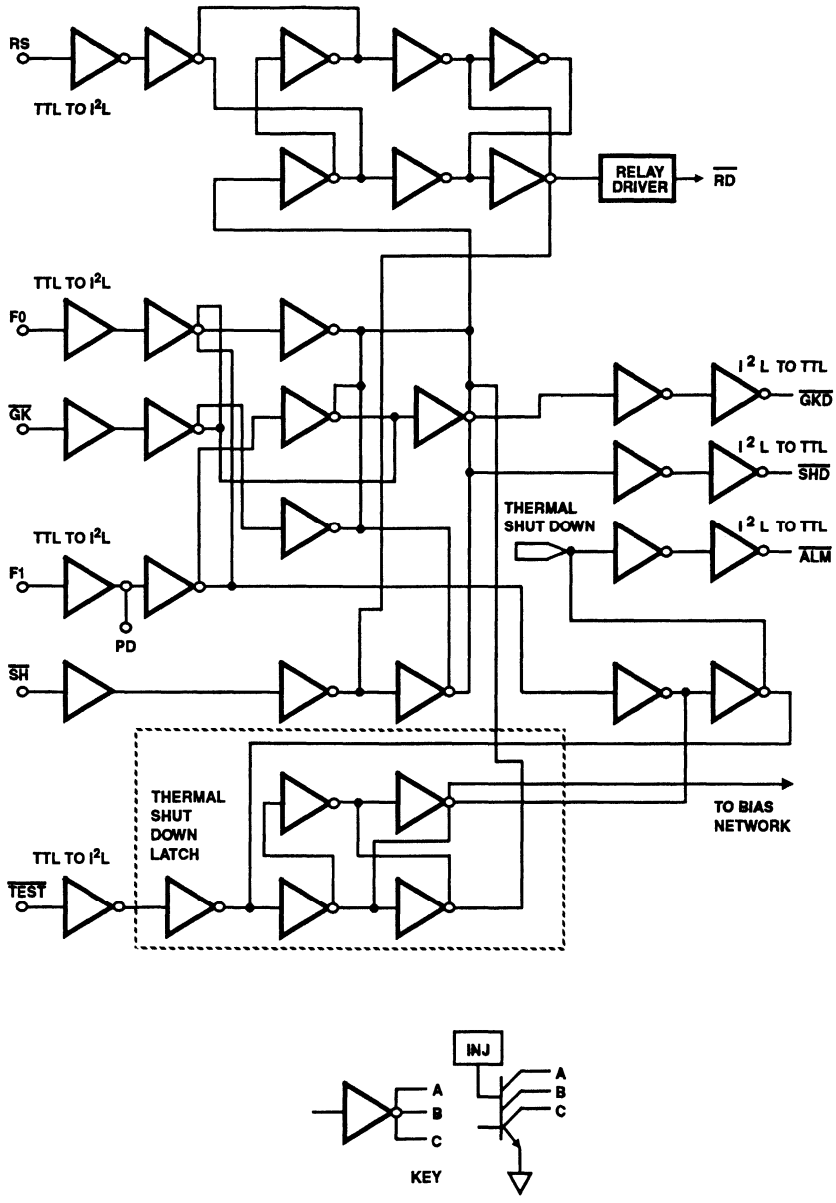
TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
50/60Hz Current T/GND R/GND	11 Cycles Limited to 10Arms	700 (Plastic)	V_{RMS}
		350 (Ceramic)	V_{RMS}

Functional Diagram (Continued)



Logic Diagram



NOTE: PRI is an independent switch driven by TTL input levels.

Applications Diagram

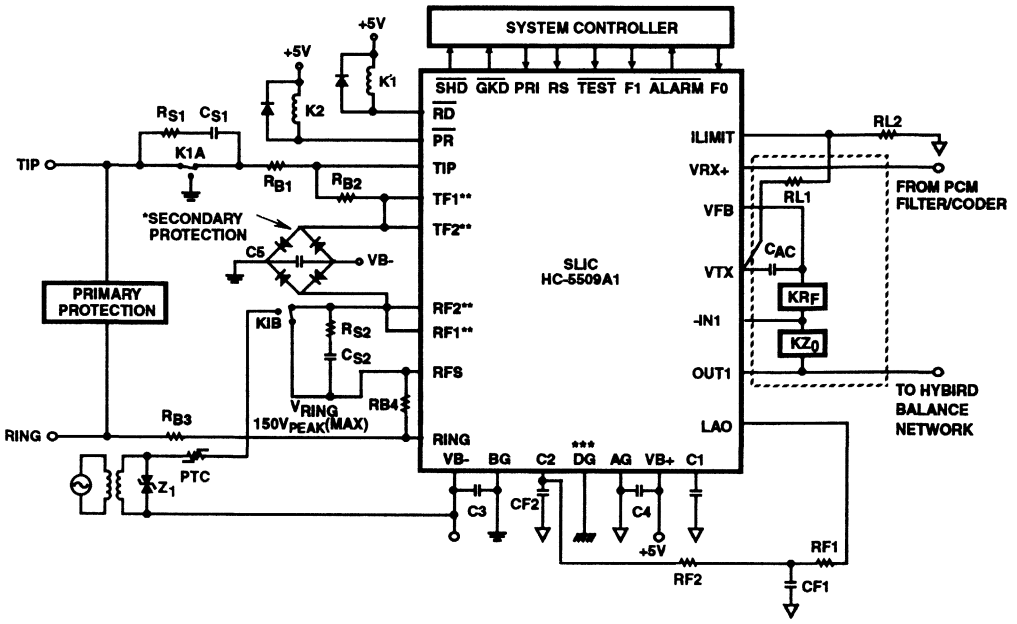


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

TYPICAL COMPONENT VALUES

C1 = 0.5µF, 30V

RF1 = RF2 = 210kΩ, 1%

CF1 = CF2 = 0.22µF, 10%, 20V Nonpolarized

C3 = 0.01µF, 100V, ±20%

C4 = 0.01µF, 100V, ±20%

C5 = 0.01µF, 100V, ±20%

C_{AC} = 0.5µF, 20V

KZ_0 = 60kΩ, (Z_0 = 600Ω, K = Scaling Factor = 100)

RL1, RL2; Current Limit Setting Resistors:

RL1 + RL2 > 90kΩ → offset

I_{LIMIT} = (0.6) (RL1 + RL2)/(200 x RL2), RL1 typically 100kΩ

KR_F = 20kΩ, RF = 2(R_{B2} + R_{B4}), K = Scaling Factor = 100)

RB_1 = RB_2 = RB_3 = RB_4 = 50Ω (1% absolute, matching requirements covered in a Tech Brief)

R_{S1} = R_{S2} = 1kΩ typically

CS1 = CS2 = 0.1µF, 200V typically, depending on V_{Ring} and line length.

Z_1 = 150V to 200V transient protector. PTC used as ring generator ballast.

* Secondary protection diode bridge recommended is 3A, 200V type.

**TF1, TF2 and RF1, RF2 are on PLCC only and should be connected together as shown.

***Not Present on DIP or SOIC packages.

NOTES:

1. All grounds (AG, BG, & DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
2. Application shows Ring Injected Ringing, a Balanced or Tip injected configuration may be used.

Additional information is contained in Application Note 549, "The HC-550X Telephone SLICs" By Geoff Phillips

HARRIS SEMICONDUCTOR

HC-5509B

SLIC
Subscriber Line Interface Circuit

March 1993

Features

- DI Monolithic High Voltage Process
- Compatible with Worldwide PBX and CO Performance Requirements
- Controlled Supply of Battery Feed Current with Programmable Current Limit
- Operates with 5V Positive Supply (V_{B+})
- Internal Ring Relay Driver and a Utility Relay Driver
- High Impedance Mode for Subscriber Loop
- High Temperature Alarm Output
- Low Power Consumption During Standby Functions
- Switch Hook, Ground Key, and Ring Trip Detection
- Selective Power Denial to Subscriber
- Voice Path Active During Power Denial
- On Chip Op-Amp for 2 Wire Impedance Matching

Applications

- Solid State Line Interface Circuit for PBX or Central Office Systems, Digital Loop Carrier Systems
- Hotel/Motel Switching Systems
- Direct Inward Dialing (DID) Trunks
- Voice Messaging PBX's
- High Voltage 2W/4W, 4W/2W Hybrid

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HC1-5509B-5	0° to +75°C	28 Lead Ceramic DIP
HC1-5509B-9	-40° to +85°C	28 Lead Ceramic DIP
HC3-5509B-5	0° to +75°C	28 Lead Plastic DIP
HC3-5509B-9	-40° to +85°C	28 Lead Plastic DIP
HC4P5509B-5	0° to +75°C	44 Lead PLCC
HC4P5509B-9	-40° to +85°C	44 Lead PLCC
HC9P5509B-5	0° to +75°C	28 Lead SOIC
HC9P5509B-9	-40° to +85°C	28 Lead SOIC

Description

The HC-5509B telephone Subscriber Line Interface Circuit integrates most of the BORSCHT functions on a monolithic IC. The device is manufactured in a Dielectric Isolation (DI) process and is designed for use as a high voltage interface between the traditional telephone subscriber pair (Tip and Ring) and the low voltage filtering and coding/decoding functions of the line card. Together with a secondary protection diode bridge and "feed" resistors, the device will withstand 1000V lightning induced surges, in plastic packages. The SLIC also maintains specified transmission performance in the presence of externally induced longitudinal currents. The BORSCHT functions that the SLIC provides are:

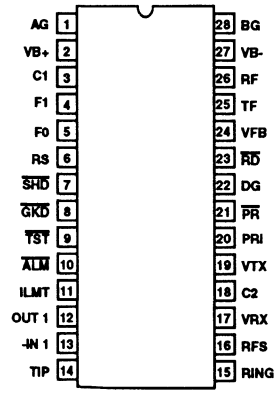
- Battery Feed with Subscriber Loop Current Limiting
- Overvoltage Protection
- Ring Relay Driver
- Supervisory Signaling Functions
- Hybrid Functions (with External Op-Amp)
- Test (or Battery Reversal) Relay Driver

In addition, the SLIC provides selective denial of power to subscriber loops, a programmable subscriber loop current limit from 20 to 60mA, a thermal shutdown with an alarm output and line fault protection. Switch hook detection, ring trip detection and ground key detection functions are also incorporated in the SLIC device.

The HC-5509B SLIC is ideally suited for line card designs in PBX and CO systems, replacing traditional transformer solutions.

Pinouts

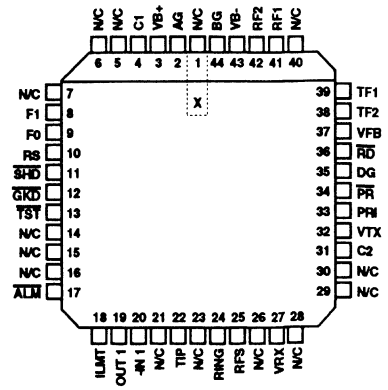
HC-5509B (PDIP, CDIP, SOIC)
TOP VIEW



TRUTH TABLE

F1	F0	ACTION
0	0	Normal Loop Feed
0	1	$\overline{RD}$ Active
1	0	Power Down Latch RESET
1	0	Power on RESET
1	1	Loop Power Denial Active

HC-5509B (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2799.2**

Absolute Maximum Ratings (Note 1)

Relay Drivers ..... -0.5V to +15V
Maximum Supply Voltages
(V_{B+}) ..... -0.5V to +7V
(V_{B+})-(V_{B-}) ..... +75V
Junction Temperature Ceramic ..... +175°C
Junction Temperature Plastic ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HC-5509B-5 ..... 0°C to +75°C
HC-5509B-9 ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Relay Drivers ..... +5V to +12V
Positive Power Supply (V_{B+}) ..... +5V ±5%
Negative Power Supply (V_{B-}) ..... -42V to -58V
Loop Resistance (R_L) ..... 200Ω to 1750Ω (Note 2)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Unless Otherwise Specified, Typical Parameters are at T_A = +25°C, Min-Max Parameters are over Operating Temperature Range, V_{B-} = -48V, V_{B+} = +5V, AG = DG = BG = 0V. All A.C. Parameters are specified at 600Ω 2-Wire terminating impedance.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
A.C. TRANSMISSION PARAMETERS					
RX Input Impedance	300Hz to 3.4kHz (Note 3)	-	100	-	kΩ
TX Output Impedance	300Hz to 3.4kHz (Note 3)	-	-	20	Ω
4W Input Overload Level	300Hz to 3.4kHz R_L = 1200Ω, 600Ω Reference	+1.5	-	-	V_{PEAK}
2W Return Loss	Matched for 600Ω (Note 3)				
SRL LO		26	35	-	dB
ERL		30	40	-	dB
SRL HI		30	40	-	dB
2W Longitudinal to Metallic Balance Off Hook	Per ANSI/IEEE STD 455-1976 (Note 3) 300Hz to 3400Hz	58	63	-	dB
4W Longitudinal Balance Off Hook	300Hz to 3400Hz (Note 3)	50	55	-	dB
Low Frequency Longitudinal Balance	R.E.A. Test Circuit	-	-	-67	dBmp
	I_{LINE} = 40mA T_A = +25°C (Note 3)	-	-	23	dBrnC
Longitudinal Current Capability	I_{LINE} = 40mA T_A = +25°C (Note 3)	-	-	30	mArms
Insertion Loss	0dBm at 1kHz, Referenced 600Ω				
2W/4W		-	±0.05	±0.2	dB
4W/2W		-	±0.05	±0.2	dB
4W/4W		-	-	±0.12	dB
Frequency Response	300Hz to 3400Hz (Note 3) Referenced to Absolute Level at 1kHz, 0dBm Referenced 600Ω	-	±0.02	±0.05	dB
Level Linearity	Referenced to -10dBm (Note 3)				
2W to 4W and 4W to 2W	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB

Electrical Specifications Unless Otherwise Specified, Typical Parameters are at T_A = +25°C, Min-Max Parameters are over Operating Temperature Range, V_{B-} = -48V, V_{B+} = +5V, AG = DG = BG = 0V. All A.C. Parameters are specified at 600Ω 2-Wire terminating impedance. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Delay	(Note 3)				
2W/4W	300Hz to 3400Hz	-	-	1	µs
4W/2W	300Hz to 3400Hz	-	-	1	µs
4W/4W	300Hz to 3400Hz	-	-	1.5	µs
Transhybrid Loss, THL	(Note 3) See Figure 1	-	40	-	dB
Total Harmonic Distortion 2W/4W, 4W/2W, 4W/4W	Reference Level 0dBm at 600Ω 300Hz to 3400Hz (Note 3)	-	-	-52	dB
Idle Channel Noise	(Note 3)				
2W and 4W	C-Message	-	-	5	dBrnC
	Psophometric	-	-	-85	dBmp
	3kHz Flat	-	-	15	dBrn
Power Supply Rejection Ratio	(Note 3) 30Hz to 200Hz, R_L = 600Ω				
V_{B+} to 2W		20	29	-	dB
V_{B+} to 4W		20	29	-	dB
V_{B-} to 2W		20	29	-	dB
V_{B-} to 4W		20	29	-	dB
V_{B+} to 4W	(Note 3) 200Hz to 16kHz, R_L = 600Ω	30	-	-	dB
V_{B-} to 2W		30	-	-	dB
V_{B-} to 4W		20	25	-	dB
V_{B-} to 4W		20	25	-	dB
Ring Sync Pulse Width		50	-	500	µs
D.C. PARAMETERS					
Loop Current Programming					
Limit Range		20	40	60	mA
Accuracy		10	-	-	%
Loop Current During Power Denial	R_L = 200Ω	-	±3	±5	mA
Fault Currents					
TIP to Ground		-	30	-	mA
RING to Ground		-	60	-	mA
TIP and RING to Ground		-	90	-	mA
Switch Hook Detection Threshold		-	12	15	mA
Ground Key Detection Threshold		-	10	-	mA
Thermal $\overline{\text{ALARM}}$ Output	Safe Operating Die Temperature Exceeded	140	-	160	°C

Electrical Specifications Unless Otherwise Specified, Typical Parameters are at T_A = +25°C, Min-Max Parameters are over Operating Temperature Range, V_{B-} = -48V, V_{B+} = +5V, AG = DG = BG = 0V. All A.C. Parameters are specified at 600Ω 2-Wire terminating impedance. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Ring Trip Detection Threshold	V_{RING} = 105V_{RMS}, f_{RING} = 20Hz	-	10	-	mA
Ring Trip Detection Period		-	100	150	ms
Dial Pulse Distortion		-	0.1	0.5	ms
Relay Driver Outputs					
On Voltage V_{OL}	I_{OL} ($\overline{PR}$) = 60mA, I_{OL} ($\overline{RD}$) = 30mA	-	0.2	0.5	V
Off Leakage Current	V_{OH} = 13.2V	-	±10	±100	µA
TTL/CMOS Logic Inputs (F0, F1, RS, $\overline{TEST}$, PRI)					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Input Current (F0, F1, RS, $\overline{TEST}$, PRI)	0V ≤ V_{IN} ≤ 5V	-	-	±100	µA
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} = 800µA	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} = 40µA	2.7	-	-	V
Power Dissipation On Hook	Relay Drivers Off	-	200	-	mW
I_{B+}	V_{B+} = +5.25V, V_{B-} = -58V, R_{LOOP} = ∞	-	-	6	mA
I_{B-}	V_{B+} = +5.25V, V_{B-} = -58V, R_{LOOP} = ∞	-6	-	-	mA
UNCOMMITED OP AMP PARAMETERS					
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Differential Input Resistance	(Note 3)	-	1	-	MΩ
Output Voltage Swing	R_L = 10kΩ	-	±3	-	V_{P-P}
Small Signal GBW	(Note 3)	-	1	-	MHz

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. May Be Extended to 1900Ω With Application Circuit.
3. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Pin Descriptions

DIP/SOIC	PLCC	SYMBOL	DESCRIPTION
1	2	AG	Analog Ground - To be connected to zero potential. Serves as a reference for the transmit output and receive input terminals.
2	3	VB+	Positive Voltage Source - Most Positive Supply.
3	4	C1	Capacitor #C1 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function.
4	8	F1	Function Address #1 - A TTL and CMOS compatible input used with F0 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on page1. F1 should be toggled high after power is applied.
5	9	F0	Function Address #0 - A TTL and CMOS compatible input used with F1 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on page 1.
6	10	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive pulse (50 - 500µs) occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring delay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5.
7	11	$\overline{SHD}$	Switch Hook Detection - An active low LS TTL compatible logic output. A line supervisory output.
8	12	$\overline{GKD}$	Ground Key Detection - An active low LS TTL compatible logic output. A line supervisory output.
9	13	$\overline{TST}$	A TTL logic input. A low on this pin will set a latch and keep the SLIC in a power down mode until the proper F1, F0 state is set and will keep $\overline{ALM}$ low. See Truth Table on page 1.
10	17	$\overline{ALM}$	A LS TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded. When $\overline{TST}$ is forced low by an external control signal, $\overline{ALM}$ is latched low until the proper F1, F0 state and $\overline{TST}$ input is brought high. The $\overline{ALM}$ can be tied directly to the $\overline{TST}$ pin to power down the part when a thermal fault is detected and then reset with F0, F1. See Truth Table on page 1. It is possible to ignore transient thermal overload conditions in the SLIC by delaying the response to the $\overline{TST}$ pin from the $\overline{ALM}$. Care must be exercised in attempting this as continued thermal overstress may reduced component life.
11	18	ILMT	Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions using a resistive voltage divider.
12	19	OUT1	The analog output of the spare operational amplifier.
13	20	-IN1	The inverting analog input of the spare operational amplifier.
14	22	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor and ring relay contact. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purpose.
15	24	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.
16	25	RFS	Ring Feed Sense - Senses RING side of the loop for Ground Key Detection. During Ring injected ringing the ring signal at this node is isolated from RF via the ring relay. For Tip injected ringing, the RF and RFS pins must be shorted.
17	27	VRX	Receive Input, Four Wire Side - A high impedance analog input. AC signals appearing at this input drive the Tip Feed and Ring Feed amplifiers differentially.
18	31	C2	Capacitor #2 - An external capacitor to be connected between this terminal and ground. It prevents false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from power lines and other noise sources. This capacitor should be nonpolarized.

Pin Descriptions (Continued)

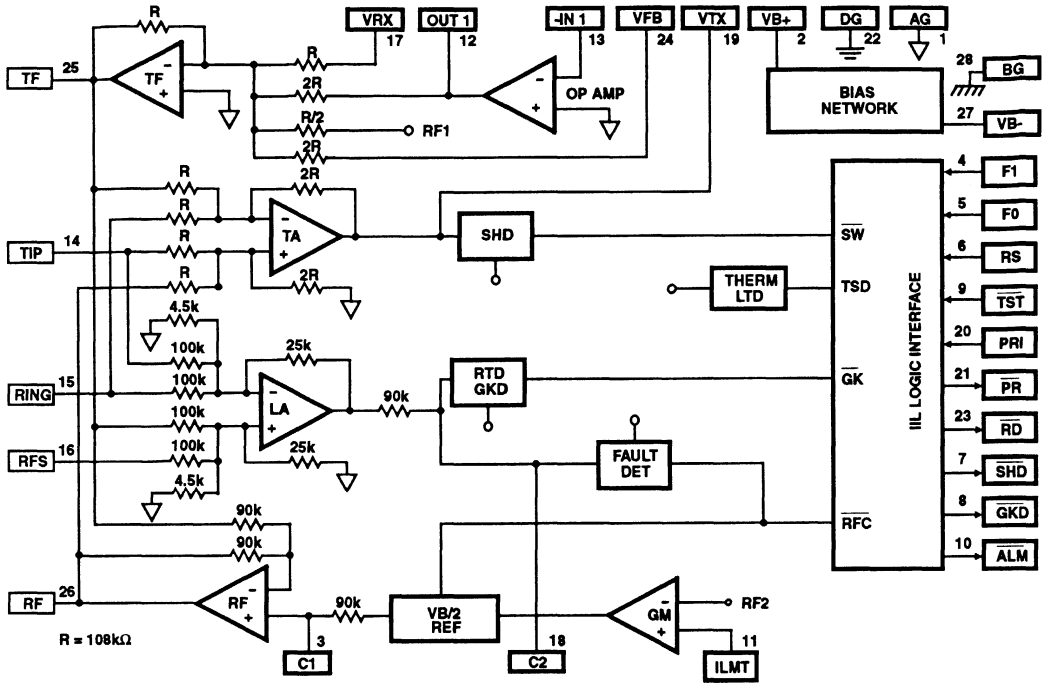
DIP/SOIC	PLCC	SYMBOL	DESCRIPTION
19	32	VTX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Transhybrid balancing must be performed beyond this output to completely implement two to four wire conversion. This output is referenced to analog ground. Since the D.C. level of this output varies with loop current, capacitive coupling to the next stage is necessary.
20	33	PRI	A TTL compatible input used to control $\overline{PR}$. PRI active High = $\overline{PR}$ active low.
21	34	$\overline{PR}$	An active low open collector output. Can be used to drive a Polarity Reversal Relay.
22	35	DG	Digital Ground - To be connected to zero potential. Serves as a reference for all digital inputs and outputs on the SLIC.
23	36	$\overline{RD}$	Ring Relay Driver - An active low open collector output. Used to drive a relay that switches ringing signals onto the 2-Wire line.
24	37	VFB	Feedback input to the tip feed amplifier; may be used in conjunction with transmit output signal and the spare op-amp to accommodate 2W line impedance matching.
25	38	TF2	Tip Feed - A low impedance analog output connected to the TIP terminal through a feed resistor. Functions with the RF terminal to provide loop current, and to feed voice signals to the telephone set and to sink longitudinal currents. Must be tied to TF1.
NA	39	TF1	Tie directly to TF2 in the PLCC application.
26	41	RF1	Ring Feed - A low impedance analog output connected to the RING terminal through a feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and to sink longitudinal currents. Tie directly to RF2.
NA	42	RF2	Tie directly to RF1 in the PLCC application.
27	43	VB-	The battery voltage source. The most negative supply.
28	44	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
	1, 5, 6, 7, 14, 15, 16, 21, 23, 26, 28, 29, 30, 40	NC	No internal connection.

NOTE:

4. All grounds (AG, BG, DG) must be applied before V_{B+} or V_{B-}. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Functional Diagram

DIP OR SOIC



Die Characteristics

Transistor Count 224
Diode Count 28
Die Dimensions ..... 174 x 120
Substrate Potential ..... Connected
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	48	12
Plastic DIP	51	21
PLCC	47	17
SOIC	72	22

Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

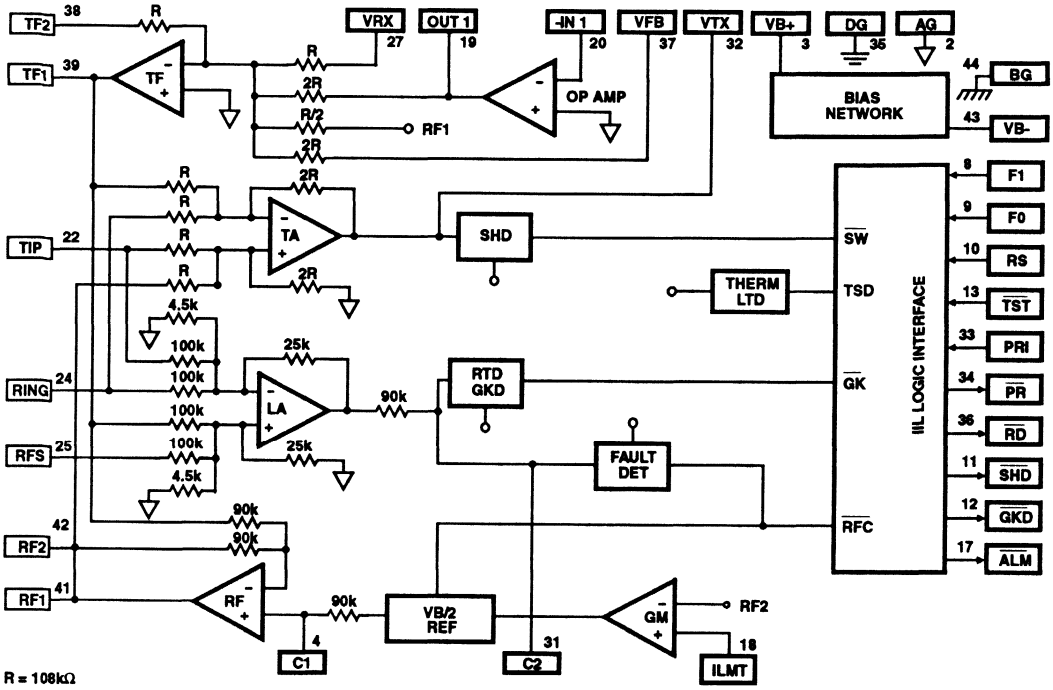
The SLIC will withstand longitudinal currents up to a maximum or 30mArms, 15mArms per leg, without any performance degradation

TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
50/60Hz Current T/GND R/GND	11 Cycles Limited to 10Arms	700 (Plastic)	V_{RMS}
		350 (Ceramic)	V_{RMS}

Functional Diagram (Continued)

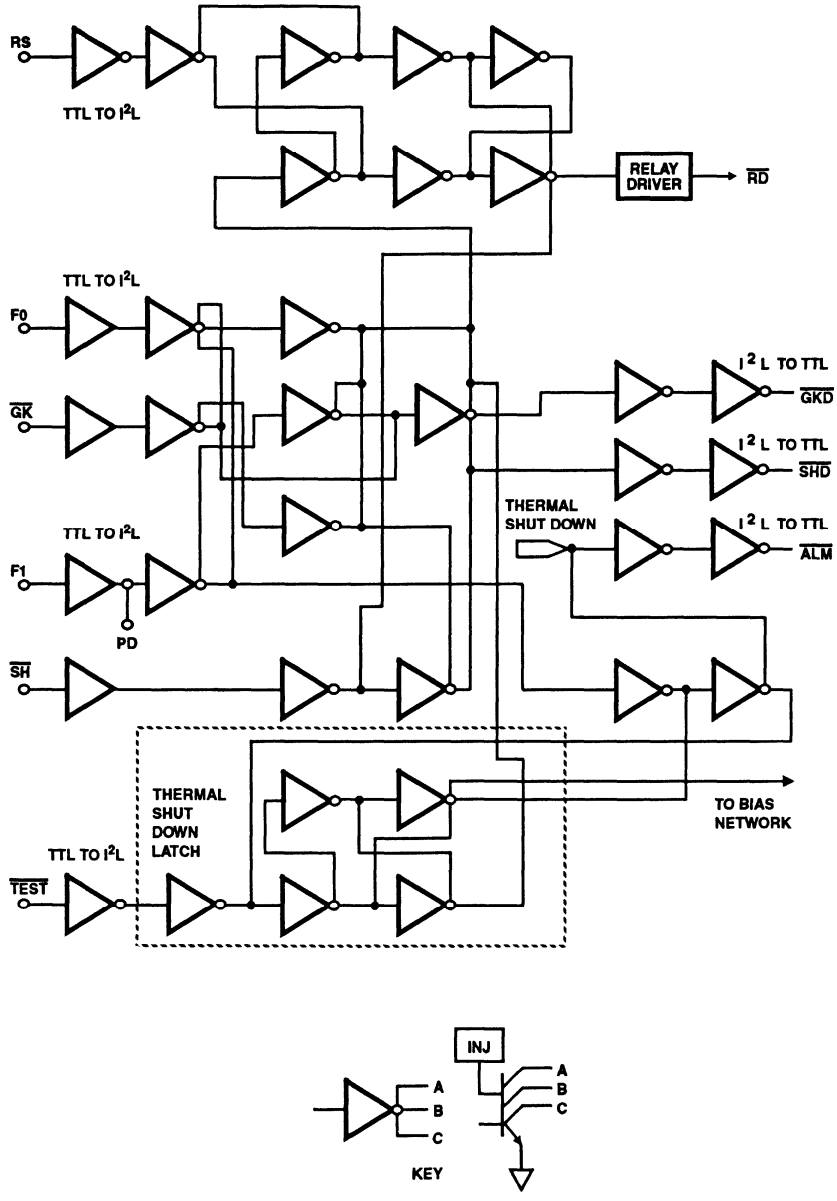
PLCC



R = 108kΩ
NC = 1, 5, 6, 7, 14, 15, 16, 21, 23, 26, 28, 29, 30, 40

8 TELECOM

Logic Diagram



Applications Diagram

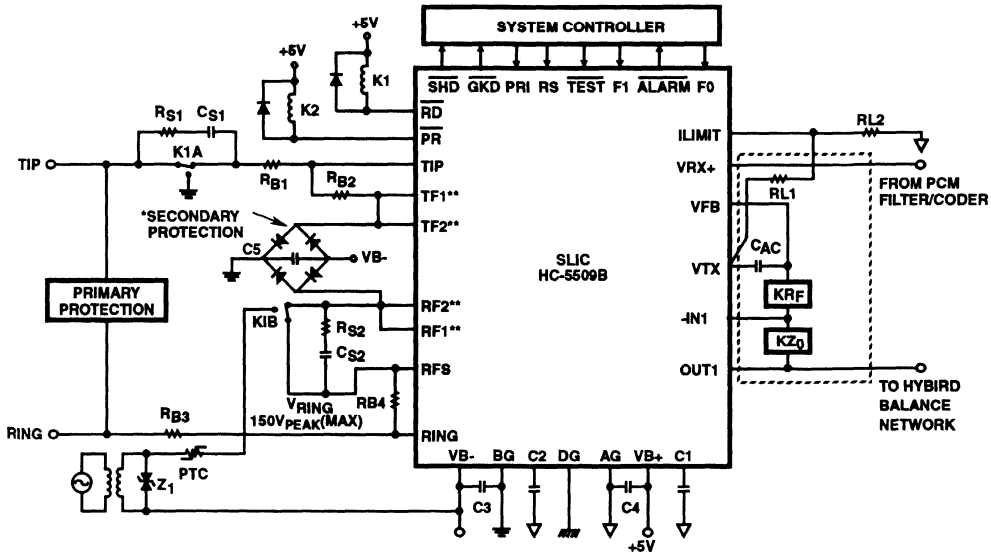


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

TYPICAL COMPONENT VALUES

C1 = 0.5µF, 30V

C2 = 0.5µF-1.0µF ±10%, 20V (Should be nonpolarized)

C3 = 0.01µF, 100V, ±20%

C4 = 0.01µF, 100V, ±20%

C5 = 0.01µF, 100V, ±20%

C_{AC} = 0.5µF, 20V

KZ_0 = 60kΩ, (Z_0 = 600Ω, k = Scaling Factor = 100)

RL1, RL2; Current Limit Setting Resistors:

RL1 + RL2 > 90kΩ → offset

I_{LIMIT} = (0.6) (RL1 + RL2)/(200 x RL2), RL1 typically 100kΩ

KR_F = 20kΩ, RF = 2(R_{B2} + R_{B4}), K = Scaling Factor = 100)

RB_1 = RB_2 = RB_3 = RB_4 = 50Ω (1% absolute, matching requirements covered in a Tech Brief)

R_{S1} = R_{S2} = 1kΩ typically

CS1 = CS2 = 0.1µF, 200V typically, depending on V_{Ring} and line length.

Z_1 = 150V to 200V transient protector. PTC used as ring generator ballast.

* Secondary protection diode bridge recommended is 3A, 200V type.

**TF1, TF2 and RF1, RF2 are on PLCC only and should be connected together as shown.

NOTES:

1. All grounds (AG, BG, & DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
2. Application shows Ring Injected Ringing, a Balanced or Tip Injected configuration may be used.

Additional information is contained in Application Note 549, "The HC-550X Telephone SLICs" By Geoff Phillips

HARRIS SEMICONDUCTOR

HC-5524

SLIC
Subscriber Line Interface Circuit

March 1993

Features

- DI Monolithic High Voltage Process
- Compatible with Worldwide PBX and DLC Performance Requirements
- Controlled Supply of Battery Feed Current With Programmable Current Limit
- Operates with 5V Positive Supply (V_B+)
- Internal Ring Relay Driver and a Utility Relay Driver
- High Impedance Mode for Subscriber Loop
- High Temperature Alarm Output
- Low Power Consumption During Standby Functions
- Switch Hook, Ground Key, and Ring Trip Detection
- Selective Power Denial to Subscriber
- Voice Path Active During Power Denial
- On Chip Op-Amp for 2 Wire Impedance Matching

Applications

- Solid State Line Interface Circuit for PBX or Digital Loop Carrier Systems
- Hotel/Motel Switching Systems
- Direct Inward Dialing (DID) Trunks
- Voice Messaging PBX's
- 2W/4W, 4W/2W Hybrid

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HC1-5524-5	0°C to +75°C	28 Lead Ceramic DIP
HC1-5524-9	-40°C to +85°C	28 Lead Ceramic DIP
HC3-5524-5	0°C to +75°C	28 Lead Plastic DIP
HC3-5524-9	-40°C to +85°C	28 Lead Plastic DIP
HC4P5524-5	0°C to +75°C	44 Lead PLCC
HC4P5524-9	-40°C to +85°C	44 Lead PLCC
HC9P5524-5	0°C to +75°C	28 Lead SOIC
HC9P5524-9	-40°C to +85°C	28 Lead SOIC

Description

The HC-5524 telephone Subscriber Line Interface Circuit integrates most of the BORSCHT functions on a monolithic IC. The device is manufactured in a Dielectric Isolation (DI) process and is designed for use as a 24V interface between the traditional telephone subscriber pair (Tip and Ring) and the low voltage filtering and coding/decoding functions of the line card. Together with a secondary protection diode bridge, the device will withstand 500V induced surges, in plastic packages. The SLIC also maintains specified transmission performance in the presence of externally induced longitudinal currents. The BORSCHT functions that the SLIC provides are:

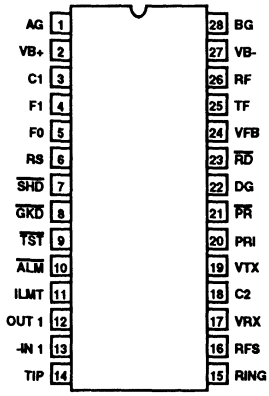
- Battery Feed with Subscriber Loop Current Limiting
- Overvoltage Protection
- Ring Relay Driver
- Supervisory Signaling Functions
- Hybrid Functions (with External Op-Amp)
- Test (or Battery Reversal) Relay Driver

In addition, the SLIC provides selective denial of power to subscriber loops, a programmable subscriber loop current limit from 20mA to 60mA, a thermal shutdown with an alarm output and line fault protection. Switch hook detection, ring trip detection and ground key detection functions are also incorporated in the SLIC device.

The HC-5524 SLIC is ideally suited for line card designs in PBX and DLC systems, replacing traditional transformer solutions.

Pinouts

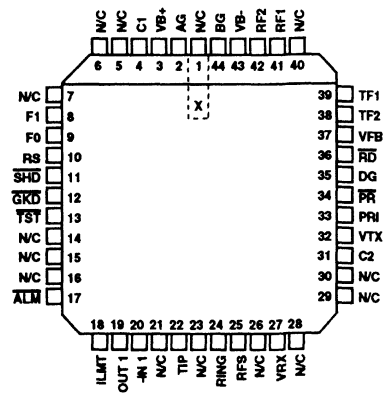
HC-5524 (PDIP, CDIP, SOIC)
TOP VIEW



TRUTH TABLE

F1	F0	Action
0	0	Normal Loop Feed
0	1	$\overline{RD}$ Active
1	0	Power Down Latch RESET
1	0	Power on RESET
1	1	Loop Power Denial Active

HC-5524 (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2798.2**

Absolute Maximum Ratings (Note 1)

Maximum Supply Voltages (V_{B+}) ..... -0.5V to +7V
(V_{B+}) - (V_{B-}) ..... +40V
Relay Drive Voltage ..... -0.5V to +15V
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HC-5524-5 ..... $0°C \le T_A \le +75°C$
HC-5524-9 ..... $-40°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$
Relay Driver Voltage ..... +5V to +12V
Positive Power Supply (V_{B+}) ..... +5V ± 5%
Negative Power Supply (V_{B-}) ..... -20V to -28V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Typical Parameters are at T_A = +25°C, V_{B+} = +5V, V_{B-} = -24V, AG = DG = BG = 0V. Min-Max Parameters are Over Operating Positive and Negative Battery Voltages and Over the Operating Temperature Range. All Parameters are Specified at 600Ω 2-Wire Terminating Impedance, Unless Otherwise Specified.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
AC TRANSMISSION PARAMETERS					
RX Input Impedance	300Hz to 3.4kHz (Note 2)	-	100	-	kΩ
TX Output Impedance		-	-	20	Ω
4W Input Overload Level	300Hz to 3.4kHz, 600Ω Reference	+1.0	-	-	V_{PEAK}
2W Return Loss	Matched for 600Ω (Note 2)				
SRL LO		26	35	-	dB
ERL		30	40	-	dB
SRL HI		30	40	-	dB
2W Longitudinal to Metallic Balance Off Hook	Per ANSI/IEEE STD 455-1976 (Note 2), 300Hz to 3400Hz	58	63	-	dB
4W Longitudinal Balance Off Hook	Per ANSI/IEEE STD 455-1976 (Note 2), 300Hz to 3400Hz (Note 2)	50	55	-	dB
Low Frequency Longitudinal Balance	R.E.A. Test Circuit	-	-80	-67	dBmp
	I_{LINE} = 40mA, T_A = +25°C (Note 2)	-	10	23	dBrnC
Longitudinal Current Capability	I_{LINE} = 40mA, T_A = +25°C (Note 2)	-	-	40	mArms
Insertion Loss					
2W/4W	-1.58dBm at 1kHz, Referenced 600Ω	-	±0.05	±0.2	dB
4W/2W	0dBm at 1kHz, Referenced 600Ω	-	±0.05	±0.2	dB
4W/4W	-1.58dBm at 1kHz, Referenced 600Ω	-	-	±0.2	dB
Frequency Response	300Hz to 3400Hz (Note 2), Referenced to Absolute Level at 1kHz, 0dBm Referenced 600Ω	-	±0.02	±0.06	dB
Level Linearity 2W to 4W and 4W to 2W	Referenced to -10dBm (Note 2)				
	+3 to -40dBm	-	-	±0.08	dB
	-40 to -50dBm	-	-	±0.12	dB
	-50 to -55dBm	-	-	±0.3	dB
Absolute Delay	(Note 2)				
2W/4W	300Hz to 3400Hz	-	-	1	µs
4W/2W	300Hz to 3400Hz	-	-	1	µs
4W/4W	300Hz to 3400Hz	-	0.95	1.5	µs
Total Harmonic Distortion 2W/4W, 4W/2W, 4W/4W	Reference Level 0dBm at 600Ω, 300Hz to 3400Hz (Note 2)	-	-	-50	dB

Electrical Specifications Typical Parameters are at T_A = +25°C, V_{B+} = +5V, V_{B-} = -24V, AG = DG = BG = 0V. Min-Max Parameters are Over Operating Positive and Negative Battery Voltages and Over the Operating Temperature Range. All Parameters are Specified at 600Ω 2-Wire Terminating Impedance, Unless Otherwise Specified. **(Continued)**

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
AC TRANSMISSION PARAMETERS (Continued)					
Idle Channel Noise 2W and 4W	(Note 2) C-Message	-	-	5	dBrnC
	Psophometric	-	-	-85	dBmp
	3kHz Flat	-	-	16	dBrn
Open Loop Voltage (V_{TIP} - V_{RING})	V_{B+} = +5V, V_{B-} = -24V	-	15.8	-	V
Power Supply Rejection Ratio	(Note 2)				
V_{B+} to 2W	30Hz to 200Hz, R_L = 600Ω	20	40	-	dB
V_{B+} to 4W		20	40	-	dB
V_{B-} to 2W		20	40	-	dB
V_{B-} to 4W		20	50	-	dB
V_{B+} to 2W	200Hz to 16kHz, R_L = 600Ω	30	40	-	dB
V_{B+} to 4W		20	28	-	dB
V_{B-} to 2W		20	50	-	dB
V_{B-} to 4W		20	50	-	dB
Ring Sync Pulse Width		50	-	500	µs
DC PARAMETERS					
Loop Current Programming Limit Range		20	40	60	mA
Accuracy		10	-	-	%
Loop Current During Power Denial	R_L = 200Ω	-	±4	±7	mA
Fault Currents TIP to Ground		-	30	-	mA
RING to Ground		-	120	-	mA
TIP and RING to Ground		-	150	-	mA
Switch Hook Detection Threshold		-	12	15	mA
Ground Key Detection Threshold		-	10	-	mA
Thermal $\overline{ALM}$ Output	Safe Operating Die Temperature Exceeded	140	-	160	°C
Ring Trip Detection Threshold	V_{RING} = 105V_{RMS}, f_{RING} = 20Hz	-	10	-	mA
Ring Trip Detection Period		-	100	150	ms
Dial Pulse Distortion		-	0.1	0.5	ms
Relay Driver Outputs On Voltage V_{OL}	I_{OL} ($\overline{PR}$) = 60mA, I_{OL} ($\overline{RD}$) = 30mA	-	0.2	0.5	V
Off Leakage Current	V_{OH} = 13.2V	-	±10	±100	µA
TTL/CMOS Logic Inputs (F0, F1, RS, $\overline{TST}$, PRI) Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V

Electrical Specifications Typical Parameters are at T_A = +25°C, V_B+ = +5V, V_B- = -24V, AG = DG = BG = 0V. Min-Max Parameters are Over Operating Positive and Negative Battery Voltages and Over the Operating Temperature Range. All Parameters are Specified at 600Ω 2-Wire Terminating Impedance, Unless Otherwise Specified. **(Continued)**

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
DC PARAMETERS (Continued)					
Input Current (F0, F1, RS, $\overline{TST}$, PRI)	$0V \le V_{IN} \le 5V$	-	-	±100	µA
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} = 800µA	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} = 40µA	2.7	-	-	V
Power Dissipation On Hook	Relay Drivers Off	-	60	-	mW
I_{B}+	V_{B}+ = +5.25V, V_{B}- = -28V, R_{LOOP} = ∞	-	-	4	mA
I_{B}-	V_{B}+ = +5.25V, V_{B}- = -28V, R_{LOOP} = ∞	-4	-	-	mA
I_{B}+	V_{B}+ = +5V, V_{B}- = -24V, R_{LOOP} = 600Ω	-	3	6	mA
I_{B}-	V_{B}+ = +5V, V_{B}- = -24V, R_{LOOP} = 600Ω	-28	-24	-	mA
UNCOMMITED OP AMP PARAMETERS					
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Differential Input Resistance	(Note 2)	-	1	-	MΩ
Output Voltage Swing	R_L = 10kΩ	-	±3	-	V_{P-P}
Small Signal GBW	(Note 2)	-	1	-	MHz

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Pin Descriptions

DIP/ SOIC	PLCC	SYMBOL	DESCRIPTION
1	2	AG	Analog Ground - To be connected to zero potential. Serves as a reference for the transmit output and receive input terminals.
2	3	VB+	Positive Voltage Source - Most Positive Supply.
3	4	C1	Capacitor #C1 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function.
4	8	F1	Function Address #1 - A TTL and CMOS compatible input used with F0 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on front page. F1 should be toggled high after power is applied.
5	9	F0	Function Address #0 - A TTL and CMOS compatible input used with F1 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on front page.
6	10	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive pulse (50 - 500µs) occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring delay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5.

Pin Descriptions (Continued)

DIP/ SOIC	PLCC	SYMBOL	DESCRIPTION
7	11	$\overline{SHD}$	Switch Hook Detection - An active low LS TTL compatible logic output. A line supervisory output.
8	12	$\overline{GKD}$	Ground Key Detection - An active low LS TTL compatible logic output. A line supervisory output.
9	13	$\overline{TST}$	A TTL logic input. A low on this pin will set a latch and keep the SLIC in a power down mode until the proper F1, F0 state is set and will keep $\overline{ALM}$ low. See Truth Table on front page.
10	17	$\overline{ALM}$	A LS TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded. When $\overline{TST}$ is forced low by an external control signal, $\overline{ALM}$ is latched low until the proper F1, F0 state and $\overline{TST}$ input is brought high. The $\overline{ALM}$ can be tied directly to the $\overline{TST}$ pin to power down the part when a thermal fault is detected and then reset with F0, F1. See Truth Table on front page. It is possible to ignore transient thermal overload conditions in the SLIC by delaying the response to the $\overline{TST}$ pin from the $\overline{ALM}$. Care must be exercised in attempting this as continued thermal overstress may reduce component life.
11	18	ILMT	Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions using a resistive voltage divider.
12	19	OUT1	The analog output of the spare operational amplifier.
13	20	-IN1	The inverting analog input of the spare operational amplifier.
14	22	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor and ring relay contact. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purposes.
15	24	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.
16	25	RFS	Ring Feed Sense - Senses RING side of the loop for Ground Key Detection. During Ring injected ringing the ring signal at this node is isolated from RF via the ring relay. For Tip injected ringing, the RF and RFS pins must be shorted.
17	27	VRX	Receive Input, Four Wire Side - A high impedance analog input. AC signals appearing at this input drive the Tip Feed and Ring Feed amplifiers differentially.
18	31	C2	Capacitor #2 - An external capacitor to be connected between this terminal and ground. It prevents false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from power lines and other noise sources. This capacitor should be nonpolarized.
19	32	VTX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Transhybrid balancing must be performed beyond this output to completely implement two to four wire conversion. This output is referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is necessary.
20	33	PRI	A TTL compatible input used to control $\overline{PR}$. PRI active High = $\overline{PR}$ active low.
21	34	$\overline{PR}$	An active low open collector output. Can be used to drive a Polarity Reversal Relay.
22	35	DG	Digital Ground - To be connected to zero potential. Serves as a reference for all digital inputs and outputs on the SLIC.
23	36	$\overline{RD}$	Ring Relay Driver - An active low open collector output. Used to drive a relay that switches ringing signals onto the 2 wire line.
24	37	VFB (Note 2)	Feedback input to the tip feed amplifier; may be used in conjunction with transmit output signal and the spare op-amp to accommodate 2W line impedance matching. (This is not used in the typical applications circuit).
25	38	TF2	Tip Feed - A low impedance analog output connected to the TIP terminal through a feed resistor. Functions with the RF terminal to provide loop current, and to feed voice signals to the telephone set and to sink longitudinal currents. Must be tied to TF1.
NA	39	TF1	Tie directly to TF2 in the PLCC application.
26	41	RF1	Ring Feed - A low impedance analog output connected to the RING terminal through a feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and to sink longitudinal currents. Tie directly to RF2.

Pin Descriptions (Continued)

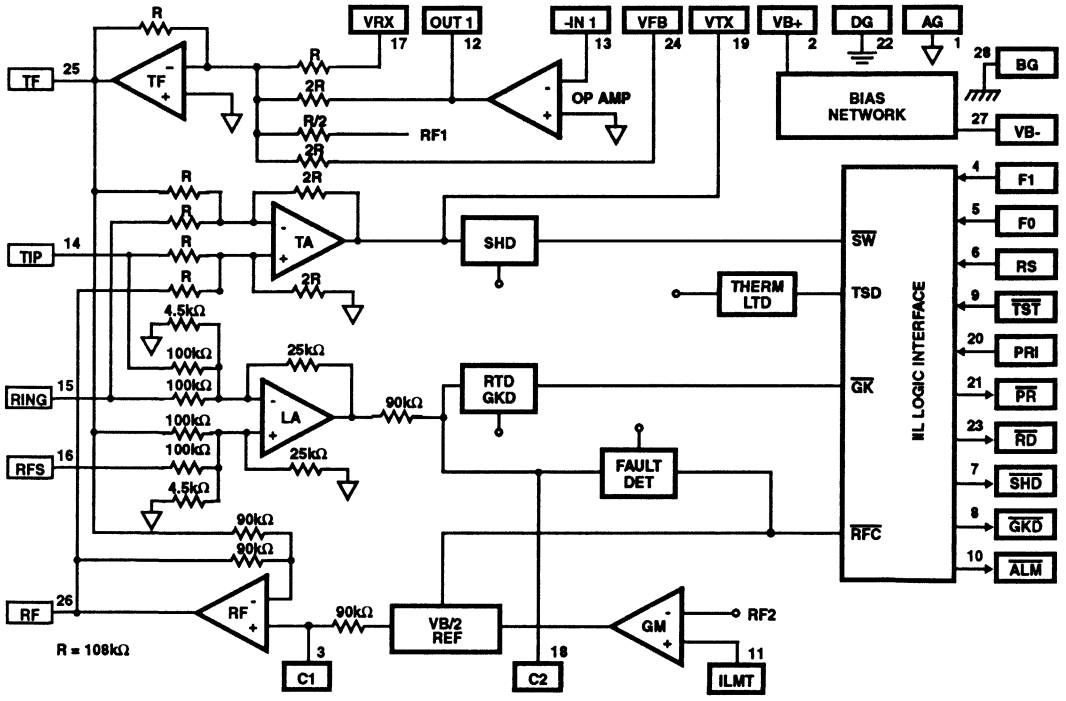
DIP/ SOIC	PLCC	SYMBOL	DESCRIPTION
NA	42	RF2	Tie directly to RF1 in the PLCC application.
27	43	VB-	The battery voltage source. The most negative supply.
28	44	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
	1, 5, 6, 7, 14, 15, 16, 21, 23, 26, 28, 29, 30, 40	NC	No internal connection.

NOTES:

1. All grounds (AG, BG, DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
2. Although not used in the typical applications circuit, V_{FB} may be used in matching complex 2-Wire impedances.

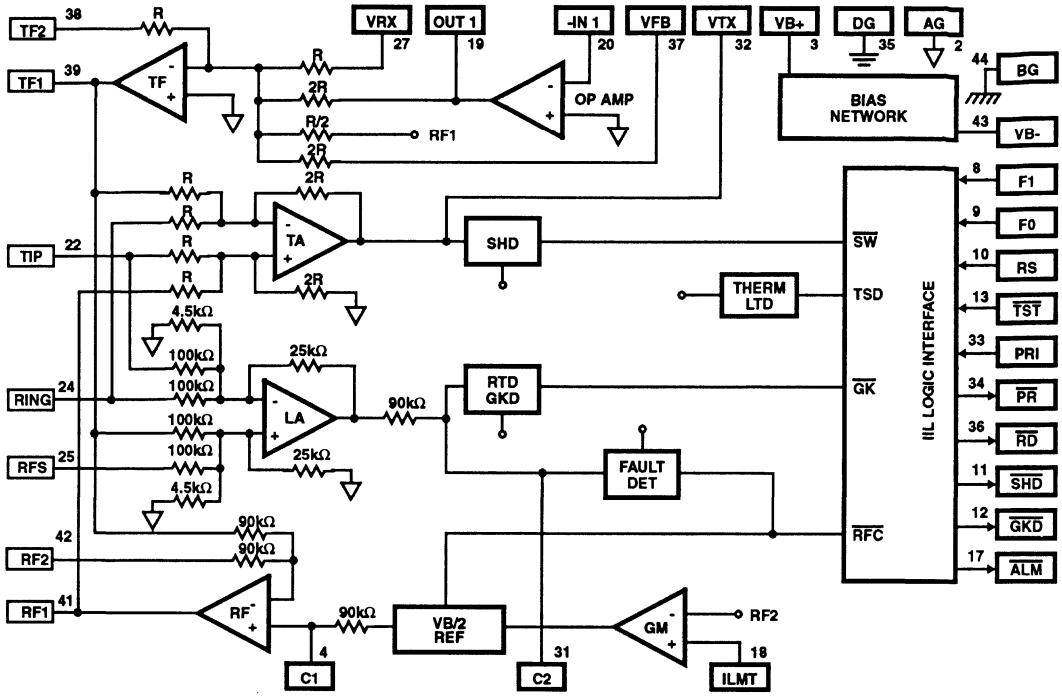
Functional Diagram

DIP OR SOIC



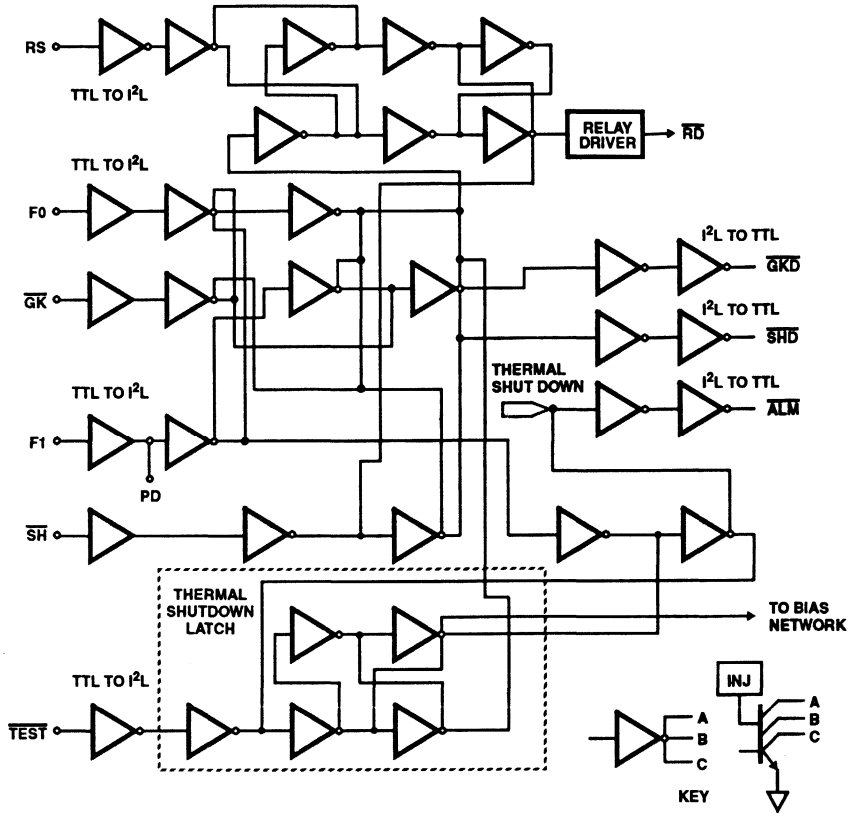
Functional Diagram (Continued)

PLCC



NOTE:
R = 108kΩ
NC = 1, 5, 6, 7, 14, 15, 16, 21
23, 26, 28, 29, 30, 40

Logic Diagram



Die Characteristics

Transistor Count 224
Diode Count 28
Die Dimensions ..... 174 x 120 mils
Substrate Potential ..... Connected
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	48	12
Plastic DIP	51	21
PLCC	47	17
SOIC	72	22

Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or 40mArms, 20mArms per leg, without any performance degradation.

TABLE 1

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/	±1000 (Plastic)	V_{PEAK}
	1000µs Fall	±500 (Ceramic)	V_{PEAK}
Metallic Surge	10µs Rise/	±1000 (Plastic)	V_{PEAK}
	1000µs Fall	±500 (Ceramic)	V_{PEAK}
T/GND	10µs Rise/	±1000 (Plastic)	V_{PEAK}
R/GND	1000µs Fall	±500 (Ceramic)	V_{PEAK}
50/60Hz Current			
T/GND	11 Cycles	700 (Plastic)	V_{RMS}
R/GND	Limited to 10Arms	350 (Ceramic)	V_{RMS}

8 TELECOM

Applications Diagram

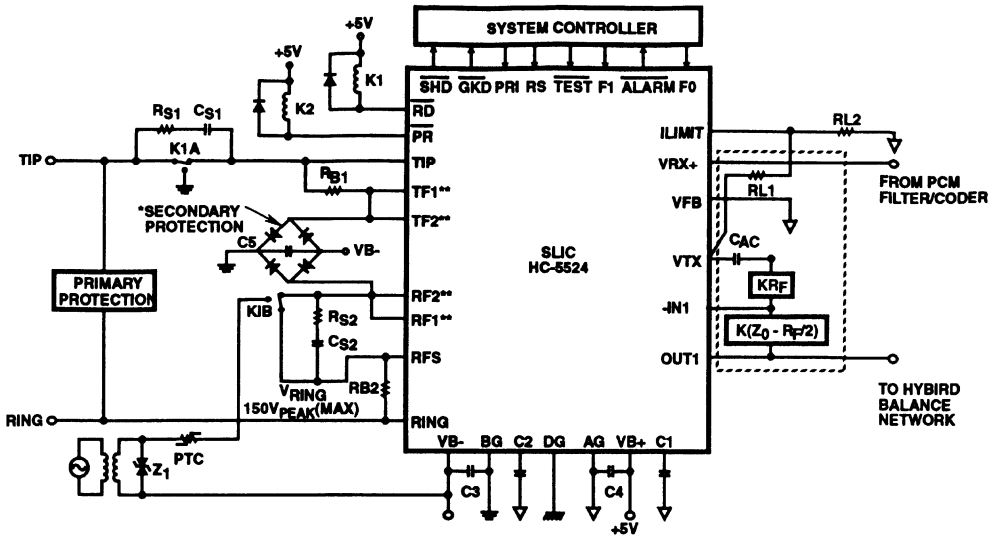


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

TYPICAL COMPONENT VALUES

C1 = 0.5µF, 20V

C2 = 0.5µF-1.0µF ±10%, 20V (Should be nonpolarized)

C3 = 0.01µF, 50V ±20%

C4 = 0.01µF, 50V ±20%

C5 = 0.01µF, 50V ±20%

C_{AC} = 0.5µF, 20V

$K(Z_0 - R_F/2)$ = 50kΩ, (Z_0 = 600Ω, K = Scaling Factor = 100)

RL1, RL2; Current Limit Setting Resistors

RL1+RL2 > 90kΩ

I_{LIMIT} = (.6) (RL1+RL2)/(200xRL2), RL1 typically 100kΩ

KR_F = 20kΩ, $R_F = 2(R_{B1}+R_{B2})$, K = Scaling Factor = 100)

$RB_1 = RB_2$ = 50Ω (1% absolute, matching requirements covered in a Tech Brief)

$R_{S1} = R_{S2}$ = 1kΩ typically

CS1 = CS2 = 0.1µF, 200V typically, depending on V_{Ring} and line length.

Z_1 = 150V to 200V transient protector. PTC used as ring generator ballast.

* Secondary protection diode bridge recommended is 3A, 200V type.

** TF1, TF2 and RF1, RF2 are on PLCC only and should be connected together as shown.

NOTES:

1. All grounds (AG, BG, & DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first
2. Application shows Ring Injected Ringing, Balanced or Tip Injected configuration may be used.

Additional information is contained in Application Note 549, "The HC-550X Telephone SLICs" By Geoff Phillips

HARRIS SEMICONDUCTOR

HC-5560

March 1993

PCM Transcoder

Features

- Single 5V Supply ..... 10mA Typ.
- Mode Selectable Coding Including:
  - AMI (T1, T1C)
  - B8ZS (T1)
  - HDB3 (PCM30)
- North American and European Compatibility
- Simultaneous Encoding and Decoding
- Asynchronous Operation
- Loop Back Control
- Transmission Error Detection
- Alarm Indication Signal
- Replaces MJ1440, MJ1471 and TCM2201 Transcoders

Applications

- North American and European PCM Transmission Lines where Pseudo Ternary Line Code Substitution Schemes are Desired
- Any Equipment that Interfaces T1, T1C, T2 or PCM30 Lines Including Multiplexers, Channel Service Units, (CSUs) Echo Cancellors, Digital Cross-Connects (DSXs), T1 Compressors, etc.

Description

The HC-5560 digital line transcoder provides encoding and decoding of pseudo ternary line code substitution schemes. Unlike other industry standard transcoders, the HC-5560 provides four worldwide compatible mode selectable code substitution schemes, including HDB3 (High Density Bipolar 3), B6ZS, B8ZS (Bipolar with 6 or 8 Zero Substitution) and AMI (Alternate Mark Inversion).

The HC-5560 is fabricated in CMOS and operates from a single 5V supply. All inputs and outputs are TTL compatible.

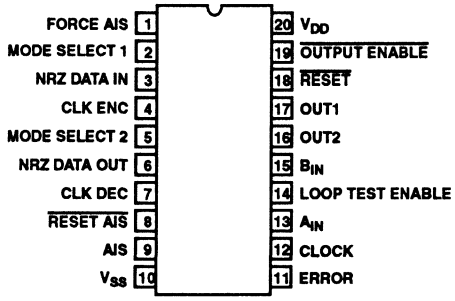
Application Note #573, "The HC-5560 Digital Line Transcoder," by D.J. Donovan is available.

Ordering Information

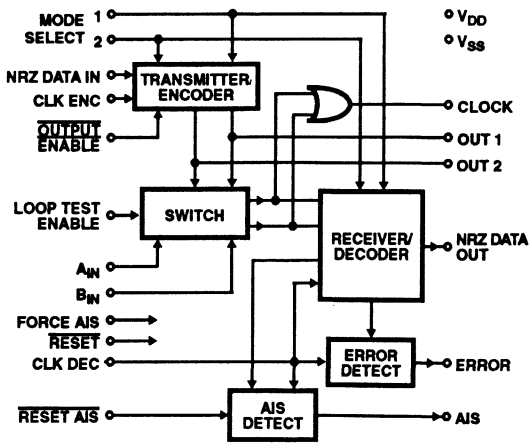
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HC3-5560-5	0°C to +70°C	20 Lead Plastic DIP

Pinout

HC-5560
(PDIP)
TOP VIEW



Functional Diagram



8 TELECOM

File Number 2887.1

Absolute Maximum Ratings

Voltage at Any Pin ..... GND -0.3V to V_{DD} + 0.3V
Maximum V_{DD} Voltage ..... +7.0V
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Operating V_{DD} ..... 5V ± 5%

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications Unless Otherwise Specified, Typical parameters at +25°C, Min-Max parameters are over operating temperature range. V_{DD} = +5V.

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS
Quiescent Device Current	I_{DD}			100	µA
Operating Device Current			10		mA
Out 1, Out 2 Low (Sink) Current (V_{OL} = 0.4V)	I_{OL1}	3.2			mA
All Other Outputs Low (Sink) Current (V_{OL} = 0.8V)	I_{OL2}	2			mA
All Outputs High (Source) Current (V_{OH} = 4.0V)	I_{OH}	2			mA
Input Low Current	I_{IL}			10	µA
Input High Current	I_{IH}			10	µA
Input Low Voltage	V_{IL}			0.8	V
Input High Voltage	V_{IH}	2.4			V
Input Capacitance	C_{IN}			8	pF

Dynamic Electrical Specifications Unless Otherwise Specified, Typical parameters at +25°C, Min-Max parameters are over operating temperature range. V_{DD} = 5V.

PARAMETERS	SYMBOL	FIGURE	MIN	TYP	MAX	UNITS
CLK ENC, CLK DEC Input Frequency	f_{CL}				8.5	MHz
CLK ENC,CLK DEC Rise Time (1.544 MHz)	t_{RCL}	1, 2		10	60	ns
Fall Time	t_{FCL}	1, 2		10	60	ns
Rise Time (2.048 MHz)	t_{RCL}	1, 2		10	40	ns
Fall Time	t_{FCL}	1, 2		10	40	ns
Rise Time (6.3212 MHz)	t_{RCL}	1, 2		10	30	ns
Fall Time	t_{FCL}	1, 2		10	30	ns
Rise Time (8.448 MHz)	t_{RCL}	1, 2		5	10	ns
Fall Time	t_{FCL}	1, 2		5	10	ns
NRZ-Data In to CLK ENC Data Setup Time	t_S	1	20			ns
Data Hold Time	t_H	1	20			ns

Dynamic Electrical Specifications Unless Otherwise Specified, Typical parameters at +25°C, Min-Max parameters are over operating temperature range. V_{DD} = 5V. **(Continued)**

PARAMETERS	SYMBOL	FIGURE	MIN	TYP	MAX	UNITS
A_{IN}, B_{IN} to CLK DEC Data Setup Time	t_S	2	15			ns
Data Hold Time	t_H	2	5			ns
CLK ENC to Out 1, Out 2	t_{DD}	1		23	80	ns
Out 1, Out 2 Pulse Width (CLK ENC Duty Cycle = 50%)						
f_{CL} = 1.544 MHz	t_W	1		324		ns
f_{CL} = 2.048 MHz	t_W	1		224		ns
f_{CL} = 6.3212 MHz	t_W	1		79		ns
f_{CL} = 8.448 MHz	t_W	1		58		ns
CLK DEC to NRZ-Data Out	t_{DD}	2		25	54	ns
Setup Time CLK DEC to $\overline{\text{Reset AIS}}$	t_{S2}	3	35			ns
Hold Time of $\overline{\text{Reset AIS}}$ = '0'	t_{H2}	3	20			ns
Setup Time $\overline{\text{Reset AIS}}$ = '1' to CLK DEC	t_{S2}	3	0			ns
$\overline{\text{Reset AIS}}$ to AIS output	t_{PD5}	3			42	ns
CLK DEC to Error output	t_{PD4}	3			62	ns

Pin Description

PIN NUMBER	FUNCTION	DESCRIPTION
1	Force AIS	Pin 19 must be at logic '0' to enable this pin. A logic '1' on this pin forces Out 1 and Out 2 to all ones. A logic '0' on this pin allows normal operation.
2, 5	Mode Select 1, Mode Select 2	MS1 MS2 functions as 0 0 AMI 0 1 B8ZS 1 0 B6ZS 1 1 HDB3
3	NRZ Data In	Input data to be encoded into ternary form. The data is clocked by the negative going edge of CLK ENC.
4	CLK ENC	Clock encoder, clock for encoding data at NRZ Data In.
6	NRZ Data Out	Decoded data from ternary inputs A_{IN} and B_{IN}.
7	CLK DEC	Clock decoder, clock for decoding ternary data on inputs A_{IN} and B_{IN}.
8, 9	$\overline{\text{Reset AIS}}$, AIS	Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS output to zero provided 3 or more zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ period or sets AIS to '1' if less than 3 zeros have been decoded in the preceding two $\overline{\text{Reset AIS}}$ periods. A period of $\overline{\text{Reset AIS}}$ is defined from the bit following the bit during which $\overline{\text{Reset AIS}}$ makes a high to low transition to the bit during which $\overline{\text{Reset AIS}}$ makes the next high to low transition.
10	V_{SS}	Ground reference.

Pin Description

PIN NUMBER	FUNCTION	DESCRIPTION
11	Error	A logic '1' indicates that a violation of the line coding scheme has been decoded.
12	Clock	"OR" function of A_{IN} and B_{IN} for clock regeneration when pin 14 is at logic '0', "OR" function of Out 1 and Out 2 when pin 14 is at logic '1'.
13, 15	A_{IN}, B_{IN}	Inputs representing the received PCM signal. A_{IN} = '1' represents a positive going '1' and B_{IN} = '1' represents a negative going '1'. A_{IN} and B_{IN} are sampled by the positive going edge of CLK DEC. A_{IN} and B_{IN} may be interchanged.
14	LTE	Loop Test Enable, this pin selects between normal and loop back operation. A logic '0' selects normal operation where encode and decode are independent and asynchronous. A logic '1' selects a loop back condition where Out 1 is internally connected to A_{IN} and Out 2 is internally connected to B_{IN}. A decode clock must be supplied.
16, 17	Out 1, Out 2	Outputs representing the ternary encoded NRZ Data In signal for line transmission. Out 1 and Out 2 are in return to zero form and are clocked out on the positive going edge of CLK ENC. The length of Out 1 and Out 2 is set by the length of the positive clock pulse.
18	$\overline{\text{Reset}}$	A logic '0' on this pin resets all internal registers to zero. A logic '1' allows normal operation of all internal registers.
19	$\overline{\text{Output Enable}}$	A logic '1' on this pin forces outputs Out 1 and Out 2 to zero. A logic '0' allows normal operation.
20	V_{DD}	Power to chip.

Functional Description

The HC-5560 TRANSCODER can be divided into six sections: transmission (coding), reception (decoding), error detection, all ones detection, testing functions, and output controls.

The transmitter codes a non-return to zero (NRZ) binary unipolar input signal (NRZ Data In) into two binary unipolar return to zero (RZ) output signals (Out 1, Out 2). These output signals represent the NRZ data stream modified according to the selected encoding scheme (i.e.,AMI, B8ZS, B6ZS, HDB3) and are externally mixed together (usually via a transistor or transformer network) to create a ternary bipolar signal for driving transmission lines.

The receiver accepts as its input the ternary data from the transmission line that has been externally split into two binary unipolar return to zero signals (A_{IN} and B_{IN}). These signals are decoded, according to the rules of the selected line code into one binary unipolar NRZ output signal (NRz Data Out).

The encoder and decoder sections of the chip perform independently (excluding loopback condition) and may operate simultaneously.

The Error output signal is active high for one cycle of CLK DEC upon the detection of any bipolar violation in the received A_{IN} and B_{IN} signals that is not part of the selected line coding scheme. The bipolar violation is not removed, however, and shows up as a pulse in the NRZ Data Out signal. In addition, the Error output signal monitors the received A_{IN} and B_{IN} signals for a string of zeros that violates the maximum consecutive zeros allowed for the selected line coding scheme (i.e., 15 for AMI, 8 for B8ZS, 6 for B6ZS, and 4 for HDB3). In the event that an excessive amount of zeros is detected, the Error output signal will be active high for one cycle of CLK DEC during the zero that exceeds the maximum number. In the case that a high level should simultaneously appear on both received input signals A_{IN} and B_{IN} a logical one is assumed and appears on the NRZ Data Out stream with the Error output active.

An input signal received at inputs A_{IN} and B_{IN} that consists of all ones (or marks) is detected and signaled by a high level at the Alarm Indication Signal (AIS) output. This is also known as Blue Code. The AIS output is set to a high level when less than three zeros are received during one period of $\overline{\text{Reset AIS}}$ immediately followed by another period of $\overline{\text{Reset AIS}}$ containing less than three zeros. The AIS output is reset to a low level upon the first period of $\overline{\text{Reset AIS}}$ containing 3 or more zeros.

A logic high level on LTE enables a loopback condition where Out 1 is internally connected to A_{IN} and Out 2 is internally connected to B_{IN} (this disables inputs A_{IN} and B_{IN} to external signals). In this condition, NRZ Data In appears at NRZ Data Out (delayed by the amount of clock cycles it takes to encode and decode the selected line code). A decode clock must be supplied for this operation.

The output controls are $\overline{\text{Output Enable}}$ and Force AIS. These pins allow normal operation, force Out 1 and Out 2 to zero, or force Out 1 and Out 2 to output all ones (AIS condition).

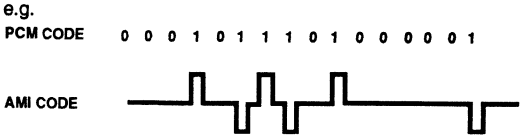
Die Characteristics

Transistor Count		4322
Die Dimensions		119 x 133 mils
Substrate Potential		+V
Process		SAJI CMOS
Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Plastic DIP	67	25

Line Code Descriptions

AMI, Alternate Mark Inversion, is used primarily in North American T1 (1.544 MHz) and T1C (3.152 MHz) carriers. Zeros are coded as the absence of a pulse and ones are coded alternately as positive or negative pulses. This type of coding reduces the average voltage level to zero to eliminate DC spectral components, thereby eliminating DC wander. To simplify timing recovery, logic 1's are encoded with 50% duty cycle pulses.

e.g.



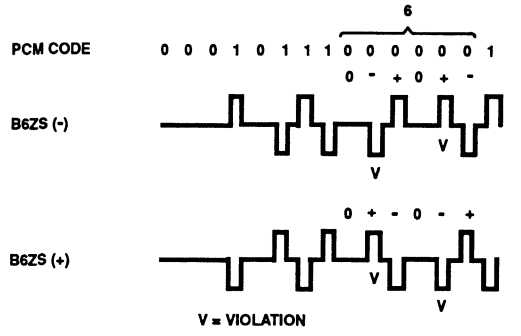
To facilitate timing maintenance at regenerative repeaters along a transmission path, a minimum pulse density of logic 1's is required. Using AMI, there is a possibility of long strings of zeros and the required density may not always exist, leading to timing jitter and therefore higher error rates.

A method for insuring minimum logic 1 density by substituting bipolar code in place of strings of 0's is called BNZS or Bipolar with N Zero Substitution. B6ZS is used commonly in North American T2 (6.3212 MHz) carriers. For every string of 6 zeros, bipolar code is substituted according to the following rule:

> If the immediate preceding pulse is of (-) polarity, then code each group of 6 zeros as 0+- 0+-, and if the immediate preceding pulse is of (+) polarity, code each group of 6 zeros as 0+- 0-+.

One can see the consecutive logic 1 pulses of the same polarity violate the AMI coding scheme.

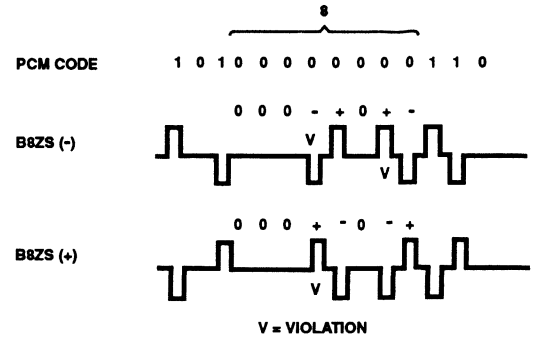
e.g.



B8ZS is used commonly in North American T1 (1.544 MHz) and T1C (3.152 MHz) carriers. For every string of 8 zeros, bipolar code is substituted according to the following rules:

1. If the immediate preceding pulse is of (-) polarity, then code each group of 8 zeros as 000-+ 0+-.
2. If the immediate preceding pulse is of (+) polarity then code each group of 8 zeros as 000+-0-+.

e.g.

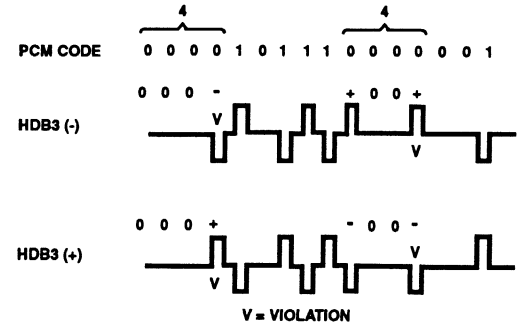


The BNZS coding schemes, in addition to eliminating DC wander, minimize timing jitter and allow a line error monitoring capability.

Another coding scheme is HDB3, high density bipolar 3, used primarily in Europe for 2.048 MHz and 8.448 MHz carriers. This code is similar to BNZS in that it substitutes bipolar code for 4 consecutive zeros according to the following rule:

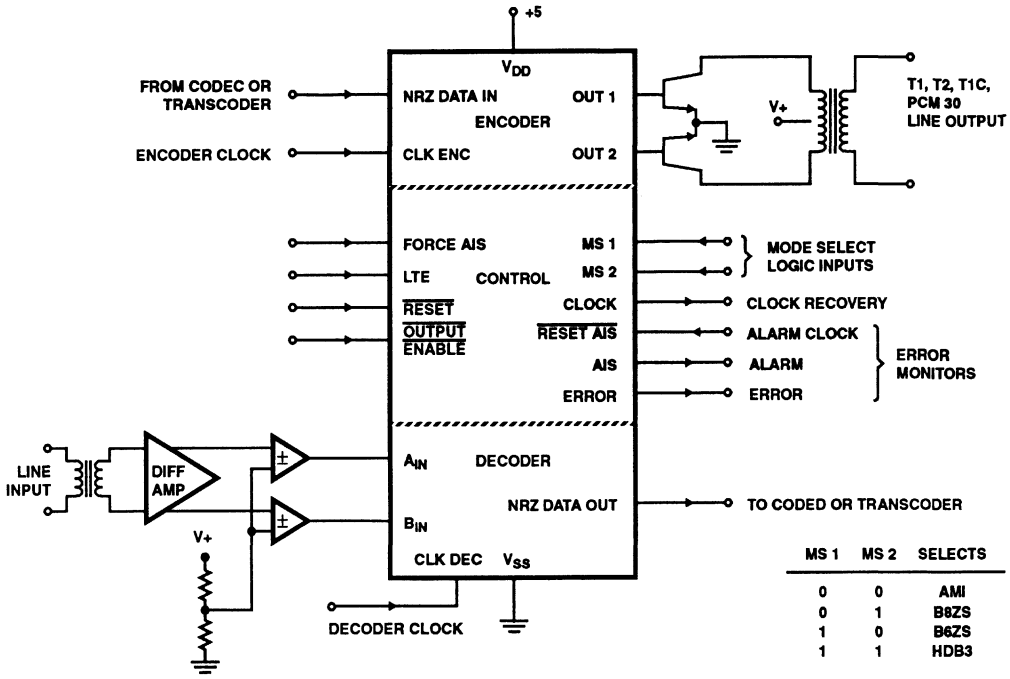
1. If the polarity of the immediate preceding pulse is (-) and there have been an odd (even) number of logic 1 pulses since the last substitution, each group of 4 consecutive zeros is coded as 000-(+00+).
2. If the polarity of the immediate preceding pulse is (+) then the substitution is 000+(-00-) for odd (even) number of logic 1 pulses since the last substitution.

e.g.



The 3 in HDB3 refers to the coding format that precludes strings of zeros greater than 3. Note that violations are produced only in the fourth bit location of the substitution code and that successive substitutions produce alternate polarity violations.

Application Diagram



MS 1	MS 2	SELECTS
0	0	AMI
0	1	B8ZS
1	0	B6ZS
1	1	HDB3

Timing Waveforms

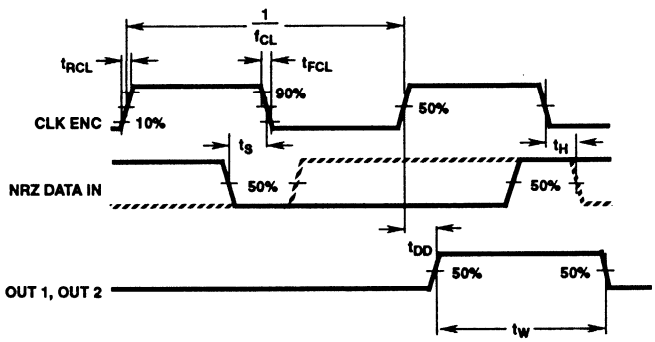


FIGURE 1. TRANSMITTER (CODER) TIMING WAVEFORMS

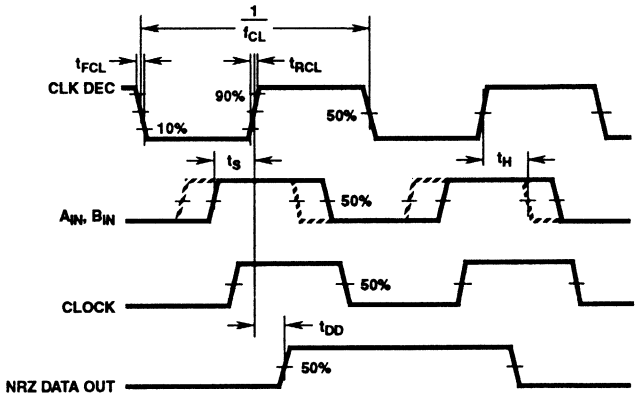


FIGURE 2. RECEIVER (DECODER) TIMING WAVEFORMS

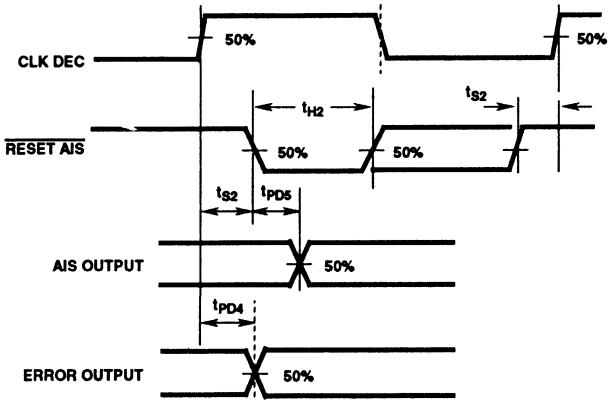


FIGURE 3. $\overline{\text{RESET AIS}}$ INPUT, AIS OUTPUT, ERROR OUTPUT

Timing Waveforms (Continued)

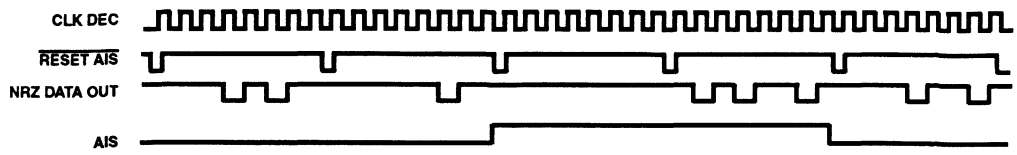


FIGURE 4.

Two consecutive periods of $\overline{\text{Reset AIS}}$, each containing less than three zeros, sets AIS to a logic '1' and remains in a logic '1' state until a period of $\overline{\text{Reset AIS}}$ contains three or more zeros

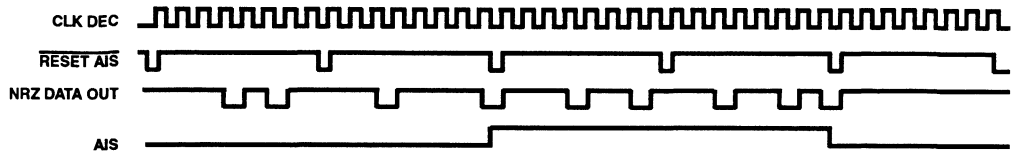


FIGURE 5.

Zeros which occur during a high to low transition of $\overline{\text{Reset AIS}}$ are counted with the zeros that occurred before the high to low transition.

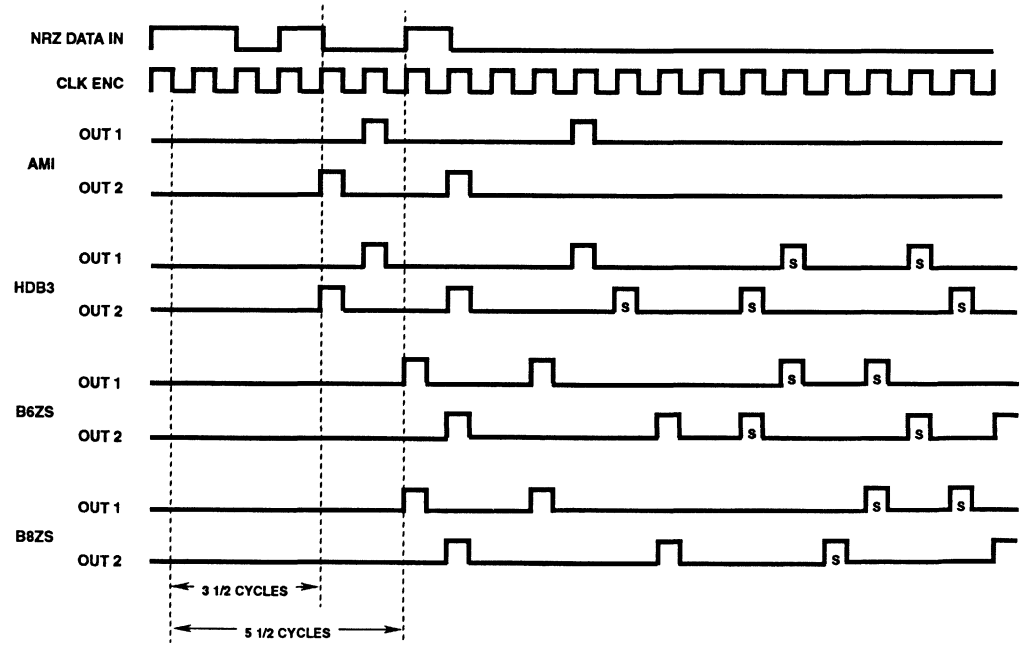


FIGURE 6. ENCODE TIMING AND DELAY

Data is clocked on the negative edge of CLK ENC and appears on Out 1 and Out 2. Out 1 and Out 2 are interchangeable. Bipolar violations and all other pulses inserted by the line coding scheme to encode strings of zeros are labeled with an "S".

Timing Waveforms (Continued)

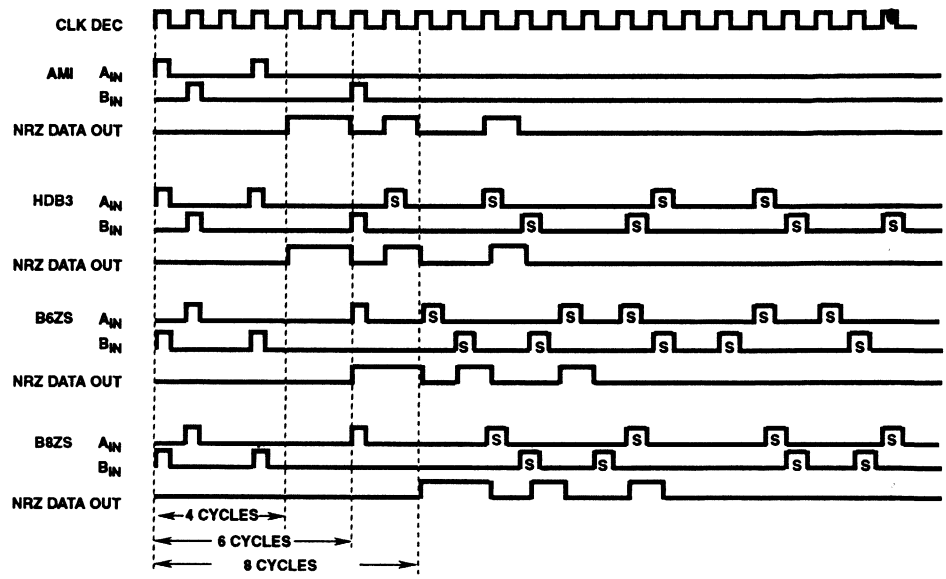


FIGURE 7. DECODE TIMING AND DELAY

Data that appears on A_{IN} and B_{IN} is clocked by the positive edge of CLK DEC, decoded, and zeros are inserted for all valid line code substitutions. The data then appears in non-return to zero to zero form at output NRZ Data Out. A_{IN} and B_{IN} are interchangeable.

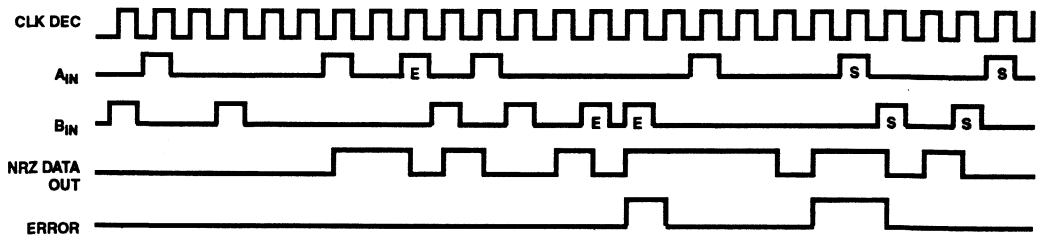


FIGURE 8.

The ERROR signal indicates bipolar violations that are not part of a valid substitution.

HARRIS SEMICONDUCTOR

HC-55536

Continuous Variable Slope Delta-Demodulator (CVSD)

March 1993

Features

- All Digital
- Requires Few External Parts
- Low Power Drain: 1.5mW from Single 3V-6V Supply
- Time Constants Determined by Clock Frequency; No Calibration or Drift Problems; Automatic Offset Adjustment
- Filter Reset by Digital Control
- Automatic Overload Recovery
- Automatic "Quiet" Pattern Generation

Applications

- Voice Decoder for Digital Systems and Speech Syntheses
- Voicemail
- Audio Manipulations; Delay Lines, Echo Generation/ Suppression, Special Effects, etc.
- Pagers/Satellites

Description

The HC-55536 is a CMOS integrated circuit used to convert serial NRZ digital data to an analog (voice) signal. Conversion is by delta demodulation, using the Continuously Variable Slope (CVSD) method of demodulation.

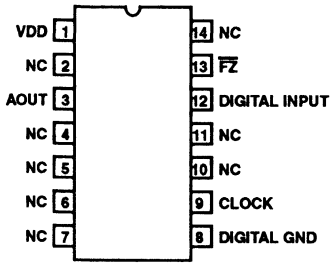
While signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by digital filters which use very low power and require no external timing components. This digital approach allows inclusion of many desirable features, which otherwise would be difficult to implement. The device is usable from 9Kbits/sec to above 64kbits/sec, and may be easily configured with the HC-55564 CVSD for a complete transmit/receive voice channel.

Ordering Information

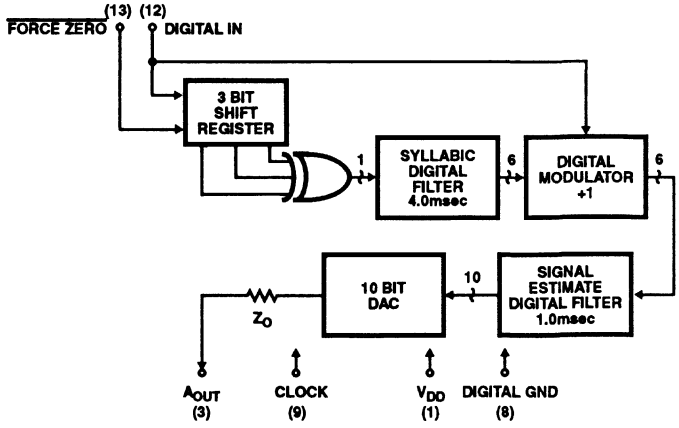
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HC1-55536-5	0°C to +75°C	14 Lead Ceramic DIP
HC1-55536-9	-40°C to +85°C	14 Lead Ceramic DIP
HC3-55536-5	0°C to +75°C	14 Lead Plastic DIP
HC3-55536-9	-40°C to +85°C	14 Lead Plastic DIP

Pinout

HC-55536
(PDIP, CDIP)
TOP VIEW



Functional Diagram



File Number **2888.1**

Absolute Maximum Ratings

Voltage at Any Pin ..... GND -0.3V to VDD +0.3V
Maximum V_{DD} Voltage ..... +7.0V
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HC-55536-5 ..... 0°C to +75°C
HC-55536-9 ..... -40°C to +85°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C
Operating V_{DD} Range ..... +3.0V to +6.0V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{DD} = +5.0V; Bit Rate = 16K Bits/sec; Typical Parameters are at +25°C. Min-Max parameters are over Operating Temperature, Unless Otherwise Specified.

PARAMETERS	SYMBOL	LIMITS			UNITS	NOTES
		MIN	TYP	MAX		
Clock Sampling Rate	CLK	9	16	64	Kbps	1
Clock Duty Cycle	I_{DD}	30		70	%	
Supply Current	V_{OH}		0.3	1.5	mA	
Logic "1" Input	V_{IH}	3.5	4.5		V	2
Logic "0" Input	V_{IL}			1.5	V	2
Audio Output Voltage	A_{OUT}		0.5	1.2	V_{RMS}	3
Audio Output Impedance	Z_{OUT}		150		kΩ	4
Syllabic Filter Time Constant	t_{SF}		4.0		ms	5
Signal Estimate Filter Time Constant	t_{SE}		1.0		ms	5
Step Size Ratio	SSR		24		dB	6
Minimum Step Size	MSS		0.1		$\%V_{DD}$	7
Signal/Noise Ratio	SNR	25			dB	8
Quieting Pattern Amplitude	VQP		10		mV_{P-P}	9
Clamping Threshold	VA_{TH}		0.75		F.S.	10

NOTES:

1. There is one NRZ data bit per clock period. Clock must be phased with digital data such that a positive clock transition occurs in the middle of each received data bit. Clock may be run at greater than 64kbps or less than 9kbps.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate and changes with negative clock transitions.
3. This output includes a DC bias of $V_{DD}/2$; therefore, an AC coupling capacitor is required unless the output filter also includes this bias.
4. Presents approximately 150kΩ in series with recovered audio voltage. Zero-signal reference is $V_{DD}/2$.
5. Note that filter time constants are inversely proportional to clock rate. Both filters approximate single pole responses.
6. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimum output.
7. The minimum audio output voltage that can be produced by the internal DAC.
8. Input signal encoded $1.2V_{RMS}$ 250Hz sinusoid.
9. The "quieting" pattern or idle-channel audio output steps at $^1/_2$ the bit rate, changing state on negative clock transitions.
10. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

Pin Description

PIN NUMBER	SYMBOL	DESCRIPTION
1	V_{DD}	Positive supply voltage.
2	NC	No internal connection is made to this pin.
3	Audio Out	Recovered audio out. Presents approximately 150kΩ source with DC offset of $V_{DD}/2$. Should be externally AC coupled.
4, 5, 6, 7	NC	No internal connection is made to these pins.
8	Digital GND	Logic Ground.
9	Clock	Sampling rote clock must be synchronized with the digital input data such that the data is valid at the positive clock transition.
10, 11	NC	No internal connection is made to these pins.
12	Digital In	Input for the received serial NRZ digital data.
13	$\overline{FZ}$	Active low logic input. Activating this input resets the internal logic and forces the recovered audio output into the "quieting" condition.
14	NC	No internal connection is made to this pin.

NOTE: No active input should be left in a "floating condition".

Die Characteristic

Transistor Count 1790
Die Dimensions ..... 147 x 82 mils
Substrate Potential ..... $+V_{DD}$
Process ..... BiMOSE

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	70	20
Plastic DIP	85	-

Figure 1 illustrates the frequency response of the HC-55536 for varying input levels. To prevent slope overload (slew rate limiting) do not exceed the 0dB boundary. The frequency response is directly proportional to the sampling rate. The output levels were measured after filtering.

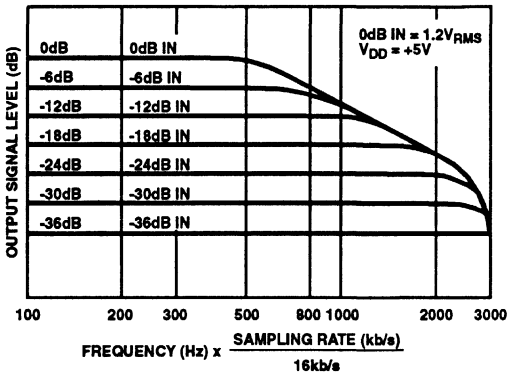
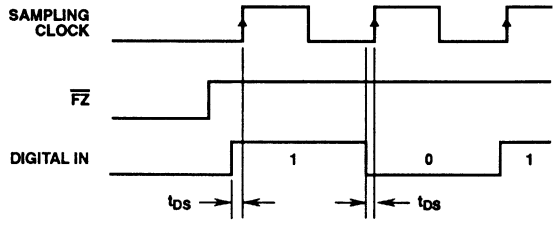


FIGURE 1. TRANSFER FUNCTION FOR CVSD AT 16kbps

Timing Waveforms

CVSD TIMING DIAGRAM



t_{DS}: DATA SET UP TIME 100ns TYPICAL

HARRIS SEMICONDUCTOR

HC-55564

Continuously Variable Slope Delta-Modulator (CVSD)

March 1993

Features

- All Digital
- Requires Few External Parts
- Low Power Drain: 1.5mW Typical From Single 3V - 6V Supply
- Time Constants Determined by Clock Frequency; No Calibration or Drift Problems: Automatic Offset Adjustment
- Half Duplex Operation Under Digital Control
- Filter Reset Under Digital Control
- Automatic Overload Recovery
- Automatic "Quiet" Pattern Generation
- AGC Control Signal Available

Applications

- Voice Transmission Over Data Channels (Modems)
- Voice/Data Multiplexing (Pair Gain)
- Voice Encryption/Scrambling
- Voicemail
- Audio Manipulations: Delay Lines, Time Compression, Echo Generation/Suppression, Special Effects, etc.
- Pagers/Satellites
- Data Acquisition Systems
- Voice I/O for Digital Systems and Speech Synthesis Requiring Small Size, Low Weight, and Ease of Reprogrammability

Description

The HC-55564 is a half duplex modulator/demodulator CMOS intergrated circuit used to convert voice signals into serial NRZ digital data and to reconvert that data into voice. The conversion is by delta-modulation, using the Continuously Variable Slope (CVSD) method of modulation/demodulation.

While the signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by very low power digital filters which require no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

The fundamental advantages of delta-modulation, along with its simplicity and serial data format, provide an efficient (low data rate/low memory requirements) method for voice digitization.

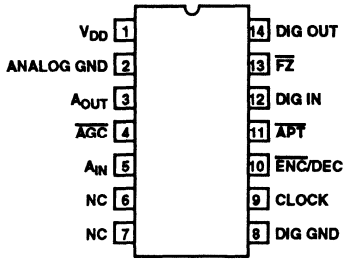
The HC-55564 is usable from 9k bits/sec to above 64kbps. See the Harris Military databook for a Mil-Std-883C compliant CVSD. Application Notes 607 and 576 are available.

Ordering Information

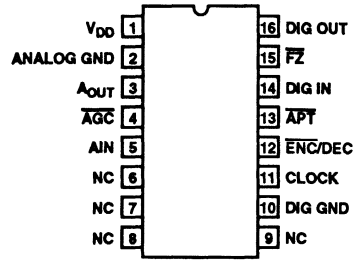
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HC1-55564-2	-55°C to +125°C	14 Lead Ceramic DIP
HC1-55564-5	0°C to +75°C	14 Lead Ceramic DIP
HC1-55564-9	-40°C to +85°C	14 Lead Ceramic DIP
HC3-55564-5	0°C to +75°C	14 Lead Plastic DIP
HC3-55564-9	-40°C to +85°C	14 Lead Plastic DIP
HC9-55564-5	0°C to +75°C	16 Lead Wide Body SOIC
HC9-55564-9	-40°C to +85°C	16 Lead Wide Body SOIC

Pinouts

HC-55564
(PDIP, CDIP)
TOP VIEW



HC-55564
(300 mil SOIC)
TOP VIEW



8 TELECOM

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2889.1**

Absolute Maximum Ratings

Voltage at Any Pin ..... GND -0.3V to V_{DD} +0.3V
Maximum V_{DD} Voltage ..... +7.0V
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HC-55564-5, -7 ..... 0°C to +75°C
HC-55564-9 ..... -40°C to +85°C
HC-55564-2 ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Operating V_{DD} ..... +3.0V to +6.0V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Unless Otherwise Specified, typical parameters are at +25°C, Min-Max are over operating temperature ranges. V_{DD} = +5.0V, Sampling Rate = 16Kbps, AG = DG = 0V, A_{IN} = 1.2Vrms.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
CLK	Sampling Rate	9	16	64	kbps	Note 1
I_{DD}	Supply Current	-	0.3	1.5	mA	
V_{IH}	Logic '1' Input	3.5	-	-	V	Note 2
V_{IL}	Logic '0' Input	-	-	1.5	V	Note 2
V_{OH}	Logic '1' Output	4.0	-	-	V	Note 3
V_{OL}	Logic '0' Output	-	-	0.4	V	Note 3
	Clock Duty Cycle	30	-	70	%	
A_{IN}	Audio Input Voltage	-	0.5	1.2	V_{RMS}	AC Coupled. Note 4
A_{OUT}	Audio Output Voltage	-	0.5	1.2	V_{RMS}	AC Coupled. Note 5
Z_{IN}	Audio Input Impedance	-	280	-	kΩ	Note 6
Z_{OUT}	Audio Output Impedance	-	150	-	kΩ	Note 6
A_{E-D}	Transfer Gain	-2.0	-	+2.0	dB	No Load, Audio In to Audio Out.
t_{SF}	Syllabic Filter Time Constant	-	4.0	-	ms	Note 7
t_{SE}	Signal Estimate Filter Time Constant	1.0	-	-	ms	Note 7
RES	Resolution	-	6	-	mV_P	A_{IN} at 100Hz. Note 8
MSS	Minimum Step Size	-	0.1	-	$\%V_{DD}$	Note 9
V_{QP}	Quieting Pattern Amplitude	-	10	-	mV_{P-P}	$\overline{FZ}$ = 0V or $\overline{APT}$ = 0V. Note 10
V_{ATH}	AGC Threshold	-	0.1	-	F.S.	Note 11
V_{CTH}	Clamping Threshold	-	0.75	-	F.S.	Note 12

NOTES:

1. There is one NRZ (Non-Return Zero) data bit per clock period. Data is clocked out on the negative clock edge. Data is clocked into the CVSD on the positive going edge (see Figure 2). Clock may be run at less than 9kbps and greater than 64kbps.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.
3. Logic outputs are CMOS compatible at supply voltage and will withstand short-circuits to V_{DD} or ground. Digital data output is NRZ and changes with negative clock transitions. Each output will drive one LS TTL load.
4. Recommended voice input range for best voice performance. Should be externally AC coupled.
5. May be used for side-tone in encode mode. Should be externally AC coupled. Varies with audio input level by ±2dB.
6. Presents series impedance with audio signal. Zero signal reference is approximately $V_{DD}/2$.
7. Note that filter time constants are inversely proportional to clock rate. Both filters approximate single pole responses.
8. The minimum audio input voltage above which encoding takes place.
9. The minimum audio output voltage change that can be produced by the internal DAC.
10. Settled value, the "quieting" pattern or idle-channel audio output steps at one-half the bit rate, changing state on negative clock transitions.
11. A logic "0" will appear at the AGC output pin when the recovered signal reaches one-half of full-scale value (positive or negative), i.e. at $V_{DD}/2$ ±25% of V_{DD}.
12. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

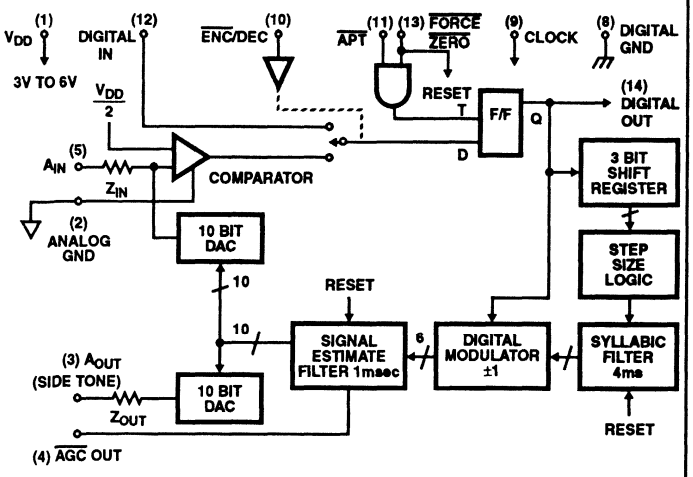
Pin Description

PIN NUMBER 14 LEAD DIP	SYMBOL	DESCRIPTION
1	V_{DD}	Positive Supply Voltage. Voltage range is +3.0V to +6.0V.
2	Analog GND	Analog Ground connection to D/A ladders and comparator.
3	A_{OUT}	Audio Out recovered from 10 bit DAC. May be used as side tone at the transmitter. Presents approximately 150 kilohm source with D.C. offset of $V_{DD}/2$. Within ±2dB of Audio Input. Should be externally AC coupled.
4	$\overline{AGC}$	Automatic Gain Control output. A logic low level will appear at this output when the recovered signal excursion reaches one-half of full scale value. In each half cycle full scale is $V_{DD}/2$. The mark-space ratio is proportional to the average signal level.
5	A_{IN}	Audio Input to comparator. Should be externally AC coupled. Presents approximately 280kΩ in series with $V_{DD}/2$.
6, 7	NC	No internal connection is made to these pins.
8	Digital GND	Logic ground. 0V reference for all logic inputs and outputs.
9	Clock	Sampling rate clock. In the decode mode, must be synchronized with the digital input data such that the data is valid at the positive clock transition. In the encode mode, the digital data is clocked out on the negative going clock transition. The clock rate equals the data rate.
10	$\overline{Encode}$/ Decode	A single CVSD can provide half-duplex operation. The encode or decode function is selected by the logic level applied to this input. A low level selects the encode mode, a high level the decode mode.
11	$\overline{APT}$	Alternate Plain Text input. Activating this input caused a digital quieting pattern to be transmitted, however; internally the CVSD is still functional and a signal is still available at the A_{OUT} port. Active low.
12	Digital In	Input for the received digital NRZ data.
13	$\overline{FZ}$	Force Zero input. Activating this input resets the internal logic and forces the digital output and the recovered audio output into the "quieting" condition. An alternating 1-0 pattern appears at the digital output at 1/2 the clock rate. When this is decoded by a receive CVSD, a $10mV_{P-P}$ inaudible signal appears at audio output. Active low.
14	Digital Out	Output for transmitted digital NRZ data.

NOTE:

1. No active input should be left in a "floating condition."

Functional Diagram (DIP PIN NUMBERS SHOWN)



Die Characteristics

Transistor Count	1897	
Die Dimensions	147 x 82	
Substrate Potential	$+V_{DD}$	
Process	BiMOSE	
Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	70	20
Plastic DIP	85	-
SOIC	98	-

Timing Waveforms

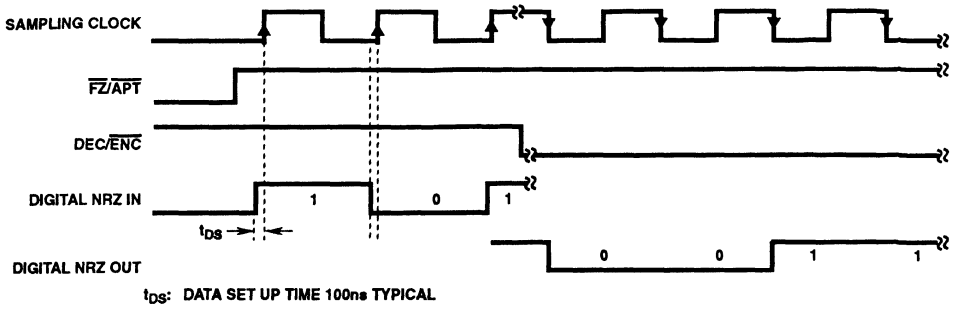


FIGURE 2. CVSD TIMING DIAGRAM

Interface Circuit for HC-55564 CVSD (DIP PIN NUMBERS SHOWN)

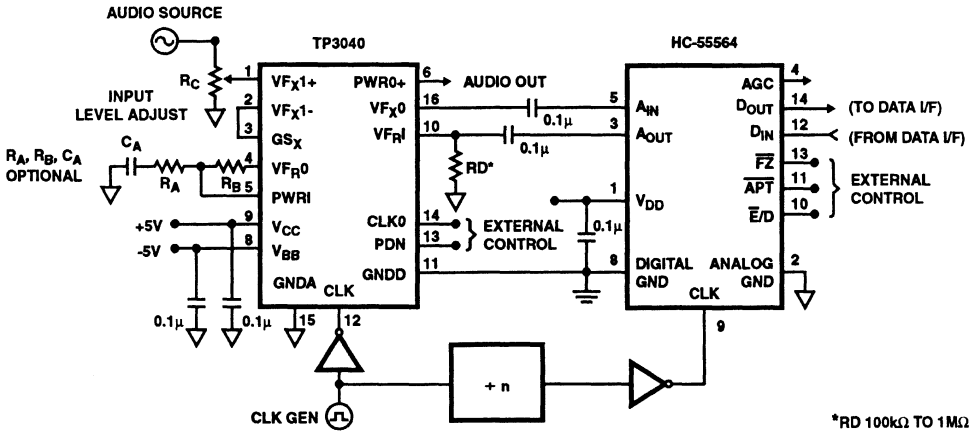


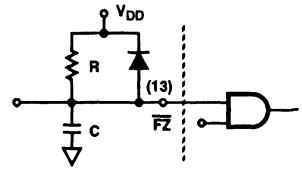
FIGURE 3.

CVSD Hookup for Evaluation

The circuit in Figure 3 is sufficient to evaluate the voice quality of the CVSD, since when encoding, the feedback signal at the audio output pin is the reconstructed audio input signal.

CVSD design considerations are as follows:

1. Care should be taken in layout to maintain isolation between analog and digital signal paths for proper noise consideration.
2. Power supply decoupling is necessary as close to the device as possible. A 0.1µf should be sufficient.
3. Ground, then power, must be present before any input signals are applied to the CVSD. Failure to observe this may cause a latchup condition which may be destructive. Latchup may be removed by cycling the power off/on. A power-up reset circuit may be used that strobes Force Zero (Pin 13) during power-up as follows:
4. Analog (signal) ground (Pin 2) should be externally tied to Digital GND (Pin 8) and power supply ground. It is recommended that the A_{IN} and A_{OUT} ground returns connect only to Pin 2.
5. Digital inputs and outputs are compatible with standard CMOS logic using the same supply voltage. All unused logic inputs must be tied to the appropriate logic level for desired operation. It is recommended that unused inputs tied high be done so through a pull-up resistor (1K - 10kΩ). TTL outputs will require 1kΩ pull-up resistors. Pins 4 and 14 will each drive CMOS logic or one low power TTL input.
6. Since the Audio Out pins are internally DC biased to $V_{DD}/2$, AC coupling is required. In general, a value of 0.1µf is sufficient for AC coupling of the CVSD audio pins to a filter circuit.
7. The AGC output may be externally integrated to drive an AGC pre-amp, or it could drive an LED indicator through a buffer to indicate proper speaking volume.



Figures 4, 5, and 6 illustrate the typical frequency response of the HC-55564 for varying input levels and for varying sampling rates. To prevent slope overload (slew limiting), the 0dB boundary should not be exceeded. The frequency response is directly proportional to the sampling clock rate. The flat bandwidth at 0dB doubles for every doubling in sampling rate. The output levels were measured in the encode mode, without filtering, from A_{IN} to A_{OUT}, at V_{DD} = +5V.
0dB = $1.2V_{RMS}$.

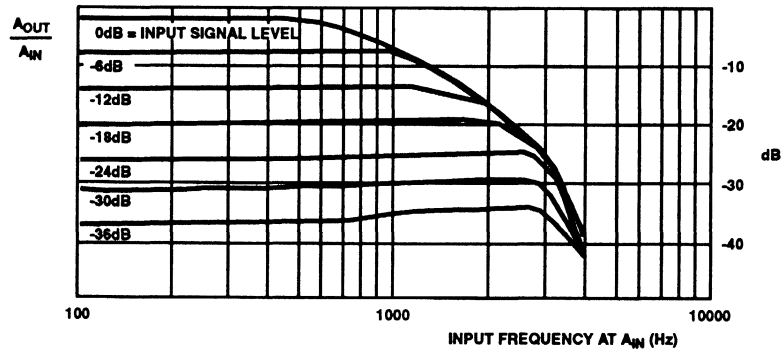


FIGURE 4. 16kbps

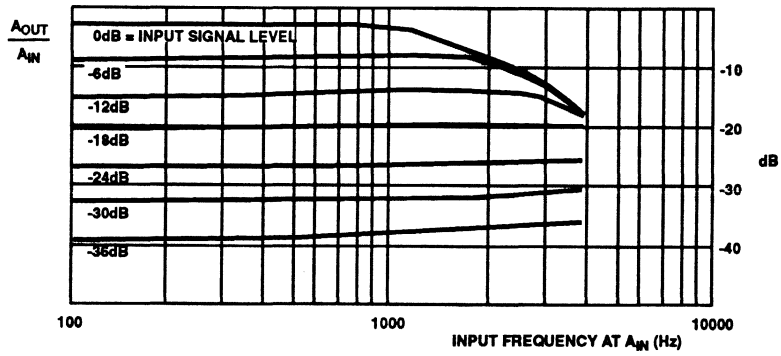


FIGURE 5. 32kbps

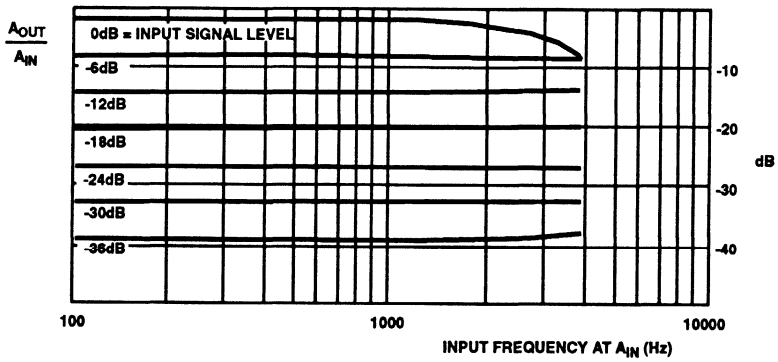


FIGURE 6. 64kbps

The following typical performance distortion graphs were realized with the test configuration of Figure 7. The measurement vehicle for Total Harmonic Distortion (THD) was an HP-339A distortion measurement set, and for 2nd and 3rd harmonic distortion, an HP-3582A spectrum analyzer. All measurement conditions were at V_{DD} = +5V, and 2nd and 3rd harmonic distortion measurements were C-message filtered. 0dB = 1.2V_{RMS}.

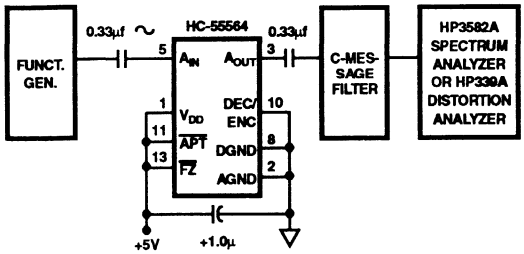


FIGURE 7. TEST AND MEASUREMENT CIRCUIT

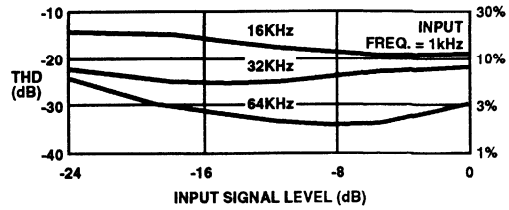
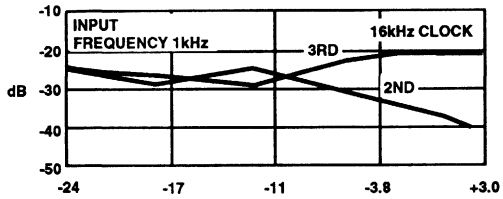


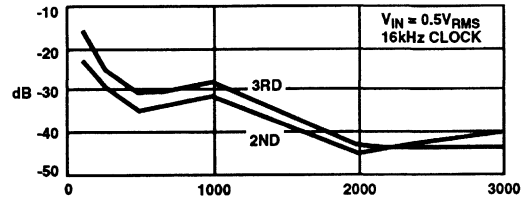
FIGURE 8. CVSD SIGNAL LEVEL vs TOTAL HARMONIC DISTORTION

CVSD INPUT LEVEL vs 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED



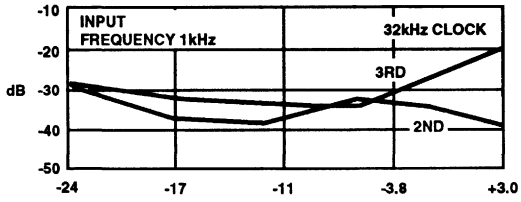
(A)

CVSD SIGNAL TO 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED



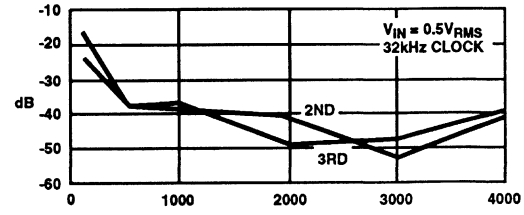
(A)

CVSD INPUT LEVEL vs 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED



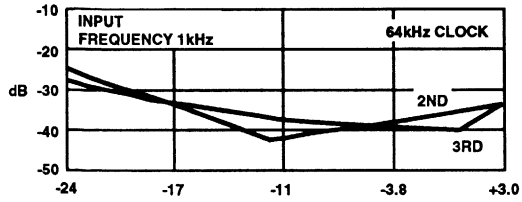
(B)

CVSD SIGNAL TO 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED



(B)

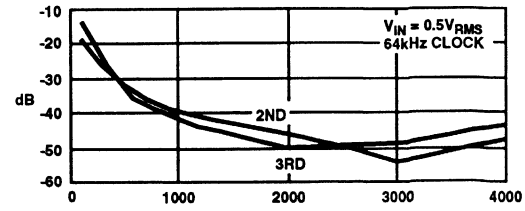
CVSD INPUT LEVEL vs 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED



(C)

FIGURE 9A, B, C. CVSD INPUT LEVEL vs 2ND AND 3RD HARMONIC DISTORTION

CVSD SIGNAL TO 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED



(C)

FIGURE 10A, B, C. CVSD INPUT FREQUENCY vs 2ND AND 3RD HARMONIC DISTORTION

LINEAR 9

HARRIS QUALITY AND RELIABILITY

Harris Quality

Introduction

Success in the integrated circuit industry means more than simply meeting or exceeding the demands of today's market. It also includes anticipating and accepting the challenges of the future. It results from a process of continuing improvement and evolution, with perfection as the constant goal.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force – from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added on or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of The Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. In addition to facilitating the development of SPC and DOX, Quality professionals support other continuous improvement tools such as control charts, measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs – with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress.

The Improvement Process

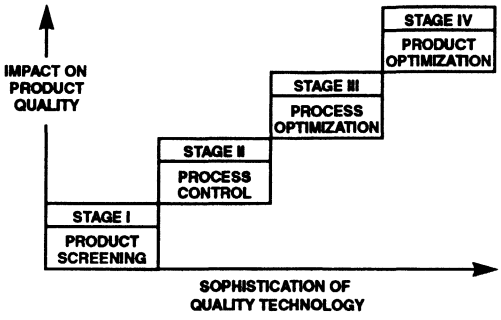


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage III to Stage IV, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

Designing for Manufacturability

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment.

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Wafer Fab	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Junction Depth	X	
	- Sheet Resistivities	X	
	- Defect Density	X	X
	- Critical Dimensions	X	X
	- Visual Inspection	X	X
	- Lot Acceptance	X	
	• Process		
	- Film Thickness	X	X
	- Implant Dosages	X	
	- Capacitance Voltage Changes	X	X
	- Conformance to Specification	X	X
	• Equipment		
	- Repeatability	X	X
	- Profiles	X	X
	- Calibration		X
	- Preventive Maintenance	X	X
Assembly	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Documentation Check		X
	- Dice Inspection	X	X
	- Wire Bond Pull Strength/Controls	X	X
	- Ball Bond Shear/Controls		X
	- Die Shear Controls		X
	- Post-Bond/Pre-Seal Visual	X	X
	- Fine/Gross Leak	X	X
	- PIND Test	X	
	- Lead Finish Visuals, Thickness	X	X
	- Solderability		X
	• Process		
	- Operator Quality Performance	X	X
	- Saw Controls	X	
	- Die Attach Temperatures	X	X
	- Seal Parameters	X	
	- Seal Temperature Profile	X	X
	- Sta-Bake Profile	X	
	- Temp Cycle Chamber Temperature	X	X
	- ESD Protection	X	X
	- Plating Bath Controls	X	X
	- Mold Parameters	X	X

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (Continued)

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Test	• JAN Self-Audit		X
	• Temperature/Humidity	X	
	• ESD Controls	X	
	• Temperature Test Calibration	X	
	• Test System Calibration	X	
	• Test Procedures		X
	• Control Unit Compliance	X	
	• Lot Acceptance Conformance	X	
	• Group A Lot Acceptance		X
Probe	• JAN Self-Audit		X
	• Wafer Repeat Correlation	X	
	• Visual Requirements	X	X
	• Documentation	X	X
	• Process Performance	X	X
Burn-In	• JAN Self-Audit		X
	• Functionality Board Check	X	
	• Oven Temperature Controls	X	
	• Procedural Conformance		X
Brand	• JAN Self-Audit		X
	• ESD Controls	X	X
	• Brand Permanency	X	X
	• Temperature/Humidity	X	
	• Procedural Conformance		X
QCI Inspection	• JAN Self-Audit		X
	• Group B Conformance		X
	• Group C and D Conformance		X

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 2).

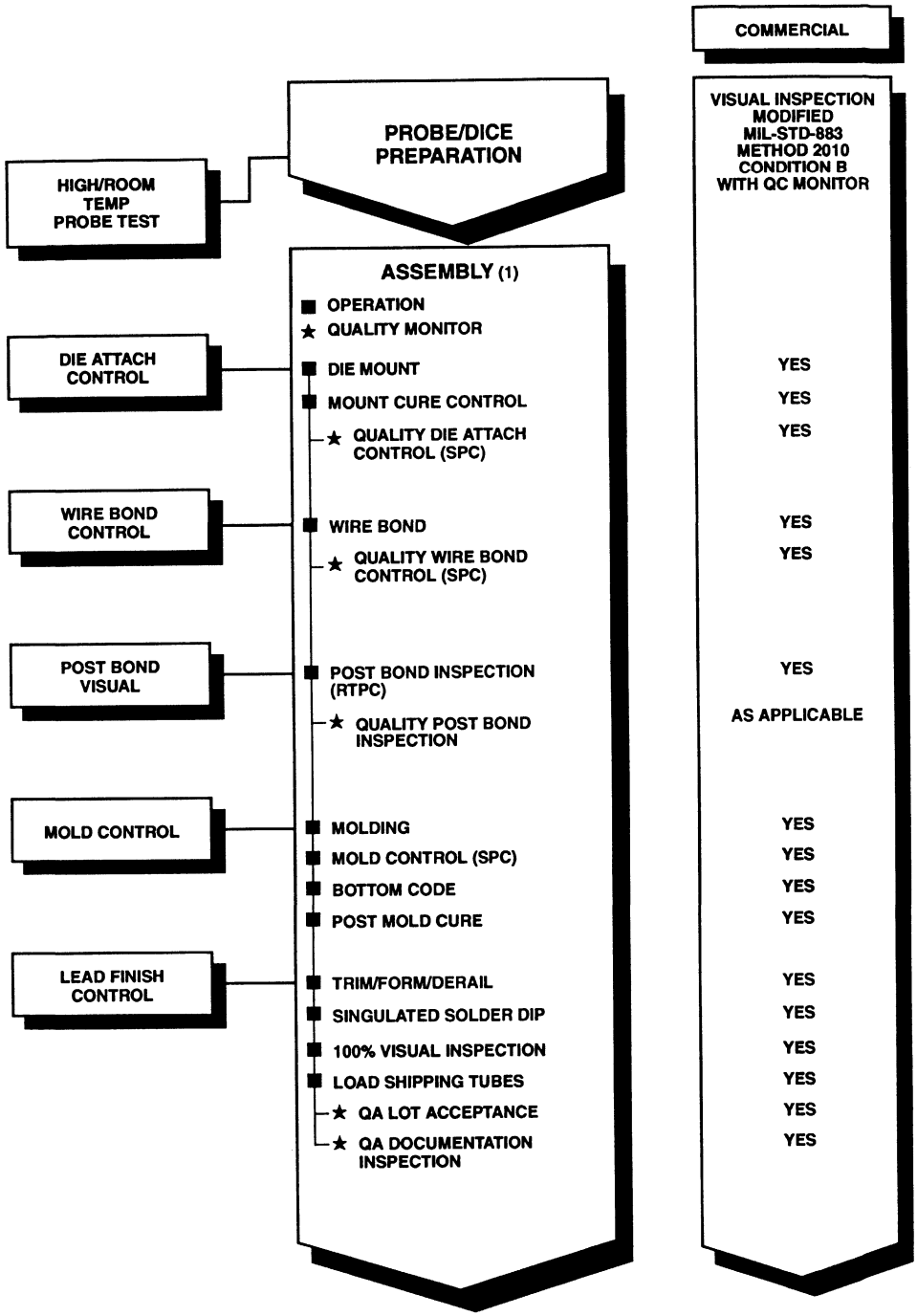
TABLE 2. HARRIS I.C. DESIGN TOOLS

DESIGN STEP	PRODUCTS	
	ANALOG	DIGITAL
Functional Simulation	Cds Spice	Cds Spice Verilog
Parametric Simulation	Cds Spice Monte Carlo	Cds Spice
Schematic Capture	Cadence	Cadence
Functional Checking	Cadence	Cadence
Rules Checking	Cadence	Cadence
Parasitic Extraction	Cadence	Cadence

Special Testing

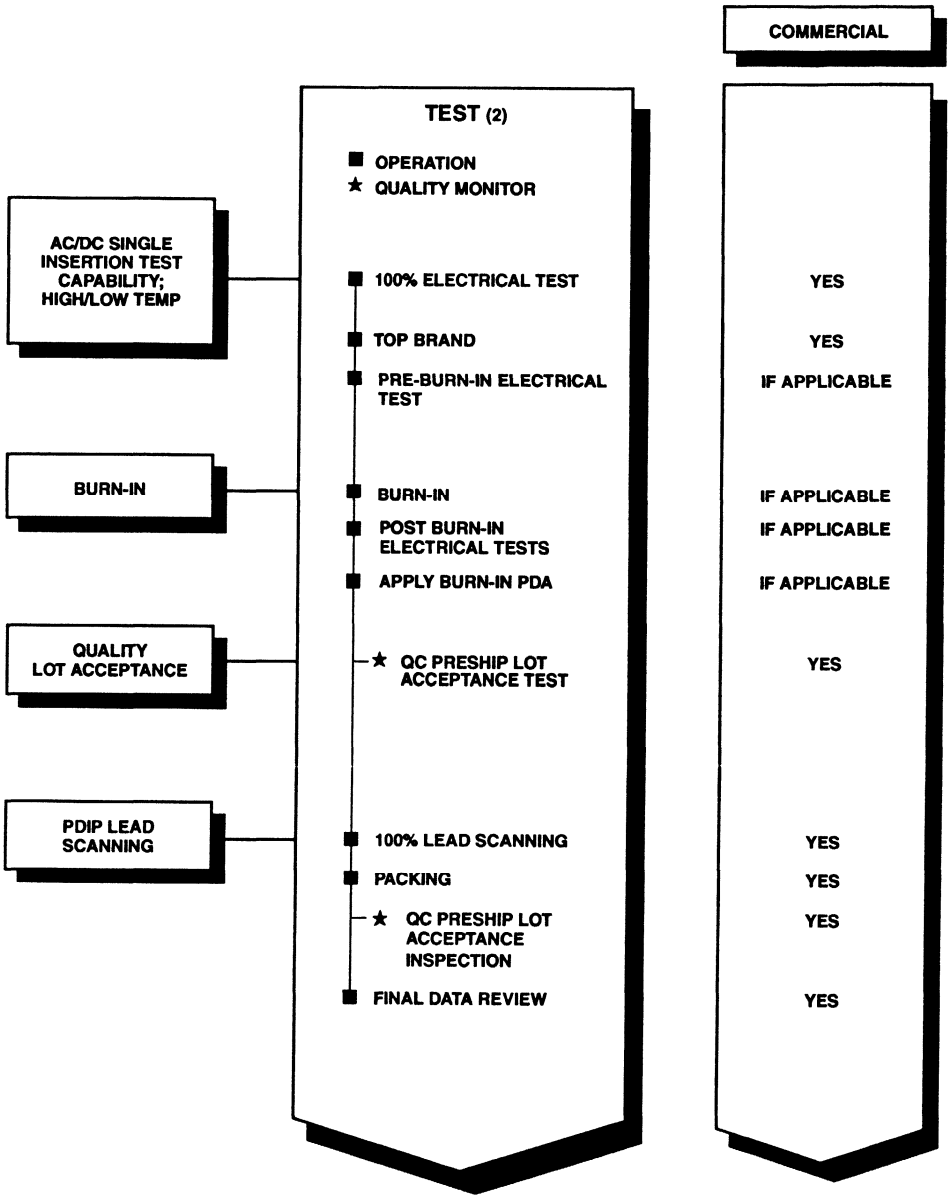
Harris Semiconductor offers several standard screen flows to support a customer's need for additional testing and reliability assurance. These flows include environmental stress testing, burn-in, and electrical testing at temperatures other than +25°C. The flows shown on pages 9-6 and 9-7 indicate the Harris standard processing flows for a Commercial Linear part in PDIP Package. In addition, Harris can supply products tested to customer specifications both for electrical requirements and for nonstandard environmental stress screening. Consult your field sales representative for details.

Harris Semiconductor Standard Processing Flows



(1) Example for a PDIP Package Part

Harris Semiconductor Standard Processing Flow (Continued)



(2) Example for a Linear Part in PDIP Package

TABLE 3. SUMMARIZING CONTROL APPLICATIONS

FAB			
• Diffusion - Junction Depth - Sheet Resistivities - Oxide Thickness - Implant Dose Calibration - Uniformity	• Thin Film - Film Thickness - Uniformity - Refractive Index - Film Composition	• Photo Resist - Critical Dimension - Resist Thickness - Etch Rates	• Measurement Equipment - Critical Dimension - Film Thickness - 4 Point Probe - Ellipsometer
ASSEMBLY			
• Pre-Seal - Die Prep Visuals - Yields - Die Attach Heater Block - Die Shear - Wire Pull - Ball Bond Shear - Saw Blade Wear - Pre-Cap Visuals	• Post-Seal - Internal Package Moisture - Tin Plate Thickness - PIND Defect Rate - Solder Thickness - Leak Tests - Module Rm. Solder Pot Temp. - Seal - Temperature Cycle	• Measurement - XRF - Radiation Counter - Thermocouples - GM-Force Measurement	
TEST			
	- Handlers/Test System - Defect Pareto Charts - Lot % Defective - ESD Failures per Month	- Monitor Failures - Lead Strengthening Quality - After Burn-In PDA	
OTHER			
• IQC - Vendor Performance - Material Criteria - Quality Levels	• Environment - Water Quality - Clean Room Control - Temperature - Humidity	• IQC Measurement/Analysis - XRF - ADE - 4 Point Probe - Chemical Analysis Equipment	

Controlling and Improving the Manufacturing Process - SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use control charts to determine the normal variabilities in processes, materials, and products. Critical process variables and performance characteristics are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that an operation is outside the process control limits or indicates a nonrandom pattern inside the limits. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 3 lists some typical manufacturing applications of control charts at Harris Semiconductor.

SPC is important, but still considered only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost. (See Table 4).

TABLE 4. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

	STAGE	APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at reducing the number of defects by studying the key variables controlling the process, and optimizing the procedures or design to yield the best result. This approach is a more time-consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in MIL-STD-883 and MIL-M-38510 are used by our quality inspectors.

The focus on this quality parameter has resulted in a continuous improvement to less than 100 PPM, and the goal is to continue improvement toward 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of Harris statisticians, private consultants, and internally developed programs, training of engineers, supervisors, and operators/technicians has been an ongoing activity in Harris Semiconductor.

Over the past years, Harris has also deployed a comprehensive training program for hourly operators and supervisors in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

Incoming Materials

Improving the quality and reducing the variability of critical incoming materials is essential to product quality enhancement, yield improvement, and cost control. With the use of statistical techniques, the influence of silicon, chemicals, gases and other materials on manufacturing is highly measurable. Current measurements indicate that results are best achieved when materials feeding a statistically controlled manufacturing line have also been produced by statistically controlled vendor processes.

To assure optimum quality of all incoming materials, Harris has initiated an aggressive program, linking key suppliers with our manufacturing lines. This user-supplier network is the Harris Vendor Certification process by which strategic vendors, who have performance histories of the highest quality, participate with Harris in a lined network; the vendor's factory acts as if it were a beginning of the Harris production line.

SPC seminars, development of open working relationships, understanding of Harris' manufacturing needs and vendor capabilities, and continual improvement programs are all part of the certification process. The sole use of engineering limits no longer is the only quantitative requirement of incoming materials.

TABLE 5. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	TOPICS COVERED
SPC, Basic	Manufacturing Operators, Non-Manufacturing Personnel	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts
SPC, Intermediate	Manufacturing Supervisors, Technicians	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Introduction to Capability
SPC, Advanced	Manufacturing Engineers, Manufacturing Managers	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Advanced Control Charts, Variance Component Analysis, Capability Analysis
Design of Experiments (DOX)	Engineers, Managers	Factorial and Fractional Designs, Blocking Designs, Nested Models, Analysis of Variance, Normal Probability Plots, Statistical Intervals, Variance Component Analysis, Multiple Comparison Procedures, Hypothesis Testing, Model Assumptions/Diagnostics
Regression	Engineers, Managers	Simple Linear Regression, Multiple Regression, Coefficient Interval Estimation, Diagnostic Tools, Variable Selection Techniques
Response Surface Methods (RSM)	Engineers, Managers	Steepest Ascent Methods, Second Order Models, Central Composite Designs, Contour Plots, Box-Behnken Designs

Specified requirements include centered means, statistical control limits, and the requirement that vendors deliver their products from their own statistically evaluated, in-control manufacturing processes.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Taper • Thickness • Total Thickness Variation • Backside Criteria • Oxygen • Carbon	• Equipment Capability Control Charts - Oxygen - Resistivity • Control Charts Related to - Enhanced Gettering - Total Thickness Variation - Total Indicated Reading - Particulates • Certificated of Analysis for all Critical Parameters • Control Charts from On-Line Processing • Certificate of Conformance
Chemicals/Photoresists/ Gases	• Chemicals - Assay - Major Contaminants • Molding Compounds - Spiral Flow - Thermal Characteristics • Gases - Impurities • Photoresists - Viscosity - Film Thickness - Solids - Pinholes	• Certificate of Analysis on all Critical Parameters • Certificate of Conformance • Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Water - Selected Parameters • Control Charts - Assay - Contaminants • Control Charts on - Photospeed - Thickness - UV Absorbance - Filterability - Water - Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Dimensional Characteristics • Certificate of Analysis for all Critical Parameters • Certificate of Conformance
Assembly Materials	• Visual Inspection • Physical Dimension Checks • Glass Composition • Bondability • Intermetallic Layer Adhesion • Ionic Contaminants • Thermal Characteristics • Lead Coplanarity • Plating Thickness • Hermeticity	• Certificate of Analysis • Certificate of Conformance • Process Control Charts on Outgoing Product Checks and In-Line Process Controls

Calibration Laboratory

Another important resource in the product assurance system is a calibration lab in each Harris Semiconductor operation site. These labs are responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both production and engineering areas. The accuracy of instruments used at Harris is traceable to a national standards. Each lab maintains a system which conforms to the current revision of MIL-STD-45662, "Calibration System Requirements."

Each instrument requiring calibration is assigned a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Manufacturing Science - CAM, JIT, TPM

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened - in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Just In Time (JIT)

The major focus of JIT is cycle time reduction and linear production. Significant improvements in these areas result in large benefits to the customer. JIT is a part of the Total Quality Management philosophy at Harris and includes Employee Involvement, Total Quality Control, and the total elimination of waste.

Some key JIT methods used for improvement are sequence of events analysis for the elimination of non-value added activities, demand/pull to improve production flow, TQC check points and Employee Involvement Teams using root cause analysis for problem solving.

JIT implementations at Harris Semiconductor have resulted in significant improvements in cycle time and linearity. The benefits from these improvements are better on time delivery, improved yield, and a more cost effective operation.

JIT, SPC, and TPM are complementary methodologies and used in conjunction with each other create a very powerful force for manufacturing improvement.

Total Productive Maintenance (TPM)

TPM or Total Productive Maintenance is a specific methodology which utilizes a definite set of principles and tools focusing on the improvement of equipment utilization. It focuses on the total elimination of the six major losses which are equipment failures, setup and adjustment, idling and minor stoppages, reduced speed, process defects, and reduced yield. A key measure of progress within TPM is the overall equipment effectiveness which indicates what percentage of the time is a particular equipment producing good parts. The basic TPM principles focus on maximum equipment utilization, autonomous maintenance, cross functional team involvement, and zero defects. There are some key tools within the TPM technical set which have proven to be very powerful to solve long standing problems. They are initial clean, P-M analysis, condition based maintenance, and quality maintenance.

Utilization of TPM has shown significant increases in utilization on many tools across the Sector and is rapidly becoming widespread and recognized as a very valuable tool to improve manufacturing competitiveness.

The major benefits of TPM are capital avoidance, reduced costs, increased capability, and increased quality. It is also very compatible with SPC techniques since SPC is a good stepping stone to TPM implementation and it is in turn a good stepping stone to JIT because a high overall equipment effectiveness guarantees the equipment to be available and operational at the right time as demanded by JIT.

Harris Reliability

The reliability operations for Harris Semiconductor are consolidated into three locations; in Palm Bay, Florida, and Research Triangle Park, North Carolina, for integrated circuits products, and Mountaintop, Pennsylvania for Power Discrete Products. This consolidation brought the reliability organizations together to form a team that possesses a broad cross section of expertise in:

- Custom Military
- Automotive ASICs
- Harsh Environment Plastic Packaging
- Advanced Methods for Design for Reliability (DFR)
- Strength in Power Semiconductor
- Chemical/Surface Analysis Capabilities

The reliability focus is customer satisfaction (external and internal) and is accomplished through the development of standards, performance metrics and service systems. These major systems are summarized below:

- A process and product development system which emphasizes getting new products to market over product design. Uses empowered cross functional development teams.
- Standard test vehicles (96 in all) for process characterization of wearout failure mechanisms using conventional stresses (for modeling FITs/MTTF) and wafer level reliability characterization during development.
- Common qualification standards and philosophy for all sites and developments.
- Matrix monitor standard - a reliability monitoring system for products in production to insure ongoing reliability and verification of continuous improvement.
- Field return failure analysis system deployed world wide to track and expedite root cause analysis and irreversible corrective actions in a timely manner for our customers. The system is called by the team name PFAST, Product Failure Analysis Solution Team. Failure analysis sites are located in Brussels, Mountaintop, Palm Bay, Singapore, Kuala Lumpur, and Hong Kong. In order to optimize our response time to the customer all locations are networked for optimum communication, trend analysis, and performance tracking.

Integrated circuits reliability home base is in Palm Bay, Florida. This new facility has consolidated the reliability organization of the standard products divisions reliability group from Palm Bay, Florida; Somerville, New Jersey; Santa Clara, California, and the Military and Aerospace Division in Palm Bay, Florida. This facility contains

- A 9,000 square foot reliability analysis laboratory,
- An 8,000 square foot reliability stress testing facility,
- A 5,000 square foot analytical (chemistry/surface analysis) laboratory,
- A 3,000 square foot of engineering office space.

The facilities are well equipped and manned with highly trained and disciplined analysts. The reliability facilities are JAN certified and certified by a host of customers including major automotive and telecommunications companies.

Process/Product/Package Qualifications

Qualification activities at Harris begin with the in-depth qualification of new wafer processes. These process qualifications focus on the use of test vehicles to characterize wearout mechanisms for each process. These data are used to establish design ground rules for each process to eliminate wearout failure during the useful life of the product. Products designed within the established ground rules are qualified individually prior to introduction. New package configurations are qualified individually prior to being available for new products. Harris qualification procedures are specified via controlled documentation.

Product/Package Reliability Monitors

Many of the accelerated stress-tests used during initial reliability qualification are also employed during the routine monitoring of standard production product. Harris' continuing reliability monitoring program consists of three groups of stress tests, labeled Matrix I, II and III. As an example, Table 7 outlines the Matrix tests used to monitor plastic packaged CMOS Logic ICs in Harris' Malaysia assembly plant, where each wafer fab technology is sampled weekly for both Matrix I and II. Matrix I consists of highly accelerated, short duration (48 hours or less) tests, which provide real-time feedback on product reliability. Matrix II consists of the more traditional, longer term stress-tests, which are similar to those used for product qualification. Finally, Matrix III, performed monthly on each package style, monitors the mechanical reliability aspects of the package. Any failures occurring on the Matrix monitors are fully analyzed and the failure mechanisms identified, with corrective actions obtained from Manufacturing and Engineering. This information along with all of the test results are routinely transmitted to a central data base in Reliability Engineering, where failure rate trends are analyzed and tracked on an ongoing basis. These data are used to drive product improvements, so as to ensure that failure rates are continuously being reduced over time.

TABLE 7. PLASTIC PACKAGED CMOS LOGIC ICS MALAYSIA RELIABILITY MONITORING TESTS.

MATRIX I

TEST	CONDITIONS	DURATION	SAMPLE
Bias Life	+175°C	48 Hours	40
HAST	+145°C, 85% RH	20 Hours	40

TABLE 7. PLASTIC PACKAGED CMOS LOGIC ICS MALAYSIA RELIABILITY MONITORING TESTS (Continued)

MATRIX II

TEST	CONDITIONS	DURATION	SAMPLE
Bias Life	+125°C	1000 Hours	50
Dynamic Life	+125°C	1000 Hours	50
Biased Humidity	+85°C, 85% RH	1000 Hours	50
Autoclave	15 PSIG, +121°C, 100% RH	192 Hours	50
Storage Life	+150°C	1000 Hours	50
Temp. Cycle	-65°C to +150°C	1000 Cycles	50
Thermal Shock	-65°C to +150°C	1000 Cycles	50

MATRIX III

TEST	CONDITIONS	SAMPLE
Solderability	Mil-Std 883/2003	15
Lead Fatigue	Mil-Std 883/2004	15
Brand Adhesion	Mil-Std 883/2015	20
Flammability	(UL-94 Vertical Burn)	5

Field Return Product Analysis System

The purpose of this system is to enable Harris' Field Sales and Quality operations to properly route, track and respond to our customers' needs as they relate to product analysis.

The Product Failure Analysis Solution Team (PFAST) consists of the group of people who must act together to provide timely, accurate and meaningful results to customers on units returned for analysis. This team includes the salesman or applications engineer who gets the parts from the customer, the PFAST controller who coordinates the response, the Product or Test Engineering people who obtain characterization and/or test data, the analysts who failure analyze the units, and the people who provide the ultimate corrective action. It is the coordinated effort of this team, through the system described in this document that will drive the Customer responsiveness and continuous improvement that will keep Harris on the forefront of the semiconductor business.

The system and procedures define the processing of product being returned by the customer for analysis performed by Product Engineering, Reliability Failure Analysis and/or Quality Engineering. This system is designed for processing "sample" returns, not entire lot returns or lot replacements.

The philosophy is that each site analyzes its own product. This applies the local expertise to the solutions and helps toward the goal of quick turn time.

Goals: quick, accurate response, uniform deliverable (consistent quality) from each site, traceability.

The PFAST system is summarized in the following steps:

1) Customer calls the sales rep about the unit(s) to return.
2) Fill out PFAST Action Request - see the PFAST form in this section. This form is all that is required to process a Field Return of samples for failure analysis. This form contains essential information necessary to perform root cause analysis. (See Figure 2).
3) The units must be packaged in a manner that prevents physical damage and prevents ESD. Send the units and PFAST form to the appropriate PFAST controller. This location can be determined at the field sales office or rep using "look-up"tables in the PFAST document.
4) The PFAST controller will log the units and route them to ATE testing for data log.
5) Test results will be reviewed and compared to customer complaint and a decision will be made to route the failure to the appropriate analytical group.
6) The customer will be contacted with the ATE test results and interim findings on the analysis. This may relieve a line down situation or provide a rapid disposition of material. The customer contact is valuable in analytical process to insure root cause is found.
7) A report will be written and sent directly to the customer with copies to sales, rep, responsible individuals with corrective actions and to the PFAST controller so that the records will capture the closure of the cycle.
8) Each report will contain a feedback form (stamped and preaddressed) so that the PFAST team can assess their performance based on the customers assessment of quality and cycle time.
9) The PFAST team objectives are to have a report in the customers hands in 28 days, or 14 days based on agreements. Interim results are given real-time.

HARRIS SEMICONDUCTOR

Request # _____
Customer Analysis # _____

PFAST ACTION REQUEST

Date: _____

ORIGINATOR _____	CUSTOMER _____
LOCATION/PHONE NO. _____	LOCATION _____
DEVICE TYPE/PART NO. _____	PURCHASE ORDER NO. _____
NO. SAMPLES RETURNED _____	QUANTITY RECEIVED _____

THE COMPLETENESS AND TIMELY RESPONSE OF THE EVALUATION IS DIRECTLY RELATED TO THE COMPLETENESS OF THE DATA PROVIDED. PLEASE PROVIDE ALL PERTINENT DATA. ATTACH ADDITIONAL SHEETS IF NECESSARY.

TYPE OF PROBLEM

1. ☐ INCOMING INSPECTION
   - ☐ 100% SCREEN ☐ SAMPLE INSPECTION
     NO. TESTED _____ NO. OF REJECTS _____
     ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
     ☐ YES ☐ NO
   - ☐ BRIEF DESCRIPTION OF EVALUATION AND RESULTS ATTACHED
2. ☐ IN PROCESS/MANUFACTURING FAILURE
   - ☐ BOARD CHECKOUT ☐ SYSTEM CHECKOUT
   - ☐ FAILED ON TURN-ON
   - ☐ FAILED AFTER _____ HOURS OPERATION
     WAS UNIT RETESTED UNDER INCOMING INSPECTION CONDITIONS? ☐ YES ☐ NO
   - ☐ BRIEF DESCRIPTION OF HOW FAILURE WAS ISOLATED TO COMPONENT ATTACHED
3. ☐ FIELD FAILURE
   - FAILED AFTER _____ HOURS OPERATION
   - ESTIMATED FAILURE RATE ____% PER 1000 HOURS
   - END USER _____ LOCATION _____
   - AMBIENT TEMPERATURE _____ C
   - MIN. _____ C MAX. _____ C
   - REL. HUMIDITY _____ %
   - ☐ END USER FAILURE CORRESPONDENCE ATTACHED

ACTION REQUESTED BY CUSTOMER

SPECIFIC ACTION REQUESTED _____

IMPACT OF FAILED UNITS ON CUSTOMER'S SITUATION: _____

CUSTOMER CONTACTS WITH SPECIFIC KNOWLEDGE OF REJECTS
NAME _____
POSITION _____ PHONE _____

DETAILS OF REJECT

(Where appropriate serialize units and specify for each)

TEST CONDITIONS RELATING TO FAILURE
- ☐ TESTER USED (MFGR/MODEL) _____
- ☐ TEST TEMPERATURE _____
- ☐ TEST TIME: ☐ CONTINUOUS TEST ☐ ONE SHOT (T = _____ SEC)
- ☐ DESCRIPTION OF ANY OBSERVED CONDITION TO WHICH FAILURE APPEARS SENSITIVE: _____

1. ☐ DC FAILURES
   - ☐ OPENS ☐ SHORTS ☐ LEAKAGE ☐ STRESS
   - ☐ POWER DRAIN ☐ INPUT LEVEL ☐ OUTPUT LEVEL
   - ☐ LIST OF FORCING CONDITIONS AND MEASURED RESULTS FOR EACH PIN IS ATTACHED
   - ☐ POWER SUPPLY SEQUENCING ATTACHED
2. ☐ AC FAILURES
   - LIST FAILING CHARACTERISTICS _____
   - ADDRESS OF FAILING LOCATION (IF APPLICABLE) _____
   - ATTACHED:
     - ☐ LIST OF POWER SUPPLY AND DRIVER LEVELS (Include pictures of waveforms).
     - ☐ LIST OF OUTPUT LEVELS AND LOADING CONDITIONS
     - ☐ INPUT AND OUTPUT TIMING DIAGRAMS
     - ☐ DESCRIPTION OF PATTERNS USED (If not standard patterns, give very complete description including address sequence).
3. ☐ PROM PROGRAMMING FAILURES
   - ADDRESS OF FAILURES _____
   - PROGRAMMER USED (MFG/MODEL/REV. NO.) _____
4. ☐ PHYSICAL/ASSEMBLY RELATED FAILURES
   - ☐ SEE COMMENTS BELOW ☐ SEE ATTACHED

Additional Comments:

FIGURE 2. PFAST ACTION REQUEST

INSTRUCTIONS FOR COMPLETING PFAST ACTION REQUEST FORM

The purpose of this form is to help us provide you with a more accurate, complete, and timely response to failures which may occur. Accurate and complete information is essential to ensure that the appropriate corrective action can be implemented. Due to this need for accurate and complete information, requests without a completed PFAST Action Request form will be returned.

Source of Problem:
This section requests the product flow leading to the failure. Mark an "X" in the appropriate boxes up to and including the step which detected the failure. Also mark an "X" in the appropriate box under ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS? to indicate whether this is a rare failure or a repeated problem.

Example 1. No incoming electrical test was performed, the units were installed onto boards, the boards functioned correctly for two hours and then 1 unit failed. The customer rarely has a failure due to this Harris device.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE _____
2. INCOMING TEST ■ NOT PERFORMED
   ☐ 100% TESTED ☐ SAMPLE TESTED
   NO. TESTED ____ NO. OF REJECTS ____
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ■ BOARD TEST ☐ SYSTEM TEST
   HOW MANY UNITS FAILED? 1
   FAILED AFTER 2 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ■ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ■ NO
4. FIELD FAILURE
   FAILED AFTER ____ HOURS OPERATION
   ESTIMATED FAILURE RATE ____% PER _____
   END USER _____ LOCATION _____
   MIN. ____ °C AVE. ____ °C MAX. ____ °C
5. OTHER _____

Example 2. 100 out of the 500 units shipped were tested at incoming and all passed. The units were installed into boards and the boards passed. The boards were installed into the system and the system failed immediately when turned on. There were 3 system failures due to this part. The customer frequently has failures of this Harris device. The 3 units were not retested at incoming.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE _____
2. INCOMING TEST ☐ NOT PERFORMED
   ☐ 100% TESTED ■ SAMPLE TESTED
   NO. TESTED 100 NO. OF REJECTS 0
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ■ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ■ BOARD TEST ■ SYSTEM TEST
   HOW MANY UNITS FAILED? 3
   FAILED AFTER 0 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ■ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ■ YES ☐ NO
4. FIELD FAILURE
   FAILED AFTER ____ HOURS OPERATION
   ESTIMATED FAILURE RATE ____% PER _____
   END USER _____ LOCATION _____
   MIN. ____ °C AVE. ____ °C MAX. ____ °C
5. OTHER _____

Action Requested by Customer:
This section should be completed with the customer's expectations. This information is essential for an appropriate response.

Reason for Electrical Reject:
This section should be completed if the type of failure could be identified. If this information is contained in attached customer correspondence there is no need to transpose onto the PFAST Action Request form.

PFAST REQUIREMENTS

The value of returning failing products is in the corrective actions that are generated. Failure to meet the following requirements can cause an erroneous conclusion and corrective action; therefore, failure to meet these requirements will result in the request being returned. Contact the local PFAST Coordinator if you have any questions.

Units with conformal coating should include the coating manufacturer and model. This is requested since the coating must be removed in order to perform electrical or hermeticity testing.

1) Units must be returned with proper ESD protection (ESD-safe shipping tubes within shielding box/bag or inserted into conductive foam within shielding box/bag). No tape, paper bags, or plastic bags should be used. This requirement ensures that the devices are not damaged during shipment back to Harris.

2) Units must be intact (lid not removed and at least part of each package lead present). This requirement is in place since the parts must be intact in order to perform electrical test. Also, opening the package can remove evidence of the cause for failure and lead to an incorrect conclusion.

3) Programmable parts (ROMs, PROMS, UVEPROMs, and EEPROMs) must include a master unit with the same pattern. This requirement is to provide the pattern so all failing locations can be identified. A master unit is required if a failure analysis is requested.

FIGURE 2. PFAST ACTION REQUEST (Continued)

Failure Analysis Laboratory

The Failure Analysis Laboratory's capabilities encompass the isolation and identification of all failure modes/failure mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. Research vital to understanding the basic physics of the failure is also undertaken.

Failure analysis is a method of enhancing product reliability and determining corrective action. It is the final and crucial step used to isolate potential reliability problems that may have occurred during reliability stressing. Accurate analysis results are imperative to assess effective corrective actions. To ensure the integrity of the analysis, correlation of the failure mechanism to the initial electrical failure is essential.

A general failure analysis procedure has been established in accordance with the current revision of MIL-STD-883, Section 5003. The analysis procedure was designed on the premise that each step should provide information on the failure without destroying information to be obtained from subsequent steps. The exact steps for an analysis are determined as the situation dictates. (See Figures 3 and 4). Records are maintained by laboratory personnel and contain data, the failure analyst's notes, and the formal Product Analysis Report.

Analytical Services Laboratory

Harris facilities, engineering, manufacturing, and product assurance are supported by the Analytical Services Laboratory. Organized into chemical or microbeam analysis methodology, staff and instrumentation from both labs cooperate in fully integrated approaches necessary to complete analytical studies. The capabilities of each area are shown below.

SPECTROSCOPIC METHODS: Colorimetry, Optical Emission, Ultraviolet Visible, Fourier Transform-Infrared, Flame Atomic Absorption, Furnace Organic Carbon Analyzer, Mass Spectrometer.

CHROMATOGRAPHIC METHODS: Gas Chromatography, Ion Chromatography.

THERMAL METHODS: Differential Scanning Colorimetry, Thermogravimetric Analysis, Thermomechanical Analysis.

PHYSICAL METHODS: Profilometry, Microhardness, Rheometry.

CHEMICAL METHODS: Volumetric, Gravimetric, Specific Ion Electrodes.

ELECTRON MICROSCOPE: Transmission Electron Microscopy, Scanning Electron Microscope.

X-RAY METHODS: Energy Dispersive X-ray Analysis (SEM), Wavelength Dispersive X-ray Analysis (SEM), X-ray Fluorescence Spectrometry, X-ray Diffraction Spectrometry.

SURFACE ANALYSIS METHODS: Scanning Auger Microprobe, Electron Spectroscopy/Chemical Analysis, Secondary Ion Mass Spectrometry, Ion Scattering Spectrometry, Ion Microprobe.

The department also maintains ongoing working arrangements with commercial, university, and equipment manufacturers' technical service laboratories, and can obtain any materials analysis in cases where instrumental capabilities are not available in our own facility.

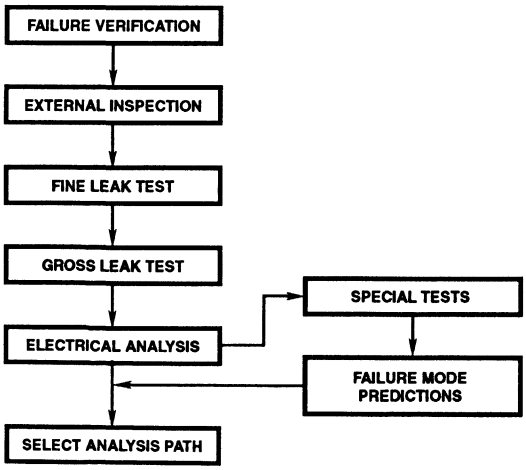


FIGURE 3. NON-DESTRUCTIVE

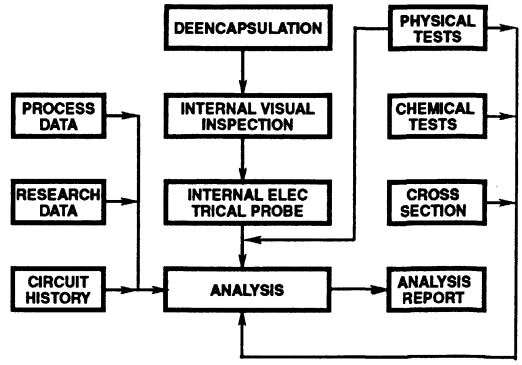


FIGURE 4. DESTRUCTIVE

Reliability Fundamentals and Calculation of Failure Rate

Table 8 below defines some of the more important terminology used in describing the lifetime of integrated circuits.

Of prime importance is the concept of "failure rate" and the calculation thereof.

Failure Rate Calculations

Reliability data may be composed of several different failure mechanisms and the combining of potentially diverse failure rates into one comprehensive failure rate is desired. The failure rate calculation is complicated because the failure mechanisms are thermally activated at differing rates. Additionally, this data is usually obtained on a number of life tests performed at unique stress temperatures. The equation below accounts for these considerations along with a statistical factor to obtain the upper confidence level (UCL) for the resulting failure rate.

$$\lambda = \left[\sum_{i=1}^{\beta} \frac{x_i}{\sum_{j=1}^{k} TDH_j \, AF_{ij}} \right] \bullet \frac{M \times 10^9}{\sum_{i=1}^{\beta} x_i}$$

where,

λ = failure rate in FITs (Number fails in 10^9 device hours)

β = # of distinct possible failure mechanisms

k = # of life tests being combined

x_i = # of failures for a given failure mechanism $i = 1, 2, \ldots \beta$

TDH_j = Total device hours of test time (unaccelerated) for Life Test j, $j = 1, 2, 3, \ldots k$

AF_{ij} = Acceleration factor for appropriate failure mechanism $i = 1, 2, \ldots k$

$M = X^2_{(\alpha, 2r+2)}/2$
where,
X^2 = chi square factor for $2r + 2$ degrees of freedom
r = total number of failures (Σx_i)
α = risk associated with UCL;
i.e. $\alpha = (100\text{-UCL}(\%))/100$

In the failure rate calculation, Acceleration Factors (AF_{ij}) are used to derate the failure rate from the thermally accelerated life test conditions to a failure rate indicative of actual use temperature. Although no standard exists, a temperature of +55°C has been popular. Harris Semiconductor Reliability Reports will derate to +55°C and will express failure rates at 60% UCL. Other derating temperatures and UCLs are available upon request.

TABLE 8. FAILURE RATE PRIMER

TERMS	DEFINITIONS/DESCRIPTION
Failure Rate λ	Measure of failure per unit of time. The failure rate typically decreases slightly over early life, and then becomes relatively constant over time. The on set of wearout will show an increasing failure rate, which should occur well beyond useful life. The useful life failure rate is based on the exponential life distribution
FIT (Failure In Time)	Measure of failure rate in 10^9 device hours; e.g., 1 FIT = 1 failure in 10^9 device hours, 100 FITS = 100 failure in 10^9 device hours, etc.
Device Hours	The summation of the number of units in operation multiplied by the time of operation.
MTTF (Mean Time To Failure)	Mean of the life distribution for the population of devices under operation or expected lifetime of an individual, MTTF = $1/\lambda$, which is the time where 63.2% of the population has failed. Exampled: For λ = 10 FITS (or 10 E-9/Hr.), MTTF = $1/\lambda$ = 100 million hours.
Confidence Level (or Limit)	Probability level at which population failure rate estimates are derived from sample life test: 10 FITs at 95% UCL means that the population failure rate is estimated to be no more that 10 FITs with 95% certainty. The upper limit of the confidence interval is used.
Acceleration Factor (AF)	A constant derived from experimental data which relates the times to failure at two different stresses. The AF allows extrapolation of failure rates from accelerated test conditions to use conditions.

Acceleration Factors

Acceleration factor is determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and has been found to be an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP\left[\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)\right]$$

where,

AF = Acceleration Factor

E_a = Thermal Activation Energy (See Table 9)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

Both T_{use} and T_{stress} (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature.

Activation Energy

The Activation Energy (E_a) of a failure mechanism is determined by performing at least two tests at different levels of stress (temperature and/or voltage). The stresses will provide the time to failure (t_f) for the two (or more) populations thus allowing the simultaneous solution for the activation energy as follows:

$$\ln (t_{f1}) = C + \frac{E_a}{kT_1} \qquad \ln (t_{f2}) = C + \frac{E_a}{kT_2}$$

By subtracting the two equations, and solving for the activation energy, the following equation is obtained:

$$E_a = \frac{k[\ln(t_{f1}) - \ln(t_{f2})]}{(1/T1 - 1/T2)}$$

where,

E_a = Thermal Activation Energy (See Table 9)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

T_1, T_2 = Life test temperatures in degrees Kelvin

TABLE 9. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3 - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3 - 0.5eV	HTOL & voltage stress screens.	Vendor statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress testing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5 - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistical Process Control of assembly processes, proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles, Statistical Process Control of photoresist/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test and HTOL.	Statistical Process Control of C-V data, oxide/interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL & oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

LINEAR 10

APPLICATION NOTE ABSTRACTS AND SPICE MODEL LISTING

AN #	TITLE	ABSTRACTS
509	A Simple Comparator Using The HA-2620	Performance characteristics, application schematics, output parameter control methods.
514	The HA-2400 PRAM Four Channel Operational Amplifier	HA-2400 PRogrammable Analog Microcircuit description, frequency compensation, applications (analog multiplexer, non-inverting programmable gain amplifier, inverting programmable gain amplifier, programmable attenuator, programmable adder-subtractor, phase selector, phase detector, synchronous rectifier, balanced modulator, integrator, ramp generator, track and hold, sample and hold, sine wave oscillator, multivibrator, active filter, programmable power supply, comparator, multiplying D/A converter).
515	Operational Amplifier Stability: Input Capacitance Considerations	Input capacitance and stability, capacitive feedback compensation, guidelines for compensation requirements.
517	Applications of a Monolithic Sample and Hold/Gated Op Amp	General Sample and Hold information and fourteen specific applications, including filtered Sample & Hold DAC de-glitcher, Integrate-Hold-Reset, gated op amp, etc
519	Operational Amplifiers Noise Prediction	Noise model and equations, procedure for computing total output noise, example, broadband noise measurement, spot noise prediction techniques, typical spot noise curves, popcorn noise discussion.
525	HA-5190/5195 Fast Settling Operational Amplifier	Internal schematic, prototyping considerations, frequency compensation, performance enhancement methods, applications.
526	HA-5190/5195 Video Applications	Video applications, video response tests, S/N ratio measurements, power supply requirements temperature considerations, design hints, prototyping tips, RF AGO amplifier, DC gain controlled video amplifier.
538	Monolithic Sample/Hold Combines Speed and Precision	Description and electrical specifications for the HA-5320 Sample/Hold Amplifier, explanation of errors sources, and HA-5320 applications.
540	HA-5170 Precision Low Noise J-FET Input Operational Amplifier	Internal design and technology, J-FET noise discussion, trimming of offset voltage, single op amp Instrumentation Amplifier, sine wave oscillator, high impedance transducer interface, current source/sink and current sense circuits.
541	Using HA-2539/2540 Very High Slew-Rate Wideband Operational Amplifiers	Prototyping considerations, output short circuit protection, offset voltage adjustment, frequency compensation, composite amplifier scheme, DC error reduction, boosting output current, increasing output signal swing, cascade amplifier, video gain block, high frequency oscillator, wideband signal splitter.
544	Micropower Op Amp Family, HA-514X, and HA-515X	Operation, noise performance, applications (remote sensor loop transmitter, charge pool power supply, low power microphone preamplifier, AGO with squelch control, Wein bridge oscillator, bar code scanner, monostable multivibrator).
546	A Method of Calculating HA-2625 Gain Bandwidth Product vs Temperature	A method of calculating Gain Bandwidth product performance versus temperature for the HA-2625 Op Amp.

See page iv for information on Ordering Literature

Application Note Abstracts (Continued)

AN #	TITLE	ABSTRACTS
548	A Designer's Guide for the HA-5033 Video Buffer	Operation, video performance, video parameter specifications, Y parameters, applications (flash converter pre-driver, coaxial line driver, video gain block, high speed sample and hold, audio drivers, crystal oscillator).
549	The HC-550X Telephone Subscriber Line Interface Circuit	Complete description of device functionality and applications of SLIC.
550	Using the HA-2541	Prototyping guidelines, thermal considerations and heat sinking, performance enhancements, applications (Wein bridge oscillator, high power gain stage, video stage with clamp, multiplexer/demultiplexer, disk drive write amplifier, gain programmable amp, composite amp).
551	Recommended Test Procedures for Operational Amplifiers	Operational amplifier test procedures for offset voltage, bias current, offset current, power supply rejection ratio, common mode rejection ratio, output voltage swing, output current, open loop gain, slew rate, full power bandwidth, transient response, settling time, GBP, phase margin. noise voltage and current, and channel separation.
552	Using the HA-2542	Prototyping guidelines, thermal considerations and heat sinking, performance enhancements, applications (multi-channel security system, unbalanced coaxial driver, flash converter driver, programmable power supply, bridge load driver, high current stage, differential line driver, DC motor speed control).
553	Using the HA-5147/ 5137/5127	Construction and operation, low noise design applications (instrumentation amplifier bridge sensor, multiplexer, precision threshold detector, audio driver, NAB amplifier, multivibrator, programmable gain stage, log amp, professional mixer).
554	Low Noise Family HA-5101/5102/5104/ 5112/5114	Low noise design, operation, applications (Electronic scales, programmable attentuator, Baxandal circuit, RIAA amplifier, NAB preamplifier, microphone amplifier, standard and simple biquads, professional mixer.
556	Thermal Safe-Operating-Areas for High Current Op Amps	Thermal management equations and curves indicating areas of V_{OUT} and I_{OUT} for safe operation. Also, the effects of packaging and heat sinking are examined.
558	Using the HV1205 AC to DC Converter	Explains the basic theory of operation of the HV-1205. Presents a discussion of external components required for operation, PC board layout recommendations and safety considerations.
571	Using Ring Sync with HC-5502A and HC5504 SLICs	Describes use of the SLICs Ring Synchronization pin and why you should use it.
573	The HC-5560 Digital Line Transcoder	Full functional and applications description of HC-5560 transcoder and line codes.
574	Understanding PCM Coding	The process of converting analog voice signals into Time Division Multiplexed (TDM) Pulse Code Modulated (PCM) format is described and illustrated.
607	Delta Modulation for Voice Transmission	Introduction to delta modulation coding techniques, 4 general applications, including digital transmission encryption, voice scrambling and audio delay. Also CVSD evaluation guidelines.
9006	HV-2405E Operation from Full Bridge	A brief discussion of function of the source resistor (R1) and the benefits of using a bridge rectifier to reduce the power dissipation in R1. Presents several points to be kept in mind when implementing the full bridge (i.e. safety aspects, filtering of output so device will reset for the next cycle and circuit operation verification with test equipment).
9101	High Current Off Line Power Supply	Explains the basic theory of operation of the HV-1205/2405E and shows how to increase the maximum output current from 50mA to greater than 250mA. A detailed description of the circuit operation, to achieve the higher currents, is presented along with suggestions for external component selection.
A007	Using the 8048/8049 Monolithic Log-Anti-Log Amplifiers	Describes in detail the operation of the ICL8048 logarithmic amplifier, and its counter-part, the ICL8049 anti-log amp.
A013	Everything You Always Wanted to Know About the 8038	This note includes 17 of the most asked questions regarding the use of the ICL8038.

See page iv for information on Ordering Literature

Application Note Abstracts (Continued)

AN #	TITLE	ABSTRACTS
A027	Power Supply Design Using the ICL8211 and ICL8212	Explains the operation of the ICL8211/12 and describes various power supply configurations. Included are positive and negative voltage regulators, constant current source, programmable current source, current limiting, voltage crowbarring, power supply window detector, etc.
A040	A Precision Four Quadrant Multiplier - The 8013	Describes, in detail, the operation of the ICL8013 analog multiplier. Included are multiplication, division, and square root applications.
A051	Principles and Applications of the ICL7660 CMOS Voltage Converter	Describes internal operation of the ICL7660. Includes a wide range of possible applications.
A053	The ICL7650 - A New Era in Glitch-Free Chopper Stabilizer Amplifiers	A brief discussion of the internal operation of the ICL7650, followed by an extensive applications section including amplifiers, comparators, log-amps, pre-amps, etc.
5290	General Purpose Op Amps	Discusses various uses of op amps.
5296	CA3018	Transistor Array
5337	CA3028	RF amplifiers in the HF and VHF ranges.
5380	FM IF Amplifiers	Discusses differential amplifier configurations.
5766	CA3020	Multipurpose wideband power amplifiers
6048	CA3094	Programmable power switch/amplifier.
6077	CA3094	OTA with power capability.
6157	CA3085	Monolithic voltage regulators.
6182	CA3059	Zero-voltage switches.
6247	CA3126	Chroma processing IC using sample and hold circuit techniques.
6257	CA3089	FM IF Subsystem.
6386	CA3130	Understanding BiMOS op amps.
6459	CA3130	Why and how to use the BiMOS op amp.
6472	CA3126	A chrominance demodulator IC with dynamic flesh correction.
6525	IC Handling	Guide to IC handling.
6668	CA3080	High performance OTA.
6669	CA3240	BiMOS op amp mates directly to system sensors.
6732	Noise Measurement	Measurement of burst noise and "popcorn" noise in ICs.
6818	CA3280	OTA simplifies complex analog designs.
6915	CA1524	Pulse-width modulators.
6998	Telecom	Telephony in Digital Evolution.
7037	Telecom	Logarithmic units of measure in telecommunications.
7127	CA3420	BiMOS amplifier circumvents low voltage limitations.
7174	CA1524	Pulse-width modulator in an electronic scale.
7175	CA3217	Integrated NTSC chrominance/luminance processor
7304	SCR Protection	Discusses SCR Protection Circuits for ICs.
8636	Video Devices	Discusses advanced video speed switches, multiplexers, cross points and buffer amplifiers.
8707	CA3450	Single chip video line driver-high speed op amp.
8742	CD22402	Sync Generator
8811	CA5470	BiMOS-E process enhances quad op amp.
ICE-402	Operating Considerations	Discusses operating considerations for solid state devices.

See page iv for information on Ordering Literature

Spice Model Listing

PART NUMBER	DESCRIPTION
CA3227	3.0GHz NPN Arrays (See Data Sheet for Model)
CA3246	3.0GHz NPN Arrays (See Data Sheet for Model)
HA-2500	Precision, High Slew Rate, Single
HA-2502	Precision, High Slew Rate, Single
HA-2510	High Slew Rate, Single
HA-2512	High Slew Rate, Single
HA-2520	+3 Stable, High Slew Rate, Single
HA-2522	+3 Stable, High Slew Rate, Single
HA-2539	Very High Slew Rate, Wideband, +10 Stable, Single
HA-2540	Wideband, Fast Settling, +10 Stable, Single
HA-2541	Wideband, Fast Settling, Unity Gain Stable, Single
HA-2542	Wideband, High Slew Rate, High Output Current, +2 Stable, Single
HA-2544	Precision, High Slew Rate, Unity Gain Stable, Single
HA-2548	Precision, High Slew Rate, Wideband, +5 Stable, Single
HA-2600	Wideband, High Input Impedance, Single
HA-2602	Wideband, High Input Impedance, Single
HA-2620	Very Wideband, Uncompensated, +5 Stable, Single
HA-2622	Very Wideband, Uncompensated, +5 Stable, Single
HA-2839	Very High Slew Rate, Wideband, +10 Stable, Single
HA-2840	Very High Slew Rate, Wideband, +10 Stable, Single
HA-2841	Wideband, Fast Settling, Unity Gain Stable, Video, Single

PART NUMBER	DESCRIPTION
HA-2842	Wideband, High Slew Rate, High Drive, Video, +2 Stable, Single
HA-2850	Low Power, High Slew Rate, Wideband, +10 Stable, Single
HA-5002	Wideband, High Slew Rate Buffer
HA-5004	100MHz Current Feedback Video Amplifier
HA-5020	100MHz Current Feedback Video Amplifier
HA-5033	Video Buffer
HA-5101	Low Noise, High Performance, Single
HA-5102	Low Noise, High Performance, Dual
HA-5104	Low Noise, High Performance, Quad
HA-5112	Low Noise, High Performance, +10 Stable, Dual
HA-5114	Low Noise, High Performance, +10 Stable, Quad
HA-5127	Low Noise, Precision, Unity Gain Stable, Single
HA-5137	Low Noise, Precision, +5 Stable, Single
HA-5147	Low Noise, Precision, +10 Stable, Single
HA-5190	Wideband, Fast-settling, +5 Stable, Single
HA-5221	Low Noise, Wideband, Precision, Single
HA-5222	Low Noise, Wideband, Precision, Dual
*HC-5509B	Spare Op Amp On Board Subscriber Line IC (SLIC)
HFA-0001	Ultra High Slew Rate, Single
HFA-0002	Low Noise, Ultra High Speed, Wideband, +10 Stable, Single
HFA-0005	Ultra High Slew Rate, Single
HFA3046, HFA3096, HFA3127, HFA3128	8GHz NPN, 5.5GHz PNP Arrays

NOTE:* Macromodel is on disk but App Note does not exist.

See page iv for information on Ordering Literature

LINEAR 11

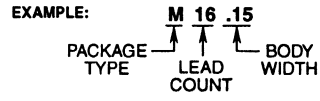
PACKAGING INFORMATION

Linear and Telecom Package Selection Guide

Using the Selection Guide:

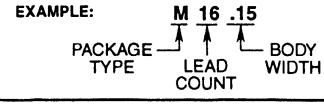
The first character of each entry indicates the package type, while the number preceding the decimal point details the package lead count. Except for Can packages, the decimal point and succeeding numbers specify the package width in inches (e.g. .15 = 150 mil width). The entire entry indicates the table containing the appropriate package dimensions (e.g. 8 lead PDIP dimension are detailed in Table E8.3). The index on page 11-1 lists page numbers for PDIP, SOIC, PLCC, CDIP, Sidebraze and Can tables.

PART NUMBER	PDIP	SOIC	PLCC	CDIP	SIDEBRAZE	CAN
CA124	E14.3	M14.15	-	-	-	-
CA1391	E8.3	-	-	-	-	-
CA1394	E8.3	-	-	-	-	-
CA139	E14.3	M14.15	-	F14.3	-	-
CA1458	E8.3	-	-	-	-	T8.C
CA1558	E8.3	-	-	-	-	T8.C
CA158	E8.3	M8.15	-	-	-	T8.C
CA224	E14.3	M14.15	-	-	-	-
CA239	E14.3	M14.15	-	F14.3	-	-
CA258	E8.3	M8.15	-	-	-	T8.C
CA2904	E8.3	M8.15	-	-	-	-
CA3018	-	-	-	-	-	T12.B
CA3020	-	-	-	-	-	T12.B
CA3028	E8.3	M8.15	-	-	-	T8.C
CA3039	-	M14.15	-	-	-	T12.B
CA3045	-	-	-	F14.3	D14.3	-
CA3046	E14.3	M14.15	-	-	-	-
CA3049	-	-	-	-	-	T12.B
CA3053	E8.3	M8.15	-	-	-	T8.C
CA3054	E14.3	M14.15	-	-	-	-
CA3060	E16.3	-	-	-	-	-
CA3078	E8.3	M8.15	-	-	-	T8.C
CA3080	E8.3	M8.15	-	-	-	T8.C
CA3081	E16.3	M16.15	-	F16.3	-	-
CA3082	E16.3	M16.15	-	F16.3	-	-
CA3083	E16.3	M16.15	-	F16.3	-	-
CA3086	E14.3	M14.15	-	F14.3	-	-
CA3089	E16.3	M20.3	-	F16.3	-	-
CA3094	E8.3	M8.15	-	-	-	T8.C
CA3096	E16.3	M16.15	-	-	-	-
CA3098	E8.3	-	-	-	-	-



Linear and Telecom Package Selection Guide (Continued)

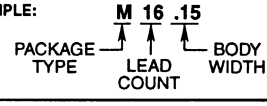
PART NUMBER	PDIP	SOIC	PLCC	CDIP	SIDEBRAZE	CAN
CA3100	E8.3	M8.15	-	-	-	T8.C
CA3102	E14.3	M14.15	-	-	-	-
CA3126	E16.3	M20.3	-	-	-	-
CA3127	E16.3	M16.15	-	F16.3	-	-
CA3130	E8.3	M8.15	-	-	-	T8.C
CA3140	E8.3	M8.15	-	-	-	T8.C
CA3141	E16.3	-	-	-	-	-
CA3146	E14.3	M14.15	-	-	-	-
CA3160	E8.3	-	-	-	-	T8.C
CA3183	E16.3	M16.15	-	-	-	-
CA3189	E16.3	-	-	-	-	-
CA3193	E8.3	-	-	-	-	T8.C
CA3194	E24.6	-	-	-	-	-
CA3217	E28.6	-	-	-	-	-
CA3227	E16.3	M16.15	-	-	-	-
CA324	E14.3	M14.15	-	-	-	-
CA3240	E8.3, E14.3	-	-	-	-	-
CA3246	E14.3	M14.15	-	-	-	-
CA3256	E18.3	M20.3	-	-	-	-
CA3260	E8.3	-	-	-	-	T8.C
CA3280	E16.3	-	-	F16.3	-	-
CA3290	E8.3, E14.3	-	-	-	-	T8.C
CA339	E14.3	M14.15	-	F14.3	-	-
CA3420	E8.3	-	-	-	-	T8.C
CA3440	E8.3	M8.15	-	-	-	T8.C
CA3450	E16.3	-	-	-	-	-
CA358	E8.3	M8.15	-	-	-	T8.C
CA5130	E8.3	M8.15	-	-	-	T8.C
CA5160	E8.3	M8.15	-	-	-	T8.C
CA5260	E8.3	M8.15	-	-	-	T8.C
CA5420	E8.3	M8.15	-	-	-	T8.C
CA5470	E14.3	M14.15	-	-	-	-
CA555	E8.3	M8.15	-	-	-	T8.C
CA741	E8.3	-	-	-	-	T8.C
CD22100	E16.3	-	-	F16.3	D16.3	-
CD22101	E24.6	-	-	F24.6	-	-
CD22102	E24.6	-	-	F24.6	-	-



Linear and Telecom Package Selection Guide (Continued)

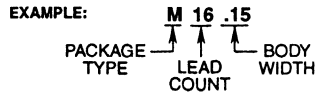
PART NUMBER	PDIP	SOIC	PLCC	CDIP	SIDEBRAZE	CAN
CD22103A	E16.3	-	-	-	D16.3	-
CD22202	E18.3	-	-	-	-	-
CD22203	E18.3	-	-	-	-	-
CD22204	E14.3	M24.3	-	-	-	-
CD22301	E18.3	-	-	-	-	-
CD22354A	E16.3	-	-	-	-	-
CD22357A	E16.3	-	-	-	-	-
CD22402	E24.6	-	-	-	D24.6	-
CD22859	E16.3	-	-	-	-	-
CD22M3493	E40.6	-	N44.65	-	-	-
CD22M3494	E40.6	-	N44.65	-	-	-
CD74HC22106	E28.6	-	-	-	-	-
HA-2400	-	-	-	F16.3	-	-
HA-2404	-	-	-	F16.3	-	-
HA-2405	E16.3	-	N20.35	F16.3	-	-
HA-2406	E16.3	M16.3	-	F16.3	-	-
HA-2420	-	-	-	F14.3	-	-
HA-2425	E14.3	M14.15	N20.35	F14.3	-	-
HA-2444	E16.3	M16.3	-	-	-	-
HA-2500	-	-	-	F8.3A	-	T8.C
HA-2502	-	-	-	F8.3A	-	T8.C
HA-2505	E8.3	-	N20.35	F8.3A	-	T8.C
HA-2510	-	-	-	F8.3A	-	T8.C
HA-2512	-	-	-	F8.3A	-	T8.C
HA-2515	E8.3	-	-	F8.3A	-	T8.C
HA-2520	-	-	-	F8.3A	-	T8.C
HA-2522	-	-	-	F8.3A	-	T8.C
HA-2525	E8.3	M8.15	N20.35	F8.3A	-	T8.C
HA-2529	E8.3	M8.15	-	F8.3A	-	T8.C
HA-2539	E14.3	M14.15	N20.35	F14.3	-	-
HA-2540	E14.3	M14.15	N20.35	F14.3	-	-
HA-2541	-	-	-	F14.3	-	T12.C
HA-2542	E14.3	-	-	F14.3	-	T12.C
HA-2544	E8.3	M8.15	N20.35	F8.3A	-	T8.C
HA-2546	E16.3	M16.3	-	F16.3	-	-
HA-2547	-	-	-	F16.3	-	-
HA-2548	E8.3	M16.3	-	-	D8.3	T8.C

EXAMPLE: M 16 .15



Linear and Telecom Package Selection Guide (Continued)

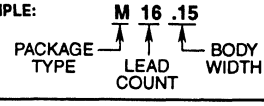
PART NUMBER	PDIP	SOIC	PLCC	CDIP	SIDEBRAZE	CAN
HA-2556	E16.3	M16.3	-	F16.3	-	-
HA-2557	E16.3	M16.3	-	F16.3	-	-
HA-2600	-	-	-	F8.3A	-	T8.C
HA-2602	-	-	-	F8.3A	-	T8.C
HA-2605	E8.3	M8.15	N20.35	F8.3A	-	T8.C
HA-2620	-	-	-	F8.3A	-	T8.C
HA-2622	-	-	-	F8.3A	-	T8.C
HA-2625	E8.3	M8.15	N20.35	F8.3A	-	T8.C
HA-2640	-	-	-	F8.3A	-	T8.C
HA-2645	-	-	-	F8.3A	-	T8.C
HA-2705	E8.3	M8.15	-	-	-	T8.C
HA-2839	E14.3	-	-	F14.3	-	-
HA-2840	E8.3, E14.3	M8.15	-	F8.3A, F14.3	-	-
HA-2841	E8.3, E14.3	M8.15	-	-	-	-
HA-2842	E8.3, E14.3	M8.15	-	-	-	-
HA-2850	E8.3, E14.3	M8.15	-	F8.3A, F14.3	-	-
HA-4741	E14.3	M16.3	N20.35	F14.3	-	-
HA-4900	-	-	-	F16.3	-	-
HA-4902	-	-	-	F16.3	-	-
HA-4905	E16.3	M16.3	N20.35	F16.3	-	-
HA-5002	E8.3	M8.15	N20.35	F8.3A	-	T8.C
HA-5004	E14.3	M14.15	-	F14.3	-	-
HA-5020	E8.3	M8.15	-	F8.3A	-	-
HA-5022	E16.3	M16.15	-	F16.3	-	-
HA-5023	E8.3	M8.15	-	F8.3A	-	-
HA-5024	E20.3	M20.3	-	F20.3	-	-
HA-5025	E14.3	M16.3	-	F14.3	-	-
HA-5033	E8.3	-	N20.35	-	-	T12.C
HA-5101	E8.3	M8.15	N20.35	F8.3A	-	T8.C
HA-5102	E8.3	M16.3	N20.35	F8.3A	-	T8.C
HA-5104	E14.3	M16.3	N20.35	F14.3	-	-
HA-5111	E8.3	M8.15	-	F8.3A	-	T8.C
HA-5112	E8.3	M16.3	-	F8.3A	-	T8.C
HA-5114	E14.3	M16.3	N20.35	F14.3	-	-
HA-5127	E8.3	M8.15	-	F8.3A	-	T8.C
HA-5130	-	-	-	F8.3A	-	T8.C
HA-5134	-	-	-	F14.3	-	-



Linear and Telecom Package Selection Guide (Continued)

PART NUMBER	PDIP	SOIC	PLCC	CDIP	SIDEBRAZE	CAN
HA-5135	-	-	-	F8.3A	-	T8.C
HA-5137	E8.3	M8.15	-	F8.3A	-	T8.C
HA-5142	E8.3	M16.3	-	F8.3A	-	T8.C
HA-5144	E14.3	M16.3	N20.35	F14.3	-	-
HA-5147	E8.3	-	-	F8.3A	-	T8.C
HA-5160	-	-	-	-	-	T8.C
HA-5162	-	-	-	-	-	T8.C
HA-5170	-	-	-	F8.3A	-	T8.C
HA-5177	E8.3	M8.15	-	F8.3A	-	T8.C
HA-5190	-	-	-	F14.3	-	T12.C
HA-5195	-	M14.15	-	F14.3	-	T12.C
HA-5221	E8.3	M8.15	-	F8.3A	-	T8.C
HA-5222	E16.3	M16.3	-	F8.3A	-	-
HA-5232	E8.3	M16.3	-	F8.3A	-	-
HA-5234	E14.3	M16.3	-	F14.3	-	-
HA-5320	E14.3	M16.3	-	F14.3	-	-
HA-5330	E14.3	-	-	F14.3	-	-
HA-5340	E14.3	M16.3	-	F14.3	-	-
HA-5350	E14.3	M14.15	-	F14.3	-	-
HA-5351	E8.3	M8.15	-	F8.3A	-	-
HA-5352	E14.3	M16.3	-	F14.3	-	-
HA-5354	E18.3	M18.3	-	F18.3	-	-
HA-7210	E8.3	M8.15	-	-	-	-
HC-5502B	E24.6	M24.3	N28.45	F24.6	-	-
HC-5504B	E24.6	M24.3	N28.45	F24.6	-	-
HC-5504DLC	E24.6	M24.3	N28.45	F24.6	-	-
HC-5509B	E28.6	M28.3	N44.65	F28.6	-	-
HC-5524	E28.6	M28.3	N44.65	F28.6	-	-
HC-55536	E14.3	-	-	F14.3	-	-
HC-55564	E14.3	-	-	F14.3	-	-
HC-5560	E20.3	-	-	-	-	-
HFA-0001	E8.3	M16.3	-	-	D14.3	-
HFA-0002	E8.3	M8.15	-	-	D8.3	T8.C
HFA0003	E8.3	M8.15	-	-	D8.3	-
HFA0003L	E16.3	M16.15	-	-	D16.3	T10.B
HFA0005	E8.3	M8.15	-	-	D8.3	T8.C
HFA1100	E8.3	M8.15	-	F8.3A	-	-

EXAMPLE: M 16 .15



Linear and Telecom Package Selection Guide (Continued)

PART NUMBER	PDIP	SOIC	PLCC	CDIP	SIDEBRAZE	CAN
HFA1105	E8.3	M8.15	-	F8.3A	-	-
HFA1106	E8.3	M8.15	-	F8.3A	-	-
HFA1110	E8.3	M8.15	-	F8.3A	-	-
HFA1112	E8.3	M8.15	-	F8.3A	-	-
HFA1113	E8.3	M8.15	-	F8.3A	-	-
HFA1120	E8.3	M8.15	-	F8.3A	-	-
HFA1130	E8.3	M8.15	-	F8.3A	-	-
HFA1135	E8.3	M8.15	-	F8.3A	-	-
HFA1145	E8.3	M8.15	-	F8.3A	-	-
HFA3046	-	M14.15	-	-	-	-
HFA3096	-	M16.15	-	-	-	-
HFA3127	-	M16.15	-	-	-	-
HFA3128	-	M16.15	-	-	-	-
HFA5250	-	M28.3	-	-	-	-
ICL7611	E8.3	M8.15	-	-	-	T8.C
ICL7612	E8.3	M8.15	-	-	-	T8.C
ICL7621	E8.3	M8.15	-	-	-	T8.C
ICL7641	E14.3	-	-	-	-	-
ICL7642	E14.3	-	-	F14.3	-	-
ICL7650S	E8.3, E14.3	M8.15, M14.15	-	F14.3	-	T8.C
ICL8013	-	-	-	-	-	T10.C
ICL8038	E14.3	-	-	F14.3	-	-
ICL8048	-	-	-	F16.3	-	-
ICL8049	-	-	-	F16.3	-	-
ICM7242	E8.3	M8.15	-	-	-	-
ICM7555	E8.3	M8.15	-	-	-	T8.C
ICM7556	E14.3	-	-	F14.3	-	-
LM1458	E8.3	-	-	-	-	T8.C
LM1558	-	-	-	-	-	T8.C
LM2902	E14.3	M14.15	-	-	-	-
LM2904	E8.3	-	-	-	-	-
LM324	E14.3	-	-	-	-	-
LM339	E14.3	-	-	-	-	-
LM358	E8.3	-	-	-	-	-
LM555	E8.3	-	-	-	-	T8.C
LM741	E8.3	-	-	-	-	T8.C

EXAMPLE: M 16 .15

- M — PACKAGE TYPE
- 16 — LEAD COUNT
- .15 — BODY WIDTH

Package Outlines

Dual-In-Line Plastic Packages

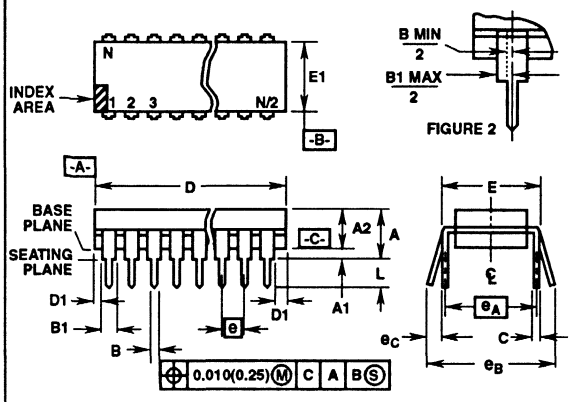


FIGURE 1

FIGURE 2

E8.3 (JEDEC MS-001-AB)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	9
C	0.008	0.015	0.204	0.381	-
D	0.348	0.430	8.84	10.92	5
D1	0.005	-	0.13	-	-
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.160	2.93	4.06	4
N	8		8		8

E14.3 (JEDEC MS-001-AC)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	9
C	0.008	0.015	0.204	0.381	-
D	0.725	0.795	18.42	20.19	5
D1	0.005	-	0.13	-	-
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.160	2.93	4.06	4
N	14		14		8

E16.3 (JEDEC MS-001-AA)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	9
C	0.008	0.015	0.204	0.381	-
D	0.745	0.840	18.93	21.33	5
D1	0.005	-	0.13	-	-
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.160	2.93	4.06	4
N	16		16		8

NOTES:

1. Controlling Dimensions: Inch. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to plane C.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. N is the maximum number of terminal positions.
9. Corner leads (1, N, N/2 and N/2 + 1) may be configured as shown in Figure 2.

Dual-In-Line Plastic Packages (Continued)

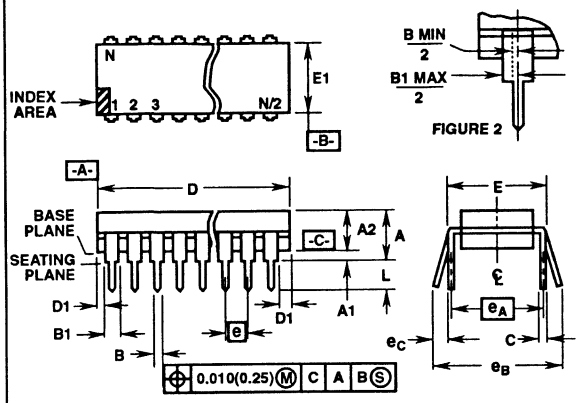


FIGURE 1

FIGURE 2

E18.3 (JEDEC MS-001-AD)
18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	9
C	0.008	0.015	0.204	0.381	-
D	0.845	0.925	21.47	23.49	5
D1	0.005	-	0.13	-	-
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.160	2.93	4.06	4
N	18		18		8

E20.3 (JEDEC MS-001-AE)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	9
C	0.008	0.015	0.204	0.381	-
D	0.925	1.060	23.5	26.9	5
D1	0.005	-	0.13	-	-
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.160	2.93	4.06	4
N	20		20		8

E22.4 (JEDEC MS-010-AA)
22 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	9
C	0.008	0.015	0.204	0.381	-
D	1.150	1.120	26.67	28.44	5
D1	0.005	-	0.13	-	-
E	0.390	0.425	9.91	10.79	6
E1	0.330	0.380	8.39	9.65	5
e	0.100 BSC		2.54 BSC		-
e_A	0.400 BSC		10.16 BSC		6
e_B	-	0.500	-	12.70	7
L	0.115	0.160	2.93	4.06	4
N	22		22		8

NOTES:

1. Controlling Dimensions: Inch. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to plane C.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. N is the maximum number of terminal positions.
9. Corner leads (1, N, N/2 and N/2 + 1) may be configured as shown in Figure 2.

Dual-In-Line Plastic Packages (Continued)

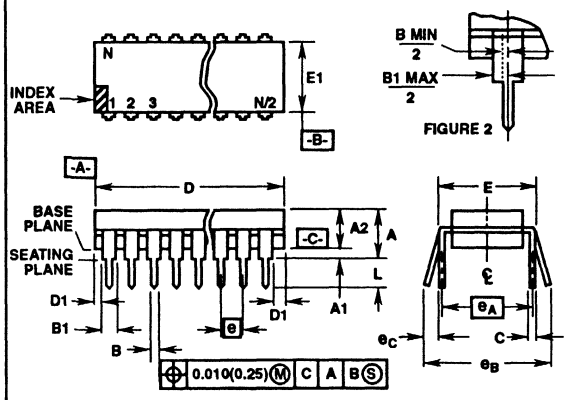


FIGURE 1

FIGURE 2

NOTES:

1. Controlling Dimensions: Inch. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to plane C.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. N is the maximum number of terminal positions.
9. Corner leads (1, N, N/2 and N/2 + 1) may be configured as shown in Figure 2.

E24.3 (JEDEC MS-001-AF)
24 LEAD NARROW BODY DUAL-IN-LINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	9
C	0.008	0.015	0.204	0.381	-
D	1.125	1.275	28.60	32.30	5
D1	0.005	-	0.13	-	-
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.160	2.93	4.06	4
N	24		24		8

E28.3 (JEDEC MS-001-AG)
28 LEAD NARROW BODY DUAL-IN-LINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	9
C	0.008	0.015	0.204	0.381	-
D	1.345	1.425	34.20	36.20	5
D1	0.005	-	0.13	-	-
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.160	2.93	4.06	4
N	28		28		8

Dual-In-Line Plastic Packages (Continued)

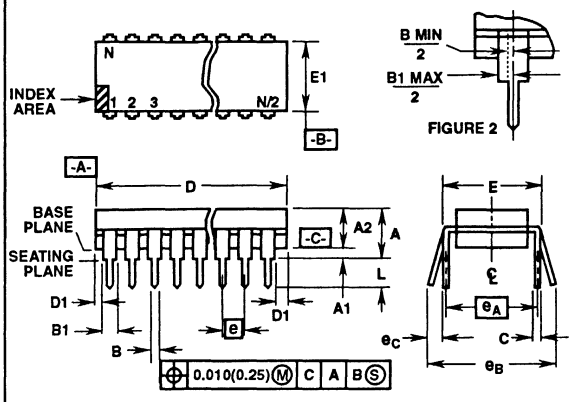


FIGURE 1

E24.6 (JEDEC MS-011-AA)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	9
C	0.008	0.015	0.204	0.381	-
D	1.150	1.290	29.3	32.7	5
D1	0.005	-	0.13	-	-
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	24		24		8

E28.6 (JEDEC MS-011-AB)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	9
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	-
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		8

E40.6 (JEDEC MS-011-AC)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	9
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	-
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		8

NOTES:

1. Controlling Dimensions: Inch. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to plane C.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. N is the maximum number of terminal positions.
9. Corner leads (1, N, N/2 and N/2 + 1) may be configured as shown in Figure 2.

Dual-In-Line Plastic Packages (Continued)

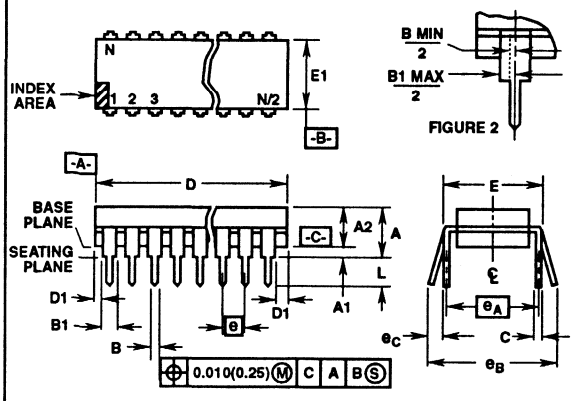


FIGURE 1

FIGURE 2

NOTES:

1. Controlling Dimensions: Inch. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to plane C.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. N is the maximum number of terminal positions.
9. Corner leads (1, N, N/2 and N/2 + 1) may be configured as shown in Figure 2.

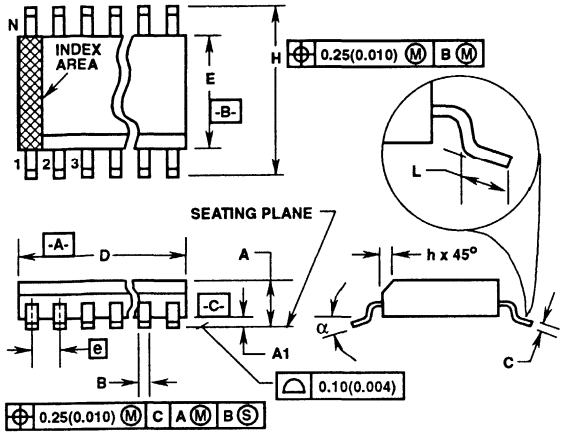
E42.6
42 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	9
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	-
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	42		42		8

E48.6 (JEDEC MS-011-AD)
48 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	9
C	0.008	0.015	0.204	0.381	-
D	2.385	2.480	60.70	63.1	5
D1	0.005	-	0.13	-	-
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	48		48		8

Small Outline (SOIC) Plastic Packages



M8.15 (JEDEC MS-012-AA)
8 LEAD SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

M14.15 (JEDEC MS-012-AB)
14 LEAD SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

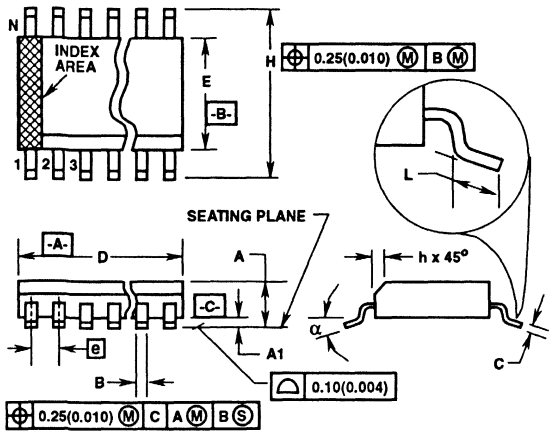
M16.15 (JEDEC MS-012-AC)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline (SOIC) Plastic Packages (Continued)



M16.3 (JEDEC MS-013-AA)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

M18.3 (JEDEC MS-013-AB)
18 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4469	0.4625	11.35	11.75	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	18		18		7
α	0°	8°	0°	8°	-

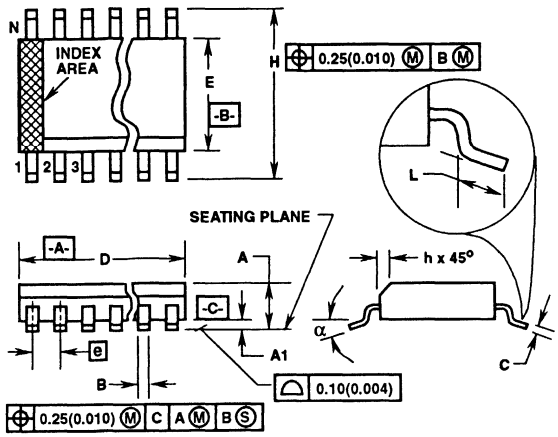
M20.3 (JEDEC MS-013-AC)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline (SOIC) Plastic Packages (Continued)



NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: Millimeter. Converted inch dimensions are not necessarily exact.

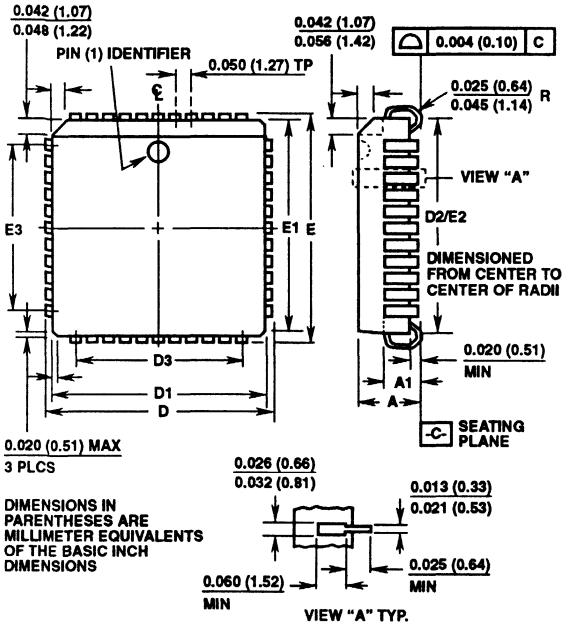
M24.3 (JEDEC MS-013-AD)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

M28.3 (JEDEC MS-013-AE)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Plastic Leaded Chip Carrier (PLCC) Packages



N20.35 (JEDEC MO-047-AA)
20 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.385	0.395	9.78	10.03	-
D1	0.350	0.356	8.89	9.042	2
D2	0.290	0.330	7.37	8.38	1
D3	0.200 REF		5.08 BSC		-
E	0.385	0.395	9.78	10.03	-
E1	0.350	0.356	8.89	9.042	2
E2	0.290	0.330	7.37	8.38	1
E3	0.200 REF		5.08 BSC		-
N	20		20		3

N28.45 (JEDEC MO-047-AB)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.430	11.582	2
D2	0.390	0.430	9.91	10.92	1
D3	0.300 REF		7.62 BSC		-
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.430	11.582	2
E2	0.390	0.430	9.91	10.92	1
E3	0.300 REF		7.62 BSC		-
N	28		28		3

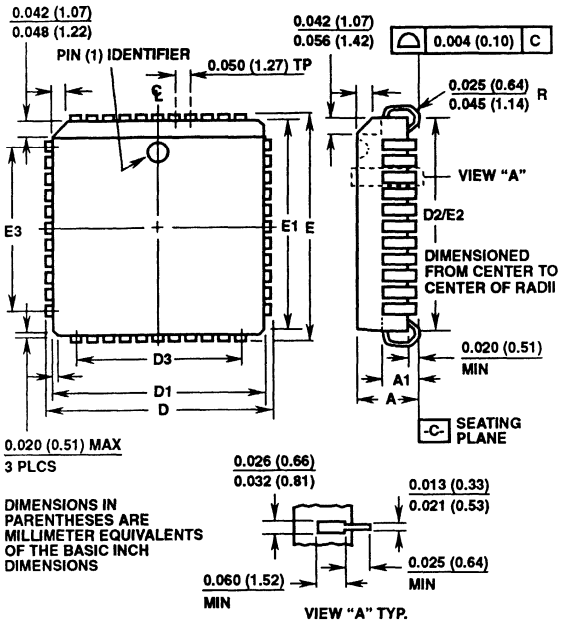
NOTES:

1. To be determined at seating plane.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.254mm/0.010 inch.
3. "N" is the number of terminal positions.
4. Controlling dimension: Inch.

N44.65 (JEDEC MO-047-AC)
44 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.685	0.695	17.40	17.65	-
D1	0.650	0.656	16.510	16.662	2
D2	0.590	0.630	14.99	16.00	1
D3	0.500 REF		12.70 BSC		-
E	0.685	0.695	17.40	17.65	-
E1	0.650	0.656	16.510	16.662	2
E2	0.590	0.630	14.99	16.00	1
E3	0.500 REF		12.70 BSC		-
N	44		44		3

Plastic Leaded Chip Carrier (PLCC) Packages (Continued)



NOTES:

1. To be determined at seating plane.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.254mm/0.010 inch.
3. "N" is the number of terminal positions.
4. Controlling dimension: Inch.

N68.95 (JEDEC MO-047-AE)

68 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

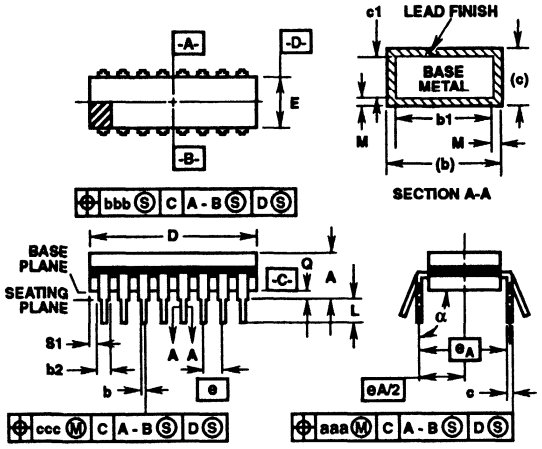
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.200	4.20	5.08	-
A1	0.090	0.130	2.29	3.30	-
D	0.985	0.995	25.02	25.27	-
D1	0.950	0.958	24.13	24.33	2
D2	0.890	0.930	22.61	23.62	1
D3	0.800 REF		20.32 BSC		-
E	0.985	0.995	25.02	25.27	-
E1	0.950	0.958	24.13	24.33	2
E2	0.890	0.930	22.61	23.62	1
E3	0.800 REF		20.32 BSC		-
N	68		68		3

N84.115 (JEDEC MO-047-AF)

84 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.200	4.20	5.08	-
A1	0.090	0.130	2.29	3.30	-
D	1.185	1.195	30.10	30.35	-
D1	1.150	1.158	29.210	29.413	2
D2	1.090	1.130	27.69	28.70	1
D3	1.000 REF		25.40 BSC		-
E	1.185	1.195	30.10	30.35	-
E1	1.150	1.158	29.210	29.413	2
E2	1.090	1.130	27.69	28.70	1
E3	1.000 REF		25.40 BSC		-
N	84		84		3

Dual-In-Line Frit-Seal Ceramic Packages



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: Inch

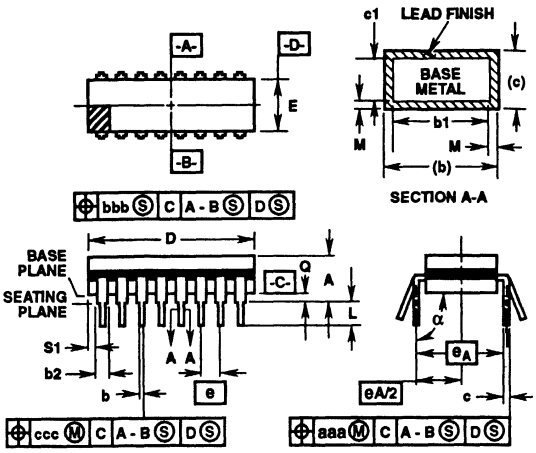
F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	8		8		8

F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		8

Dual-In-Line Frit-Seal Ceramic Packages (Continued)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: Inch

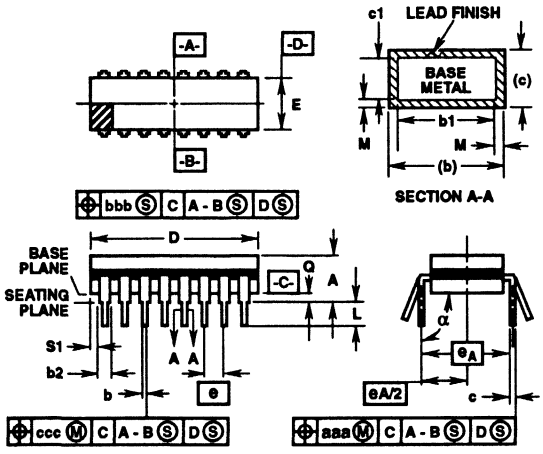
F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

F18.3 MIL-STD-1835 GDIP1-T18 (D-6, CONFIGURATION A)
18 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.960	-	24.38	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	18		18		8

Dual-In-Line Frit-Seal Ceramic Packages (Continued)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: Inch

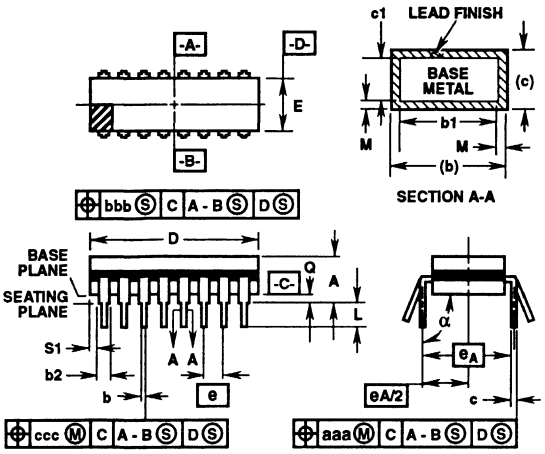
F20.3 MIL-STD-1835 GDIP1-T20 (D-8, CONFIGURATION A)
20 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.060	-	26.92	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	20		20		8

F24.6 MIL-STD-1835 GDIP1-T24 (D-3, CONFIGURATION A)
24 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.120	0.200	3.05	5.08	-
Q	0.015	0.075	0.38	1.91	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	24		24		8

Dual-In-Line Frit-Seal Ceramic Packages (Continued)



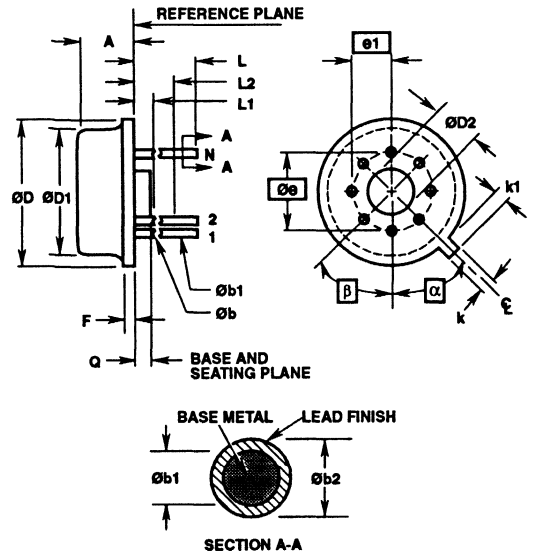
F28.6 MIL-STD-1835 GDIP1-T28 (D-10, CONFIGURATION A)
28 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	28		28		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: Inch

Metal Can Packages



NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI 414.5M - 1982.
6. Controlling dimension: Inch.

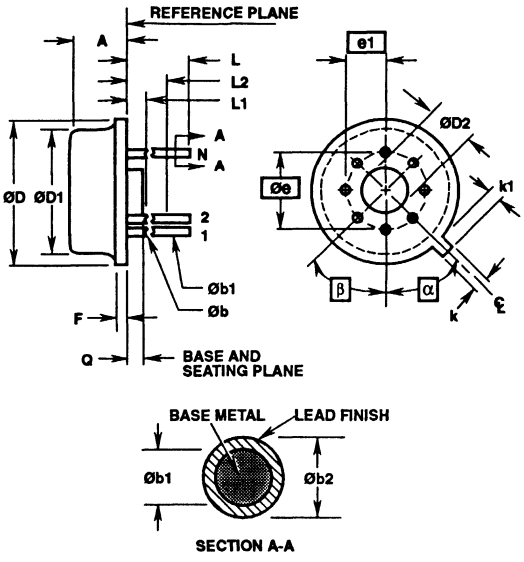
T8.C MIL-STD-1835 MACY1-X8 (A1)
8 LEAD TO-99 METAL CAN

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	45° BSC		45° BSC		3
β	45° BSC		45° BSC		3
N	8		8		4

T10.B MIL-STD-1835 MACY1-X10 (A2)
10 LEAD TO-100 METAL CAN

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.230 BSC		5.84 BSC		-
e1	0.115 BSC		2.92 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	36° BSC		36° BSC		3
β	36° BSC		36° BSC		3
N	10		10		4

Metal Can Packages (Continued)



NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI 414.5M - 1982.
6. Controlling dimension: Inch.

T10.C

10 LEAD TO-100 METAL CAN

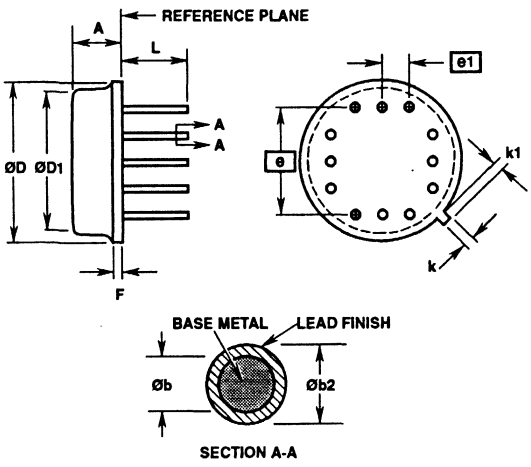
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	-	-	-	-	-
e	0.230 BSC		5.84 BSC		-
e1	0.115 BSC		2.92 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	-	-	-	-	-
α	36° BSC		36° BSC		3
β	36° BSC		36° BSC		3
N	10		10		4

T12.B

12 LEAD TO-101 METAL CAN

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	-	-	-	-	-
e	0.230 BSC		5.84 BSC		-
e1	0.115 BSC		2.92 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	-	-	-	-	-
α	30° BSC		30° BSC		3
β	30° BSC		30° BSC		3
N	12		12		4

Metal Can Packages (Continued)



T12.C

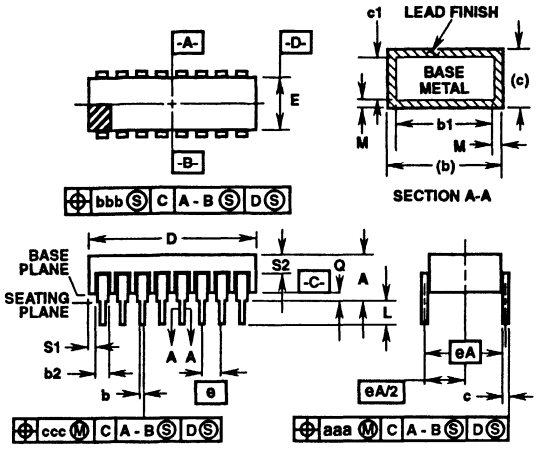
12 LEAD TO-8 METAL CAN

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.130	0.150	3.30	3.81	-
Øb	0.016	0.019	0.41	0.48	-
Øb2	0.016	0.021	0.41	0.53	-
ØD	0.585	0.615	14.86	15.62	-
ØD1	0.540	0.560	13.72	14.22	-
e	0.400 BSC		10.16 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	0.020	0.040	0.51	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.560	12.70	14.22	-
N	12		12		3

NOTES:

1. The reference, base, and seating planes are the same for this variation.
2. Measured from maximum diameter of the product.
3. N is the maximum number of terminal positions.
4. Dimensioning and tolerancing per ANSI 414.5M - 1982.
5. Controlling dimension: Inch.

Dual-In-Line Metal-Seal Ceramic Packages



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
9. N is the maximum number of terminal positions.
10. Braze fillets shall be concave.
11. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
12. Controlling dimension: Inch.

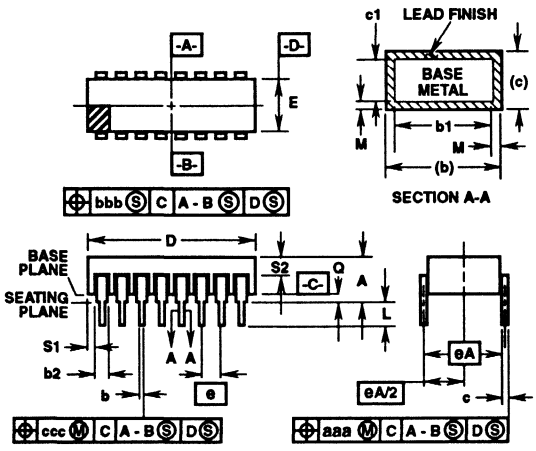
D8.3 MIL-STD-1835 CDIP2-T8 (D-4, CONFIGURATION C)
8 LEAD DUAL-IN-LINE METAL-SEAL CERAMIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	8
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	8		8		9

D14.3 MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C)
14 LEAD DUAL-IN-LINE METAL-SEAL CERAMIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	8
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		9

Dual-In-Line Metal-Seal Ceramic Packages (Continued)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
9. N is the maximum number of terminal positions.
10. Braze fillets shall be concave.
11. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
12. Controlling dimension: Inch.

D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD DUAL-IN-LINE METAL-SEAL CERAMIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	8
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		9

D24.6 MIL-STD-1835 CDIP2-T24 (D-3, CONFIGURATION C)
24 LEAD DUAL-IN-LINE METAL-SEAL CERAMIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.120	0.200	3.05	5.08	-
Q	0.015	0.075	0.38	1.91	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	8
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	24		24		9

LINEAR 12

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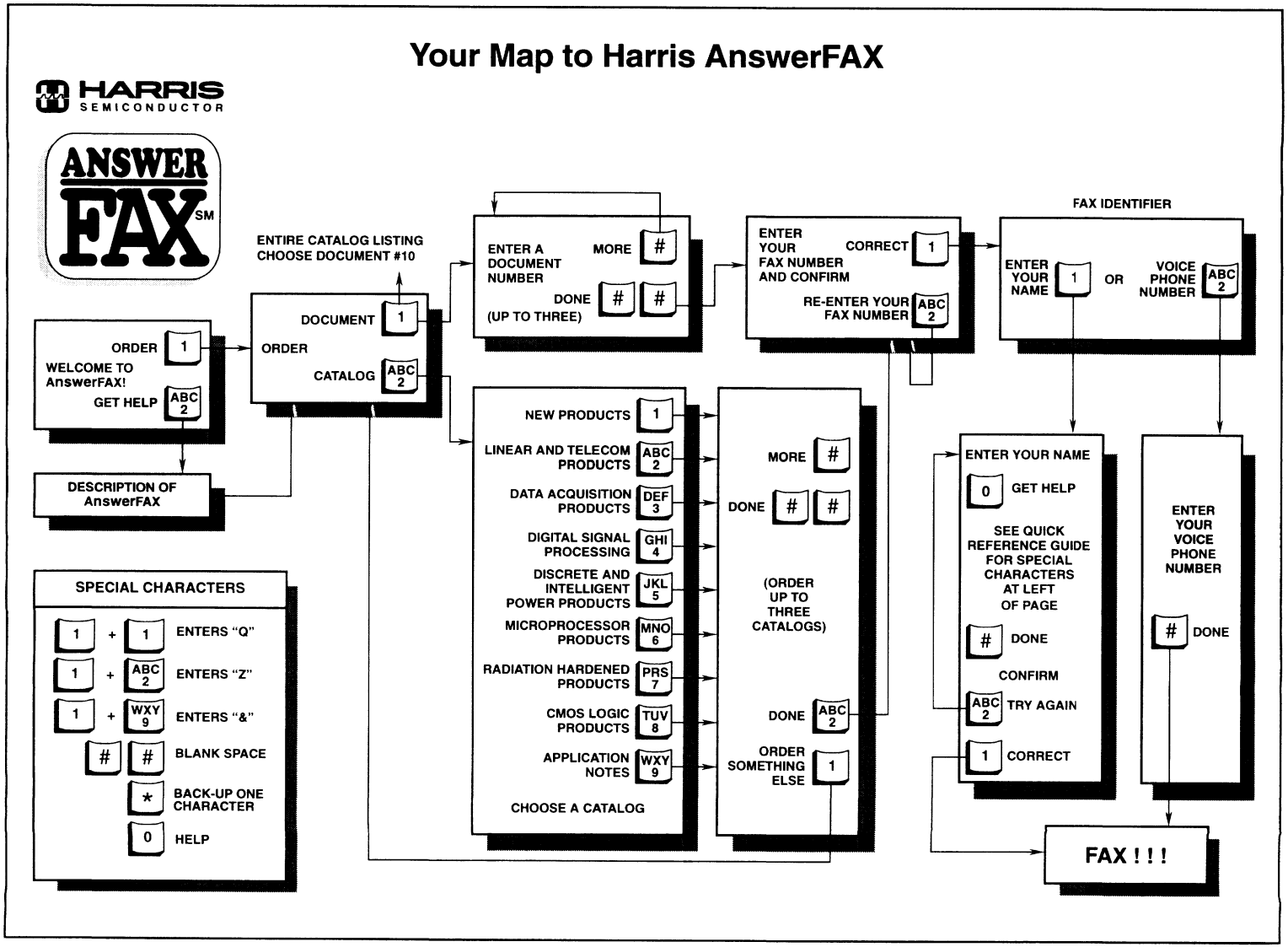
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	PSG201.21	**PRODUCT SELECTION GUIDE** (NEW 1994: 616pp) Key product information on all Harris Semiconductor devices. Sectioned (Linear, Data Acquisition, Digital Signal Processing, Telecom, Intelligent Power, Discrete Power, Digital Microprocessors and Hi-Rel/Military and Rad Hard) for easy use and includes cross references and alphanumeric part number index.
	DB500B	**LINEAR AND TELECOM ICs** (1993: 1,312pp) Product specifications for: op amps, comparators, S/H amps, differential amps, arrays, special analog circuits, telecom ICs, and power processing circuits.
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	DB450C	**TRANSIENT VOLTAGE SUPPRESSION DEVICES** (1994: 400pp) Product specifications of Harris varistors and surgectors. Also, general informational chapters such as: "Voltage Transients - An Overview," "Transient Suppression - Devices and Principles," "Suppression - Automotive Transients."
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	DB235B	**RADIATION HARDENED** (1993: 2,232pp) Harris technologies used include dielectric isolation (DI), Silicon-on-Sapphire (SOS), and Silicon-on-Insulator (SOI). The Harris radiation-hardened products include the CD4000, HCS/HCTS and ACS/ACTS logic families, SRAMs, PROMs, op amps, analog multiplexers, the 80C85/80C86 microprocessor family, analog switches, gate arrays, standard cells and custom devices.
	DB260.2	**CDP6805 CMOS MICROCONTROLLERS & PERIPHERALS** (1995: 436pp) This data book represents the full line of Harris Semiconductor CDP6805 products for commercial applications and supersedes previously published CDP6805 data books under the Harris, GE, RCA or Intersil names.
	DB303	**MICROPROCESSOR PRODUCTS** (1992: 1,156pp) For commercial and military applications. Product specifications on CMOS microprocessors, peripherals, data communications, and memory ICs.
	DB309	**MCT/IGBT/DIODES** (1994: 528pp) This data book fully describes Harris Semiconductor's line of MOS Controlled Thyristors, Insulated Gate Bipolar Transistors (IGBTs) and Power Diodes/Rectifiers.
	Analog Military	**ANALOG MILITARY** (1989: 1,264pp) This data book describes Harris' military line of Linear, Data Acquisition, and Telecommunications circuits.
	DB312	**ANALOG MILITARY DATA BOOK SUPPLEMENT** (1994: 432pp) The 1994 Military Data Book Supplement, combined with the 1989 Analog Military Product Data Book, contain detailed technical information on the extensive line of Harris Semiconductor Linear and Data Acquisition products for Military (MIL-STD-883, DESC SMD and JAN) applications and supersedes all previously published Linear and Data Acquisition Military data books. For applications requiring Radiation Hardened products, please refer to the 1993 Harris Radiation Hardened Product Data Book (document #DB235B)
	Digital Military	**DIGITAL MILITARY** (1989: 680pp) Harris CMOS digital ICs – microprocessors, peripherals, data communications and memory – are included in this data book.
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9051	AN051	Principles and Applications of the ICL7660 CMOS Voltage Converter (9 pages)
9052	AN052	Tips for Using Single Chip 3.5 Digit A/D Converters (9 pages)
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9120	AN120	Interfacing the 80C286-16 With the 80287-10 (2 pages)
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9521	AN521	Getting the Most Out of CMOS Devices for Analog Switching Jobs (7 pages)
9522	AN522	Digital to Analog Converter Terminology (3 pages)
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9525	AN525	HA-5190/5195 Fast Settling Operational Amplifier (4 pages)
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9532	AN532	Common Questions Concerning CMOS Analog Switches (4 pages)
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96077	AN6077	An IC Operational-Transconductance-Amplifier (OTA) With Power Capability (12 pages)
96101	AN6101	COS/MOS Phase-Locked-Loop A Versatile Building Block for Micro-Power Digital and Analog Applications (4 pages)
96157	AN6157	Applications of the CA3085 Series Monolithic IC Voltage Regulators (11 pages)
96182	AN6182	Features and Applications of Integrated Circuit Zero-Voltage Switches (CA3058, CA3059 and CA3079) (31 pages)
96230	AN6230	Using the CD4047A in COS/MOS Timing Applications (13 pages)
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AnswerFAX Technical Support Application Note Listing

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
96459	AN6459	Why Use the CMOS Operational Amplifiers and How to Use it (4 pages)
96466	AN6466	Astable and Monostable Oscillators Using COS/MOS Digital Integrated Circuits (6 pages)
96498	AN6498	Design of Fixed and Programmable Counters Using the CD4018 COS/MOS Presettable Divide-By-"N" Counter (6 pages)
96532	AN6532	Fundamentals of Testing COS/MOS Integrated Circuits (9 pages)
96525	AN6525	Guide to Better Handling and Operation of CMOS Integrated Circuits (3 pages)
96558	AN6558	Understanding Buffered and Unbuffered CMOS Characteristics (5 pages)
96565	AN6565	Design of Clock Generators For Use With COSMAC Microprocessor CDP1802 (3 pages)
96587	AN6587	Noise Immunity of COS/MOS B-Series Integrated Circuits (8 pages)
96595	AN6595	Interfacing Analog and Digital Displays with CMOS Integrated Circuits (6 pages)
96602	AN6602	Interfacing COS/MOS with Other Logic Families (12 pages)
96669	AN6669	FET-Bipolar Monolithic Op Amps Mate Directly to Sensitive Sources (3 pages)
96716	AN6716	Low-Power Digital Frequency Synthesizers Utilizing COS/MOS ICs (15 pages)
96739	AN6739	COS/MOS Rate Multipliers-Versatile Circuits for Synthesizing Digital Functions (12 pages)
96883	AN6883	Simplified Design of Astable RC Oscillators Using the CD4060B or Two CMOS Inverters (1 page)
96915	AN6915	Application of CA1524 Series Pulse-Width Modulator ICs (18 pages)
96948	AN6948	Parallel Clocking of Sequential CMOS Devices (1 page)
96970	AN6970	Understanding and Using the CDP1855 Multiply/Divide Unit (11 pages)
97063	AN7063	Understanding the CDP1851 Programmable I/O (7 pages)
97174	AN7174	The CA1524E Pulse-Width Modulator-Driver for an Electronic Scale (2 pages)
97244	AN7244	Understanding Power MOSFETs (4 pages)
97254	AN7254	Switching Waveforms of the L^2FET: A 5 Volt Gate-Drive Power MOSFET (8 pages)
97260	AN7260	Power MOSFET Switching Waveforms: A New Insight (7 pages)
97275	AN7275	User's Guide to the CDP1879 and CDP1879C1 CMOS Real-Time Clocks (18 pages)
97315	AN7315	Power Consumption in QMOS Logic Circuits (6 pages)
97323	AN7323	Modification of LSTTL Test Programs to Test HCT High-Speed-CMOS Logic ICs (4 pages)
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97326	AN7326	Applications of the CA3228E Speed Control System (16 pages)
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97332	AN7332	The Application of Conductivity-Modulated Field-Effect Transistors (5 pages)
97337	AN7337	Astable Multivibrator Design Using High-Speed QMOS ICs (5 pages)
97367	AN7367	Linear Application of the CD54/74HCU04 QMOS Hex Inverter (12 pages)
97374	AN7374	The CDP1871A Keyboard Encoder (9 pages)
98602	AN8602	The IGBTs - A New High Conductance MOS-Gated Device (3 pages)
98603	AN8603	Improved IGBTs with Fast Switching Speed and High-Current Capability (4 pages)
98610	AN8610	Spicing-Up Spice II Software for Power MOSFET Modeling (8 pages)
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98640	AN8640	Using Advanced CMOS Logic in a VME Data Bus System (8 pages)
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98742	AN8742	Application of the CD22402 Video Sync Generator (4 pages)

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98743	AN8743	Micropower Crystal-Controlled Oscillator Design Using CMOS Inverters (8 pages)
98754	AN8754	Method of Measurement of Simultaneous Switching Transient (3 pages)
98756	AN8756	A Comparative Description of the UART (16 pages)
98759	AN8759	Low Cost Data Acquisition System Features SPI A/D Converter (9 pages)
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98829	AN8829	SP600 and SP601 an HVIC MOSFET/IGBT Driver for Half-Bridge Topologies (6 pages)
98906	AN8906	Noise Aspects of Applying Advanced CMOS (AC/ACT) Semiconductors (62 pages) or Call Harris Semiconductor (407) 724-3739 and request by mail
98910	AN8910	An Introduction to Behavioral Simulation Using Harris AC/ACT Logic SmartModels™ From Logic Automation Inc. (9 pages)
99001	AN9001	Measuring Ground and VCC Bounce in Advanced High Speed (AC/ACT/FCT) CMOS Logic ICs (4 pages)
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99003	AN9003	Low-Voltage Metal-Oxide Varistor - Protection for Low Voltage (≤5V) ICs (13 pages)
99004	AN9004	Advanced High Speed CMOS Logic in a PCB Transmission Line Environment (7 pages)
99010	AN9010	HIP2500 High Voltage (500V_{DC}) Half-Bridge Driver IC (8 pages)
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99102	AN9102	Noise Aspects of Applying Advanced CMOS Semiconductors (9 pages)
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99106	AN9106	Special ESD Considerations for the HS-65643RH and HS-65647RH Radiation Hardened SOS SRAMs (2 pages)
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99206	AN9206	Correlating on Extended Data Lengths (2 pages)
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99208	AN9208	High Frequency Power Converters (10 pages)
99209	AN9209	A Spice-2 Subcircuit Representation for Power MOSFETs, Using Empirical Methods (4 pages)
99210	AN9210	A New PSpice Subcircuit for the Power MOSFET Featuring Global Temperature Options (12 pages)
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99332	AN9332	Using the HI1276 Evaluation Board (10 pages)
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99336	AN9336	Mult-Meter Display Converter Eases DMM Design (6 pages)
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99404	AN9404	HIP4080A, 80V High Frequency H-Bridge Driver (12 pages)
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99406	AN9406	Using the HI20201/03 Evaluation Kit (11 pages)
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99408	AN9408	The HIP2030 MCT/IGBT Gate Driver Provides Isolated Control Signals to Switch Power Devices (7 pages)
99411	AN9411	Using the HI1171 Evaluation Kit (6 pages)
99412	AN9412	Using the HI5702 Evaluation Board (11 pages)
660001	MM0001	HFA-0001 Spice Operational Amplifier Macro-Model (4 pages)
660002	MM0002	HFA-0002 Spice Operational Amplifier Macro-Model (4 pages)

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660005	MM0005	HFA-0005 Spice Operational Amplifier Marco-Model (4 pages)
662500	MM2500	HA2500/02 Spice Operational Amplifier Macro-Model (5 pages)
662510	MM2510	HA-2510/12 Spice Operational Amplifier Macro-Model (4 pages)
662520	MM2520	HA-2520/22 Spice Operational Amplifier Macro-Model (4 pages)
662539	MM2539	HA-2539 Spice Operational Amplifier Macro-Model (4 pages)
662540	MM2540	HA-2540 Spice Operational Amplifier Macro-Model (4 pages)
662541	MM2541	HA-2541 Spice Operational Amplifier Macro-Model (5 pages)
662542	MM2542	HA-2542 Spice Operational Amplifier Macro-Model (5 pages)
662544	MM2544	HA-2544 Spice Operational Amplifier Macro-Model (5 pages)
662548	MM2548	HA-2548 Spice Operational Amplifier Macro-Model (5 pages)
662600	MM2600	HA-2600/02 Spice Operational Amplifier Macro-Model (5 pages)
662620	MM2620	HA-2620/22 Spice Operational Amplifier Macro-Model (5 pages)
662839	MM2839	HA-2839 Spice Operational Amplifier Macro-Model (4 pages)
662840	MM2840	HA-2840 Spice Operational Amplifier Macro-Model (4 pages)
662841	MM2841	HA-2841 Spice Operational Amplifier Macro-Model (4 pages)
662842	MM2842	HA-2842 Spice Operational Amplifier Macro-Model (4 pages)
662850	MM2850	HA-2850 Spice Operational Amplifier Macro-Model (4 pages)

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663046	MM3046	HFA3046/3096/3127/3128 Transistor Array Spice Models (4 pages)
665002	MM5002	HA-5002 Spice Buffer Amplifier Macro-Model (4 pages)
665004	MM5004	HA-5004 Spice Current Feedback Amplifier Macro-Model (4 pages)
665020	MM5020	HA-5020 Spice Current Feedback Operational Amplifier Macro-Model (4 pages)
665033	MM5033	HA-5033 Spice Buffer Amplifier Macro-Model (4 pages)
665101	MM5101	HA-5101 Spice Operational Amplifier Macro-Model (5 pages)
665102	MM5102	HA-5102 Spice Operational Amplifier Macro-Model (5 pages)
665104	MM5104	HA-5104 Spice Operational Amplifier Macro-Model (5 pages)
665112	MM5112	HA-5112 Spice Operational Amplifier Macro-Model (5 pages)
665114	MM5114	HA-5114 Spice Operational Amplifier Macro-Model (5 pages)
665127	MM5127	HA-5127 Spice Operational Amplifier Macro-Model (4 pages)
665137	MM5137	HA-5137 Spice Operational Amplifier Macro-Model (4 pages)
665147	MM5147	HA-5147 Spice Operational Amplifier Macro-Model (4 pages)
665190	MM5190	HA-5190 Spice Operational Amplifier Macro-Model (4 pages)
665221	MM5221	HA-5221/22 Spice Operational Amplifier Macro-Model (4 pages)
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FAX: 214 733 0819

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Suite 180
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TEL: (512) 343-2321
FAX: 512 343-2487

8350 Meadow Rd., Suite 174
Dallas, TX 75231
TEL: (214) 265-4600
FAX: 214 265 4668

Corporate Atrium II, Suite 140
10701 Corporate Dr.
Stafford, TX 77477
TEL: (713) 240-6082
FAX: 713 240 6094

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Compass Mktg. & Sales, Inc.
5 Triad Center, Suite 320
Salt Lake City, UT 84180
TEL: (801) 322-0391
FAX: 801 322-0392

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Northwest Marketing Assoc.
12835 Bel-Red Road
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Bellevue, WA 98005
TEL: (206) 455-5846
FAX: 206 451 1130

WISCONSIN
Oasis Sales
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FAX: 414 782 7921

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25 Hub Dr.
Melville, NY 11747
TEL: (516) 391-1300
FAX: 516 391 1644

Electronics Marketing Corporation (EMC)
1150 West Third Avenue
Columbus, OH 43212
TEL: (614) 299-4161
FAX: 614 299 4121

Farnell Electronic Services
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Canada L4K 3N6
TEL: (416) 798-4884
FAX: 416 798 4889

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128 Carnegie Row
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TEL: (617) 769-6000, x156
FAX: 617 762 8931

Hamilton Hallmark
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Culver City, CA 90230
TEL: (310) 558-2000
FAX: 310 558 2809 (Mil)
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Newark Electronics
4801 N. Ravenswood
Chicago, IL 60640
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FAX: 312 275-9596

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FAX: 408 988-2747

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Obsolete Products:

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TEL: (408) 629-4789
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Orlando, FL 32810-2696
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Burbank, CA 91504-1052
TEL: (818) 768-7400
FAX: (818) 767-7038

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FAX: 407 994-5518

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Graftec Brasil Ltda.
Rua baroneza De ITU 336 - 5
01231-000 - Sao Paulo - SP
Brasil
TEL: 55-11-826-5407
FAX: 55-11-826-6526

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Mercure Center
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FAX: 32 2 724 2205/...09

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Eurodis Electronics GmbH
Lamezanstrasse 10
A - 1232 Vienna
TEL: 43 1 61062-0
FAX: 43 1 610625

DENMARK
Delco AS
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DK - 2200 Copenhagen N
TEL: 45 35 82 12 00
FAX: 45 35 82 12 05

FINLAND
J. Havulinna & Son
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FAX: 33 1 39 46 40 54

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FAX: 49 89 6377891

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FAX: 49 4106 6 88 50

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D - 64720 Michelstadt
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FAX: 49 7544 7 25 55

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Madrid
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FAX: 34 1 352 1147

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Ashton-In-Makerfield
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Bothwell Road
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Eurodis Electronics GmbH
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A - 1232 Wien
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DK - 2605 Brondby
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Italahdenkatu, 18
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FAX: 358 069 22326

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P.O. Box 51
SF - 02630 ESPOO
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Arrow Electronique
73 - 79, Rue des Solets
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F - 94663 Rungis Cedex
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Avnet EMG France
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F-92320 Chatillon Sous Bagneux
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FAX: 33 1 49 65 25 39

CCI Electronique
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Silic 577
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